S71NSI28JC0 Based MCP

Stacked Multi-Chip Product (MCP)

I28 Megabit (8M x I6 bit) CMOS I.8 Volt-only Simultaneous Read/Write, Burst-mode Multi-plexed Flash Memory with 64Megabit (4M x I6-Bit) CellularRAM

ADVANCE INFORMATION

Data Sheet

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See Notice On Data Sheet Designations for definitions.

Publication Number S71NS-J-00 **Revision** A **Amendment** 0 **Issue Date** March 17, 2005

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ADVANCE INFORMATION

General Description

The S71NS-J Series is a product line of stacked Multi-Chip Product (MCP) packages and consists of the following items:

- One or more S29NS-J flash memory die
- Cellular RAM Type pSRAM

The products covered by this document are listed in the table below. For details about their specifications, please refer to the individual constituent datasheet for further details.

Device	Flash Density	pSRAM Density
	128 Mb	64 Mb
S71NS128JC0	■	■

Distinctive Characteristics

MCP Features

- **Power supply voltage of 1.7 V to 1.95 V**
- **Burst Speed: 54 MHz, 66 MHz**
- **Package**
  - 9.95 x 10.95 mm
- **Operating Temperature**
  - Wireless, –25°C to +85°C

Notice On Data Sheet Designations

Spansion LLC issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Spansion LLC is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion LLC therefore places the following conditions upon Advance Information content:

> "This document contains information on one or more products under development at Spansion LLC. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion LLC reserves the right to change or discontinue work on this proposed product without notice."

Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

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Combination

Some data sheets will contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document will distinguish these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion LLC deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local AMD or Fujitsu sales office.

Contents

Tables

Figures

1 Product Selector Guide

Device	Model Numbers	pSRAM Density	Flash Speed	pSRAM Speed (MHz)	pSRAM (Cellular RAM) Supplier	Package
S71NS128JC0	VN	64 Mb	70 ns/66 MHz	70 ns/66 MHz	CellularRAM 2	NLA060 9.95 x 10.95 mm
	VP		70 ns/54 MHz	70 ns/54 MHz		

2 Ordering Information

The ordering part number is formed by a valid combination of the following:

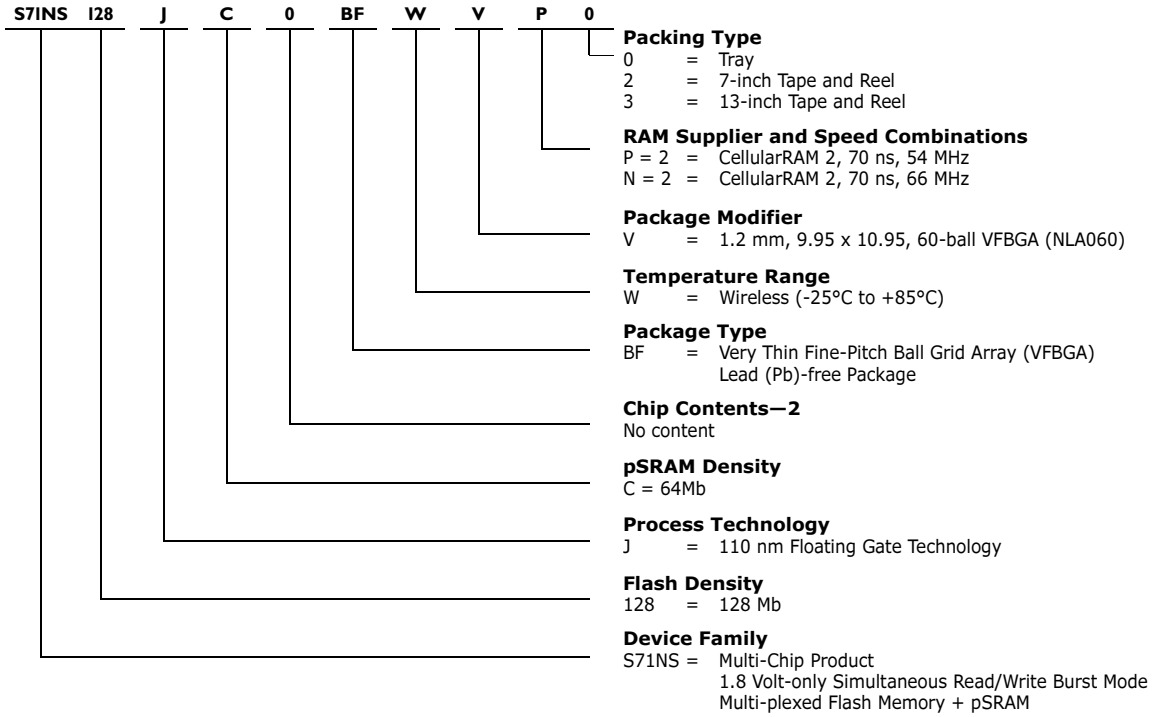


Table 2.1 MCP Configurations and Valid Combinations

Valid Combinations						
S71NS128J	C	0	BF	W	V	P, N

Package Marking Note:

The package marking omits the leading S from the ordering part number.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

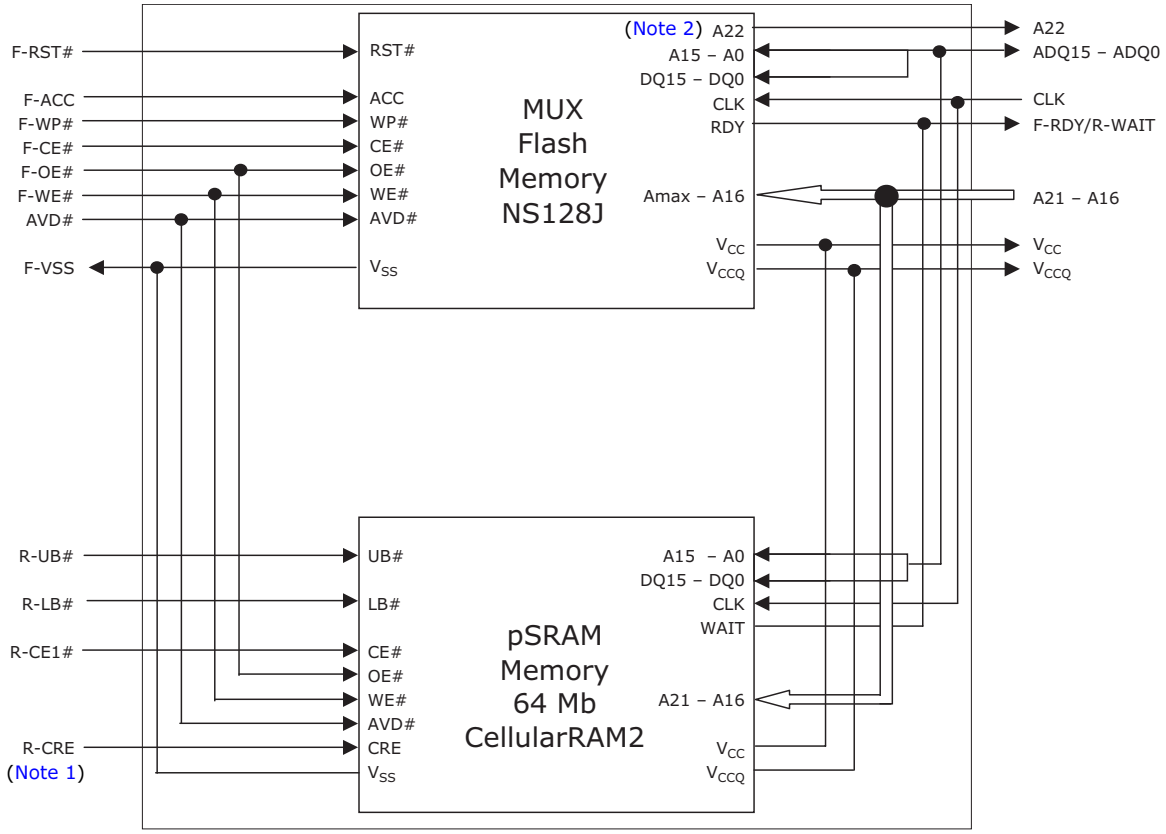
3 Input/Output Descriptions

Table 3.1 identifies the input and output package connections provided on the device.

Table 3.1 Input/Output Descriptions

Symbol	Description
A22 – A16	Address inputs
ADQ15 – ADQ0	Multi-plexed Address/Data
OE#	Output Enable input. Asynchronous relative to CLK for the Burst mode.
WE#	Write Enable input.
V_{SS}	Ground
NC	No Connect; not connected internally
RDY	Ready output. Indicates the status of the Burst read. The WAIT# pin of the pSRAM is tied to RDY.
CLK	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at V_{IL} or V_{IH} while in asynchronous mode
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs. Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched. High = device ignores address inputs
F-RST#	Hardware reset input. Low = device resets and returns to reading array data
F-WP#	Hardware write protect input. At V_{IL}, disables program and erase functions in the four outermost sectors. Should be at V_{IH} for all other conditions.
F-ACC	Accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.
R-CE1#	Chip-enable input for pSRAM.
F1-CE#	Chip-enable input for Flash 1. Asynchronous relative to CLK for Burst Mode.
R-CRE	Control Register Enable (pSRAM). For CellularRAM only.
F-VCC	Flash 1.8 Volt-only single power supply.
R-VCC	pSRAM Power Supply.
R-UB#	Upper Byte Control (pSRAM).
R-LB#	Lower Byte Control (pSRAM)
DNU	Do Not Use

4 MCP Block Diagram



Notes:

1. *R-CRE is only present in Cellular RAM compatible pSRAM.*
2. *A22 is address for Flash only.*

Figure 4.1 MCP Block Diagram

5 Connection Diagrams/Physical Dimensions

This section contains the I/O designations and package specifications for the S71NS-J.

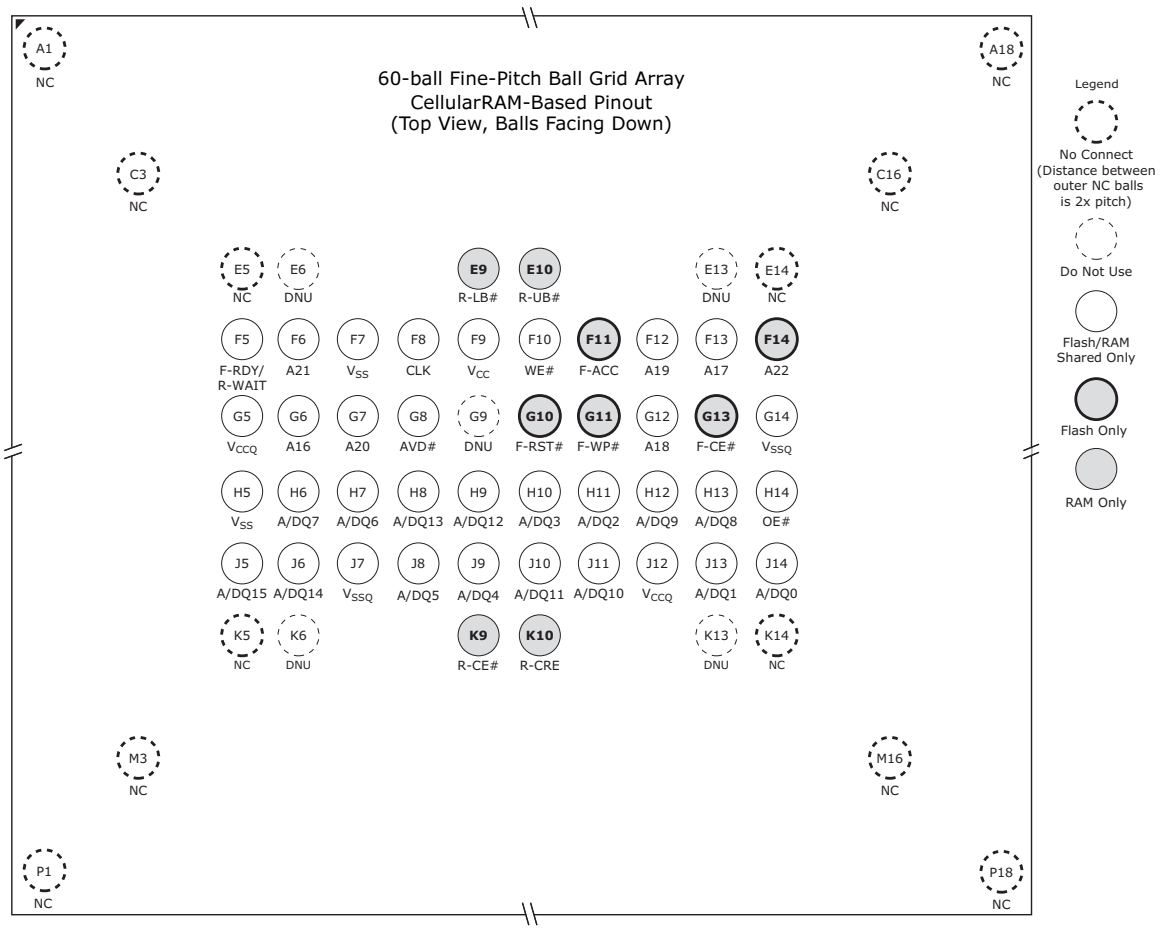
5.1 Special Handling Instructions for FBGA Packages

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

5.2 Connection Diagrams

5.2.1 CellularRAM Based Pinout, 60-Ball, VFBGA



Note: *3.Addresses are shared between Flash and RAM depending on the density of the pSRAM.*

MCP	Flash-Only Addresses	Shared Addresses	Shared AD Pins
S71NS128JC0	A22	A21 – A16	ADQ15 – ADQ0

Figure 5.1 CellularRAM Based Pinout, 60-Ball, VFBGA

5.2.2 Look Ahead Connection Diagram
60-ball x16 MUX NOR Flash + x16 MUX pSRAM on Shared Bus

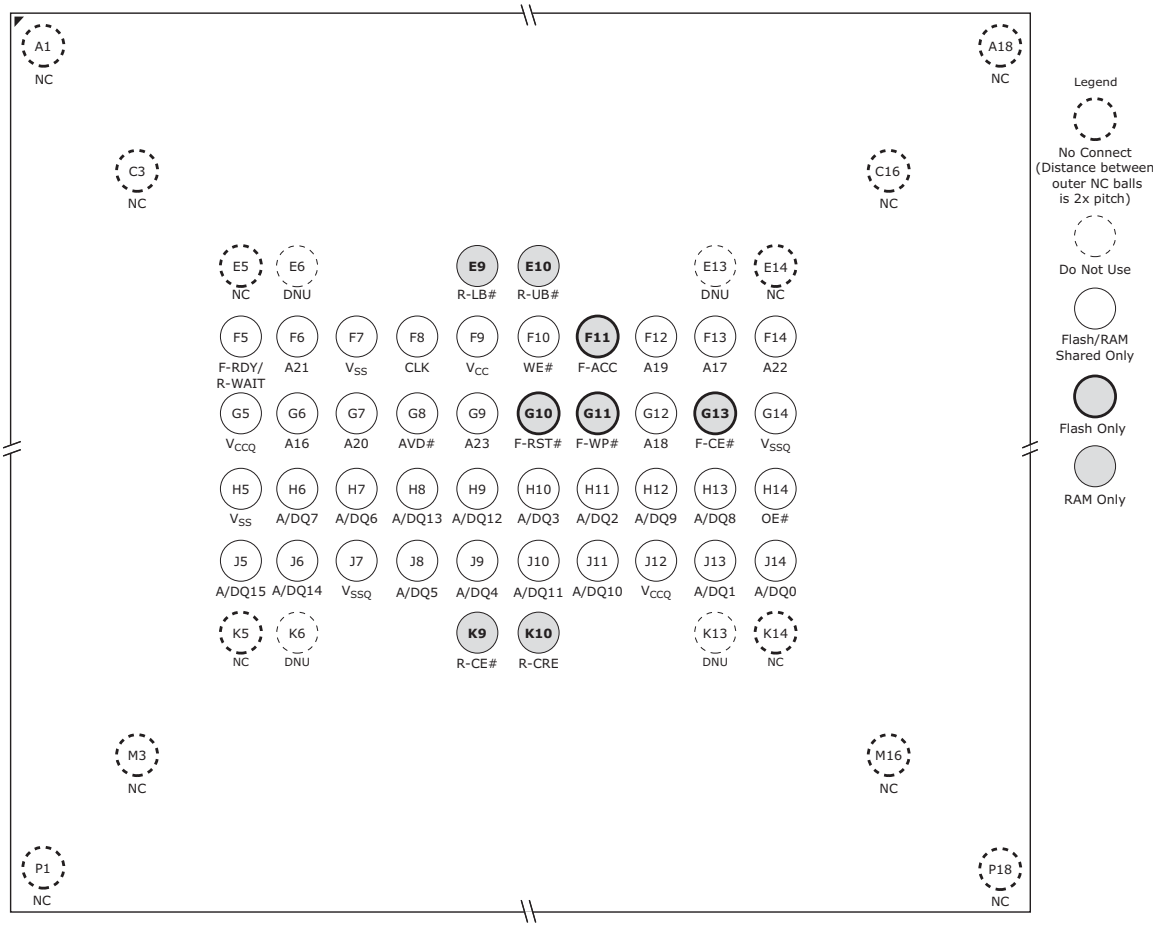
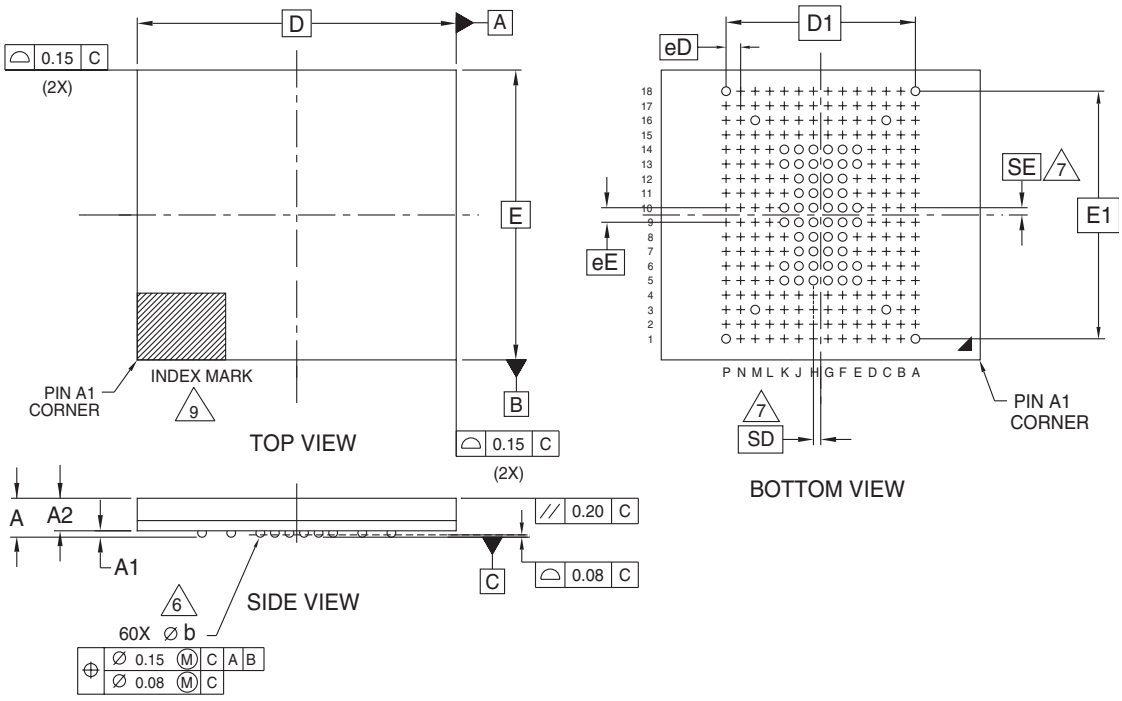


Figure 5.2 Look Ahead Connection Diagram
60-ball x16 MUX NOR Flash + x16 MUX pSRAM on Shared Bus

5.3 Physical Dimensions

5.3.1 NLA060—60-ball VFBGA



PACKAGE	NLA 060			
JEDEC	N/A			
D x E	10.95 mm x 9.95 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.85	---	0.97	BODY THICKNESS
D	10.95 BSC.			BODY SIZE
E	9.95 BSC.			BODY SIZE
D1	6.50 BSC.			MATRIX FOOTPRINT
E1	8.50 BSC.			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	18			MATRIX SIZE E DIRECTION
n	60			BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC.			BALL PITCH
eD	0.50 BSC			BALL PITCH
SD / SE	0.25 BSC.			SOLDER BALL PLACEMENT
	A2–A17,B1–B18,C1,C2,C4–C15,C17,C18 D1–D18,E1,E2,E3,E4,E7,E8,E11,E12,E15,E16,E17,E18 F1,F2,F3,F4,F15,F16,F17,F18,G1,G2,G3,G4,G15,G16,G17,G18 H1,H2,H3,H4,H15,H16,H17,H18,J1,J2,J3,J4,J15,J16,J17,J18 K1,K2,K3,K4,K7,K8,K11,K12,K15,K16,K17,K18 L1 –L18,M1,M2,M4–M15,M17,M18,N1–N18,P2–P17			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

3483 \ 16-038.22 \ 3.11.5

Figure 5.3 Physical Dimensions, NLA060—60-ball VFBGA

S29NS128J/S29NS064J/S29NS032J/ S29NS016J

28 Megabit (8 M x 16-Bit), 64 Megabit (4 M x 16-Bit),
32 Megabit (2 M x 16-Bit), and 16 Megabit (1 M x 16 Bit),
110 nm CMOS 1.8 Volt-only Simultaneous Read/Write, Burst Mode Flash Memories

Data Sheet

ADVANCE INFORMATION

Distinctive Characteristics

- **Single 1.8 volt read, program and erase (1.7 to 1.95 volt)**
- **Multiplexed Data and Address for reduced I/O count**
  - A15–A0 multiplexed as DQ15–DQ0
  - Addresses are latched by AVD# control input when CE# low
- **Simultaneous Read/Write operation**
  - Data can be continuously read from one bank while executing erase/program functions in other bank
  - Zero latency between read and write operations
- **Read access times at 66/54 MHz (C_L=30 pF)**
  - Burst access times of 11/13.5 ns at industrial temperature range
  - Asynchronous random access times of 65/70 ns
  - Synchronous random access times of 71/87.5 ns
- **Burst Modes**
  - Continuous linear burst
  - 8/16/32 word linear burst with wrap around
  - 8/16/32 word linear burst without wrap around
- **Power dissipation (typical values, 8 bits switching, C_L = 30 pF)**
  - Burst Mode Read: 25 mA
  - Simultaneous Operation: 40 mA
  - Program/Erase: 15 mA
  - Standby mode: 9 µA
- **Sector Architecture**
  - Four 8 Kword sectors
  - Two hundred fifty-five (S29NS128J), one hundred twenty-seven (S29NS064J),sixty-three (S29NS032J), or thirty-one (S29NS016J) 32 Kword sectors
  - Four banks (see next page for sector count and size)
- **Sector Protection**
  - Software command sector locking
  - WP# protects the two highest sectors
  - All sectors locked when V_{PP} = V_{IL}
- **Handshaking feature**
  - Provides host system with minimum possible latency by monitoring RDY
- **Supports Common Flash Memory Interface (CFI)**
- **Software command set compatible with JEDEC 42.4 standards**
  - Backwards compatible with Am29F and Am29LV families
- **Manufactured on 110 nm process technology**
- **Embedded Algorithms**
  - Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Data# Polling and toggle bits**
  - Provides a software method of detecting program and erase operation completion
- **Erase Suspend/Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset input (RESET#)**
  - Hardware method to reset the device for reading array data
- **CMOS compatible inputs and outputs**
- **Cycling Endurance: 1 million cycles per sector typical**
- **Data Retention: 20 years typical**

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General Description

The S29NS128J, S29NS064J, S29NS032J and S29NS016J are 128 Mbit, 64 Mbit, 32 Mbit and 16 Mbit. 1.8 Volt-only, Simultaneous Read/Write, Burst Mode Flash memory devices, organized as 8,388,608, 4,194,304, 2,097,152 and 1,048,576. words of 16 bits each. These devices use a single V_{CC} of 1.7 to 1.95 V to read, program, and erase the memory array. A 12.0-volt V_{PP} may be used for faster program performance if desired. These devices can also be programmed in standard EPROM programmers.

The devices are offered at the following speeds:

Clock Speed	Burst Access (ns)	Synch. Initial Access (ns)	Asynch. Initial Access (ns)	Output Loading
66 MHz	11	71	65	30 pF
54 MHz	13.5	87.5	70	

The devices operate within the temperature range of −25°C to +85°C, and are offered in Very Thin FBGA packages.

Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture divides the memory space into four banks. The device allows a host system to program or erase in one bank, then immediately and simultaneously read from another bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The devices are structured as shown in the following tables:

S29NS128J			
Bank A Sectors		Bank B, C & D Sectors	
Quantity	Size	Quantity	Size
4	8 Kwords	64	32 Kwords
63	32 Kwords		
32 Mbits total		96 Mbits total	

S29NS064J			
Bank A Sectors		Bank B, C & D Sectors	
Quantity	Size	Quantity	Size
4	8 Kwords	32	32 Kwords
31	32 Kwords		
16 Mbits total		48 Mbits total	

S29NS032J			
Bank A Sectors		Bank B, C & D Sectors	
Quantity	Size	Quantity	Size
4	8 Kwords	16	32 Kwords
15	32 Kwords		
8 Mbits total		24 Mbits total	

S29NS016J			
Bank A Sectors		Bank B, C & D Sectors	
Quantity	Size	Quantity	Size
4	8 Kwords	8	32 Kwords
7	32 Kwords		
4 Mbits total		12 Mbits total	

The devices use Chip Enable (CE#), Write Enable (WE#), Address Valid (AVD#) and Output Enable (OE#) to control asynchronous read and write operations. For burst operations, the devices additionally require Ready (RDY) and Clock (CLK). This implementation allows easy interface with minimal glue logic to microprocessors/microcontrollers for high performance read operations.

The devices offer complete compatibility with the **JEDEC 42.4 single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Reading data out of the device are similar to reading from other Flash or EPROM devices.

The host system can detect whether a program or erase operation is complete by using the device **status bit** DQ7 (Data# Polling) and DQ6/DQ2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The devices are fully erased when shipped from the factory.

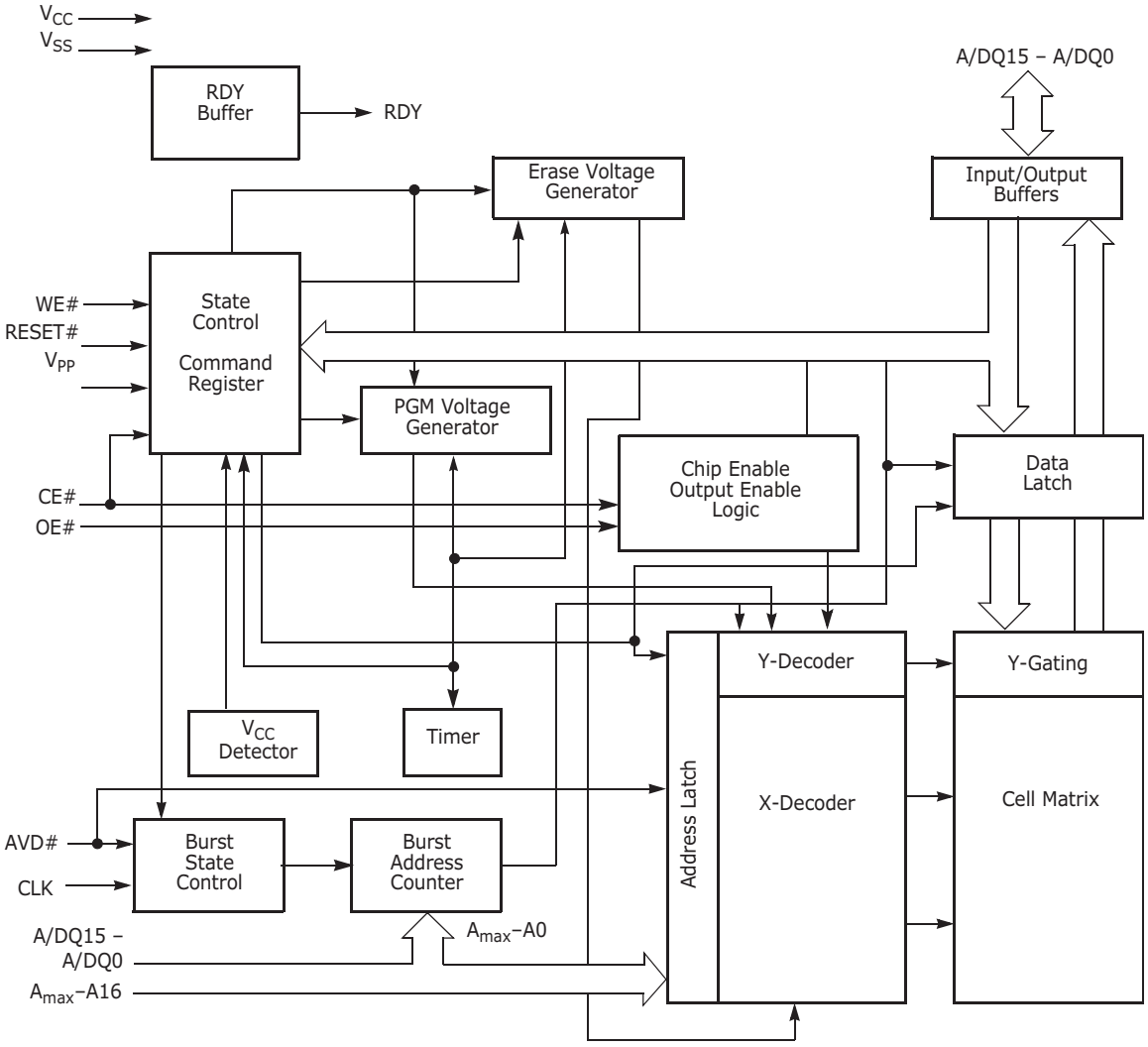
Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The devices also offer three types of data protection at the sector level. The **sector lock/unlock command sequence** disables or re-enables both program and erase operations in any sector. When at V_{IL}, **WP#** locks the highest two sectors. Finally, when **V_{PP}** is at V_{IL}, all sectors are locked.

The devices offer two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

6 Product Selector Guide

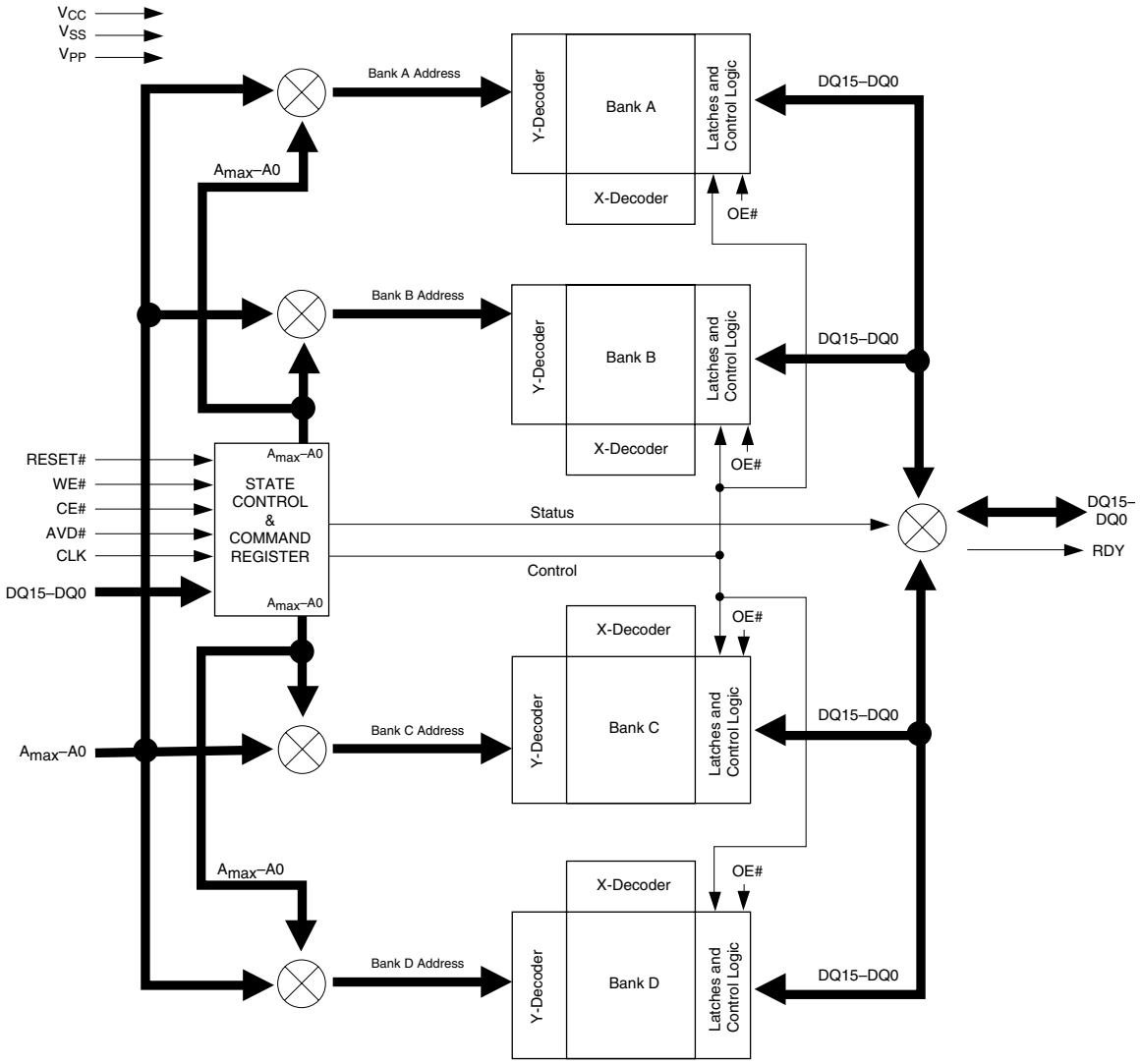
Part Number	S29NS128J, S29NS064J, S29N032J, 29NS016J	
Burst Frequency	**66 MHz**	**54 MHz**
Max Initial Synchronous Access Time, ns (T_{IACC})	71	87.5
Max Burst Access Time, ns (T_{BACC})	11	13.5
Max Asynchronous Access Time, ns (T_{ACC})	65	70
Max CE# Access Time, ns (T_{CE})		
Max OE# Access Time, ns (T_{OE})	11	13.5

7 Block Diagram



Note: *A_{max} indicates the highest order address bit.*

8 Block Diagram of Simultaneous Operation Circuit



Notes:

1. *A15–A0 are multiplexed with DQ15–DQ0.*
2. *Amax indicates the highest order address bit.*

9 Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 9.1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 9.1 Device Bus Operations

Operation	CE#	OE#	WE#	A_{max}–16	A/DQ15–0	RESET#	CLK	AVD#
Asynchronous Read	L	L	H	Addr In	I/O	H	L	
Write	L	H	L	Addr In	I/O	H	H/L	
Standby (CE#)	H	X	X	X	HIGH Z	H	H/L	X
Hardware Reset	X	X	X	X	HIGH Z	L	X	X
Burst Read Operations								
Load Starting Burst Address	L	H	H	Addr In	Addr In	H		
Advance Burst to next address with appropriate Data presented on the Data Bus	L	L	H	X	Burst Data Out	H		H
Terminate current Burst read cycle	H	X	H	X	HIGH Z	H		X
Terminate current Burst read cycle via RESET#	X	X	H	X	HIGH Z	L	X	X
Terminate current Burst read cycle and start new Burst read cycle	L	H	H	X	I/O	H		

Legend: *L = Logic 0, H = Logic 1, X = Don't Care.*

9.1 Requirements for Asynchronous Read Operation (Non-Burst)

To read data from the memory array, the system must assert a valid address on A/DQ15–A/DQ0 and A_{max}–A16, while AVD# and CE# are at V_{IL}. WE# should remain at V_{IH}. Note that CLK must remain at V_{IL} during asynchronous read operations. The rising edge of AVD# latches the address, after which the system can drive OE# to V_{IL}. The data will appear on A/DQ15–A/DQ0 (Figure 17.4). Since the memory array is divided into four banks, each bank remains enabled for read access until the command register contents are altered.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the outputs. The output enable access time (t_{OE}) is the delay from the falling edge of OE# to valid data at the output.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

9.2 Requirements for Synchronous (Burst) Read Operation

The device is capable of seven different burst read modes (Table 10.9): continuous burst read; 8-, 16-, and 32-word linear burst reads with wrap around; and 8-, 16-, and 32-word linear burst reads without wrap around.

9.2.1 Continuous Burst

When the device first powers up, it is enabled for asynchronous read operation. The device will automatically be enabled for burst mode and addresses will be latched on the first rising edge on the CLK input, while AVD# is held low for one clock cycle. Prior to activating the clock signal, the system should determine how many wait states are desired for the initial word (t_{IACC}) of each burst session. The system would then write the Set Configuration Register command sequence.

The initial word is output t_{IACC} after the rising edge of the first CLK cycle. Subsequent words are output t_{BACC} after the rising edge of each successive clock cycle, which automatically increments the internal address counter. **Note that the device has a fixed internal address boundary that occurs every 64 words, starting at address 00003Fh. The transition from the highest address to 000000h is also a boundary crossing**. During a boundary crossing, there is a two-cycle latency between the valid read at address 00003Eh and the valid read at address 00003Fh (or between addresses offset from these values by the same multiple of 64 words). RDY is deasserted during the two-cycle latency, and it is reasserted in the third cycle to indicate that the data at address 00003Fh (or offset from 3Fh by a multiple of 64 words) is ready (Figure 17.12).

The device will continue to output continuous, sequential burst data, wrapping around to address 000000h after it reaches the highest addressable memory location, until the system asserts CE# high, RESET# low, or AVD# low in conjunction with a new address. See Table 9.1. The reset command does *not* terminate the burst read operation.

If the host system crosses the bank boundary while reading in burst mode, and the device is not programming or erasing, a two-cycle latency will occur as described above. If the host system crosses the bank boundary while the device is programming or erasing, the device will provide asynchronous read status information. The clock will be ignored. After the host has completed status reads, or the device has completed the program or erase operation, the host can restart a burst operation using a new address and AVD# pulse.

If the clock frequency is less than 6 MHz during a burst mode operation, additional latencies will occur. RDY indicates the length of the latency by pulsing low.

9.2.2 8-, 16-, and 32-Word Linear Burst with Wrap Around

These three modes are of the linear wrap around design, in which a fixed number of words are read from consecutive addresses. In each of these modes, the burst addresses read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode (see Table 9.2.)

Table 9.2 Burst Address Groups

Mode	Group Size	Group Address Ranges
8-word	8 words	0-7h, 8-Fh, 10-17h, 18-1Fh...
16-word	16 words	0-Fh, 10-1Fh, 20-2Fh, 30-3Fh...
32-word	32 words	00-1Fh, 20-3Fh, 40-5Fh, 60-7Fh...

As an example: if the starting address in the 8-word mode is 39h, the address range to be read would be 38-3Fh, and the burst sequence would be 39-3A-3B-3C-3D-3E-3F-38h. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group. In a similar fashion, the 16-word and 32-word Linear Wrap modes begin their burst sequence on the starting address written to the device, and then wrap back to the first address in the selected address group. **Note that in these three burst read modes the address pointer does not cross the boundary that occurs every 64 words; thus, no wait states are inserted (except during the initial access).**

9.2.3 8-, 16-, and 32-Word Linear Burst without Wrap Around

In these modes, a fixed number of words (predefined as 8,16,or 32 words) are read from consecutive addresses starting with the initial word, which is written to the device. When the number of words has been read completely, the burst read operation stops and the RDY output goes low. There is no group limitation and is different from the Linear Burst with Wrap Around.

See Table 10.9 and Table 10.16 for the command of setting the 8-, 16-, and 32- Word Burst without Wrap Around.

As an example, for 8-word length Burst Read, if the starting address written to the device is 39h, the burst sequence would be 39-3A-3B-3C-3D-3E-3F-40h, and the read operation will be terminated at 40h. In a similar fashion, the 16-word and 32-word modes begin their burst sequence on the starting address written to the device, and Continuously Read to the predefined word length, 16 or 32 words.

The operation is similar to the Continuous Burst, but will stop the operation at fixed word length. It is possible the device crosses the fixed internal address boundary that occurs every 64 words during burst read; a latency occurs before data appears for the next address and RDY is pulsing low. If the host system crosses the bank boundary, the device will react in the same manner as in the Continuous Burst.

If the clock frequency is less than 6 MHz during a burst mode operation, additional latencies will occur. RDY indicates the length of the latency by pulsing low.

9.3 Programmable Wait State

The programmable wait state feature indicates to the device the number of additional clock cycles that must elapse after AVD# is driven active before data will be available. Upon power up, the device defaults to the maximum of seven total cycles. The total number of wait states is programmable from two to seven cycles.

The wait state command sequence requires three cycles; after the two unlock cycles, the third cycle address should be written according to the desired wait state as shown in Table 10.9. Address bits A11-A0 should be set to 555h, while addresses bits A17-A12 set the wait state. For further details, see Set Configuration Register Command Sequence.

9.3.1 Handshaking Feature

The handshaking feature allows the host system to simply monitor the RDY signal from the device to determine when the initial word of burst data is ready to be read. The host system should use the wait state command sequence to set the number of wait states for optimal burst mode operation (03h for 54 and 66 MHz clock). The initial word of burst data is indicated by the rising edge of RDY after OE# goes low.

The handshaking feature may be verified by writing the autoselect command sequence to the device. See Autoselect Command Sequence for details.

For optimal burst mode performance on devices without the handshaking option, the host system must set the appropriate number of wait states in the flash device depending on such factors as clock frequency, presence of a boundary crossing, or an odd or even starting address. See Set Configuration Register Command Sequence for more information.

The autoselect function allows the host system to distinguish flash devices that have handshaking from those that do not. See Autoselect Command Sequence for more information.

9.4 Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in one of the other three banks of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 17.15 shows how read and write cycles may be initiated for simultaneous operation with zero latency. See the DC Characteristics table for read-while-program and read-while-erase current specifications.

9.5 Writing Commands/Command Sequences

The device has inputs/outputs that accept both address and data information. To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive AVD# and CE# to V_{IL}, and OE# to V_{IH} when providing an address to the device, and drive WE# and CE# to V_{IL}, and OE# to V_{IH}. when writing commands or data.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 7 indicates the address space that each sector occupies. The device address space is divided into four banks: Bank A contains both 8 Kword boot sectors in addition to 32 Kword sectors, while Banks B, C, and D contain only 32 Kword sectors. A *bank address* is the address bits required to uniquely select a bank. Similarly, a *sector address* is the address bits required to uniquely select a sector.

Refer to the DC Characteristics table for write mode current specifications. RESET#: Hardware Reset Input contains timing specification tables and timing diagrams for write operations.

9.5.2 Accelerated Program Operation

The device offers accelerated program operations through the V_{PP} input. This function is primarily intended to allow faster manufacturing throughput at the factory. If the system asserts V_{ID} on this input, the device automatically enters the aforementioned Unlock Bypass mode and uses the higher voltage on the input to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{ID} from the V_{PP} input returns the device to normal operation.

9.5.3 Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. See Autoselect Functions and Autoselect Command Sequence for more information.

9.6 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# inputs are both held at V_{CC} ± 0.2 V. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the standby current specification.

9.7 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enters this mode when addresses remain stable for t_{ACC} + 60 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

9.8 RESET#: Hardware Reset Input

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.2 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.2 V, the standby current will be greater.

RESET# may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the device requires a time of t_{READYW} (during Embedded Algorithms) before the device is ready to read data again. If RESET# is asserted when a program or erase operation is not executing, the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after RESET# returns to V_{IH}.

See the AC Characteristics tables for RESET# parameters and to Figure 17.5 for the timing diagram.

9.8.4 V_{CC} Power-up and Power-down Sequencing

The device imposes no restrictions on V_{CC} power-up or power-down sequencing. Asserting RESET# to V_{IL} is required during the entire V_{CC} power sequence until the respective supplies reach their operating voltages. Once V_{CC} attains its operating voltage, de-assertion of RESET# to V_{IH} is permitted.

9.9 Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state.

9.10 Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 10.16 for command definitions).

The device offers three types of data protection at the sector level:

- The sector lock/unlock command sequence disables or re-enables both program and erase operations in any sector.
- When WP# is at V_{IL},
  - SA257 and SA258 are locked (S29NS128J)
  - SA129 and SA130 are locked (S29NS064J)
  - SA65 and SA66 are locked (S29NS032J)
  - SA33 and SA34 are locked (S29NS016J)
- When V_{PP} is at V_{IL}, all sectors are locked.

9.11 WP# Boot Sector Protection

The WP# signal will be latched at a specific time in the embedded program or erase sequence. To prevent a write to the top two sectors, WP# must be asserted (WP#=V_{IL}) on the last write cycle of the embedded sequence (i.e., 4th write cycle in embedded program, 6th write cycle in embedded erase).

If using the Unlock Bypass feature: on the 2nd program cycle, after the Unlock Bypass command is written, the WP# signal must be asserted on the 2nd cycle.

If selecting multiple sectors for erasure: The WP# protection status is latched only on the 6th write cycle of the embedded sector erase command sequence when the first sector is selected. If additional sectors are selected for erasure, they are subject to the WP# status that was latched on the 6th write cycle of the command sequence.

The following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

9.11.5 Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

9.11.6 Write Pulse *Glitch* Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

9.11.7 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

10 Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 10.1–10.4. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 10.1–10.4. The system must write the reset command to return the device to the autoselect mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, Contact your local Spansion sales office for copies of these documents.

Table 10.1 CFI Query Identification String

Addresses	Data				Description
	S29NS128J	S29NS064J	S29NS032J	S29NS016J	
10h 11h 12h	0051h 0052h 0059h				Query Unique ASCII string *QRY*
13h 14h	0002h 0000h				Primary OEM Command Set
15h 16h	0040h 0000h				Address for Primary Extended Table
17h 18h	0000h 0000h				Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h				Address for Alternate OEM Extended Table (00h = none exists)

Table 10.2 System Interface String

Addresses	Data				Description
	S29NS128J	S29NS064J	S29NS032J	S29NS016J	
1Bh	0017h				V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0019h				V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h				V_{PP} Min. voltage (00h = no V_{PP} pin present) Refer to 4Dh
1Eh	0000h				V_{PP} Max. voltage (00h = no V_{PP} pin present) Refer to 4Eh
1Fh	0003h				Typical timeout per single byte/word write 2^N µs
20h	0000h				Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	0009h				Typical timeout per individual block erase 2^N ms
22h	0000h				Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0005h				Max. timeout for byte/word write 2^N times typical
24h	0000h				Max. timeout for buffer write 2^N times typical
25h	0004h				Max. timeout per individual block erase 2^N times typical
26h	0000h				Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 10.3 Device Geometry Definition

Addresses	Data				Description
	S29NS128J	S29NS064J	S29NS032J	S29NS016J	
27h	0018h	0017h	0016h	0015h	Device Size = 2^N byte
28h 29h	0001h 0000h				Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0000h 0000h				Max. number of bytes in multi-byte write = 2^N (00h = not supported)
2Ch	0002h				Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	00FEh 0000h 0000h 0001h	007Eh 0000h 0000h 0001h	003Eh 0000h 0000h 0001h	001Eh 0000h 0000h 0001h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	0003h 0000h 0040h 0000h				Erase Block Region 2 Information
35h 36h 37h 38h	0000h 0000h 0000h 0000h				Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h				Erase Block Region 4 Information

Table 10.4 Primary Vendor-Specific Extended Query

Addresses	Data				Description
	S29NS128J	S29NS064J	S29NS032J	S29NS016J	
40h 41h 42h	0050h 0052h 0049h				Query-unique ASCII string *PRI*
43h	0031h				Major version number, ASCII
44h	0033h				Minor version number, ASCII
45h	0000h				Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Revision Number (Bits 7-2)
46h	0002h				Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h				Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0000h				Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0005h				Sector Protect/Unprotect scheme 05 = 29BDS/N128 mode
4Ah	00C0h	0060h	0030h	0018h	Simultaneous Operation Number of Sectors in all banks except boot bank
4Bh	0001h				Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0000h				Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	00B5h				ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	00C5h				ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0003h				Top/Bottom Boot Sector Flag 0001h = Top/Middle Boot Device, 0002h = Bottom Boot Device, 03h = Top Boot Device
50h	0000h				Program Suspend. 00h = not supported
57h	0004h				Bank Organization: X = Number of banks
58h	0040h	0020h	0010h	0008h	Bank D Region Information. X = Number of sectors in bank
59h	0040h	0020h	0010h	0008h	Bank C Region Information. X = Number of sectors in bank
5Ah	0040h	0020h	0010h	0008h	Bank B Region Information. X = Number of sectors in bank
5Bh	0043h	0023h	0013h	0008h	Bank A Region Information. X = Number of sectors in bank
5Ch	0002h				Process Technology. 00h = 230 nm, 01h = 170 nm, 02h = 130 nm/110 nm

Table I0.5 Sector Address Table, S29NSI28J

Sector	Sector Size	Address Range	Sector	Sector Size	Address Range	Sector	Sector Size	Address Range
Bank D								
SA0	32 Kwords	000000h–007FFFh	SA22	32 Kwords	0B0000h–0B7FFFh	SA43	32 Kwords	158000h–15FFFFh
SA1	32 Kwords	008000h–00FFFFh	SA23	32 Kwords	0B8000h–0BFFFFh	SA44	32 Kwords	160000h–167FFFh
SA2	32 Kwords	010000h–017FFFh	SA24	32 Kwords	0C0000h–0C7FFFh	SA45	32 Kwords	168000h–16FFFFh
SA3	32 Kwords	018000h–01FFFFh	SA25	32 Kwords	0C8000h–0CFFFFh	SA46	32 Kwords	170000h–177FFFh
SA4	32 Kwords	020000h–027FFFh	SA26	32 Kwords	0D0000h–0D7FFFh	SA47	32 Kwords	178000h–17FFFFh
SA5	32 Kwords	028000h–02FFFFh	SA27	32 Kwords	0D8000h–0DFFFFh	SA48	32 Kwords	180000h–187FFFh
SA6	32 Kwords	030000h–037FFFh	SA28	32 Kwords	0E0000h–0E7FFFh	SA49	32 Kwords	188000h–18FFFFh
SA7	32 Kwords	038000h–03FFFFh	SA29	32 Kwords	0E8000h–0EFFFFh	SA50	32 Kwords	190000h–197FFFh
SA8	32 Kwords	040000h–047FFFh	SA30	32 Kwords	0F0000h–0F7FFFh	SA51	32 Kwords	198000h–19FFFFh
SA9	32 Kwords	048000h–04FFFFh	SA31	32 Kwords	0F8000h–0FFFFFh	SA52	32 Kwords	1A0000h–1A7FFFh
SA10	32 Kwords	050000h–057FFFh	SA32	32 Kwords	100000h–107FFFh	SA53	32 Kwords	1A8000h–1AFFFFh
SA11	32 Kwords	058000h–05FFFFh	SA33	32 Kwords	108000h–10FFFFh	SA54	32 Kwords	1B0000h–1B7FFFh
SA12	32 Kwords	060000h–067FFFh	SA34	32 Kwords	110000h–117FFFh	SA55	32 Kwords	1B8000h–1BFFFFh
SA13	32 Kwords	068000h–06FFFFh	SA35	32 Kwords	118000h–11FFFFh	SA56	32 Kwords	1C0000h–1C7FFFh
SA14	32 Kwords	070000h–077FFFh	SA36	32 Kwords	120000h–127FFFh	SA57	32 Kwords	1C8000h–1CFFFFh
SA15	32 Kwords	078000h–07FFFFh	SA37	32 Kwords	128000h–12FFFFh	SA58	32 Kwords	1D0000h–1D7FFFh
SA16	32 Kwords	080000h–087FFFh	SA38	32 Kwords	130000h–137FFFh	SA59	32 Kwords	1D8000h–1DFFFFh
SA17	32 Kwords	088000h–08FFFFh	SA39	32 Kwords	138000h–13FFFFh	SA60	32 Kwords	1E0000h–1E7FFFh
SA18	32 Kwords	090000h–097FFFh	SA40	32 Kwords	140000h–147FFFh	SA61	32 Kwords	1E8000h–1EFFFFh
SA19	32 Kwords	098000h–09FFFFh	SA41	32 Kwords	148000h–14FFFFh	SA62	32 Kwords	1F0000h–1F7FFFh
SA20	32 Kwords	0A0000h–0A7FFFh	SA42	32 Kwords	150000h–157FFFh	SA63	32 Kwords	1F8000h–1FFFFFh
SA21	32 Kwords	0A8000h–0AFFFFh						
Bank C								
SA64	32 Kwords	200000h–207FFFh	SA85	32 Kwords	2A8000h–2AFFFFh	SA106	32 Kwords	350000h–357FFFh
SA65	32 Kwords	208000h–20FFFFh	SA86	32 Kwords	2B0000h–2B7FFFh	SA107	32 Kwords	358000h–35FFFFh
SA66	32 Kwords	210000h–217FFFh	SA87	32 Kwords	2B8000h–2BFFFFh	SA108	32 Kwords	360000h–367FFFh
SA67	32 Kwords	218000h–21FFFFh	SA88	32 Kwords	2C0000h–2C7FFFh	SA109	32 Kwords	368000h–36FFFFh
SA68	32 Kwords	220000h–227FFFh	SA89	32 Kwords	2C8000h–2CFFFFh	SA110	32 Kwords	370000h–377FFFh
SA69	32 Kwords	228000h–22FFFFh	SA90	32 Kwords	2D0000h–2D7FFFh	SA111	32 Kwords	378000h–37FFFFh
SA70	32 Kwords	230000h–237FFFh	SA91	32 Kwords	2D8000h–2DFFFFh	SA112	32 Kwords	380000h–387FFFh
SA71	32 Kwords	238000h–23FFFFh	SA92	32 Kwords	2E0000h–2E7FFFh	SA113	32 Kwords	388000h–38FFFFh
SA72	32 Kwords	240000h–247FFFh	SA93	32 Kwords	2E8000h–2EFFFFh	SA114	32 Kwords	390000h–397FFFh
SA73	32 Kwords	248000h–24FFFFh	SA94	32 Kwords	2F0000h–2F7FFFh	SA115	32 Kwords	398000h–39FFFFh
SA74	32 Kwords	250000h–257FFFh	SA95	32 Kwords	2F8000h–2FFFFFh	SA117	32 Kwords	3A8000h–3AFFFFh
SA75	32 Kwords	258000h–25FFFFh	SA96	32 Kwords	300000h–307FFFh	SA118	32 Kwords	3B0000h–3B7FFFh
SA76	32 Kwords	260000h–267FFFh	SA97	32 Kwords	308000h–30FFFFh	SA119	32 Kwords	3B8000h–3BFFFFh
SA77	32 Kwords	268000h–26FFFFh	SA98	32 Kwords	310000h–317FFFh	SA120	32 Kwords	3C0000h–3C7FFFh
SA78	32 Kwords	270000h–277FFFh	SA99	32 Kwords	318000h–31FFFFh	SA121	32 Kwords	3C8000h–3CFFFFh
SA79	32 Kwords	278000h–27FFFFh	SA100	32 Kwords	320000h–327FFFh	SA122	32 Kwords	3D0000h–3D7FFFh
SA80	32 Kwords	280000h–287FFFh	SA101	32 Kwords	328000h–32FFFFh	SA123	32 Kwords	3D8000h–3DFFFFh
SA81	32 Kwords	288000h–28FFFFh	SA102	32 Kwords	330000h–337FFFh	SA124	32 Kwords	3E0000h–3E7FFFh
SA82	32 Kwords	290000h–297FFFh	SA103	32 Kwords	338000h–33FFFFh	SA125	32 Kwords	3E8000h–3EFFFFh
SA83	32 Kwords	298000h–29FFFFh	SA104	32 Kwords	340000h–347FFFh	SA126	32 Kwords	3F0000h–3F7FFFh
SA84	32 Kwords	2A0000h–2A7FFFh	SA105	32 Kwords	348000h–34FFFFh	SA127	32 Kwords	3F8000h–3FFFFFh

Table 10.5 Sector Address Table, S29NS128J (Continued)

Sector	Sector Size	Address Range	Sector	Sector Size	Address Range	Sector	Sector Size	Address Range
				Bank B				
SA128	32 Kwords	400000h–407FFFh	SA150	32 Kwords	4B0000h–4B7FFFh	SA171	32 Kwords	558000h–55FFFFh
SA129	32 Kwords	408000h–40FFFFh	SA151	32 Kwords	4B8000h–4BFFFFh	SA172	32 Kwords	560000h–567FFFh
SA130	32 Kwords	410000h–417FFFh	SA152	32 Kwords	4C0000h–4C7FFFh	SA173	32 Kwords	568000h–56FFFFh
SA131	32 Kwords	418000h–41FFFFh	SA153	32 Kwords	4C8000h–4CFFFFh	SA174	32 Kwords	570000h–577FFFh
SA132	32 Kwords	420000h–427FFFh	SA154	32 Kwords	4D0000h–4D7FFFh	SA175	32 Kwords	578000h–57FFFFh
SA133	32 Kwords	428000h–42FFFFh	SA155	32 Kwords	4D8000h–4DFFFFh	SA176	32 Kwords	580000h–587FFFh
SA134	32 Kwords	420000h–427FFFh	SA156	32 Kwords	4E0000h–4E7FFFh	SA177	32 Kwords	588000h–58FFFFh
SA135	32 Kwords	438000h–43FFFFh	SA157	32 Kwords	4E8000h–4EFFFFh	SA178	32 Kwords	590000h–597FFFh
SA136	32 Kwords	430000h–437FFFh	SA158	32 Kwords	4F0000h–4F7FFFh	SA179	32 Kwords	598000h–59FFFFh
SA137	32 Kwords	448000h–44FFFFh	SA159	32 Kwords	4F8000h–4FFFFFh	SA180	32 Kwords	5A0000h–5A7FFFh
SA138	32 Kwords	450000h–457FFFh	SA160	32 Kwords	500000h–507FFFh	SA181	32 Kwords	5A8000h–5AFFFFh
SA139	32 Kwords	458000h–45FFFFh	SA161	32 Kwords	508000h–50FFFFh	SA182	32 Kwords	5B0000h–5B7FFFh
SA140	32 Kwords	460000h–467FFFh	SA162	32 Kwords	510000h–517FFFh	SA183	32 Kwords	5B8000h–5BFFFFh
SA141	32 Kwords	468000h–46FFFFh	SA163	32 Kwords	518000h–51FFFFh	SA184	32 Kwords	5C0000h–5C7FFFh
SA142	32 Kwords	470000h–477FFFh	SA164	32 Kwords	520000h–527FFFh	SA185	32 Kwords	5C8000h–5CFFFFh
SA143	32 Kwords	478000h–47FFFFh	SA165	32 Kwords	528000h–52FFFFh	SA186	32 Kwords	5D0000h–5D7FFFh
SA144	32 Kwords	480000h–487FFFh	SA166	32 Kwords	530000h–537FFFh	SA187	32 Kwords	5D8000h–5DFFFFh
SA145	32 Kwords	488000h–48FFFFh	SA167	32 Kwords	538000h–53FFFFh	SA188	32 Kwords	5E0000h–5E7FFFh
SA146	32 Kwords	490000h–497FFFh	SA168	32 Kwords	540000h–547FFFh	SA189	32 Kwords	5E8000h–5EFFFFh
SA147	32 Kwords	498000h–49FFFFh	SA169	32 Kwords	548000h–54FFFFh	SA190	32 Kwords	5F0000h–5F7FFFh
SA148	32 Kwords	4A0000h–4A7FFFh	SA170	32 Kwords	550000h–557FFFh	SA191	32 Kwords	5F8000h–5FFFFFh
SA149	32 Kwords	4A8000h–4AFFFFh						
				Bank A				
SA192	32 Kwords	600000h–607FFFh	SA215	32 Kwords	6B8000h–6BFFFFh	SA237	32 Kwords	768000h–76FFFFh
SA193	32 Kwords	608000h–60FFFFh	SA216	32 Kwords	6C0000h–6C7FFFh	SA238	32 Kwords	770000h–777FFFh
SA194	32 Kwords	610000h–617FFFh	SA217	32 Kwords	6C8000h–6CFFFFh	SA239	32 Kwords	778000h–77FFFFh
SA195	32 Kwords	618000h–61FFFFh	SA218	32 Kwords	6D0000h–6D7FFFh	SA240	32 Kwords	780000h–787FFFh
SA196	32 Kwords	620000h–627FFFh	SA219	32 Kwords	6D8000h–6DFFFFh	SA241	32 Kwords	788000h–78FFFFh
SA197	32 Kwords	628000h–62FFFFh	SA220	32 Kwords	6E0000h–6E7FFFh	SA242	32 Kwords	790000h–797FFFh
SA198	32 Kwords	630000h–637FFFh	SA221	32 Kwords	6E8000h–6EFFFFh	SA243	32 Kwords	798000h–79FFFFh
SA199	32 Kwords	638000h–63FFFFh	SA222	32 Kwords	6F0000h–6F7FFFh	SA244	32 Kwords	7A0000h–7A7FFFh
SA200	32 Kwords	640000h–647FFFh	SA223	32 Kwords	6F8000h–6FFFFFh	SA245	32 Kwords	7A8000h–7AFFFFh
SA201	32 Kwords	648000h–64FFFFh	SA224	32 Kwords	700000h–707FFFh	SA246	32 Kwords	7B0000h–7B7FFFh
SA202	32 Kwords	650000h–657FFFh	SA225	32 Kwords	708000h–70FFFFh	SA247	32 Kwords	7B8000h–7BFFFFh
SA203	32 Kwords	658000h–65FFFFh	SA226	32 Kwords	710000h–717FFFh	SA248	32 Kwords	7C0000h–7C7FFFh
SA204	32 Kwords	660000h–667FFFh	SA227	32 Kwords	718000h–71FFFFh	SA249	32 Kwords	7C8000h–7CFFFFh
SA205	32 Kwords	668000h–66FFFFh	SA228	32 Kwords	720000h–727FFFh	SA250	32 Kwords	7D0000h–7D7FFFh
SA206	32 Kwords	670000h–677FFFh	SA229	32 Kwords	728000h–72FFFFh	SA251	32 Kwords	7D8000h–7DFFFFh
SA207	32 Kwords	678000h–67FFFFh	SA230	32 Kwords	730000h–737FFFh	SA252	32 Kwords	7E0000h–7E7FFFh
SA208	32 Kwords	680000h–687FFFh	SA231	32 Kwords	738000h–73FFFFh	SA253	32 Kwords	7E8000h–7EFFFFh
SA209	32 Kwords	688000h–68FFFFh	SA232	32 Kwords	740000h–747FFFh	SA254	32 Kwords	7F0000h–7F7FFFh
SA210	32 Kwords	690000h–697FFFh	SA233	32 Kwords	748000h–74FFFFh	SA255	8 Kwords	7F8000h–7F9FFFh
SA211	32 Kwords	698000h–69FFFFh	SA234	32 Kwords	750000h–757FFFh	SA256	8 Kwords	7FA000h–7FBFFFh
SA212	32 Kwords	6A0000h–6A7FFFh	SA235	32 Kwords	758000h–75FFFFh	SA257	8 Kwords	7FC000h–7FDFFFh
SA213	32 Kwords	6A8000h–6AFFFFh	SA236	32 Kwords	760000h–767FFFh	SA258	8 Kwords	7FE000h–7FFFFFh
SA214	32 Kwords	6B0000h–6B7FFFh						

Table I0.6 Sector Address Table, S29NS064J

Sector	Sector Size	Address Range	Sector	Sector Size	Address Range	Sector	Sector Size	Address Range
				Bank D				
SA0	32 Kwords	000000h–007FFFh	SA11	32 Kwords	058000h–05FFFFh	SA22	32 Kwords	0B0000h–0B7FFFh
SA1	32 Kwords	008000h–00FFFFh	SA12	32 Kwords	060000h–067FFFh	SA23	32 Kwords	0B8000h–0BFFFFh
SA2	32 Kwords	010000h–017FFFh	SA13	32 Kwords	068000h–06FFFFh	SA24	32 Kwords	0C0000h–0C7FFFh
SA3	32 Kwords	018000h–01FFFFh	SA14	32 Kwords	070000h–077FFFh	SA25	32 Kwords	0C8000h–0CFFFFh
SA4	32 Kwords	020000h–027FFFh	SA15	32 Kwords	078000h–07FFFFh	SA26	32 Kwords	0D0000h–0D7FFFh
SA5	32 Kwords	028000h–02FFFFh	SA16	32 Kwords	080000h–087FFFh	SA27	32 Kwords	0D8000h–0DFFFFh
SA6	32 Kwords	030000h–037FFFh	SA17	32 Kwords	088000h–08FFFFh	SA28	32 Kwords	0E0000h–0E7FFFh
SA7	32 Kwords	038000h–03FFFFh	SA18	32 Kwords	090000h–097FFFh	SA29	32 Kwords	0E8000h–0EFFFFh
SA8	32 Kwords	040000h–047FFFh	SA19	32 Kwords	098000h–09FFFFh	SA30	32 Kwords	0F0000h–0F7FFFh
SA9	32 Kwords	048000h–04FFFFh	SA20	32 Kwords	0A0000h–0A7FFFh	SA31	32 Kwords	0F8000h–0FFFFFh
SA10	32 Kwords	050000h–057FFFh	SA21	32 Kwords	0A8000h–0AFFFFh			
				Bank C				
SA32	32 Kwords	100000h–107FFFh	SA43	32 Kwords	158000h–15FFFFh	SA54	32 Kwords	1B0000h–1B7FFFh
SA33	32 Kwords	108000h–10FFFFh	SA44	32 Kwords	160000h–167FFFh	SA55	32 Kwords	1B8000h–1BFFFFh
SA34	32 Kwords	110000h–117FFFh	SA45	32 Kwords	168000h–16FFFFh	SA56	32 Kwords	1C0000h–1C7FFFh
SA35	32 Kwords	118000h–11FFFFh	SA46	32 Kwords	170000h–177FFFh	SA57	32 Kwords	1C8000h–1CFFFFh
SA36	32 Kwords	120000h–127FFFh	SA47	32 Kwords	178000h–17FFFFh	SA58	32 Kwords	1D0000h–1D7FFFh
SA37	32 Kwords	128000h–12FFFFh	SA48	32 Kwords	180000h–187FFFh	SA59	32 Kwords	1D8000h–1DFFFFh
SA38	32 Kwords	130000h–137FFFh	SA49	32 Kwords	188000h–18FFFFh	SA60	32 Kwords	1E0000h–1E7FFFh
SA39	32 Kwords	138000h–13FFFFh	SA50	32 Kwords	190000h–197FFFh	SA61	32 Kwords	1E8000h–1EFFFFh
SA40	32 Kwords	140000h–147FFFh	SA51	32 Kwords	198000h–19FFFFh	SA62	32 Kwords	1F0000h–1F7FFFh
SA41	32 Kwords	148000h–14FFFFh	SA52	32 Kwords	1A0000h–1A7FFFh	SA63	32 Kwords	1F8000h–1FFFFFh
SA42	32 Kwords	150000h–157FFFh	SA53	32 Kwords	1A8000h–1AFFFFh			
				Bank B				
SA64	32 Kwords	200000h–207FFFh	SA75	32 Kwords	258000h–25FFFFh	SA86	32 Kwords	2B0000h–2B7FFFh
SA65	32 Kwords	208000h–20FFFFh	SA76	32 Kwords	260000h–267FFFh	SA87	32 Kwords	2B8000h–2BFFFFh
SA66	32 Kwords	210000h–217FFFh	SA77	32 Kwords	268000h–26FFFFh	SA88	32 Kwords	2C0000h–2C7FFFh
SA67	32 Kwords	218000h–21FFFFh	SA78	32 Kwords	270000h–277FFFh	SA89	32 Kwords	2C8000h–2CFFFFh
SA68	32 Kwords	220000h–227FFFh	SA79	32 Kwords	278000h–27FFFFh	SA90	32 Kwords	2D0000h–2D7FFFh
SA69	32 Kwords	228000h–22FFFFh	SA80	32 Kwords	280000h–287FFFh	SA91	32 Kwords	2D8000h–2DFFFFh
SA70	32 Kwords	230000h–237FFFh	SA81	32 Kwords	288000h–28FFFFh	SA92	32 Kwords	2E0000h–2E7FFFh
SA71	32 Kwords	238000h–23FFFFh	SA82	32 Kwords	290000h–297FFFh	SA93	32 Kwords	2E8000h–2EFFFFh
SA72	32 Kwords	240000h–247FFFh	SA83	32 Kwords	298000h–29FFFFh	SA94	32 Kwords	2F0000h–2F7FFFh
SA73	32 Kwords	248000h–24FFFFh	SA84	32 Kwords	2A0000h–2A7FFFh	SA95	32 Kwords	2F8000h–2FFFFFh
SA74	32 Kwords	250000h–257FFFh	SA85	32 Kwords	2A8000h–2AFFFFh			
				Bank A				
SA96	32 Kwords	300000h–307FFFh	SA108	32 Kwords	360000h–367FFFh	SA120	32 Kwords	3C0000h–3C7FFFh
SA97	32 Kwords	308000h–30FFFFh	SA109	32 Kwords	368000h–36FFFFh	SA121	32 Kwords	3C8000h–3CFFFFh
SA98	32 Kwords	310000h–317FFFh	SA110	32 Kwords	370000h–377FFFh	SA122	32 Kwords	3D0000h–3D7FFFh
SA99	32 Kwords	318000h–31FFFFh	SA111	32 Kwords	378000h–37FFFFh	SA123	32 Kwords	3D8000h–3DFFFFh
SA100	32 Kwords	320000h–327FFFh	SA112	32 Kwords	380000h–387FFFh	SA124	32 Kwords	3E0000h–3E7FFFh
SA101	32 Kwords	328000h–32FFFFh	SA113	32 Kwords	388000h–38FFFFh	SA125	32 Kwords	3E8000h–3EFFFFh
SA102	32 Kwords	330000h–337FFFh	SA114	32 Kwords	390000h–397FFFh	SA126	32 Kwords	3F0000h–3F7FFFh
SA103	32 Kwords	338000h–33FFFFh	SA115	32 Kwords	398000h–39FFFFh	SA127	8 Kwords	3F8000h–3F9FFFh
SA104	32 Kwords	340000h–347FFFh	SA116	32 Kwords	3A0000h–3A7FFFh	SA128	8 Kwords	3FA000h–3FBFFFh
SA105	32 Kwords	348000h–34FFFFh	SA117	32 Kwords	3A8000h–3AFFFFh	SA129	8 Kwords	3FC000h–3FDFFFh
SA106	32 Kwords	350000h–357FFFh	SA118	32 Kwords	3B0000h–3B7FFFh	SA130	8 Kwords	3FE000h–3FFFFFh
SA107	32 Kwords	358000h–35FFFFh	SA119	32 Kwords	3B8000h–3BFFFFh			

Table 10.7 Sector Address Table, S29NS032J

Sector	Sector Size	Address Range	Sector	Sector Size	Address Range	Sector	Sector Size	Address Range
				Bank D				
SA0	32 Kwords	000000h–007FFFh	SA6	32 Kwords	030000h–037FFFh	SA11	32 Kwords	058000h–05FFFFh
SA1	32 Kwords	008000h–00FFFFh	SA7	32 Kwords	038000h–03FFFFh	SA12	32 Kwords	060000h–067FFFh
SA2	32 Kwords	010000h–017FFFh	SA8	32 Kwords	040000h–047FFFh	SA13	32 Kwords	068000h–06FFFFh
SA3	32 Kwords	018000h–01FFFFh	SA9	32 Kwords	048000h–04FFFFh	SA14	32 Kwords	070000h–077FFFh
SA4	32 Kwords	020000h–027FFFh	SA10	32 Kwords	050000h–057FFFh	SA15	32 Kwords	078000h–07FFFFh
SA5	32 Kwords	028000h–02FFFFh						
				Bank C				
SA16	32 Kwords	080000h–087FFFh	SA22	32 Kwords	0B0000h–0B7FFFh	SA27	32 Kwords	0D8000h–0DFFFFh
SA17	32 Kwords	088000h–08FFFFh	SA23	32 Kwords	0B8000h–0BFFFFh	SA28	32 Kwords	0E0000h–0E7FFFh
SA18	32 Kwords	090000h–097FFFh	SA24	32 Kwords	0C0000h–0C7FFFh	SA29	32 Kwords	0E8000h–0EFFFFh
SA19	32 Kwords	098000h–09FFFFh	SA25	32 Kwords	0C8000h–0CFFFFh	SA30	32 Kwords	0F0000h–0F7FFFh
SA20	32 Kwords	0A0000h–0A7FFFh	SA26	32 Kwords	0D0000h–0D7FFFh	SA31	32 Kwords	0F8000h–0FFFFFh
SA21	32 Kwords	0A8000h–0AFFFFh						
				Bank B				
SA32	32 Kwords	100000h–107FFFh	SA38	32 Kwords	130000h–137FFFh	SA43	32 Kwords	158000h–15FFFFh
SA33	32 Kwords	108000h–10FFFFh	SA39	32 Kwords	138000h–13FFFFh	SA44	32 Kwords	160000h–167FFFh
SA34	32 Kwords	110000h–117FFFh	SA40	32 Kwords	140000h–147FFFh	SA45	32 Kwords	168000h–16FFFFh
SA35	32 Kwords	118000h–11FFFFh	SA41	32 Kwords	148000h–14FFFFh	SA46	32 Kwords	170000h–177FFFh
SA36	32 Kwords	120000h–127FFFh	SA42	32 Kwords	150000h–157FFFh	SA47	32 Kwords	178000h–17FFFFh
SA37	32 Kwords	128000h–12FFFFh						
				Bank A				
SA48	32 Kwords	180000h–187FFFh	SA55	32 Kwords	1B8000h–1BFFFFh	SA61	32 Kwords	1E8000h–1EFFFFh
SA49	32 Kwords	188000h–18FFFFh	SA56	32 Kwords	1C0000h–1C7FFFh	SA62	32 Kwords	1F0000h–1F7FFFh
SA50	32 Kwords	190000h–197FFFh	SA57	32 Kwords	1C8000h–1CFFFFh	SA63	8 Kwords	1F8000h–1F9FFFh
SA51	32 Kwords	198000h–19FFFFh	SA58	32 Kwords	1D0000h–1D7FFFh	SA64	8 Kwords	1FA000h–1FBFFFh
SA52	32 Kwords	1A0000h–1A7FFFh	SA59	32 Kwords	1D8000h–1DFFFFh	SA65	8 Kwords	1FC000h–1FDFFFh
SA53	32 Kwords	1A8000h–1AFFFFh	SA60	32 Kwords	1E0000h–1E7FFFh	SA66	8 Kwords	1FE000h–1FFFFFh
SA54	32 Kwords	1B0000h–1B7FFFh						

Table 10.8 Sector Address Table, S29NS016J

Sector	Sector Size	Address Range	Sector	Sector Size	Address Range	Sector	Sector Size	Address Range
				Bank D				
SA0	32 Kwords	000000h–007FFFh	SA3	32 Kwords	018000h–01FFFFh	SA6	32 Kwords	030000h–037FFFh
SA1	32 Kwords	008000h–00FFFFh	SA4	32 Kwords	020000h–027FFFh	SA7	32 Kwords	038000h–03FFFFh
SA2	32 Kwords	010000h–017FFFh	SA5	32 Kwords	028000h–02FFFFh			
				Bank C				
SA8	32 Kwords	040000h–047FFFh	SA11	32 Kwords	058000h–05FFFFh	SA14	32 Kwords	070000h–077FFFh
SA9	32 Kwords	048000h–04FFFFh	SA12	32 Kwords	060000h–067FFFh	SA15	32 Kwords	078000h–07FFFFh
SA10	32 Kwords	050000h–057FFFh	SA13	32 Kwords	068000h–06FFFFh			
				Bank B				
SA16	32 Kwords	080000h–087FFFh	SA19	32 Kwords	098000h–09FFFFh	SA22	32 Kwords	0B0000h–0B7FFFh
SA17	32 Kwords	088000h–08FFFFh	SA20	32 Kwords	0A0000h–0A7FFFh	SA23	32 Kwords	0B8000h–0BFFFFh
SA18	32 Kwords	090000h–097FFFh	SA21	32 Kwords	0A8000h–0AFFFFh			
				Bank A				
SA24	32 Kwords	0C0000h–0C7FFFh	SA28	32 Kwords	0E0000h–0E7FFFh	SA32	8 Kwords	0FA000h–0FBFFFh
SA25	32 Kwords	0C8000h–0CFFFFh	SA29	32 Kwords	0E8000h–0EFFFFh	SA33	8 Kwords	0FC000h–0FDFFFh
SA26	32 Kwords	0D0000h–0D7FFFh	SA30	32 Kwords	0F0000h–0F7FFFh	SA34	8 Kwords	0FE000h–0FFFFFh
SA27	32 Kwords	0D8000h–0DFFFFh	SA31	8 Kwords	0F8000h–0F9FFFh			

10.1 Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 10.16 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the rising edge of AVD#. All data is latched on the rising edge of WE#. See AC Characteristics for timing diagrams.

10.2 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data in asynchronous mode. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See Erase Suspend/Erase Resume Commands for more information.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See Reset Command, for more information.

See also Requirements for Asynchronous Read Operation (Non-Burst) and Requirements for Synchronous (Burst) Read Operation in Device Bus Operations for more information. The Asynchronous Read and Synchronous/Burst Read tables provide the read parameters, and Figure 17.2 and Figure 17.4 show the timings.

10.3 Set Configuration Register Command Sequence

The configuration register command sequence instructs the device to set a particular number of clock cycles for the initial access in burst mode. The number of wait states that should be programmed into the device is directly related to the clock frequency. The first two cycles of the command sequence are for unlock purposes. On the third cycle, the system should write C0h to the address associated with the intended wait state setting (see Table 10.9). Address bits A17–A12 determine the setting. Note that addresses A_{max} – A18 are shown as *0* but are actually don't care.

Table 10.9 Burst Mode

Burst Mode ↓	Third Cycle Addresses for Wait States						
	Wait States→	**0**	**1**	**2**	**3**	**4**	**5**
	Clock Cycles→	**2**	**3**	**4**	**5**	**6**	**7**
Continuous		00555h	01555h	02555h	03555h	04555h	05555h
8-word Linear (wrap around)		08555h	09555h	0A555h	0B555h	0C555h	0D555h
16-word Linear (wrap around)		10555h	11555h	12555h	13555h	14555h	15555h
32-word Linear (wrap around)		18555h	19555h	1A555h	1B555h	1C555h	1D555h
8-word Linear (no wrap around)		28555h	29555h	2A555h	2B555h	2C555h	2D555h
16-word Linear (no wrap around)		30555h	31555h	32555h	33555h	34555h	35555h
32-word Linear (no wrap around)		38555h	39555h	3A555h	3B555h	3C555h	3D555h

Note: *The burst mode is set in the third cycle of the Set Wait State command sequence.*

The device defaults to the maximum seven cycle wait state setting at power up. It is recommended that the wait state command sequence be written, even if the default wait state value is desired, to ensure the device is set as expected. A hardware reset will set the wait state to the default setting.

10.3.1 Handshaking Feature

The host system should set address bits A17–A12 to *000011* for a clock frequency of 54 or 66 MHz, assuming continuous burst is desired in both cases, for optimal burst operation.

Table 10.10 describes the typical number of clock cycles (wait states) for various conditions.

Table 10.10 Wait States for Handshaking

Conditions at Address	Typical No. of Clock Cycles after AVD# Low	
	40 MHz	54/66 MHz
Initial address is even	4	5
Initial address is odd	5	6
Initial address is even, and is at boundary crossing*	6	7
Initial address is odd, and is at boundary crossing*	7	8

** In the 8-, 16- and 32-word burst read modes, the address pointer does not cross 64-word boundaries when wrap around is enabled (at address 3Fh, and at addresses offset from 3Fh by multiples of 64).*

The autoselect function allows the host system to determine whether the flash device is enabled for handshaking. See Autoselect Command Sequence for more information.

10.4 Sector Lock/Unlock Command Sequence

The sector lock/unlock command sequence allows the system to determine which sectors are protected from accidental writes. When the device is first powered up, all sectors are locked. To unlock a sector, the system must write the sector lock/unlock command sequence. Two cycles are first written: addresses are don't care and data is 60h. During the third cycle, the sector address (SLA) and unlock command (60h) is written, while specifying with address A6 whether that sector should be locked (A6 = V_{IL}) or unlocked (A6 = V_{IH}). After the third cycle, the system can continue to lock or unlock additional cycles, or exit the sequence by writing F0h (reset command).

Note that the last two outermost boot sectors can be locked by taking the WP# signal to V_{IL}. Also, if V_{PP} is at V_{IL} all sectors are locked; if the V_{PP} input is at V_{ID}, all sectors are unlocked.

10.5 Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

10.6 Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 10.16 shows the address and data requirements. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence. The following table describes the address requirements for the various autoselect functions, and the resulting data. BA represents the bank address, and SA represent the sector address. The device ID is read in three cycles.

Table 10.11 Autoselect Device ID

Description	Address	Read Data			
		S29NS128J	S29NS064J	S29NS032J	S29NS016J
Manufacturer ID	(BA) + 00h	0001h			
Device ID, Word 1	(BA) + 01h	007Eh	277Eh	2A7Eh	297Eh
Device ID, Word 2	(BA) + 0Eh	0016h	2702h	2A24h	2915h
Device ID, Word 3	(BA) + 0Fh	0000h	2700h	2A00h	2900h
Sector Block Lock/Unlock	(SA) + 02h	0001h (locked), 0000h (unlocked)			
Revision ID	(BA) + 03h	TBD, Based on Nokia spec			

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

10.7 Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 10.16 shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by monitoring DQ7 or DQ6/DQ2. See Write Operation Status for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from *0* back to a *1*.** Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bit to indicate the operation was successful. However, a succeeding read will show that the data is still *0*. Only erase operations can convert a *0* to a *1*.

10.7.2 Unlock Bypass Command Sequence

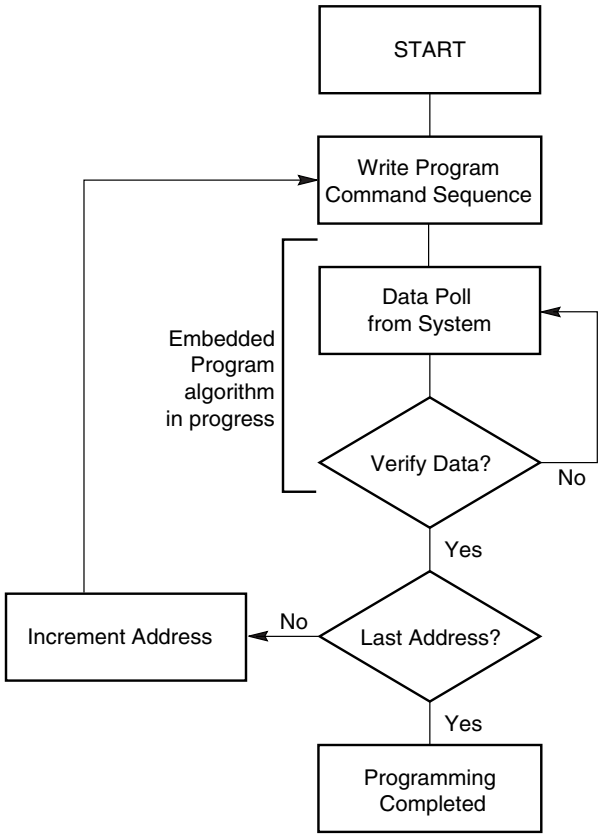
The unlock bypass feature allows the system to program to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program com-

mand sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 10.16 shows the requirements for the unlock bypass command sequences.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need only contain the data 00h. The bank then returns to the read mode.

The device offers accelerated program operations through the V_{PP} input. When the system asserts V_{PP} on this input, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the V_{PP} input to accelerate the operation.

Figure 10.1 illustrates the algorithm for the program operation. See the Erase/Program Operations table in See AC Characteristics for parameters, and Figure 17.6 for timing diagrams.



Note: *See Table 10.16 for program command sequence.*

Figure 10.1 Program Operation

10.8 Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these oper-

ations. Table 10.16 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6/DQ2. See Write Operation Status for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 10.2 illustrates the algorithm for the erase operation. See the Erase/Program Operations table in AC Characteristics for parameters, and Figure 17.7 for timing diagrams.

10.9 Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 10.16 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of no less than t_{SEA} (sector erase accept) occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than t_{SEA}, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode.** The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (see DQ3: Sector Erase Timer). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7 or DQ6/ DQ2 in the erasing bank. See Write Operation Status for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 10.2 illustrates the algorithm for the erase operation. See the Erase/Program Operations table in the AC Characteristics for parameters, and Figure 17.7 for timing diagrams.

10.9.1 Accelerated Sector Group Erase

Under certain conditions, the device can erase sectors in parallel. This method of erasing sectors is faster than the standard sector erase command sequence. Table 10.12 lists the sector erase groups.

The accelerated sector group erase function must not be used more than 100 times per sector. In addition, accelerated sector group erase should be performed at room temperature (30 ± 10°C).

Table 10.12 Accelerated Sector Erase Groups, S29NS128J

SA0–SA7	SA40–SA47	SA88–SA95	SA120–SA127	SA160–SA167	SA192–SA199	SA224–SA231
SA8–SA15	SA48–SA55	SA80–SA87	SA128–SA135	SA168–SA175	SA200–SA207	SA232–SA239
SA16–SA23	SA56–SA63	SA96–SA103	SA136–SA143	SA176–SA183	SA208–SA215	SA240–SA247
SA24–SA31	SA64–SA71	SA104–SA111	SA144–SA151	SA184–SA191	SA216–SA223	SA248–SA254
SA32–SA39	SA72–SA79	SA112–SA119	SA152–SA159			

Table 10.13 Accelerated Sector Erase Groups, S29NS064J

SA0–SA7	SA32–SA39	SA56–SA63	SA80–SA87	SA104–SA111
SA8–SA15	SA40–SA47	SA64–SA71	SA88–SA95	SA112–SA119
SA16–SA23	SA48–SA55	SA72–SA79	SA96–SA103	SA120–SA126
SA24–SA31				

Table 10.14 Accelerated Sector Erase Groups, S29NS032J

SA0–SA3	SA16-SA19	SA28-SA31	SA40-SA43	SA52-SA55
SA4–SA7	SA20-SA23	SA32-SA35	SA44-SA47	SA56–SA59
SA8–SA11	SA24-SA27	SA36-SA39	SA48-SA51	SA60–SA62
SA12-SA15				

Table 10.15 Accelerated Sector Erase Groups, S29NS016J

SA0–SA1	SA8-SA9	SA14-SA15	SA20-SA21	SA26-SA27
SA2–SA3	SA10-SA11	SA16-SA17	SA24-SA25	SA28-SA29
SA4–SA5	SA12-SA13	SA18-SA19	SA24-SA25	SA30
SA6–SA7				

Use the following procedure to perform accelerated sector group erase:

1. Unlock all sectors in a sector group to be erased using the sector lock/unlock command sequence. All sectors that remain locked will not be erased.
2. Apply 12 V to the V_{PP} input. This voltage must be applied at least 1 µs before executing step 3.
3. Write 80h to any address within a sector group to be erased.
4. Write 10h to any address within a sector group to be erased.
5. Monitor status bits DQ2/DQ6 or DQ7 to determine when erasure is complete, just as in the standard erase operation. See Write Operation Status for further details.
6. Lower V_{PP} from 12 V to V_{CC}.
7. Relock sectors as required.

10.10 Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, program data to, any sector not selected for erasure. The system may also lock or unlock any sector while the erase operation is suspended. **The system must not write the sector lock/unlock command to sectors selected for erasure.** The bank address is required when writing this command. This command is valid only during the sector erase operation, including the minimum t_{SEA} time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

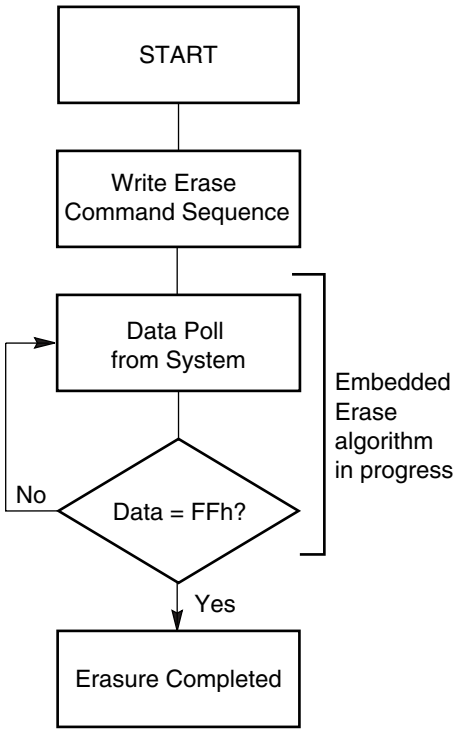
When the Erase Suspend command is written during the sector erase operation, the device requires t_{ESL} (erase suspend latency) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device *erase suspends* all sectors selected for erasure.) The system may also lock or unlock any sector while in the erase-suspend-read mode. Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See Write Operation Status for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. See Autoselect Functions and Autoselect Command Sequence for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



Notes:

1. *See Table 10.16 for erase command sequence.*
2. *See DQ3: Sector Erase Timer for information on the sector erase timer.*

Figure 10.2 Erase Operation

Table 10.16 Command Definitions

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–6)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Asynchronous Read (7)		1	RA	RD										
Reset (8)		1	XXX	F0										
Autoselect (9)	Manufacturer ID	4	555	AA	2AA	55	(BA)555	90	(BA)X00	0001				
	Device ID	6	555	AA	2AA	55	(BA)555	90	(BA)X01	(Note 10)	(BA)X0E	(Note 11)	(BA) X0F	(Note 12)
	Sector Lock Verify (13)	4	555	AA	2AA	55	(SA)555	90	(SA)X02	(Note 13)				
	Revision ID (14)	4	555	AA	2AA	55	(BA)555	90	(BA)X03	(Note 14)				
Unlock Bypass	Mode Entry	3	555	AA	2AA	55	555	20						
	Program (15)	2	XXX	A0	PA	PD								
	Reset (16)	2	BA	90	XXX	00								
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (17)		1	BA	B0										
Erase Resume (18)		1	BA	30										
Sector Lock/Unlock		3	XXX	60	XXX	60	SLA	60						
Set Config. Register (19)		3	555	AA	2AA	55	(CR)555	C0						
CFI Query (20)		1	55	98										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A_{max}–A13 uniquely select any sector.

BA = Address of the bank (A22–A21 for S29NS128J, A21–A20 for S29NS064J, A20–A19 for S29NS032J, A19–A18 for S29NS016J) that is being switched to autoselect mode, is in bypass mode, or is being erased.

SLA = Address of the sector to be locked. Set sector address (SA) and either A6 = 1 for unlocked or A6 = 0 for locked.

CR = Configuration Register set by address bits A17–A12.

Notes:

1. *See Table 9.1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD and PD.*
5. *Unless otherwise noted, address bits A_{max}–A12 are don't cares.*
6. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.*
7. *No unlock or command cycles required when bank is reading array data.*
8. *The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information).*
9. *The fourth cycle of the autoselect command sequence is a read cycle. The system must read device IDs across the 4th, 5th, and 6th cycles, The system must provide the bank address. See Autoselect Command Sequence for more information.*
10. *For S29NS128J, the data is 007Eh. For S29NS064J, the data is 277Eh. For S29NS032J, the data is 2A7Eh. For S29NS016J, the data is 297Eh.*
11. *For S29NS128J, the data is 0016h. For S29NS064J, the data is 2702h, for S29NS032J, the data is 2A24h, for S29NS016J, the data is 2915h.*
12. *For S29NS128J, the data is 0000h, for S29NS064J, the data is 2700h, for S29NS032J, the data is 2A00h for S29NS016J, the data is 2900h.*
13. *The data is 0000h for an unlocked sector and 0001h for a locked sector.*
14. *The data is TBD, based on Nokia spec.*
15. *The Unlock Bypass command sequence is required prior to this command sequence.*
16. *The Unlock Bypass Reset command is required to return to reading array data when the bank is in the unlock bypass mode.*
17. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
18. *The Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*
19. *The addresses in the third cycle must contain, on A17–A12, the additional wait counts to be set. See Set Configuration Register Command Sequence.*
20. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

II Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 11.2 and the following subsections describe the function of these bits. DQ7 and DQ6 each offers a method for determining whether a program or erase operation is complete or in progress.

II.I DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

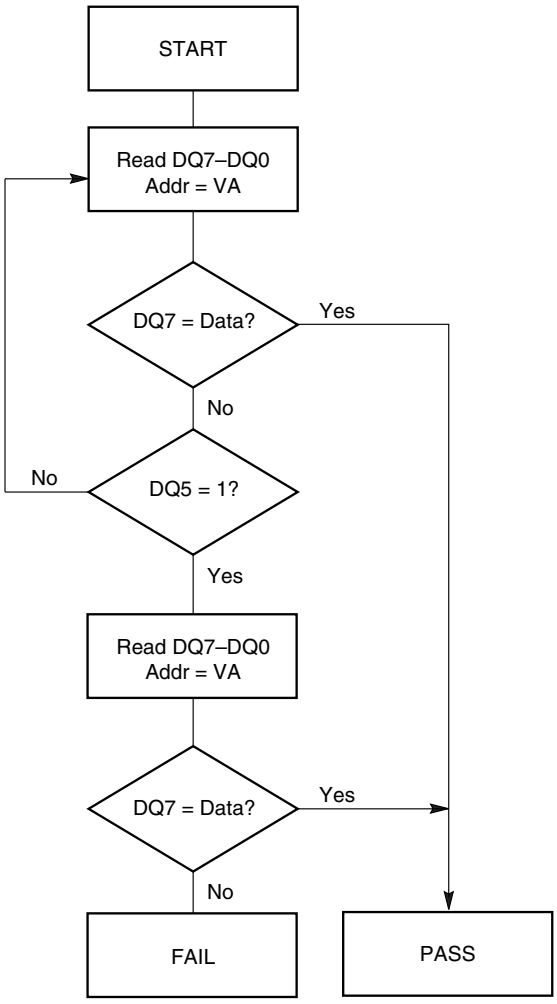
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately t_{PSP}, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a *0* on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a *1* on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately t_{ASP} (all sectors protected toggle time), then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6–DQ0 may be still invalid. Valid data on DQ7–DQ0 will appear on successive read cycles.

Table 11.2 shows the outputs for Data# Polling on DQ7. Figure 11.1 shows the Data# Polling algorithm. Figure 17.9 in AC Characteristics shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid Address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.*

Figure 11.1 Data# Polling Algorithm

11.2 RDY: Ready

The RDY pin is a dedicated status output that indicates valid output data on A/DQ15–A/DQ0 during burst (synchronous) reads. When RDY is asserted (RDY = V_{OH}), the output data is valid and can be read. When RDY is de-asserted (RDY = V_{OL}), the system should wait until RDY is re-asserted before expecting the next word of data.

In synchronous (burst) mode with CE# = OE# = V_{IL}, RDY is de-asserted under the following conditions: during the initial access; after crossing the internal boundary between addresses 3Eh and 3Fh (and addresses offset from these by a multiple of 64); and when the clock frequency is less than 6 MHz (in which case RDY is de-asserted every third clock cycle). The RDY pin will also switch during status reads when a clock signal drives the CLK input. In addition, RDY = V_{OH} when CE# = V_{IL} and OE# = V_{IH}, and RDY is Hi-Z when CE# = V_{IH}.

In asynchronous (non-burst) mode, the RDY pin does not indicate valid or invalid output data. Instead, RDY = V_{OH} when CE# = V_{IL}, and RDY is Hi-Z when CE# = V_{IH}.

11.3 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address in the same bank, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. Note that OE# must be low during toggle bit status reads. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately t_{ASP}, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately after t_{PSP} the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

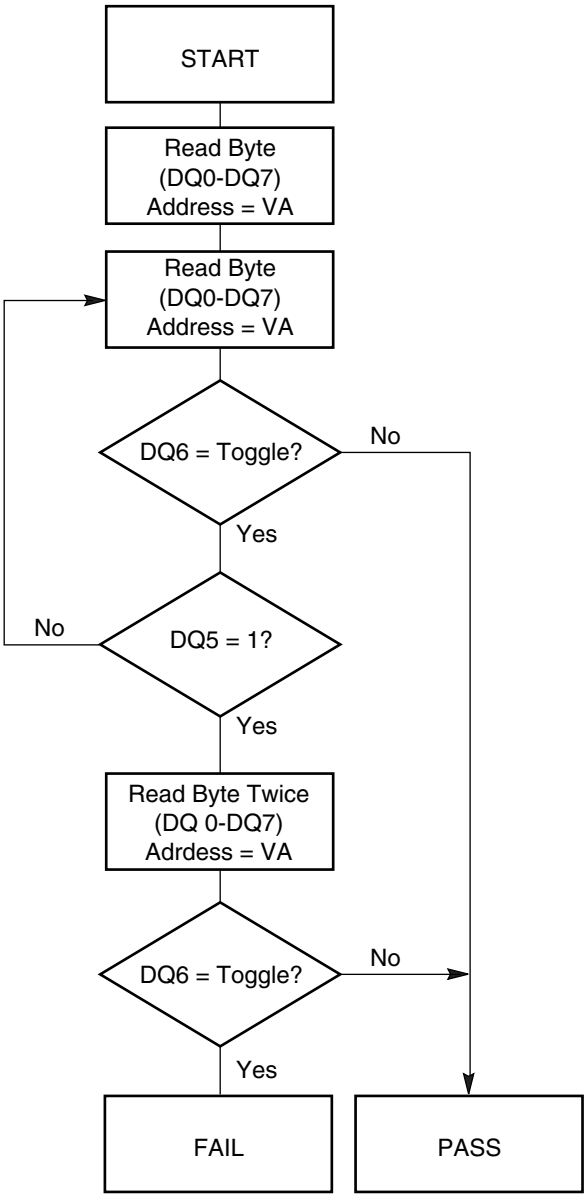
See the following for additional information: (toggle bit flowchart), DQ6: Toggle Bit I (description), Figure 17.10 (toggle bit timing diagram), and Table 11.1 (compares DQ2 and DQ6).

11.4 DQ2: Toggle Bit II

The *Toggle Bit II* on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. Note that OE# must be low during toggle bit status reads. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 11.2 to compare outputs for DQ2 and DQ6.

See the following for additional information: (toggle bit flowchart), DQ6: Toggle Bit I (description), Figure 17.10 (toggle bit timing diagram), and Table 11.1 (compares DQ2 and DQ6).



Note: *The system should recheck the toggle bit even if DQ5 = 1 because the toggle bit may stop toggling as DQ5 changes to 1. See DQ6: Toggle Bit I and DQ2: Toggle Bit II for more information.*

Figure 11.2 Toggle Bit Algorithm

Table 11.1 DQ6 and DQ2 Indications

If device is	and the system reads	then DQ6	and DQ2
programming,	at any address,	toggles,	does not toggle.
actively erasing,	at an address within a sector selected for erasure,	toggles,	also toggles.
	at an address within sectors *not* selected for erasure,	toggles,	does not toggle.
erase suspended,	at an address within a sector selected for erasure,	does not toggle,	toggles.
	at an address within sectors *not* selected for erasure,	returns array data,	returns array data. The system can read from any sector not selected for erasure.
programming in erase suspend	at any address,	toggles,	is not applicable.

11.5 Reading Toggle Bits DQ6/DQ2

Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see DQ5: Exceeded Timing Limits). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

11.6 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a *1*, indicating that the program or erase cycle was not successfully completed.

The device may output a *1* on DQ5 if the system tries to program a *1* to a location that was previously programmed to *0*. **Only an erase operation can change a *0* back to a *1***. Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a *1*.

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

11.7 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a *0* to a *1*. If the time between additional sector erase commands from the system can be assumed to be less than t_{SEA}, the system need not monitor DQ3. Also, see Sector Erase Command Sequence.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is *1*, the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is *0*, the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 11.2 shows the status of DQ3 relative to the other status bits.

Table 11.2 Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle
Erase Suspend Mode	Erase Suspend Read (Note 4)	Erase Suspended Sector	1	No toggle	0	N/A	Toggle
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data
	Erase Suspend Program		DQ7#	Toggle	0	N/A	N/A

Notes:

1. *DQ5 switches to 1 when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See DQ5: Exceeded Timing Limits for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. See DQ7: Data# Polling and DQ2: Toggle Bit II for further details.*
3. *When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.*
4. *The system may read either asynchronously or synchronously (burst) while in erase suspend. RDY will function exactly as in non-erase-suspended mode.*

I2 Absolute Maximum Ratings

Storage Temperature . . . . . −65°C to +150°C

Ambient Temperature
with Power Applied. . . . . −65°C to +125°C

Voltage with Respect to Ground,
All Inputs and I/Os except V_{PP} (Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V

V_{CC} (Note 1) . . . . . −0.5 V to +2.5 V

V_{PP} (Note 2) . . . . . −0.5 V to +12.5 V

Output Short Circuit Current (Note 3). . . . . 100 mA

Notes:

1. *Minimum DC voltage on input or I/Os is −0.5 V. During voltage transitions, input at I/Os may undershoot V_{SS} to −2.0 V for periods of up to 20 ns during voltage transitions inputs might overshooot to V_{CC} +0.5 V for periods up to 20 ns. See Figure 12.1. Maximum DC voltage on output and I/Os is V_{CC} + 0.5 V. During voltage transitions outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 12.2.*
2. *Minimum DC input voltage on V_{PP} is −0.5 V. During voltage transitions, V_{PP} may undershoot V_{SS} to −2.0 V for periods of up to 20 ns. See Figure 12.1. Maximum DC input voltage on V_{PP} is +12.5 V which may overshoot to +13.5 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

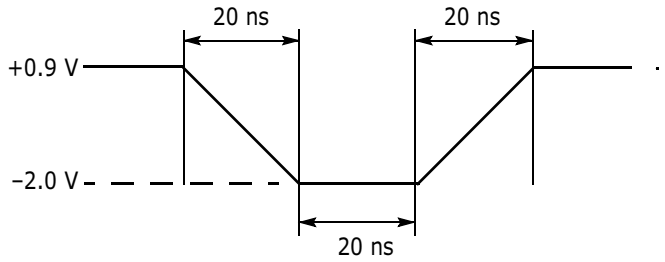


Figure I2.1 Maximum Negative Overshoot Waveform

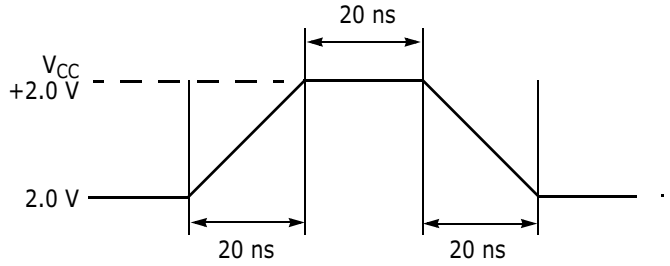


Figure I2.2 Maximum Positive Overshoot Waveform

I2.1 Operating Ranges

Ambient Temperature (T_A) . . . . . −25°C to +85°C

V_{CC} Supply Voltages

V_{CC} min . . . . . +1.7 V

V_{CC} max . . . . . +1.95 V

Note: *Operating ranges define those limits between which the functionality of the device is guaranteed.*

13 DC Characteristics

13.1 CMOS Compatible

Parameter	Description (Notes)	Test Conditions (Note 1)		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1	µA
I_{CCB}	V_{CC} Active Burst Read Current (5)	CE# = V_{IL}, OE# = V_{IL}			25	30	mA
I_{CC1}	V_{CC} Active Asynchronous Read Current (2)	CE# = V_{IL}, OE# = V_{IH}	5 MHz		12	16	mA
			1 MHz		3.5	5	mA
I_{CC2}	V_{CC} Active Write Current (3)	CE# = V_{IL}, OE# = V_{IH}, $V_{PP} = V_{IH}$			15	40	mA
I_{CC3}	V_{CC} Standby Current (4)	CE# = V_{IH}, RESET# = V_{IH}			9	40	µA
I_{CC4}	V_{CC} Reset Current	RESET# = V_{IL}, CLK = V_{IL}			9	40	µA
I_{CC5}	V_{CC} Active Current (Read While Write)	CE# = V_{IL}, OE# = V_{IL}			40	60	mA
I_{PPW}	Accelerated Program Current (6)	V_{PP} = 12 V			7	15	mA
I_{CCW}					5	10	
I_{PPE}	Accelerated Erase Current (6)	V_{PP} = 12 V			7	15	mA
I_{CCE}					5	10	
V_{IL}	Input Low Voltage			–0.5		0.4	V
V_{IH}	Input High Voltage			V_{CC} – 0.4		V_{CC} + 0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, $V_{CC} = V_{CC\ min}$				0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CC} – 0.1			V
V_{ID}	Voltage for Accelerated Program			11.5		12.5	V
V_{LKO}	Low V_{CC} Lock-out Voltage			1.0		1.4	V

Notes:

1. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Device enters automatic sleep mode when addresses are stable for t_{ACC} + 60 ns. Typical sleep mode current is equal to I_{CC3}.*
5. *Specifications assume 8 I/Os switching and continuous burst length.*
6. *Not 100% tested. V_{PP} is not a power supply pin.*

14 Test Conditions

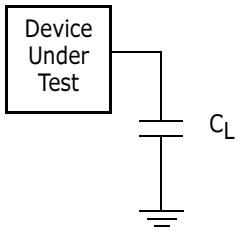
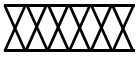
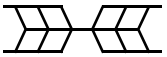


Figure 14.1 Test Setup

Table 14.1 Test Specifications

Test Condition	All Speeds	Unit
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–V_{CC}	V
Input timing measurement reference levels	$V_{CC}/2$	V
Output timing measurement reference levels	$V_{CC}/2$	V

15 Key to Switching Waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

16 Switching Waveforms

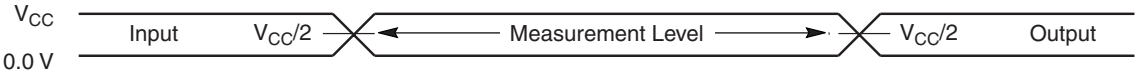


Figure 16.1 Input Waveforms and Measurement Levels

17 AC Characteristics

17.1 V_{CC} Power-up

Parameter	Description	Test Setup	Speed	Unit
t_{VCS}	V_{CC} Setup Time	Min	50	µs
t_{RSTH}	RESET# Low Hold Time	Min	50	µs

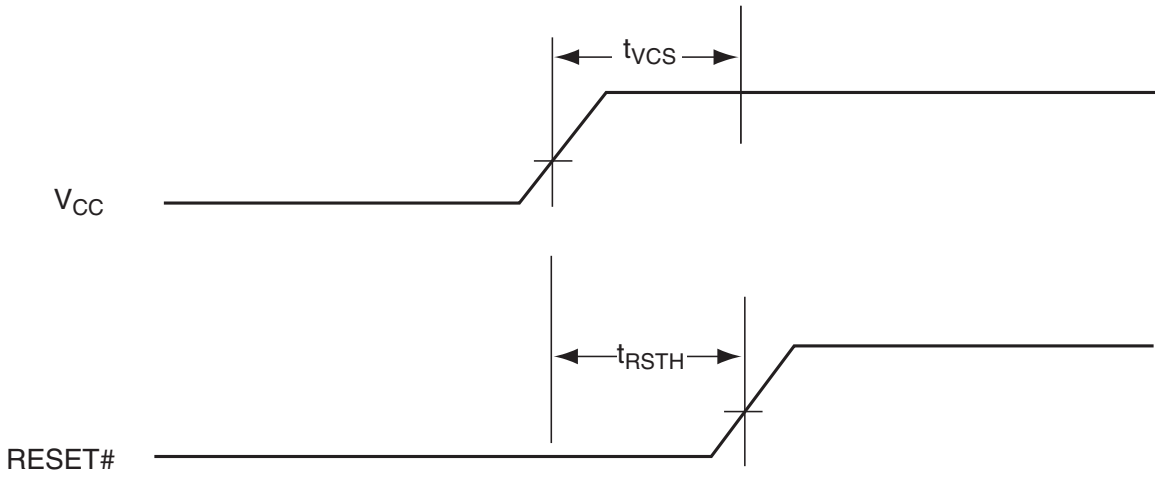


Figure 17.1 V_{CC} Power-up Diagram

17.2 CLK Characterization

Parameter	Description		0P (66 MHz)	0L (54 MHz)	Unit
f_{CLK}	CLK Frequency	Max	66	54	MHz
t_{CLK}	CLK Period	Min	15	18.5	ns
t_{CH}	CLK High Time	Min	3.5	4.5	ns
t_{CL}	CLK Low Time				
t_{CR}	CLK Rise Time	Max	3	3	ns
t_{CF}	CLK Fall Time				

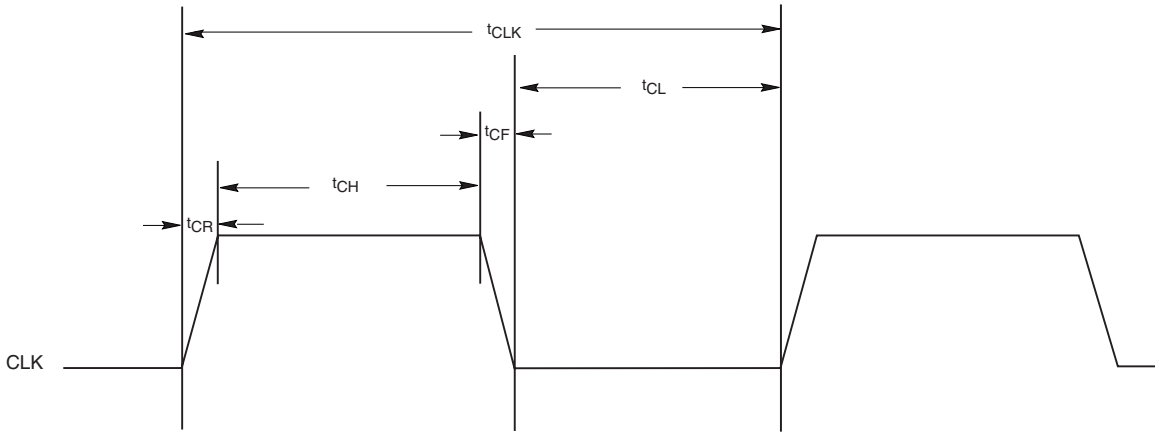
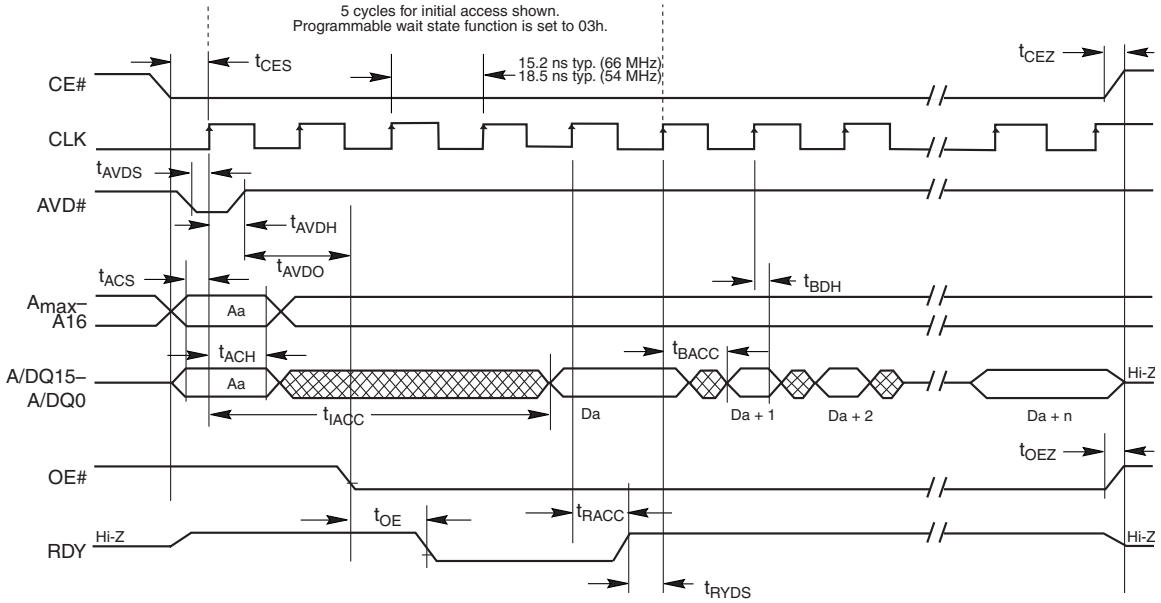


Figure 17.1 CLK Characterization

I7.3 Synchronous/Burst Read

Parameter		Description		0P (66 MHz)	0L (54 MHz)	Unit
JEDEC	Standard					
	t_{IACC}	Initial Access Time	Max	71	87.5	ns
	t_{BACC}	Burst Access Time Valid Clock to Output Delay	Max	11	13.5	ns
	t_{AVDS}	AVD# Setup Time to CLK	Min	4	5	ns
	t_{AVDH}	AVD# Hold Time from CLK	Min	6	7	ns
	t_{AVDO}	AVD# High to OE# Low	Min	0		ns
	t_{ACS}	Address Setup Time to CLK	Min	4	5	ns
	t_{ACH}	Address Hold Time from CLK	Min	6	7	ns
	t_{BDH}	Data Hold Time from Next Clock Cycle (Note)	Min	3		ns
	t_{OE}	Output Enable to Data, PS, or RDY Valid	Max	11	13.5	ns
	t_{CEZ}	Chip Enable to High Z	Max	10		ns
	t_{OEZ}	Output Enable to High Z	Max	10		ns
	t_{CES}	CE# Setup Time to CLK	Min	4	5	ns
	t_{RDYS}	RDY Setup Time to CLK	Min	4	5	ns
	t_{RACC}	Ready access time from CLK	Max	11	13.5	ns

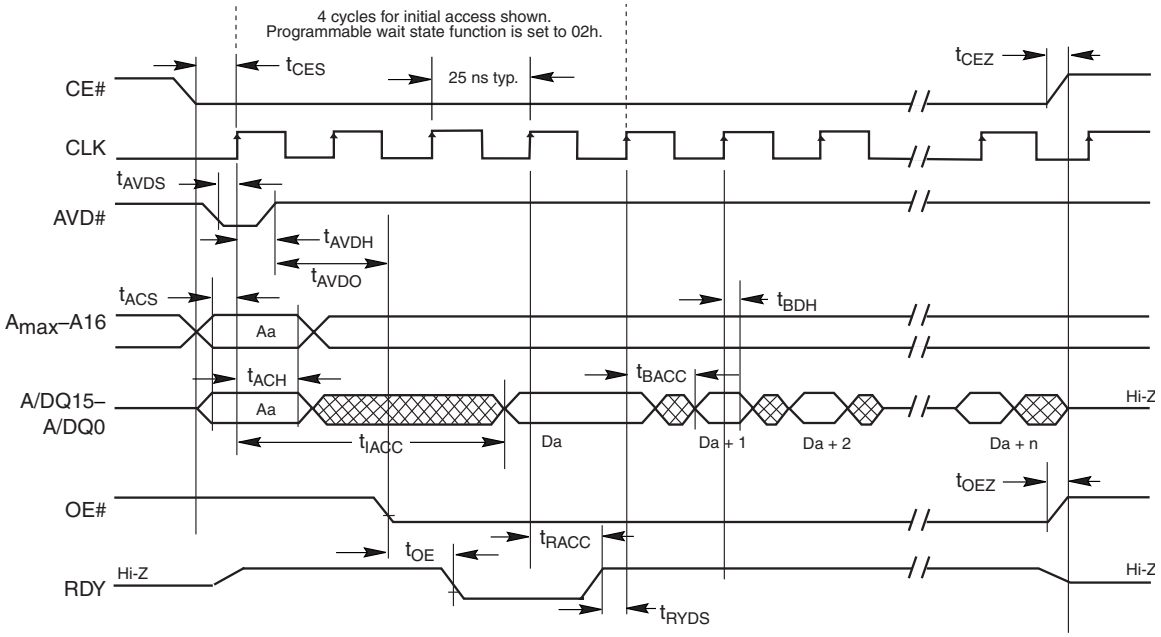
Note: *Not 100% tested*



Notes:

1. *Figure shows total number of clock set to five.*
2. *If any burst address occurs at a 64-word boundary, two additional clock cycles are inserted and are indicated by RDY.*

Figure I7.2 Burst Mode Read (66 and 54 MHz)



Notes:

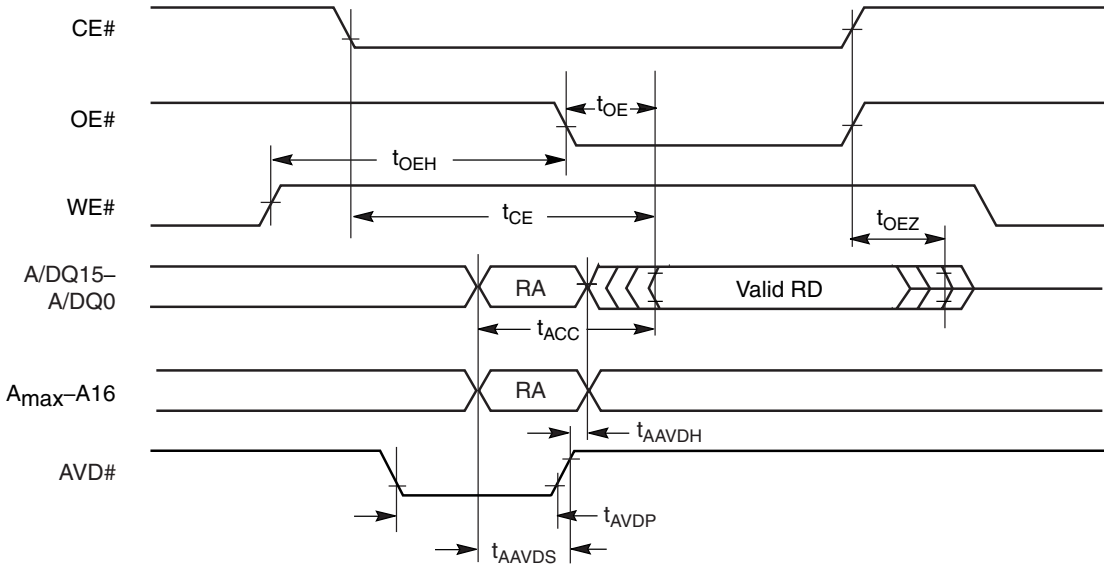
1. *Figure shows total number of clock cycles set to four.*
2. *If any burst address occurs at a 64-word boundary, two additional clock cycle are inserted, and are indicated by RDY.*

Figure I7.3 Burst Mode Read (40 MHz)

I7.4 Asynchronous Read

Parameter		Description			0P (66 MHz)	0L (54 MHz)	Unit
JEDEC	Standard						
	t_{CE}	Access Time from CE# Low		Max	65	70	ns
	t_{ACC}	Asynchronous Access Time		Max	65	70	ns
	t_{AVDP}	AVD# Low Time		Min	11	12	ns
	t_{AAVDS}	Address Setup Time to Rising Edge of AVD		Min	4	5	ns
	t_{AAVDH}	Address Hold Time from Rising Edge of AVD		Min	6	7	ns
	t_{OE}	Output Enable to Output Valid		Max	11	13.5	ns
	t_{OEH}	Output Enable Hold Time	Read	Min	0		ns
			Toggle and Data# Polling	Min	10		ns
	t_{OEZ}	Output Enable to High Z (See Note)		Max	10		ns

Note: *Not 100% tested.*



Note: *RA = Read Address, RD = Read Data.*

Figure I7.4 Asynchronous Mode Read

I7.5 Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Readyw}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	35	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	200	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs

Note: *Not 100% tested.*

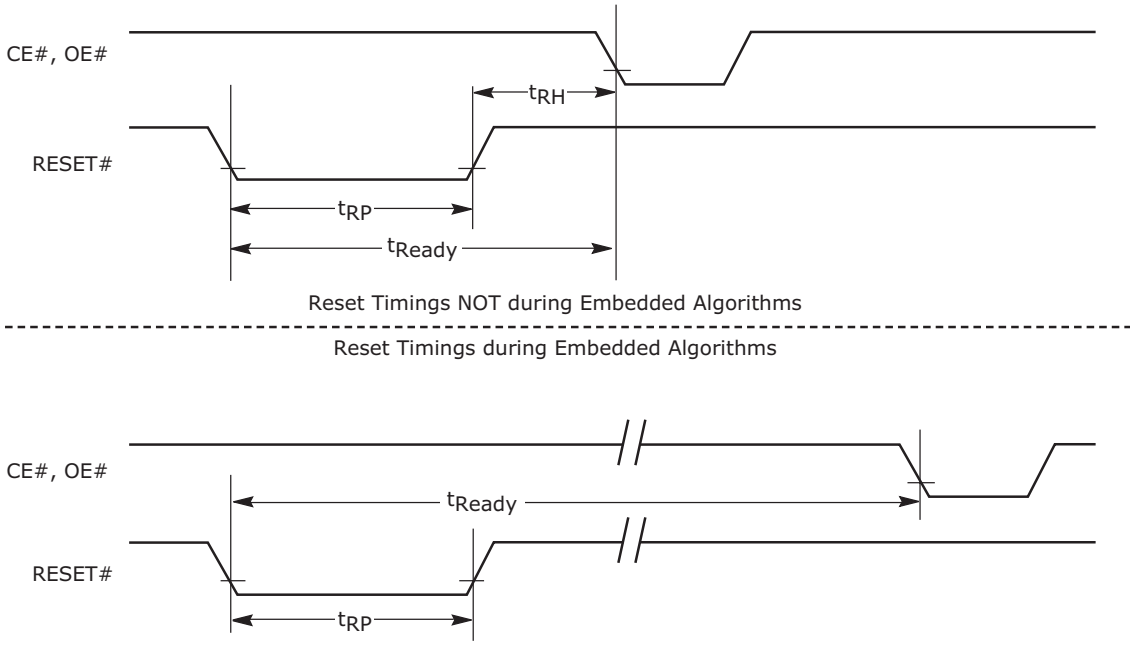


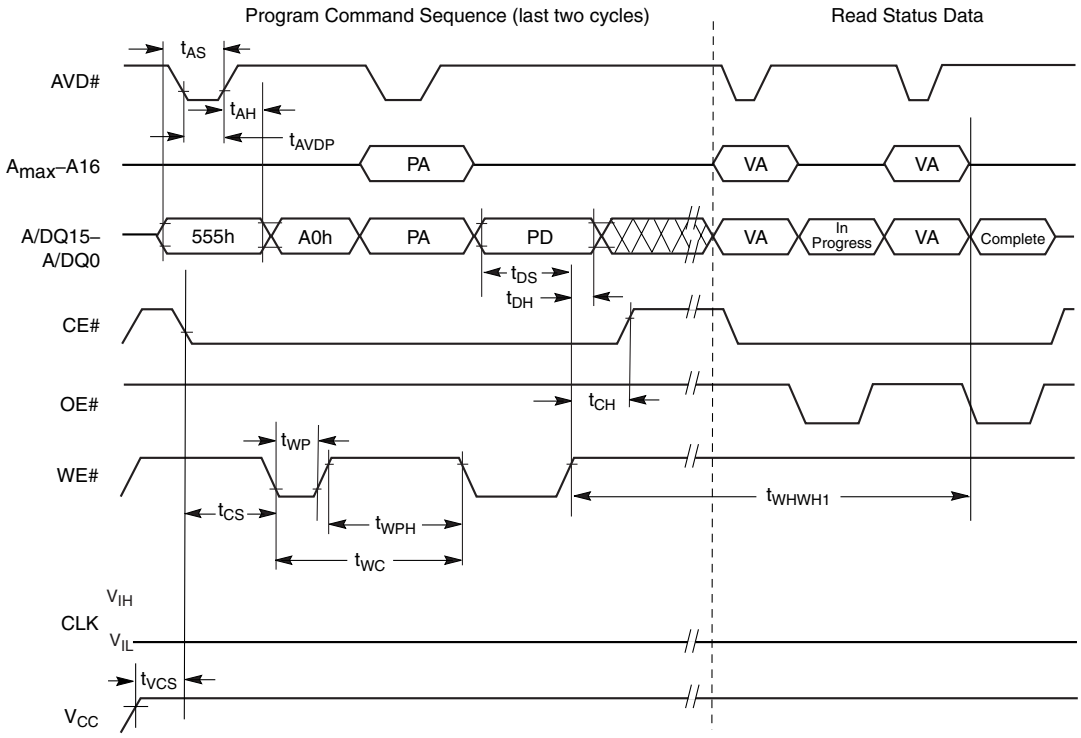
Figure I7.5 Reset Timings

I7.6 Erase/Program Operations

Parameter		Description		0P (66 MHz)	0L (54 MHz)	Unit
JEDEC	Standard					
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	45	80	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	4	5	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	6	7	ns
	t_{AVDP}	AVD# Low Time	Min	11	12	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	25	45	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write	Typ	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time	Typ	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time	Typ	0		ns
t_{WLWH}	t_{WP}/t_{WRL}	Write Pulse Width	Typ	25	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Typ	20	30	ns
	$t_{SR/W}$	Latency Between Read and Write Operations	Min	0		ns
	t_{VPP}	V_{PP} Rise and Fall Time	Min	500		ns
	t_{VPS}	V_{PP} Setup Time (During Accelerated Programming)	Min	1		µs
	t_{VCS}	V_{CC} Setup Time	Min	50		µs
	t_{SEA}	Sector Erase Accept Time-out	Max	50		µs
	t_{ESL}	Erase Suspend Latency	Max	35		µs
	t_{ASP}	Toggle Time During Sector Protection	Typ	100		µs
	t_{PSP}	Toggle Time During Programming Within a Prot	Typ	1		µs

Notes:

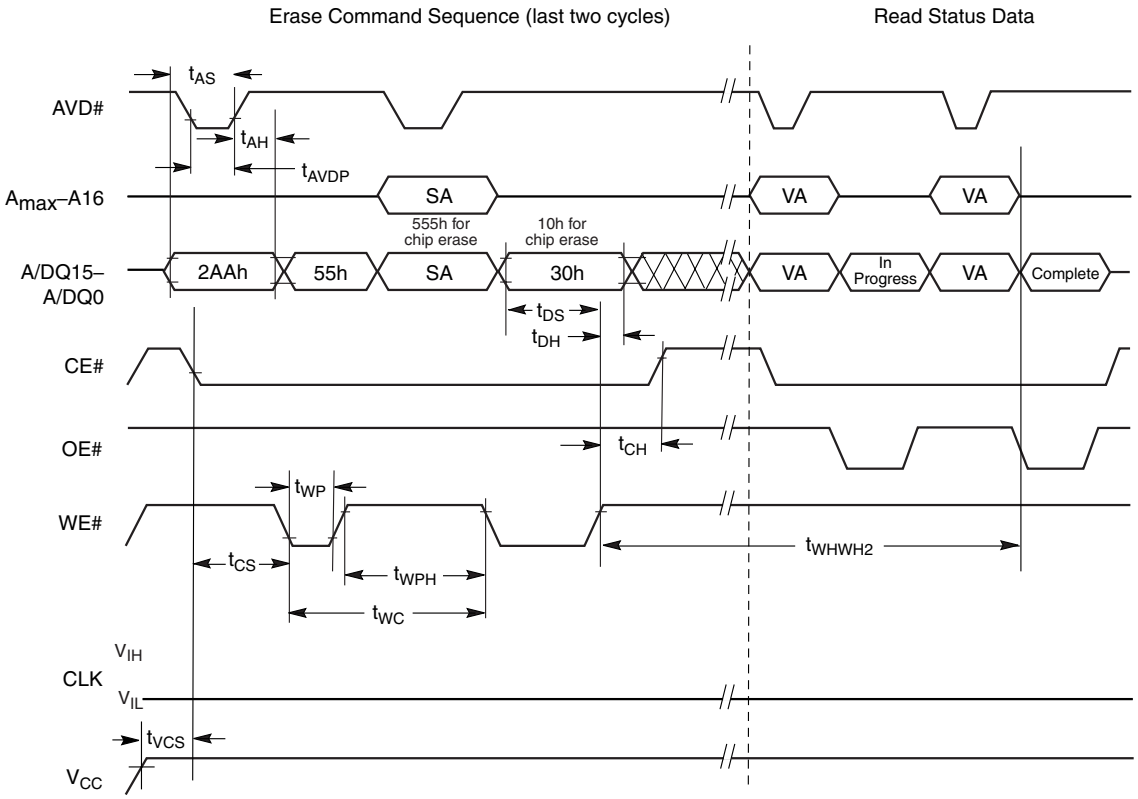
1. *Not 100% tested.*
2. *See Erase and Programming Performance for more information.*
3. *Does not include the preprogramming time.*



Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. In progress *and* complete *refer to status of program operation.*
3. *A_{max}–A16 are don't care during command sequence unlock cycles.*

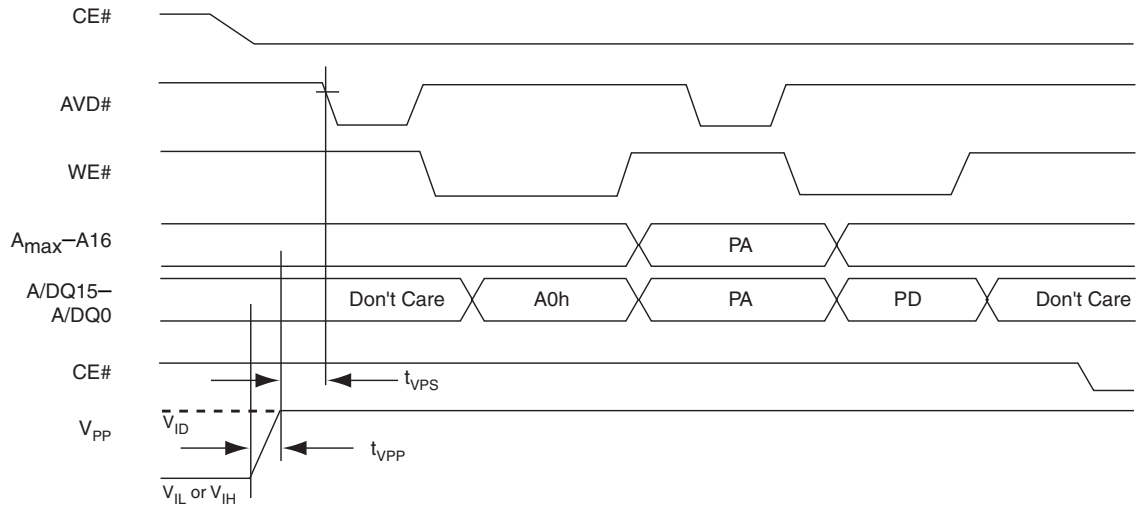
Figure I7.6 Program Operation Timings



Notes:

1. *SA is the sector address for Sector Erase.*
2. *Address bits A_{max}–A16 are don't cares during unlock cycles in the command sequence.*

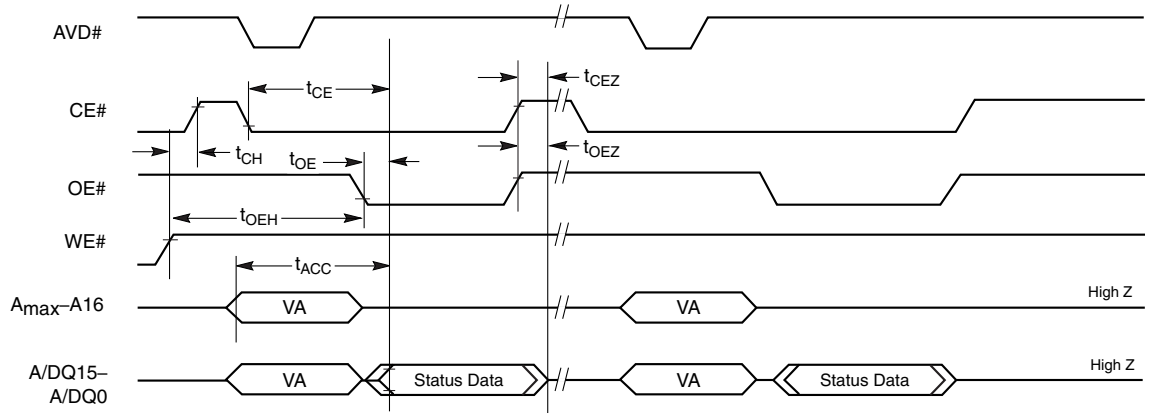
Figure I7.7 Chip/Sector Erase Operations



Notes:

1. *V_{PP} can be left high for subsequent programming pulses.*
2. *Use setup and hold times from conventional program operation.*

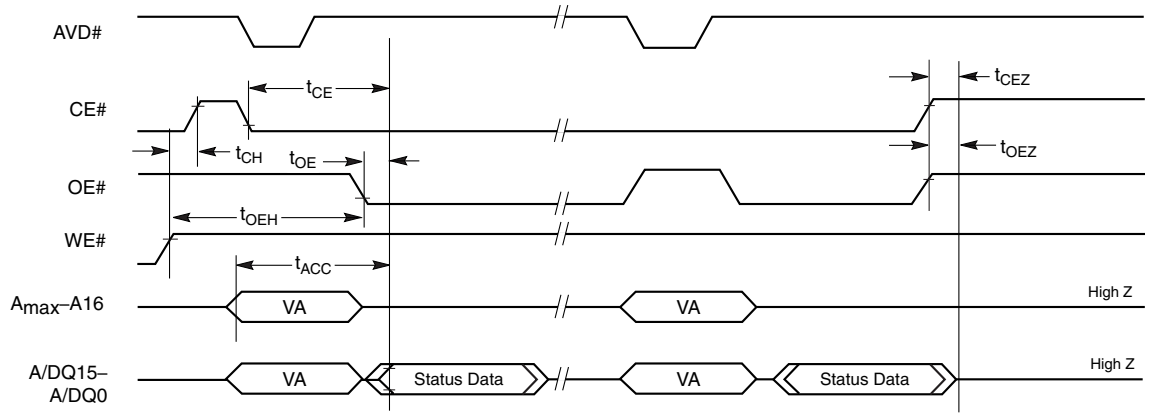
Figure I7.8 Accelerated Unlock Bypass Programming Timing



Notes:

1. *All status reads are asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, and Data# Polling will output true data.*

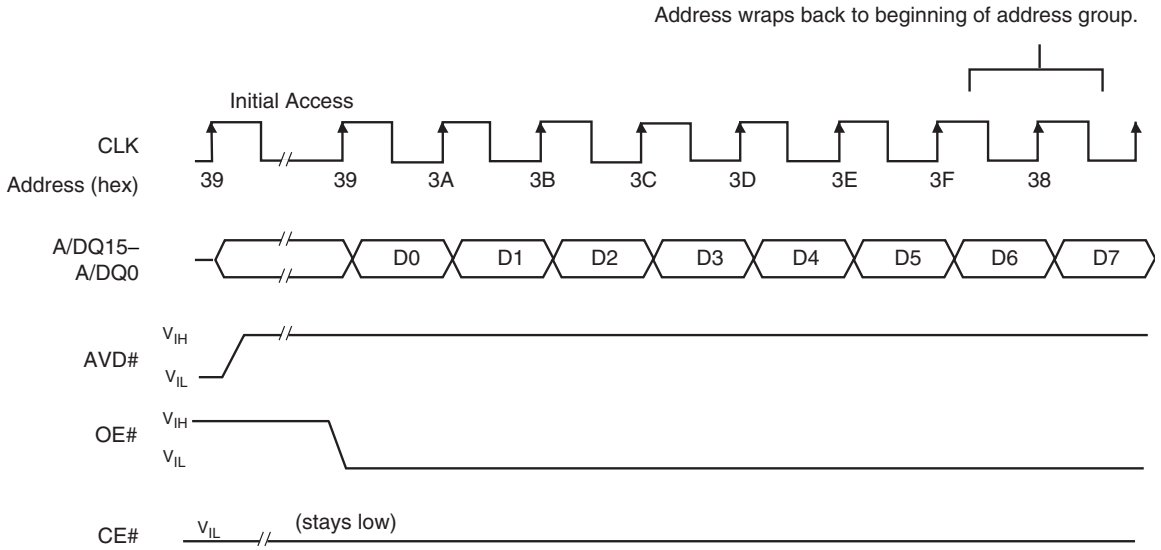
Figure I7.9 Data# Polling Timings (During Embedded Algorithm)



Notes:

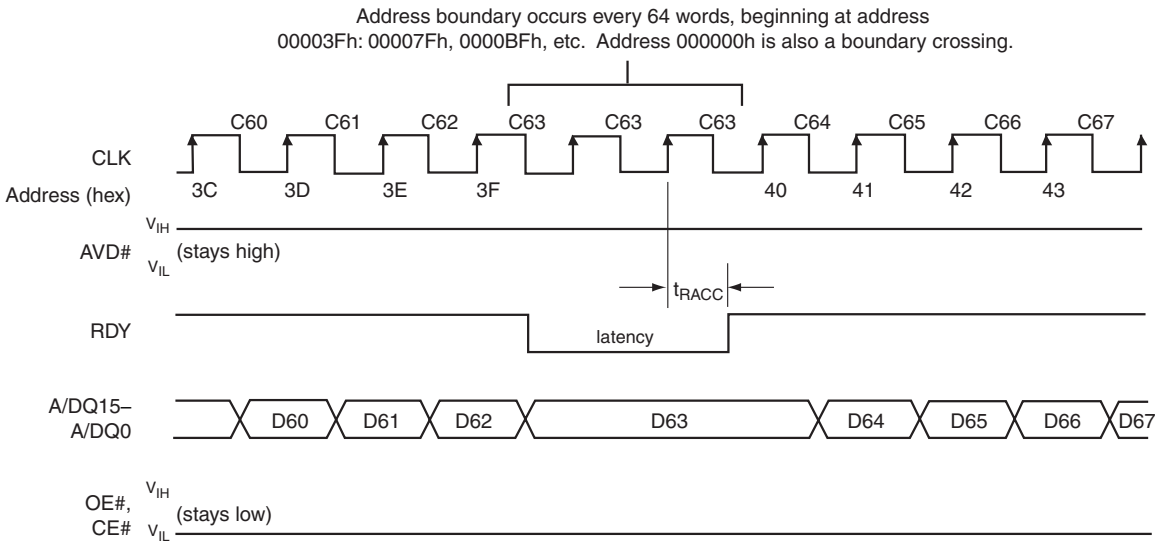
1. *All status reads are asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.*

Figure I7.10 Toggle Bit Timings (During Embedded Algorithm)



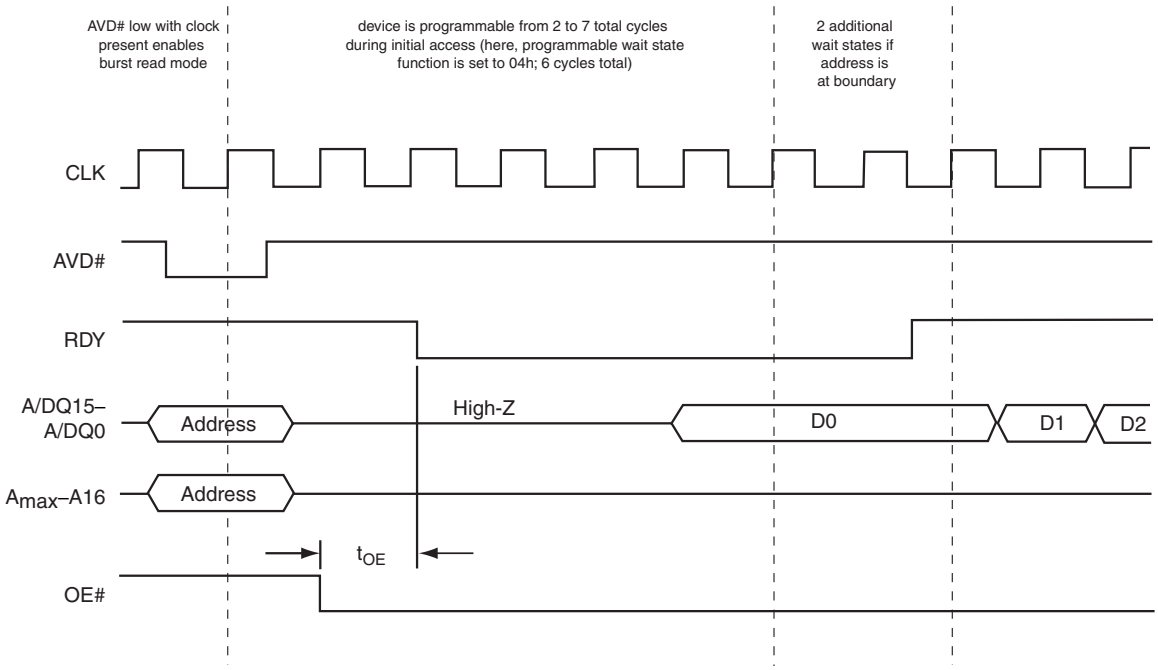
Note: *8-word linear burst mode shown. 16- and 32-word linear burst read modes behave similarly. D0 represents the first word of the linear burst.*

Figure 17.11 8-, 16-, and 32-Word Linear Burst Address Wrap Around



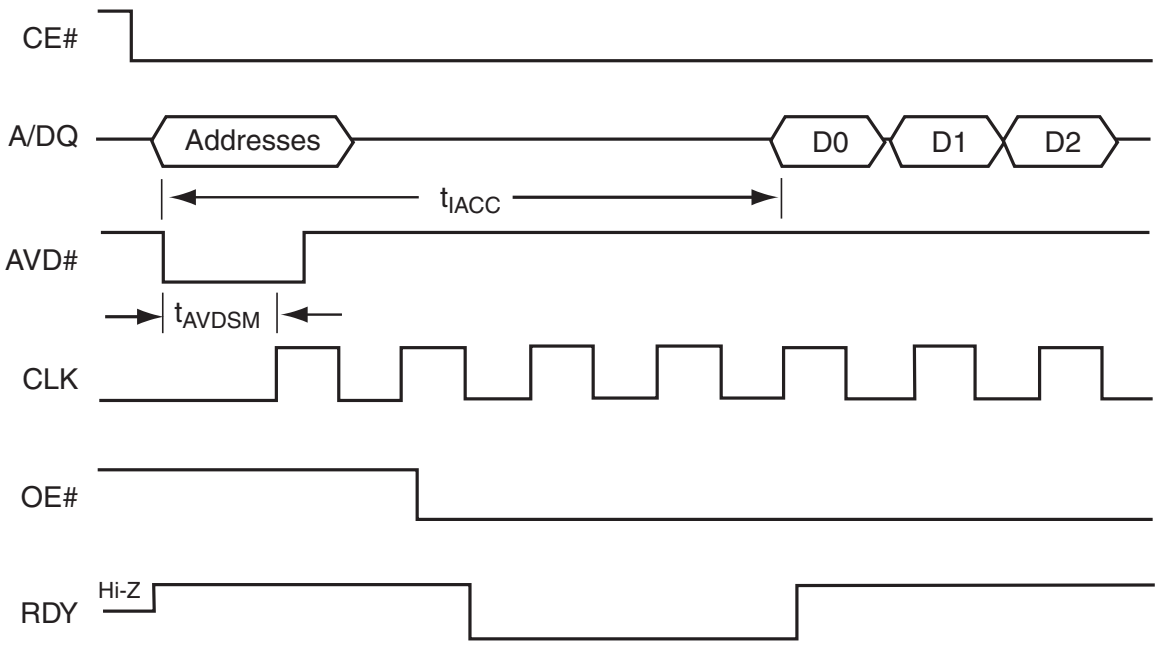
Note: *Cxx indicates the clock that triggers data Dxx on the outputs; for example, C60 triggers D60.*

Figure 17.12 Latency with Boundary Crossing



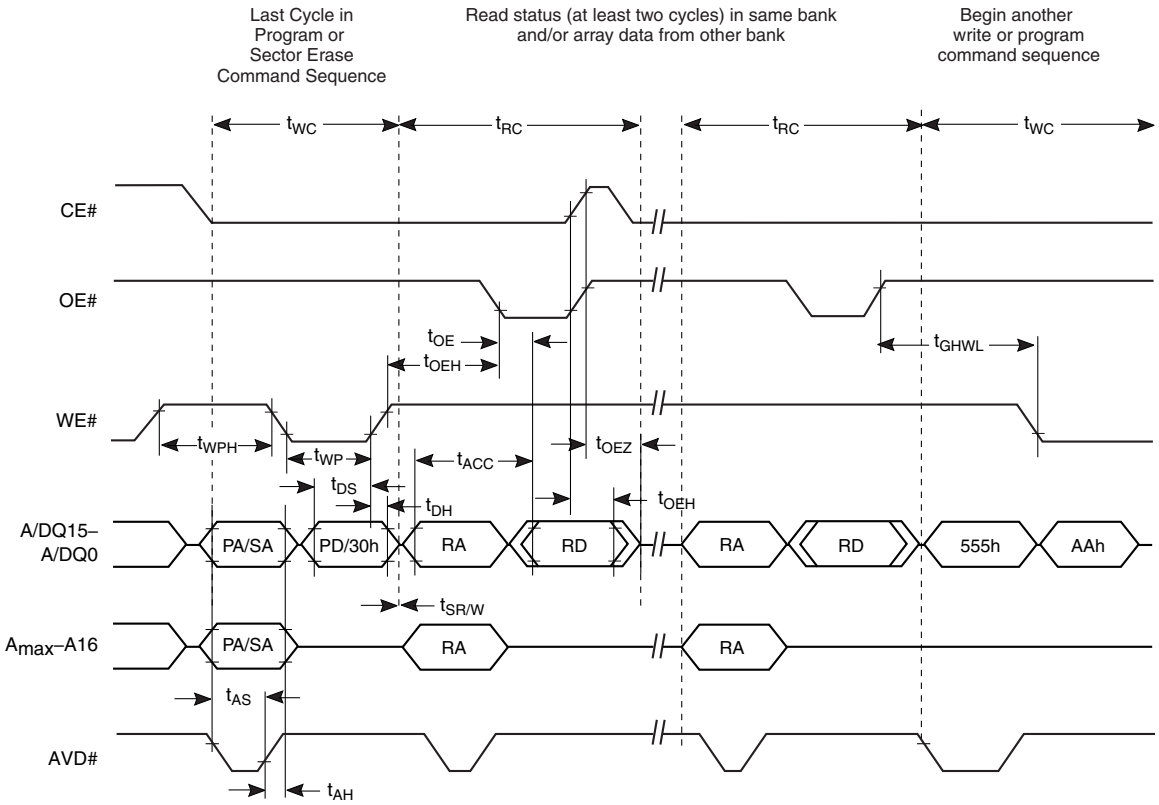
Note: *Devices should be programmed with wait states as discussed in the Programmable Wait State.*

Figure 17.13 Initial Access at 3Eh with Address Boundary Latency



Note: *If t_{AVDSM} > 1 CLK cycle, wait state usage is reduced. Figure shows 40 MHz clock, handshaking enabled. Wait state usage is 4 clock cycles instead of 5. Note that t_{AVDSM} must be less than 76 µs for burst operation to begin.*

Figure 17.14 Example of Extended Valid Address Reducing Wait State Usage



Note: *Breakpoints in waveforms indicate that system may alternately read array data from the* non-busy bank *while checking the status of the program or erase operation in the* busy *bank. The system should read status twice to ensure valid information.*

Figure 17.15 Back-to-Back Read/Write Cycle Timings

18 Erase and Programming Performance

Parameter			Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	32 Kword		0.4	5	s	Excludes 00h programming prior to erasure (Note 4)
	8 Kword		0.2	5		
Chip Erase Time		128 Mb	108		s	
		64 Mb	54			
		32 Mb	27			
		16 Mb	13.5			
Word Programming Time			9	210	µs	Excludes system level overhead (Note 5)
Accelerated Word Programming Time			4	120	µs	
Chip Programming Time (Note 3)		128 Mb	96	288	s	Excludes system level overhead (Note 5)
		64 Mb	48	144		
		32 Mb	24	72		
		16 Mb	12	36		
Accelerated Chip Programming Time		128 Mb	32	96	s	
		64 Mb	16	48		
		32 Mb	8	24		
		16 Mb	4	12		
Accelerated Chip Erase Time		128 Mb	50		s	
		64 Mb	25			
		32 Mb	12.5			
		16 Mb	6.25			

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 1.8 V V_{CC}, 100,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 1.7 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 10.16 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 100,000 cycles.*

19 Device History

Device	Revision	Burst Speed	Extended Code (Hex)	Major Reason(s) for Change
S29NS128J	First	66 MHZ	012E	Initial release
S29NS128J	Second (ES)	66 MHz	012D	Endurance fix
S29NS128J	Second (ES)	54 MHz	011D	Endurance fix
S29NS128J	First (Production)	66 MHZ	0121	Production
S29NS128J	First (Production)	54 MHz	0111	Production
S29NS064J	First (ES)	66 MHZ	012E	Initial Release
S29NS064J	First (ES)	54 MHz	011E	Initial Release
S29NS064J	First (Production)	66 MHZ	0121	Production
S29NS064J	First (Production)	54 MHz	0111	Production
S29NS032J	First (ES)	54 MHz	011E	Initial Release
S29NS032J	First (Production)	54 MHz	0111	Production
S29NS016J	First (ES)	54 MHz	011E	Initial Release
S29NS016J	First (Production)	54 MHz	0111	Production

CellularRAM Type 2

64 Megabit
Burst CellularRAM

Features

- **Single device supports asynchronous, page, and burst operations**
- **V_{CC}, V_{CCQ}Voltages**
  - 1.70 V–1.95 V V_{CC}
  - 1.70 V–3.30 V V_{CCQ}
- **Random Access Time: 70 ns**
- **Burst Mode Write Access**
  - Continuous burst
- **Burst Mode Read Access**
  - 4, 8, or 16 words, or continuous burst
- **Page Mode Read Access**
  - Sixteen-word page size
  - Interpage Read access: 70ns
  - Intrapage Read access: 20ns
- **Low-Power Consumption**
  - Asynchronous Read < 25 mA
  - Intrapage Read < 15 mA
  - Initial access, burst Read < 35 mA
  - Continuous burst Read < 15m A
  - Standby: 120 µA

General Description

CellularRAM™ products are High-speed, CMOS dynamic random access memories developed for low-power, portable applications. These devices include an industry standard burst mode Flash interface that dramatically increases Read/Write bandwidth compared with other low-power SRAM or Pseudo SRAM offerings.

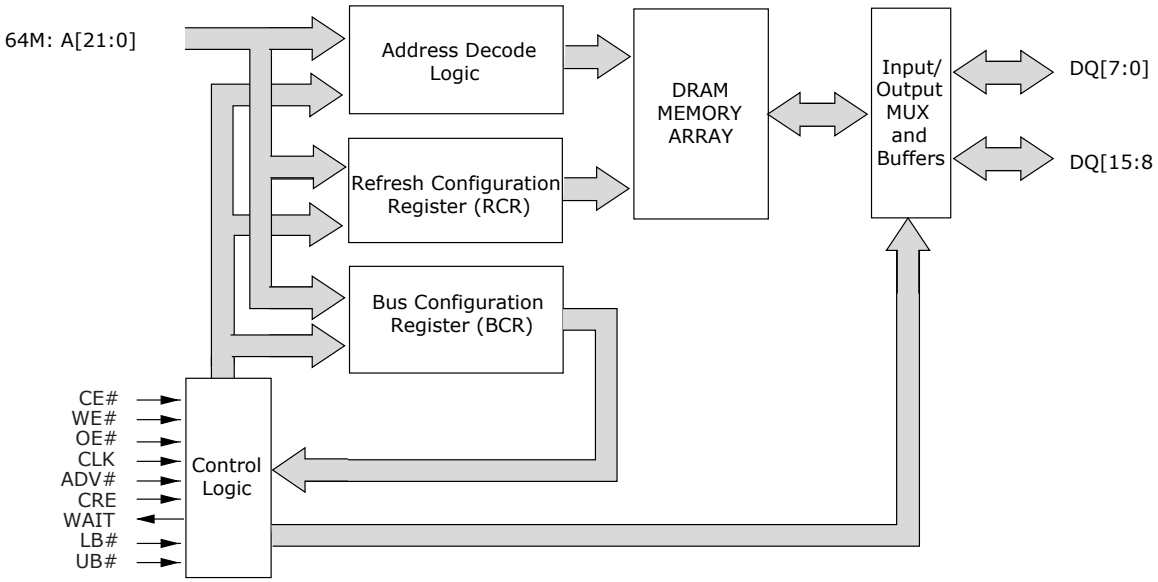
To operate seamlessly on a burst Flash bus, CellularRAM products incorporate a transparent self-refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device Read/Write performance.

Two user-accessible control registers define device operation. The bus configuration register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

Special attention has been focused on standby current consumption during self refresh. CellularRAM products include three mechanisms to minimize standby current. Partial array refresh (PAR) enables the system to limit refresh to only that part of the DRAM array that contains essential data. Temperature compensated refresh (TCR) adjusts the refresh rate to match the device temperature—the refresh rate decreases at lower temperatures to minimize current consumption during standby. Deep power-down (DPD) enables the system to halt the refresh operation altogether when no vital information is stored in the device. The system-configurable refresh mechanisms are accessed through the RCR.

Publication Number S71NS-J-00 **Revision** A **Amendment** 0 **Issue Date** March 17, 2005

20 Functional Block Diagram



Note: *Functional block diagrams illustrate simplified device operation. See truth table, ball descriptions, and timing diagrams for detailed information.*

Figure 20.1 Functional Block Diagram

Table 20.1 Signal Descriptions

Symbol	Type	Description
64M: A[21:0]	Input	Address Inputs: Inputs for addresses during Read and Write operations. Addresses are internally latched during Read and Write cycles. The address lines are also used to define the value to be loaded into the BCR or the RCR.
CLK	Input	Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK is static (High or Low) during asynchronous access Read and Write operations and during Page Read Access operations.
ADV#	Input	Address Valid: Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV# during asynchronous Read and Write operations. ADV# can be held Low during asynchronous Read and Write operations.
CRE	Input	Configuration Register Enable: When CRE is High, Write operations load the RCR or BCR.
CE#	Input	Chip Enable: Activates the device when Low. When CE# is High, the device is disabled and goes into standby or deep power-down mode.
OE#	Input	Output Enable: Enables the output buffers when Low. When OE# is High, the output buffers are disabled.
WE#	Input	Write Enable: Determines if a given cycle is a Write cycle. If WE# is Low, the cycle is a Write to either a configuration register or to the memory array.
LB#	Input	Lower Byte Enable. DQ[7:0]
UB#	Input	Upper Byte Enable. DQ[15:8]
DQ[15:0]	Input/Output	Data Inputs/Outputs.
Wait	Output	Wait: Provides data-valid feedback during burst Read and Write operations. The signal is gated by CE#. Wait is used to arbitrate collisions between refresh and Read/Write operations. Wait is asserted when a burst crosses a row boundary. Wait is also used to mask the delay associated with opening a new internal page. Wait is asserted and should be ignored during asynchronous and page mode operations. Wait is High-Z when CE# is High.
V_{CC}	Supply	Device Power Supply: (1.7V–1.95V) Power supply for device core operation.
V_{CCQ}	Supply	I/O Power Supply: (1.7V–3.30V) Power supply for input/output buffers.
V_{SS}	Supply	V_{SS} must be connected to ground.
V_{SSQ}	Supply	V_{SS}Q must be connected to ground.

Note: *The CLK and ADV# inputs can be tied to V_{SS} if the device is always operating in asynchronous or page mode. Wait is asserted but should be ignored during asynchronous and page mode operations.*

Table 20.2 Bus Operations—Asynchronous Mode

Mode	Power	CLK (Note 1)	ADV#	CE#	OE#	WE#	CRE	LB#/UB#	Wait (Note 2)	DQ[15:0] (Note 3)	Notes
Read	Active	X	L	L	L	H	L	L	Low-Z	Data-Out	4
Write	Active	X	L	L	X	L	L	L	Low-Z	Data-In	4
Standby	Standby	X	X	H	X	X	L	X	High-Z	High-Z	5, 6
No Operation	Idle	X	X	L	X	X	L	X	Low-Z	X	4, 6
Configuration Register	Active	X	L	L	H	L	H	X	Low-Z	High-Z	
DPD	Deep Power-down	X	X	H	X	X	X	X	High-Z	High-Z	7

Notes:
1. *CLK may be High or Low, but must be static during synchronous Read, synchronous Write, burst suspend, and DPD modes; and to achieve standby power during standby and active modes.*
2. *The Wait polarity is configured through the bus configuration register (BCR[10]).*
3. *When LB# and UB# are in select mode (Low), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.*
4. *The device consumes active power in this mode whenever addresses are changed.*
5. *When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.*
6. *V_{IN} = V_{CC}Q or 0V; all device balls must be static (unswitched) to achieve standby current.*
7. *DPD is maintained until RCR is reconfigured.*

Table 20.3 Bus Operations—Burst Mode

Mode	Power	CLK (Note 1)	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	Wait (Note 2)	DQ[15:0] (Note 3)	Notes
Async Read	Active	X	L	L	L	H	L	L	Low-Z	Data-Out	4
Async Write	Active	X	L	L	X	L	L	L	Low-Z	Data-In	4
Standby	Standby	X	X	H	X	X	L	X	High-Z	High-Z	5, 6
No Operation	Idle	X	X	L	X	X	L	X	Low-Z	X	4, 6
Initial Burst Read	Active		L	L	X	H	L	L	Low-Z	Data-Out	4, 8
Initial Burst Write	Active		L	L	H	L	L	X	Low-Z	Data-In	4, 8
Burst Continue	Active		H	L	X	X	L	X	Low-Z	Data-In or Data-Out	4, 8
Burst Suspend	Active	X	X	L	H	X	L	X	Low-Z	High-Z	4, 8
Configuration Register	Active		L	L	H	L	H	X	Low-Z	High-Z	8
DPD	Deep Power-Down	X	X	H	X	X	X	X	High-Z	High-Z	7

Notes:
1. *CLK may be High or Low, but must be static during asynchronous Read, synchronous Write, burst suspend, and DPD modes; and to achieve standby power during standby and active modes.*
2. *The Wait polarity is configured through the bus configuration register (BCR[10]).*
3. *When LB# and UB# are in select mode (Low), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.*
4. *The device will consume active power in this mode whenever addresses are changed.*
5. *When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.*
6. *V_{IN} = V_{CC}Q or 0V; all device balls must be static (unswitched) to achieve standby current.*
7. *DPD is maintained until RCR is reconfigured.*
8. *Burst mode operation is initialized through the bus configuration register (BCR[15]).*

21 Functional Description

The CellularRAM bus interface supports both asynchronous and burst mode transfers. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous Read protocol.

21.1 Power-Up Initialization

CellularRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings (see Table 24.1 and Table 24.4). V_{CC} and V_{CCQ} must be applied simultaneously. When they reach a stable level at or above 1.7V, the device will require 150 µs to complete its self-initialization process. During the initialization period, CE# should remain High. When initialization is complete, the device is Ready for normal operation.

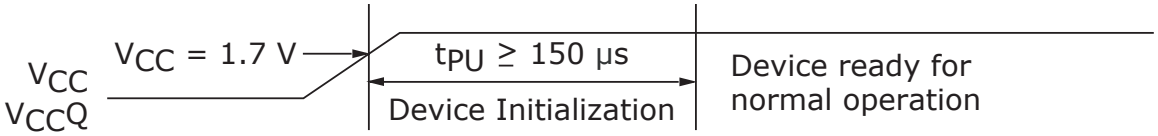


Figure 21.1 Power-Up Initialization Timing

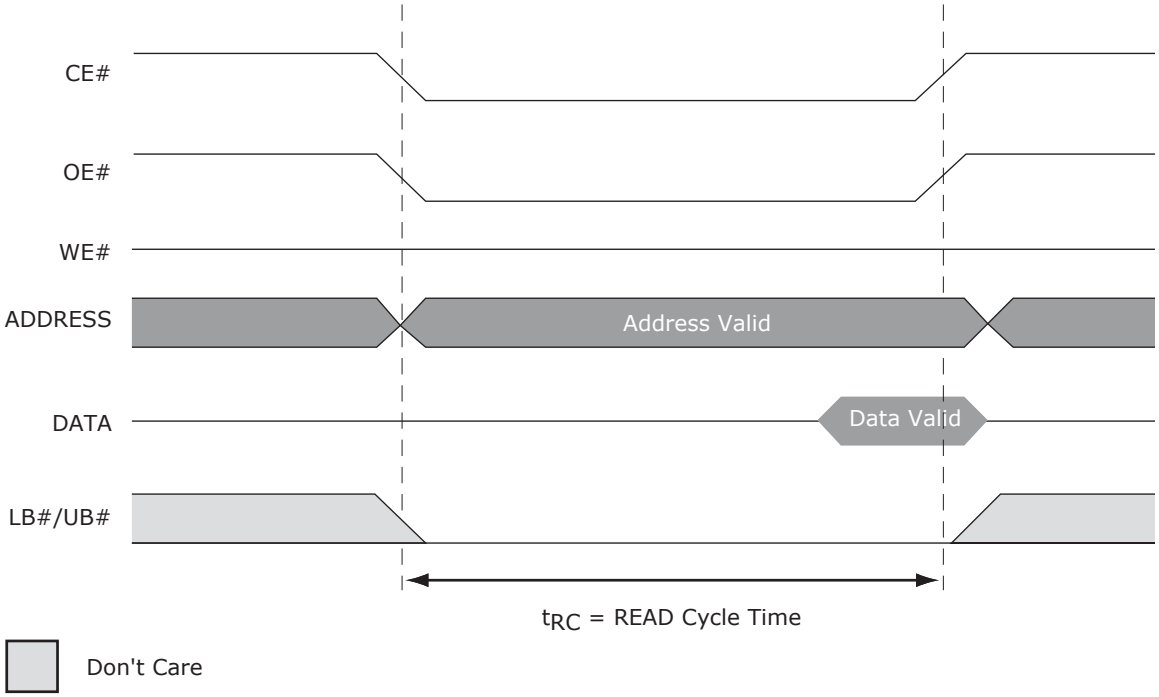
22 Bus Operating Modes

CellularRAM products incorporate a burst mode interface found on Flash products targeting low-power, wireless applications. This bus interface supports asynchronous, page mode, and burst mode Read and Write transfers. The specific interface supported is defined by the value loaded into the BCR. Page mode is controlled by the refresh configuration register (RCR[7]).

22.1 Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry standard SRAM control bus (CE#, OE#, WE#, LB#/ UB#). Read operations (Figure 22.1) are initiated by bringing CE#, OE#, and LB#/UB# Low while keeping WE# High. Valid data will be driven out of the I/Os after the specified access time has elapsed. Write operations (Figure 22.2) occur when CE#, WE#, and LB#/ UB# are driven Low. During asynchronous Write operations, the OE# level is a *don't care*, and WE# will override OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). Asynchronous operations (page mode disabled) can either use the ADV input to latch the address, or ADV can be driven Low during the entire Read/Write operation.

During asynchronous operation, the CLK input must be held static (High or Low, no transitions). Wait will be driven while the device is enabled and its state should be ignored. WE# low time must be limited to t_{CEM}.



Note: *ADV must remain Low for page mode operation.*

Figure 22.1 Read Operation (ADV# Low)

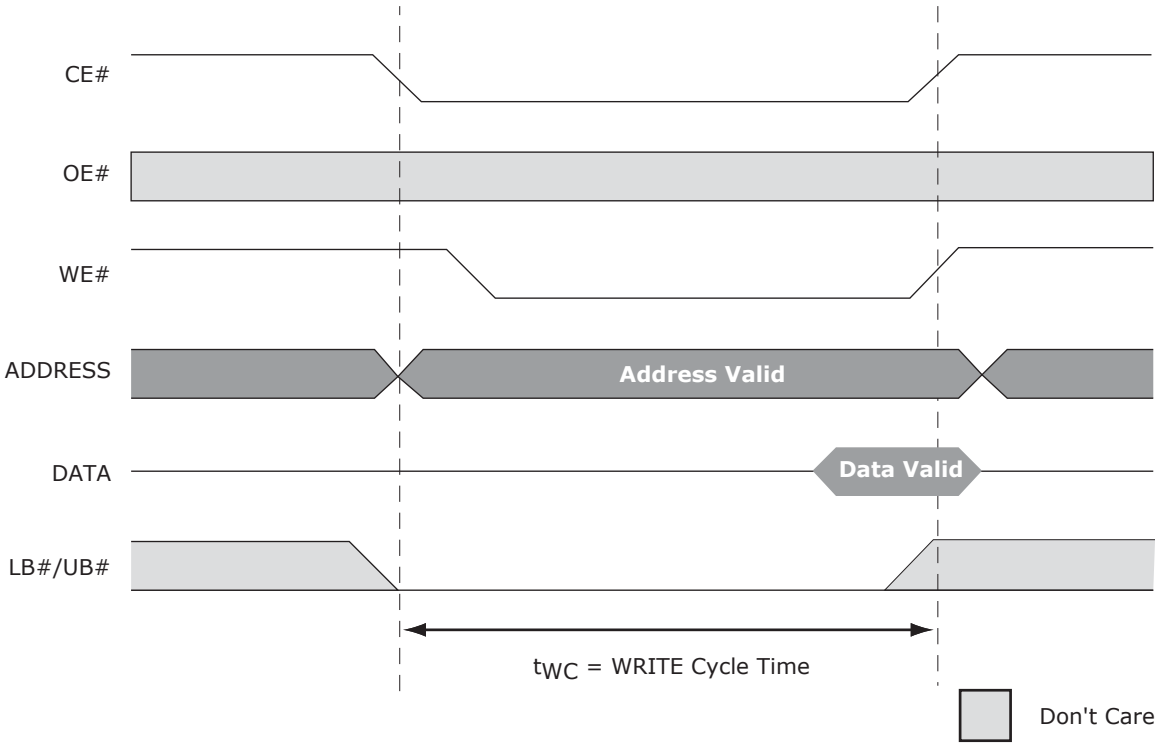


Figure 22.2 Write Operation (ADV# Low)

22.2 Page Mode Read Operation

Page mode is a performance-enhancing extension to the legacy asynchronous Read operation. In page mode-capable products, an initial asynchronous Read access is performed, then adjacent addresses can be Read quickly by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Addresses A[4] and higher must remain fixed during the entire page mode access. Figure 22.3 shows the timing for a page mode access. Page mode takes advantage of the fact that adjacent addresses can be Read in a shorter period of time than random addresses. Write operations do not include comparable page mode functionality.

During asynchronous page mode operation, the CLK input must be static (HIGH or LOW - no transitions). CE# must be driven High upon completion of a page mode access. WAIT is driven while the device is enabled and its state should be ignored. Page mode is enabled by setting RCR[7] to High. ADV must be driven Low during all page mode Read accesses. The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than t_{CEM}.

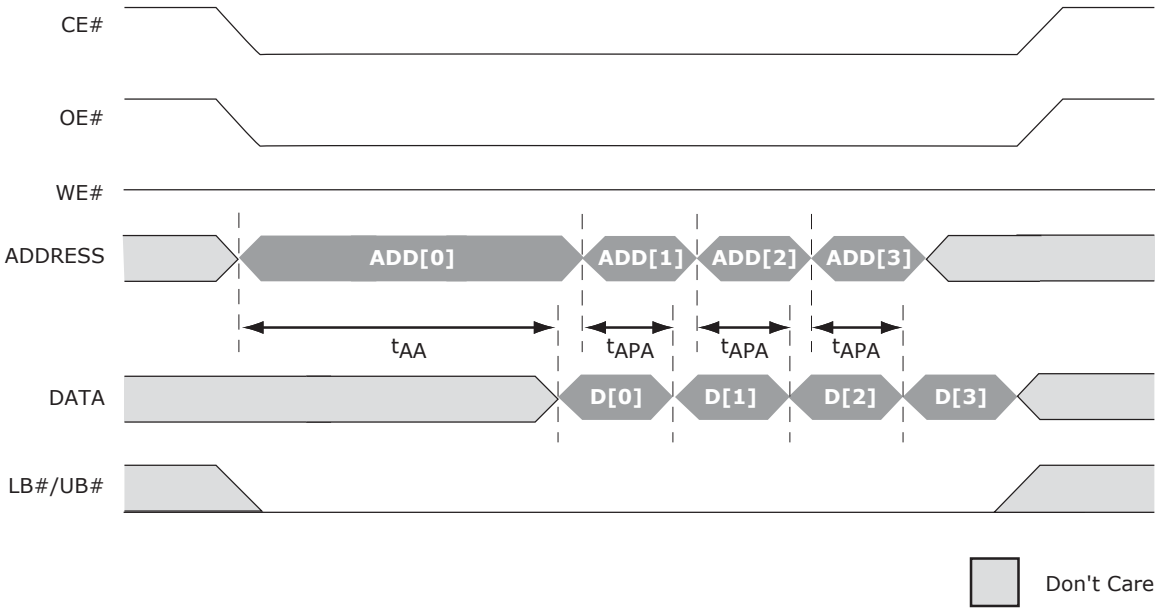


Figure 22.3 Page Mode Read Operation (ADV# Low)

22.3 Burst Mode Operation

Burst mode operations enable High-speed synchronous Read and Write operations. Burst operations consist of a multi-clock sequence that must be performed in an ordered fashion. After CE# goes Low, the address to access is latched on the rising edge of the next clock that ADV# is Low. During this first clock rising edge, WE# indicates whether the operation is going to be a Read (WE# = High, Figure 22.4) or Write (WE# = Low, Figure 22.5).

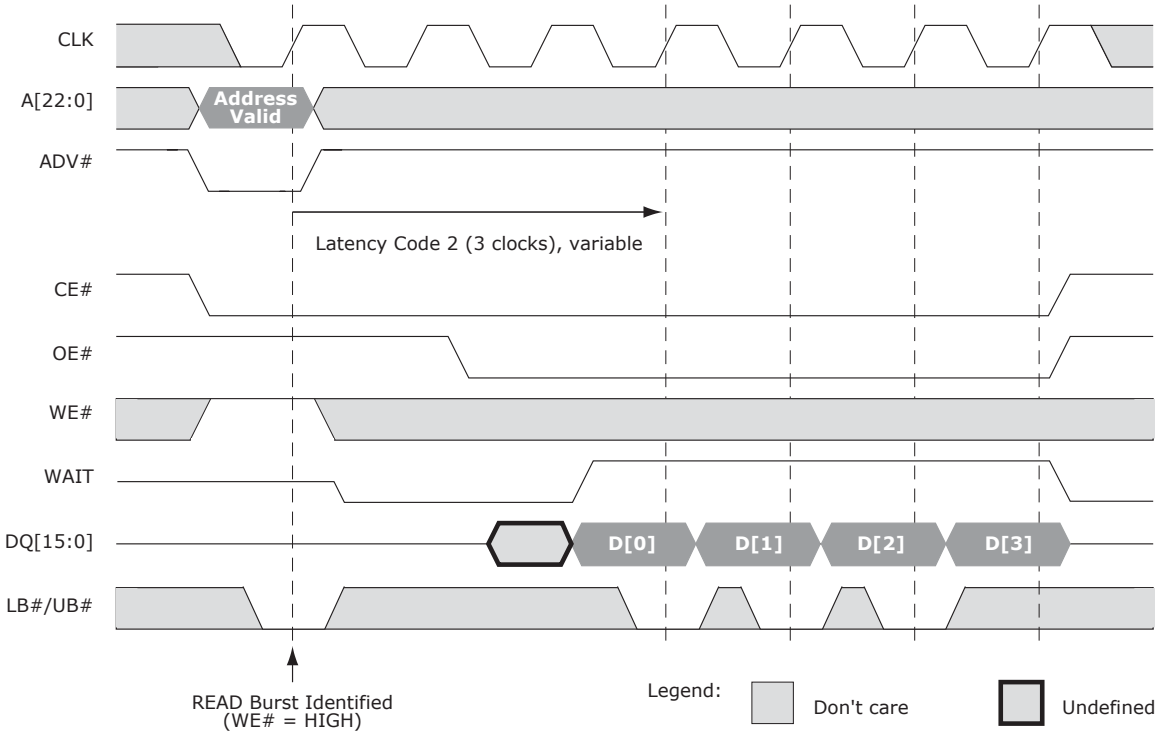
The size of a burst can be specified in the BCR either as a fixed length or continuous. Fixed-length bursts consist of four, eight, or sixteen words. Continuous bursts have the ability to start at a specified address and burst through the entire memory.

The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and CellularRAM device.

The WAIT output is asserted as soon as CE# goes LOW, and is de-asserted to indicate when data is to be transferred into (or out of) the memory. WAIT is again asserted if the burst crosses the boundary between 128-word rows. Once the CellularRAM device has restored the previous row's data and accessed the next row, Wait will be deasserted and the burst can continue (Figure 27.11).

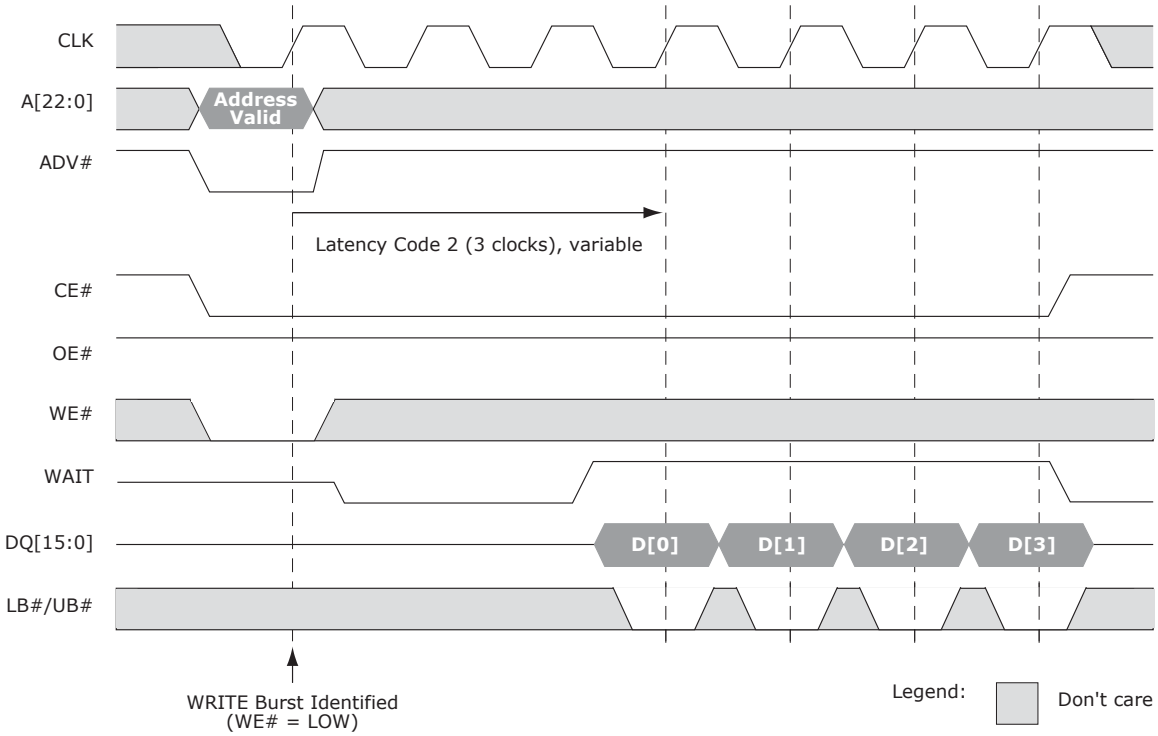
To access other devices on the same bus without the timing penalty of the initial latency for a new burst, burst mode can be suspended. Bursts are suspended by stopping CLK. CLK can be stopped High or Low. If another device will use the data bus while the burst is suspended, OE# should be taken High to disable the CellularRAM outputs; otherwise, OE# can remain Low. Note that the Wait output will continue to be active, and as a result no other devices should directly share the Wait connection to the controller. To continue the burst sequence, OE# is taken Low, then CLK is restarted after valid data is available on the bus.

The CE# low time is limited by refresh considerations. CE# must not stay low longer than t_{CEM} unless row boundaries are crossed at least every t_{CEM}. If a burst suspension causes CE# to remain Low for longer than t_{CEM}, CE# should be taken High and the burst restarted with a new CE# Low/ ADV# low cycle.



Note: *Non-default BCR settings: Variable latency; latency code two (three clocks); Wait active Low; Wait asserted during delay.*

Figure 22.4 Burst Mode Read (4-word burst)



Note: *Non-default BCR settings: Variable latency; latency code two (three clocks); Wait active Low; Wait asserted during delay.*

Figure 22.5 Burst Mode Write (4-word burst)

22.4 Mixed-Mode Operation

The device can support a combination of synchronous Read and asynchronous Write operations when the BCR is configured for synchronous operation. The asynchronous Write operation requires that the clock (CLK) remain static (High or Low) during the entire sequence. The ADV# signal can be used to latch the target address, or it can remain Low during the entire Write operation. CE# can remain Low when transitioning between mixed-mode operations with fixed latency enabled. Note that the t_{CKA} period is the same as a Read or Write cycle. This time is required to ensure adequate refresh. Mixed-mode operation facilitates a seamless interface to legacy burst mode Flash memory controllers. See Figure 27.19, Asynchronous Write Followed by Burst Read (timing diagram).

22.5 Wait Operation

The Wait output on a CellularRAM device is typically connected to a shared, system-level Wait signal (Figure 22.6). The shared Wait signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus.

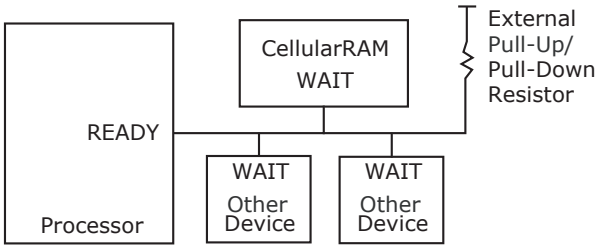


Figure 22.6 Wired or Wait Configuration

Once a Read or Write operation has been initiated, Wait goes active to indicate that the CellularRAM device requires additional time before data can be transferred. For Read operations, Wait will remain active until valid data is output from the device. For Write operations, Wait will indicate to the memory controller when data will be accepted into the CellularRAM device. When Wait transitions to an inactive state, the data burst will progress on successive clock edges.

CE# must remain asserted during Wait cycles (Wait asserted and Wait configuration BCR[8] = 1). Bringing CE# High during Wait cycles may cause data corruption. (Note that for BCR[8] = 0, the actual Wait cycles end one cycle after Wait de-asserts, and for row boundary crossings, start one cycle after the Wait signal asserts.)

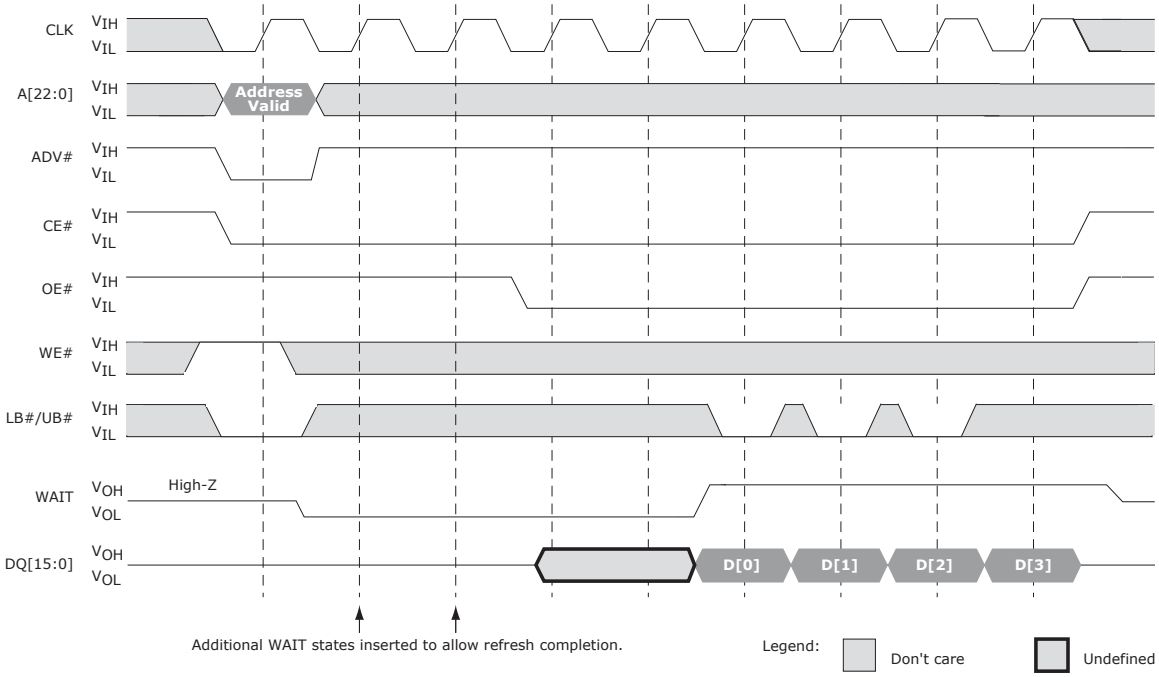
The WAIT output also performs an arbitration role when a Read or Write operation is launched while an on-chip refresh is in progress. If a collision occurs, the Wait pin is asserted for additional clock cycles until the refresh has completed (Figure 22.7 and Figure 22.8). When the refresh operation has completed, the Read or Write operation will continue normally.

Wait is also asserted when a continuous Read or Write burst crosses the boundary between 128-word rows. The Wait assertion allows time for the new row to be accessed, and permits any pending refresh operations to be performed.

22.6 LB#/UB# Operation

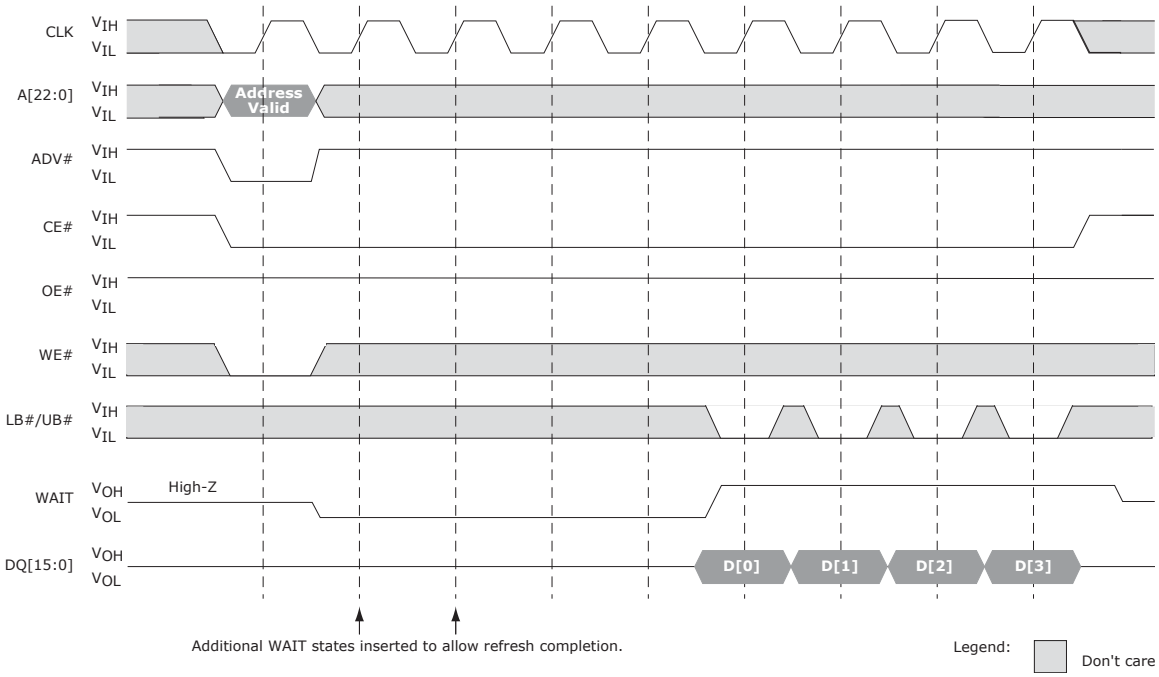
The LB# enable and UB# enable signals support byte-wide data transfers. During Read operations, the enabled byte(s) are driven onto the DQs. The DQs associated with a disabled byte are put into a High-Z state during a Read operation. During Write operations, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During an asynchronous Write cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first.

When both the LB# and UB# are disabled (High) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains Low.



Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*

Figure 22.7 Refresh Collision During Read Operation



Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*

Figure 22.8 Refresh Collision During Write Operation

23 Low-Power Operation

23.1 Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation. Standby operation occurs when CE# is High.

The device will enter a reduced power state upon completion of a Read or Write operation, or when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

23.2 Temperature Compensated Refresh

Temperature compensated refresh (TCR) is used to adjust the refresh rate depending on the device operating temperature. DRAM technology requires increasingly frequent refresh operation to maintain data integrity as temperatures increase. More frequent refresh is required due to increased leakage of the DRAM capacitive storage elements as temperatures rise. A decreased refresh rate at lower temperatures will facilitate a savings in standby current.

TCR allows for adequate refresh at four different temperature thresholds (+15°C, +45°C, +70°C, and +85°C). The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. For example, if the case temperature is 50°C, the system can minimize self refresh current consumption by selecting the 70°C setting. The +15°C and +45°C settings would result in inadequate refreshing and cause data corruption.

23.3 Partial Array Refresh

Partial array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, three-quarter array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (Table 24.5). Read and Write operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

23.4 Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled by rewriting the RCR, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume. During this 150µs period, the current consumption will be higher than the specified standby levels, but considerably lower than the active current specification.

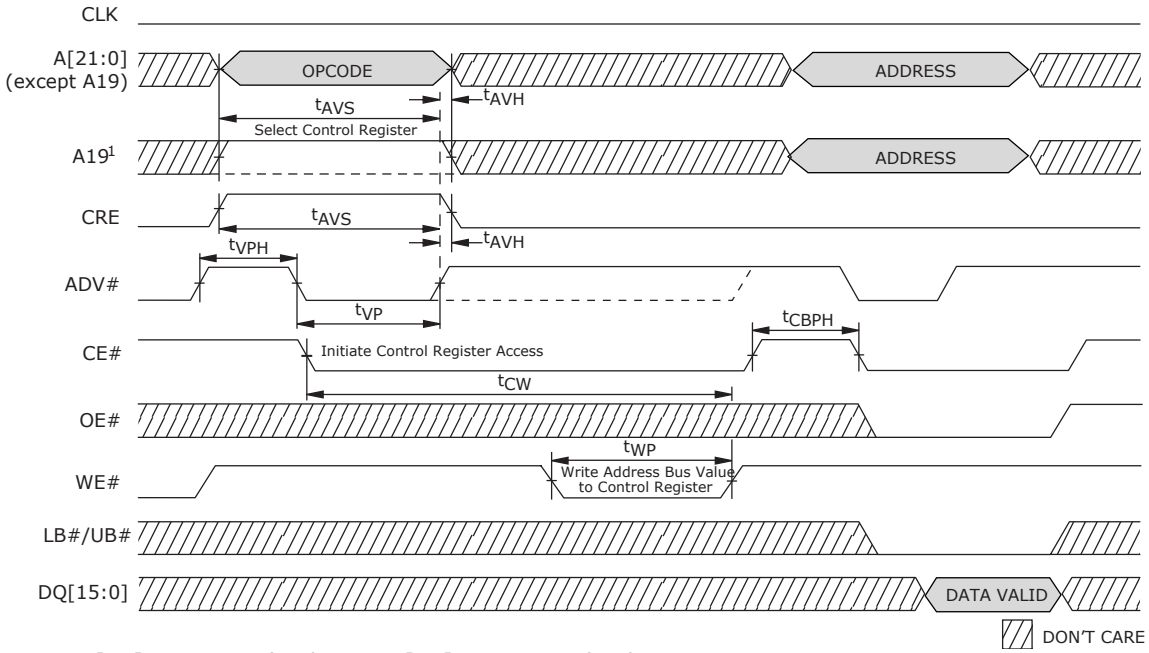
DPD cannot be enabled or disabled by writing to the RCR using the software access sequence; the RCR should be accessed using CRE instead.

24 Configuration Registers

Two user-accessible configuration registers define the device operation. The bus configuration register (BCR) defines how the CellularRAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up, and can be updated any time the devices are operating in a standby state.

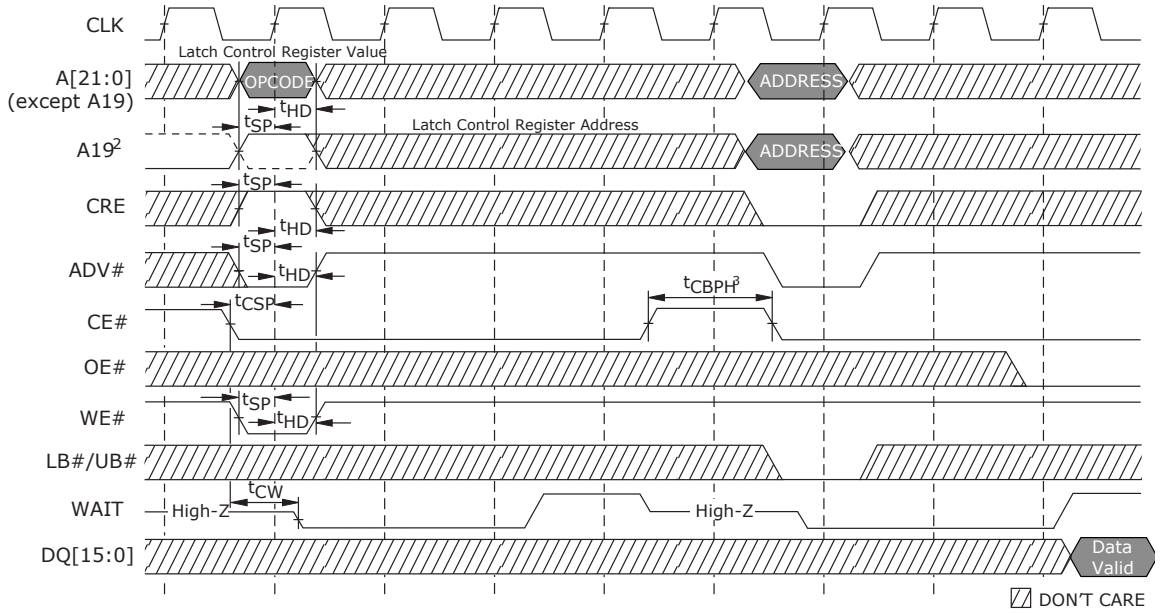
24.1 Access Using CRE

The configuration registers are loaded using either a synchronous or an asynchronous operation when the configuration register enable (CRE) input is High (see Figure 24.2). When CRE is Low, a Read or Write operation will access the memory array. The register values are written via address pins A[21:0]. In an asynchronous Write, the values are latched into the configuration register on the rising edge of ADV#, CE#, or WE#, whichever occurs first; LB# and UB# are *Don't Care*. The BCR is accessed when A[19] is High; the RCR is accessed when A[19] is Low.



Note: *A[19] = LOW to load RCR; A[19] = HIGH to load BCR.*

Figure 24.1 Configuration Register WRITE in Asynchronous Mode Followed by READ ARRAY Operation



Note: *A[19] = Low to load RCR; A[19] = High to load BCR.*

Figure 24.2 Configuration Register WRITE in Synchronous Mode Followed by READ ARRAY Operation

24.2 Software Access

Software access of the configuration registers uses a sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be read or modified using the software sequence.

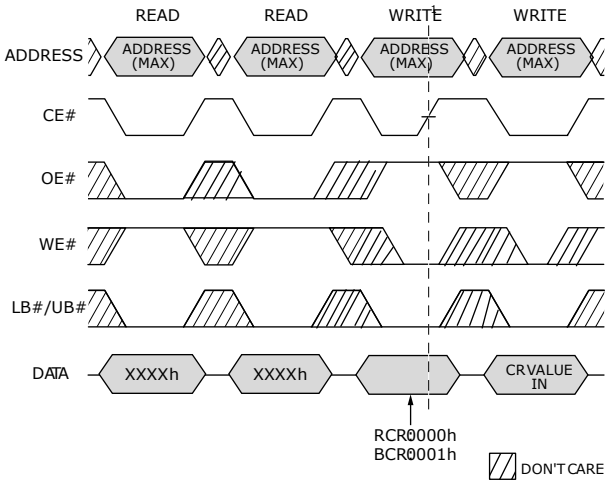
The configuration registers are loaded using a four step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations (see Figure 24.3). The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 24.4). Note that a third READ cycle cancels the access sequence.

The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (3FFFFFh for 64Mb); the content at this address is changed by using this sequence (note that this is a deviation from the CellularRAM specification).

The data value presented during the third operation (WRITE) in the sequence defines whether the BCR or the RCR is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR. During the fourth operation, the data bus is used to transfer data in to or out of the configuration registers.

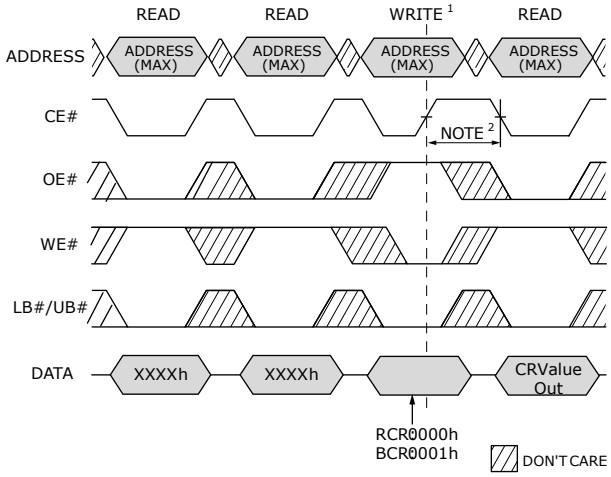
The use of the software sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for the control register enable (CRE) pin. If the software mechanism is used, the CRE pin can simply be tied to V_{SS}. The port line often used for CRE control purposes is no longer required.

Software access of the RCR should not be used to enter or exit DPD.



Note: *The WRITE on the third cycle must be CE# controlled.*

Figure 24.3 Load Configuration Register



Notes:

1. *The WRITE on the third cycle must be CE# controlled.*
2. *CE# must be HIGH for 150ns before performing the cycle that reads a configuration register.*

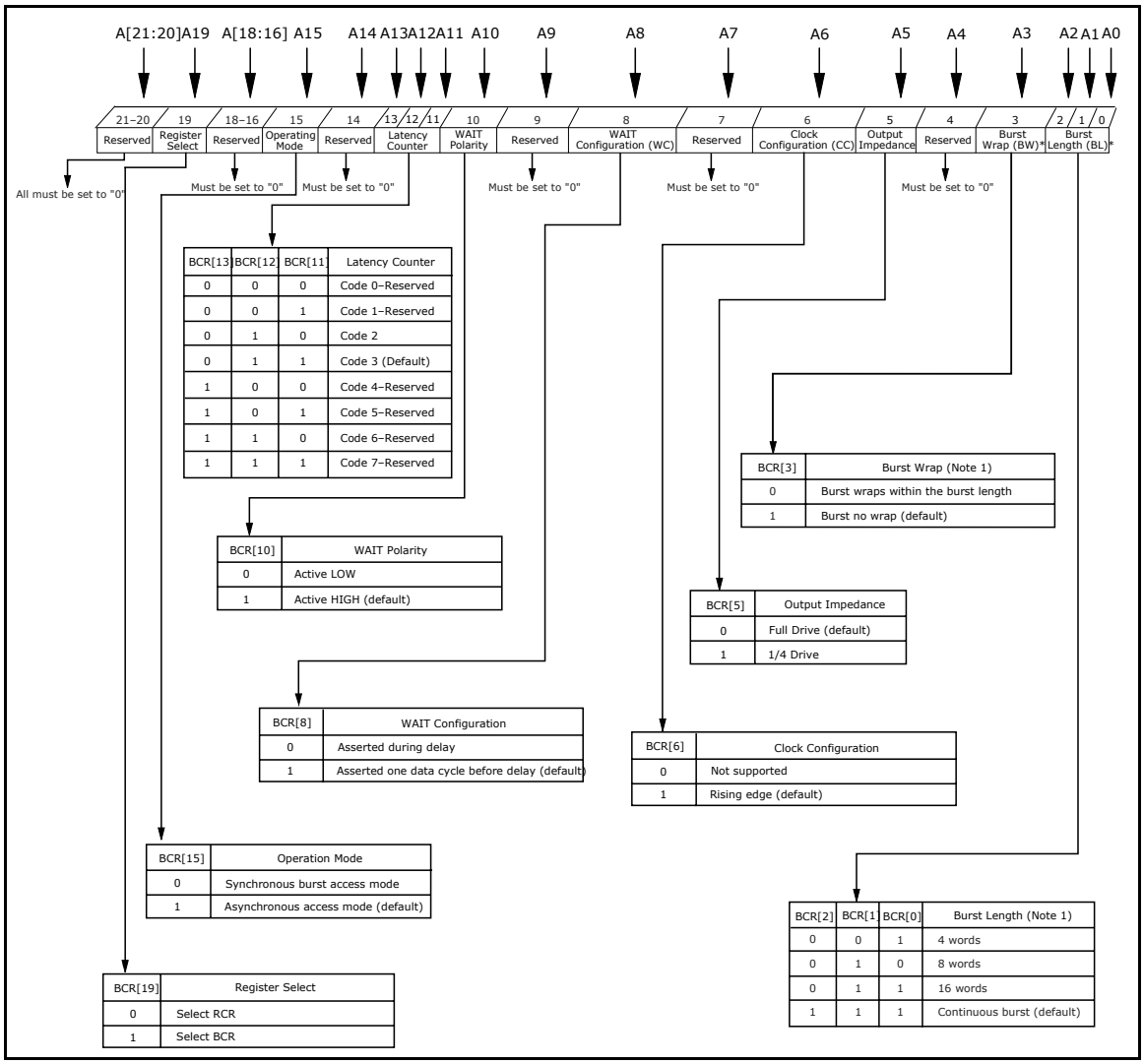
Figure 24.4 Read Configuration Register

24.3 Bus Configuration Register

The BCR defines how the CellularRAM device interacts with the system memory bus. Page mode operation is enabled by a bit contained in the RCR. Table 24.1 below describes the control bits in the BCR. At power-up, the BCR is set to 9D4Fh.

The BCR is accessed using CRE and A[19] High, or through the configuration register software sequence with DQ = 0001h on the third cycle.

Table 24.1 Bus Configuration Register Definition



Note: *All burst Writes are continuous.*

Table 24.2 Sequence and Burst Length

Burst Wrap		Starting Address	4-Word Burst Length	8-Word Burst Length	16-Word Burst Length	Continuous Burst
BCR[3]	Wrap	(Decimal)	Linear	Linear	Linear	Linear
0	Yes	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-…
		1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-2-3-4-5-6-7-…
		2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-4-5-6-7-8-…
		3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-4-5-6-7-8-9-…
		4		4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-7-8-9-10-…
		5		5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-6-7-8-9-10-11-…
		6		6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-8-9-10-11-12-…
		7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-8-9-10-11-12-13-…
		…			…	…
		14			14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-16-17-18-19-20-…
		15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-18-19-20-21…
1	No	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-…
		1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16	1-2-3-4-5-6-7-…
		2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17	2-3-4-5-6-7-8-…
		3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18	3-4-5-6-7-8-9-…
		4		4-5-6-7-8-9-10-11	4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19	4-5-6-7-8-9-10-…
		5		5-6-7-8-9-10-11-12	5-6-7-8-9-10-11-12- 13-…-15-16-17-18-19-20	5-6-7-8-9-10-11…
		6		6-7-8-9-10-11-12-13	6-7-8-9-10-11-12-13- 14-…-16-17-18-19-20-21	6-7-8-9-10-11-12…
		7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13- 14-…-17-18-19-20-21-22	7-8-9-10-11-12-13…
		…			…	…
		14			14-15-16-17-18-19-…-23-24-25-26-27-28-29	14-15-16-17-18-19-20-…
		15			15-16-17-18-19-20-…-24-25-26-27-28-29-30	15-16-17-18-19-20-21-…

24.3.1 Burst Length (BCR[2:0]): Default = Continuous Burst

Burst lengths define the number of words the device outputs during burst Read operations. The device supports a burst length of 4, 8, or 16 words. The device can also be set in continuous burst mode where data is output sequentially without regard to address boundaries; the internal address wraps to 000000h if the device is read past the last address. Write bursts are always performed using continuous burst mode.

24.3.2 Burst Wrap (BCR[3]): Default = No Wrap

The burst-wrap option determines if a 4-, 8-, or 16-word Read burst wraps within the burst length or steps through sequential addresses. If the wrap option is not enabled, the device accesses data from sequential addresses without regard to burst boundaries; the internal address wraps to 000000h if the device is read past the last address.

24.3.3 Output Impedance (BCR[5]): Default = Outputs Use Full Drive Strength

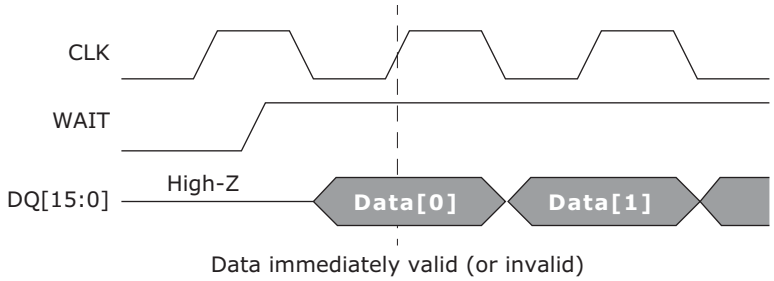
The output driver strength can be altered to full, one-half, or one-quarter strength to adjust for different data bus loading scenarios. The reduced-strength options are intended for stacked chip (Flash + CellularRAM) environments when there is a dedicated memory bus. The reduced-drive-strength option minimizes the noise generated on the data bus during Read operations. Normal output drive strength should be selected when using a discrete CellularRAM device in a more heavily loaded data bus environment. Outputs are configured at full drive strength during testing.

24.3.4 Wait Configuration (BCR[8]): Default = Wait Transitions One Clock Before Data Valid/Invalid

The Wait configuration bit is used to determine when Wait transitions between the asserted and the de-asserted state with respect to valid data presented on the data bus. The memory controller will use the Wait signal to coordinate data transfer during synchronous Read and Write operations. When BCR[8] = 0, data will be valid or invalid on the clock edge immediately after Wait transitions to the de-asserted or asserted state, respectively (Figure 24.5 and Figure 24.7). When A8 = 1, the Wait signal transitions one clock period prior to the data bus going valid or invalid (Figure 24.6).

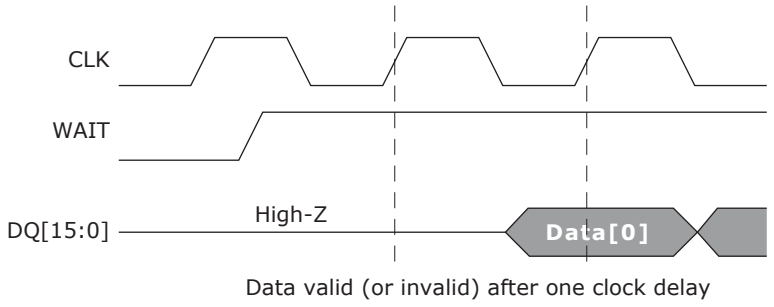
24.3.5 Wait Polarity (BCR[10]): Default = Wait Active High

The Wait polarity bit indicates whether an asserted Wait output should be High or Low. This bit will determine whether the Wait signal requires a pull-up or pull-down resistor to maintain the de-asserted state.



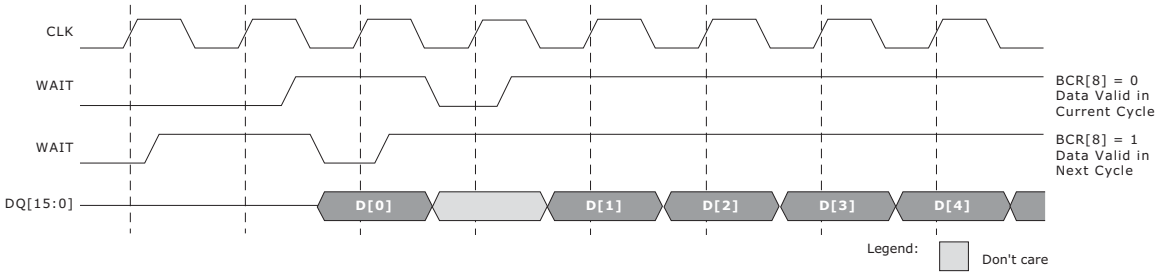
Note: *Data valid/invalid immediately after Wait transitions (BCR[8] = 0). See Figure 24.7.*

Figure 24.5 Wait Configuration (BCR[8] = 0)



Note: *Valid/invalid data delayed for one clock after Wait transitions (BCR[8] = 1). See Figure 24.7.*

Figure 24.6 Wait Configuration (BCR[8] = I)



Note: *Non-default BCR setting: Wait active Low.*

Figure 24.7 Wait Configuration During Burst Operation

24.3.6 Latency Counter (BCR[13:11]): Default = Three-Clock Latency

The latency counter bits determine how many clocks occur between the beginning of a Read or Write operation and the first data value transferred. Latency codes from two (three clocks) to six (seven clocks) are allowed (see Table 24.3 and Figure 24.8 below).

Table 24.3 Variable Latency Configuration Codes

Latency Configuration Code	Max Input Clk Frequency (MHz)	
	70 ns/80 MHz	70 ns/66 MHz
2 (3 clocks)	53 (18.75 ns)	44 (22.7 ns)
3 (4 clocks)—default	80 (12.5 ns)	66 (15.2 ns)

Note: *Clock rates below 50MHz are allowed as long as t_{CSP} specifications are met.*

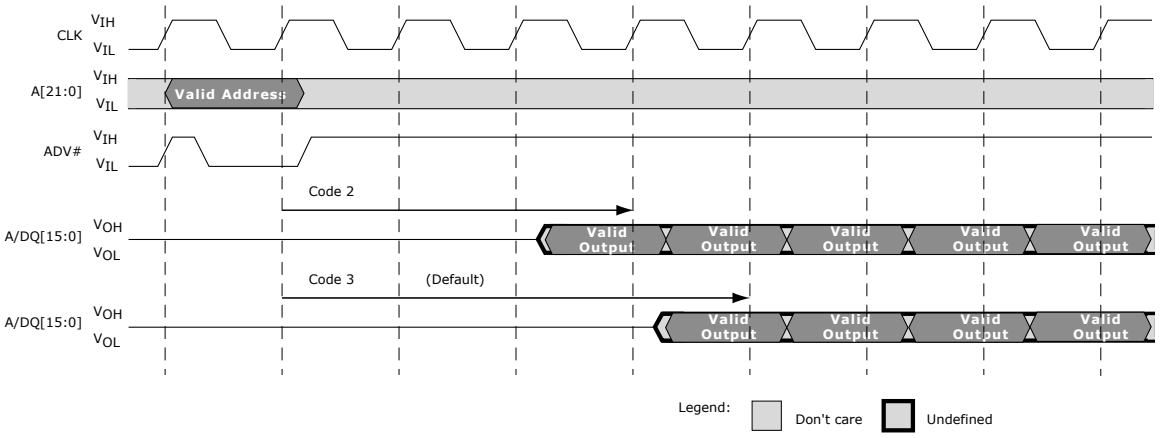


Figure 24.8 Latency Counter (Variable Initial Latency, No Refresh Collision)

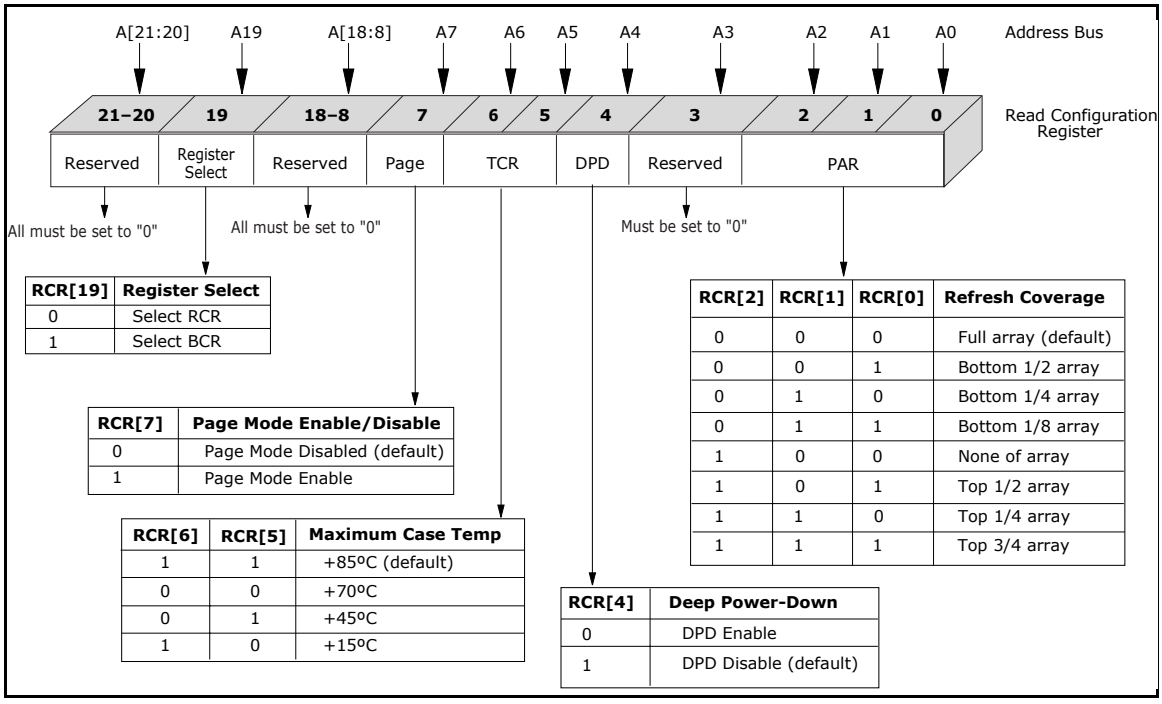
24.3.7 Operating Mode (BCR[15]): Default = Asynchronous Operation

The operating mode bit selects either synchronous burst operation or the default asynchronous mode of operation.

24.4 Refresh Configuration Register

The refresh configuration register (RCR) defines how the CellularRAM device performs its transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the RCR. Table 24.4 below describes the control bits used in the RCR. At power-up, the RCR is set to 0070h. The RCR is accessed using CRE and A[19] Low, or through the configuration register software access sequence with DQ = 0000h on the third cycle.

Table 24.4 Refresh Configuration Register Mapping



24.4.1 Partial Array Refresh (RCR[2:0]): Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, three-quarters array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 24.5).

Table 24.5 64Mb Address Patterns for PAR (RCR[4] = l)

RCR[2]	RCR[1]	RCR[0]	Active Section	Address Space	Size	Density
0	0	0	Full die	000000h–3FFFFFh	4 Meg x 16	64Mb
0	0	1	One-half of die	000000h–2FFFFFh	2 Meg x 16	32Mb
0	1	0	One-quarter of die	000000h–1FFFFFh	1 Meg x 16	16Mb
0	1	1	One-eighth of die	000000h–0FFFFFh	512 K x 16	8Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	100000h–3FFFFFh	2 Meg x 16	32Mb
1	1	0	One-quarter of die	200000h–3FFFFFh	1 Meg x 16	16Mb
1	1	1	One-eighth of die	300000h–3FFFFFh	512 K x 16	8Mb

24.4.2 Deep Power-Down (RCR[4]): Default = DPD Disabled

The deep power-down bit enables and disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume.

Deep power-down is enabled when RCR[4] = 0, and remains enabled until RCR[4] is set to *1*.

24.4.3 Temperature Compensated Refresh (RCR[6:5]): Default = +85ºC Operation

The TCR bits allow for adequate refresh at four different temperature thresholds (+15ºC, +45ºC, +70ºC, and +85ºC). The setting selected must be for a temperature higher than the case temperature of the CellurlarRAM device. If the case temperature is +50ºC, the system can minimize self refresh current consumption by selecting the +70ºC setting. The +15ºC and +45ºC settings would result in inadequate refreshing and cause data corruption.

24.4.4 Page Mode Operation (RCR[7]): Default = Disabled

The page mode operation bit determines whether page mode is enabled for asynchronous Read operations. In the power-up default state, page mode is disabled.

25 Absolute Maximum Ratings

Voltage to Any Ball Except V_{CC}, $V_{CC}Q$ Relative to V_{SS} . . . . . –0.50V to (4.0V or V_{CCQ} + 0.3V, whichever is less)

Voltage on V_{CC} Supply Relative to V_{SS} . . . . . –0.2V to +2.45V

Voltage on V_{CCQ} Supply Relative to V_{SS} . . . . . –0.2V to +4.0V

Storage Temperature (plastic) . . . . . –55ºC to +150ºC

Operating Temperature (case)

Wireless (See Note) . . . . . 30ºC to +85ºC

Industrial . . . . . –40°C to +85°C

Soldering Temperature and Time

10 s (lead only) . . . . . +260°C

Note: *–30°C exceeds the CellularRAM Workgroup 1.0 specification of –25°C.*

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

26 DC Characteristics

Table 26.1 Electrical Characteristics and Operating Conditions

Description	Conditions	Symbol		Min	Max	Units	Notes
Supply Voltage		V_{CC}		1.70	1.95	V	
I/O Supply Voltage		V_{CCQ}	W: 1.8V	1.70	3.30	V	
Input High Voltage		V_{IH}		1.4	$V_{CC}Q$ + 0.2	V	2
Input Low Voltage		V_{IL}		-0.20	0.4	V	3
Output High Voltage	I_{OH} = -0.2mA	V_{OH}		0.80 $V_{CC}Q$		V	4
Output Low Voltage	I_{OL} = +0.2mA	V_{OL}			0.20 $V_{CC}Q$	V	4
Input Leakage Current	V_{IN} = 0 to $V_{CC}Q$	I_{LI}			1	µA	
Output Leakage Current	OE# = V_{IH} or Chip Disabled	I_{LO}			1	µA	
Operating Current							
Asynchronous Random Read	V_{IN} = $V_{CC}Q$ or 0V Chip Enabled, IOUT = 0	$I_{CC}1$	-70		25	mA	5
Asynchronous Page Read			-70		15		
Initial Access, Burst Read	V_{IN} = $V_{CC}Q$ or 0V Chip Enabled, IOUT = 0	$I_{CC}1$	80 MHz		35	mA	5
			66 MHz		30		
Continuous Burst Read			80 MHz		18		
			66 MHz		15		
Continuous Burst Write	V_{IN} = $V_{CC}Q$ or 0V Chip Enabled, I_{OUT} = 0	$I_{CC}2$	80 MHz		35	mA	5
			66 MHz		30		
Standby Current	V_{IN} = $V_{CC}Q$ or 0V CE# = $V_{CC}Q$	I_{SB}	64 M		120	µA	6

Notes:

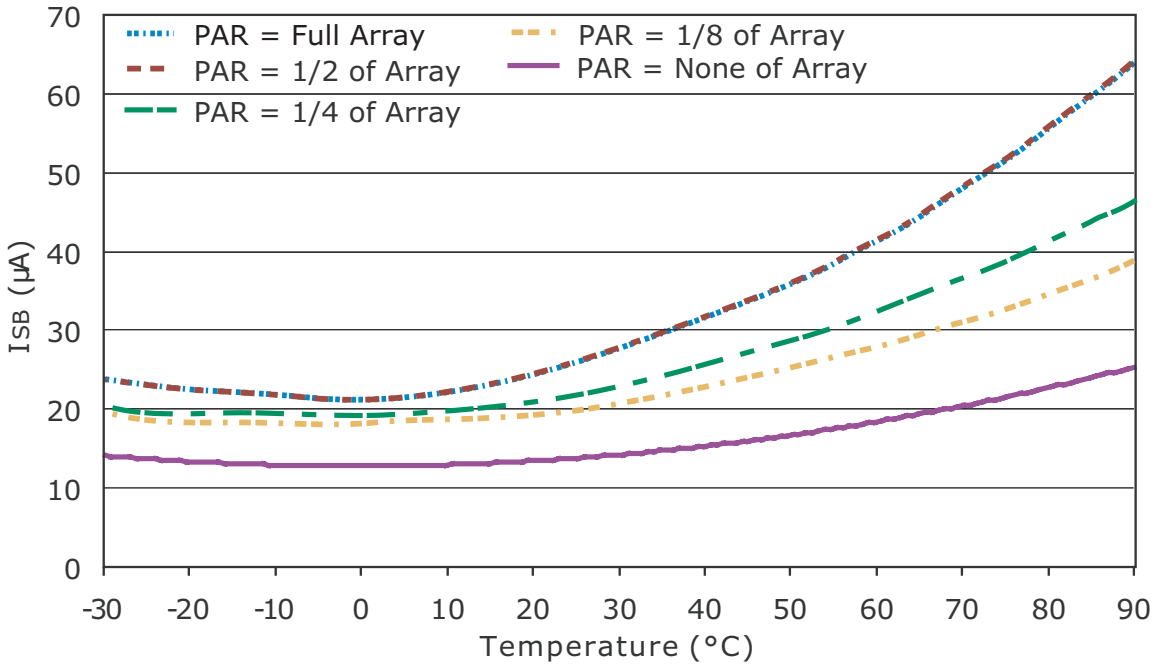
1. *Wireless Temperature (-25ºC < TC < +85ºC); Industrial Temperature (-40ºC < TC < +85ºC).*
2. *Input signals may overshoot to $V_{CC}Q$ + 1.0V for periods less than 2ns during transitions.*
3. *Input signals may undershoot to V_{SS} - 1.0V for periods less than 2ns during transitions.*
4. *BCR[5:4] = 00b.*
5. *This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.*
6. *ISB (MAX) values measured with PAR set to FULL ARRAY and TCR set to +85°C. To achieve Low standby current, all inputs must be driven to either $V_{CC}Q$ or V_{SS}.*

Table 26.2 Maximum Standby Currents for Applying PAR and TCR Settings

PAR	TCR		
	+15°C (RCR[6:5] = 10b)	+45°C (RCR[6:5] = 01b)	+85°C (RCR[6:5] = 11b)
Full Array	70	85	120
1/2 Array	65	80	115
1/4 Array	60	75	110
1/8 Array	57	70	105
0 Array	50	55	70

Notes:

1. *For RCR[6:5] = 00b (default), refer to Figure 26.1 for typical values.*
2. *To achieve low standby current, all inputs must be driven to either V_{CCQ} or V_{SS}. ISB might be slightly higher for up to 500ms after power-up, or after changes to the PAR array partition.*
3. *Values of TCR for 85 are 100% tested. Values of TCR for 15 and 45 are sampled only.*



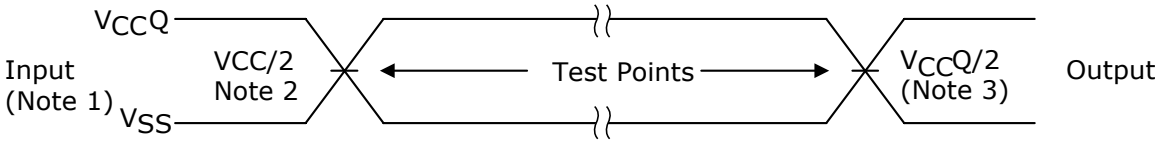
Note: *Typical ISB currents for each PAR setting with the appropriate TCR selected, or temperature sensor enabled.*

Figure 26.1 Typical Refresh Current vs. Temperature (I_{TCR})

Table 26.3 Deep Power-Down Specifications

Description	Conditions	Symbol	Typ	Units
Deep Power-down	V_{IN} = V_{CC}Q or 0V; +25°C	I_{ZZ}	10	µA

27 AC Characteristics



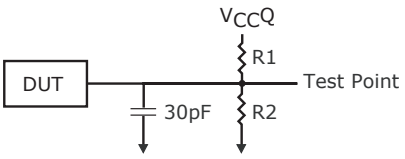
Notes:
1. *AC test inputs are driven at $V_{CC}Q$ for a logic 1 and V_{SS} for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.*
2. *Input timing begins at $V_{CC}/2$. Due to the possibility of a difference between V_{CC} and V_{CCQ}, the input test point may not be shown to scale.*
3. *Output timing ends at $V_{CC}Q/2$.*

Figure 27.1 AC Input/Output Reference Waveform

Table 27.1 Capacitance

Description	Conditions	Symbol	Min	Max	Units	Notes
Input Capacitance	T_C = +25ºC; f = 1 MHz; V_{IN} = 0V	C_{IN}	2.0	6	pF	1
Input/Output Capacitance (DQ)		C_{IO}	3.5	6	pF	1

Note: *These parameters are verified in device characterization and are not 100% tested.*



Note: *All tests are performed with the outputs configured for full drive strength (BCR[5] = 0).*

Figure 27.2 Output Load Circuit

Table 27.2 Output Load Circuit

$V_{CC}Q$	R1/R2
1.8 V	2.7 KΩ
2.5 V	3.7 KΩ
3.0 V	4.5 KΩ

Table 27.3 Asynchronous Read Cycle Timing Requirements

Parameter	Symbol	70ns		Units	Notes
		Min	Max		
Address Access Time	t_{AA}		70	ns	
ADV# Access Time	t_{AADV}		70	ns	
Page Access Time	t_{APA}		20	ns	
Address Hold from ADV# High	t_{AVH}	5		ns	
Address Setup to ADV# High	t_{AVS}	10		ns	
LB#/UB# Access Time	t_{BA}		70	ns	
LB#/UB# Disable to DQ High-Z Output	t_{BHZ}		8	ns	4
LB#/UB# Enable to Low-Z Output	t_{BLZ}	10		ns	3
Maximum CE# Pulse Width	t_{CEM}		8	µs	
CE# Low to Wait Valid	t_{CEW}	1	7.5	ns	
Chip Select Access Time	t_{CO}		70	ns	
CE# Low to ADV# High	t_{CVS}	10		ns	
Chip Disable to DQ and Wait High-Z Output	t_{HZ}		8	ns	4
Chip Enable to Low-Z Output	t_{LZ}	10		ns	3
Output Enable to Valid Output	t_{OE}		20	ns	
Output Hold from Address Change	t_{OH}	5		ns	
Output Disable to DQ High-Z Output	t_{OHZ}		8	ns	4
Output Enable to Low-Z Output	t_{OLZ}	5		ns	3
Page Cycle Time	t_{PC}	20		ns	
Read Cycle Time	t_{RC}	70		ns	
ADV# Pulse Width Low	t_{VP}	10		ns	
ADV# Pulse Width High	t_{VPH}	10		ns	

Notes:

1. *All tests are performed with the outputs configured for full drive strength (BCR[5] = 0).*
2. *High-Z to Low-Z timings are tested with the circuit shown in Figure 27.2. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.*
3. *Low-Z to High-Z timings are tested with the circuit shown in Figure 27.2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.*

Table 27.4 Burst Read Cycle Timing Requirements

Parameter	Symbol	70ns/80 MHz		70ns/66 MHz		Units	Notes
		Min	Max	Min	Max		
Burst to Read Access Time (Variable Latency)	t_{ABA}		46.5		56	ns	
CLK to Output Delay	t_{ACLK}		9		11	ns	
Burst OE# Low to Output Delay	t_{BOE}		20		20	ns	
CE# High between Subsequent Mixed-Mode Operations	t_{CBPH}	5		5		ns	
CE# Low to Wait Valid	t_{CEW}	1	7.5	1	7.5	ns	
CLK Period	t_{CLK}	12.5	20	15	20	ns	
CE# Setup Time to Active CLK Edge	t_{CSP}	4.5	20	5	20	ns	
Hold Time from Active CLK Edge	t_{HD}	2		2		ns	
Chip Disable to DQ and Wait High-Z Output	t_{HZ}		8		8	ns	2
CLK Rise or Fall Time	t_{KHKL}		1.8		2.0	ns	
CLK to Wait Valid	t_{KHTL}		9		11	ns	
CLK to DQ High-Z Output	t_{KHZ}	3	8	3	8	ns	
CLK to Low-Z Output	t_{KLZ}	2	5	2	5	ns	
Output Hold from CLK	t_{KOH}	2		2		ns	
CLK High or Low Time	t_{KP}	4		5		ns	
Output Disable to DQ High-Z Output	t_{OHZ}		8		8	ns	2
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns	3
Setup Time to Active CLK Edge	t_{SP}	3		3		ns	
Maximum CE# Pulse Width	t_{CBPH}		8		8	µs	2

Notes:

1. *All tests are performed with the outputs configured for full drive strength (BCR[5] = 0).*
2. *Low-Z to High-Z timings are tested with the circuit shown in Figure 27.2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.*
3. *High-Z to Low-Z timings are tested with the circuit shown in Figure 27.2. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.*

Table 27.5 Asynchronous Write Cycle Timing Requirements

Parameter	Symbol	70 ns		Units	Notes
		Min	Max		
Address and ADV# Low Setup Time	t_{AS}	0		ns	
Address Hold from ADV# Going High	t_{AVH}	5		ns	
Address Setup to ADV# Going High	t_{AVS}	10			
Address Valid to End of Write	t_{AW}	70		ns	
LB#/UB# Select to End of Write	t_{BW}	70		ns	
CE# Low to Wait Valid	t_{CEW}	1	7.5	ns	
Async Address-to-Burst Transition Time	t_{CKA}	70		ns	
CE# Low to ADV# High	t_{CVS}	10		ns	
Chip Enable to End of Write	t_{CW}	70		ns	
Data Hold from Write Time	t_{DH}	0		ns	
Data Write Setup Time	t_{DW}	23		ns	
Chip Disable to Wait High-Z Output	t_{HZ}		8	ns	
Chip Enable to Low-Z Output	t_{LZ}	10		ns	3
End Write to Low-Z Output	t_{OW}	5		ns	3
ADV# Pulse Width	t_{VP}	10		ns	
ADV# Pulse Width High	t_{VPH}	10		ns	
ADV# Setup to End of Write	t_{VS}	70		ns	
Write Cycle Time	t_{WC}	70		ns	
Write to DQ High-Z Output	t_{WHZ}		8	ns	2
Write Pulse Width	t_{WP}	46		ns	
Write Pulse Width High	t_{WPH}	10		ns	
Write Recovery Time	t_{WR}	0		ns	
CE# High between subsequent asynchronous operations	t_{CPH}	5		ns	

Notes:

1. *Low-Z to High-Z timings are tested with the circuit shown in Figure 27.2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.*
2. *High-Z to Low-Z timings are tested with the circuit shown in Figure 27.2. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.*

Table 27.6 Burst Write Cycle Timing Requirements

Parameter	Symbol	70ns/80 MHz		70ns/66 MHz		Units	Notes
		Min	Max	Min	Max		
CE# High between Subsequent Mixed-Mode Operations	t_{CBPH}	5		5		ns	
CE# Low to Wait Valid	t_{CEW}	1	7.5	1	7.5	ns	
Clock Period	t_{CLK}	12.5	20	15	20	ns	
CE# Setup to CLK Active Edge	t_{CSP}	4.5	20	5	20	ns	
Hold Time from Active CLK Edge	t_{HD}	2		2		ns	
Chip Disable to Wait High-Z Output	t_{HZ}		8		8	ns	
CLK Rise or Fall Time	t_{KHKL}		1.8		2.0	ns	
Clock to Wait Valid	t_{KHTL}		9		11	ns	
CLK High or Low Time	t_{KP}	4		5		ns	
Setup Time to Activate CLK Edge	t_{SP}	3		3		ns	
Minimum CE# Pulse Width	t_{CEM}		8		8	µs	

Notes:

1. *When configured for synchronous mode (BCR[15] = 0), a refresh opportunity must be provided every t_{CEM}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for greater than 15ns.*
2. *Clock rates below 50 MHz (t_{CLK} > 20ns) are allowed as long as t_{CSP} specifications are met.*

27.1 Timing Diagrams

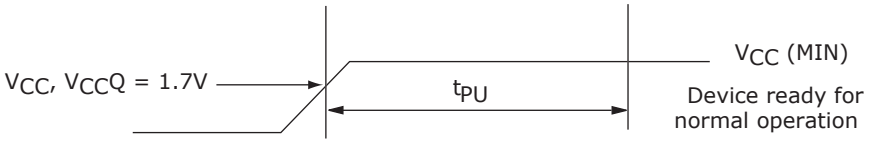


Figure 27.3 Initialization Period

Table 27.1 Initialization Timing Parameters

Parameter	Symbol	70ns/80 MHz		85ns/66 MHz		Units	Notes
		Min	Max	Min	Max		
Initialization Period (required before normal operations)	t_{PU}		150		150	µs	

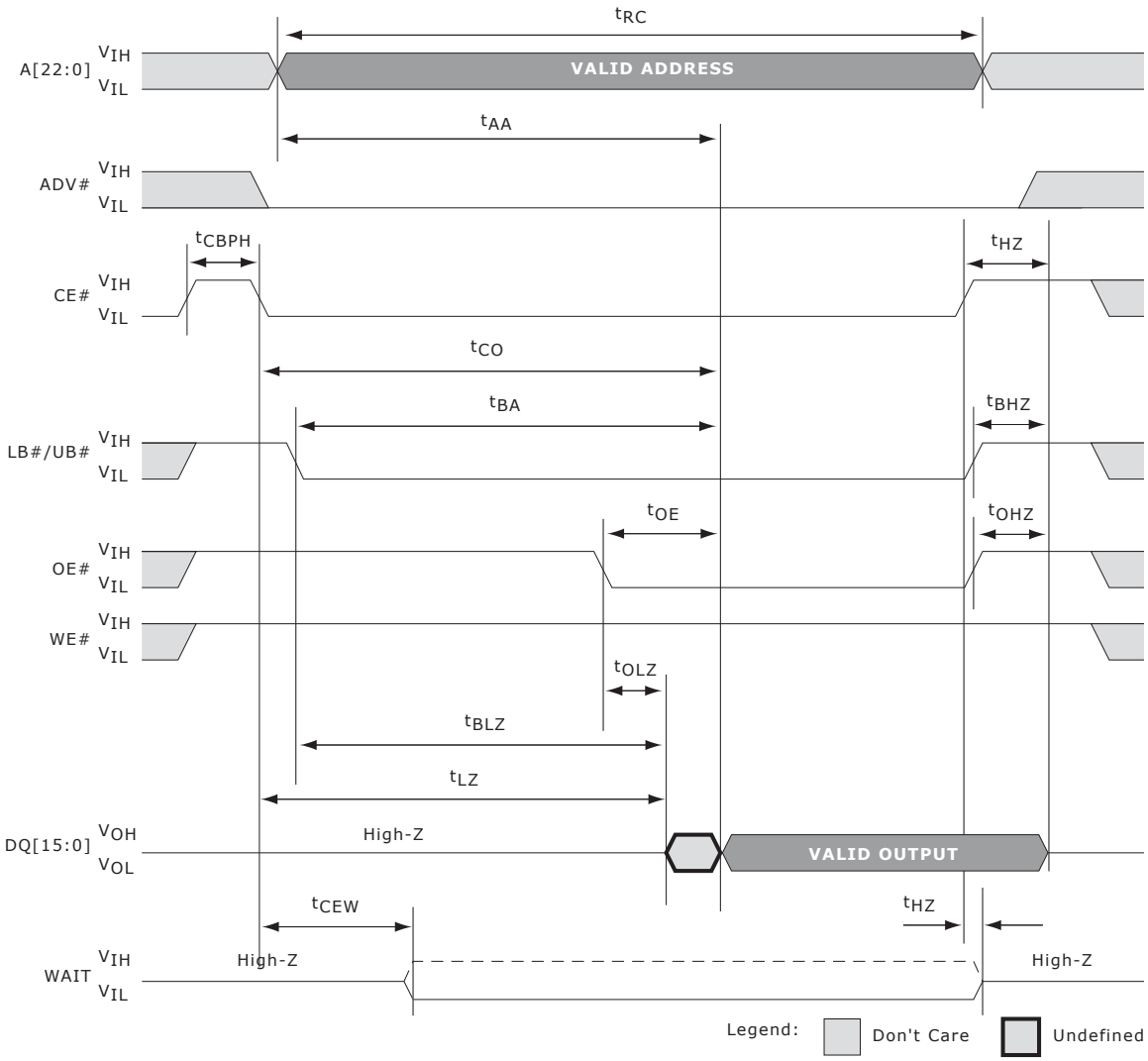


Figure 27.4 Asynchronous Read

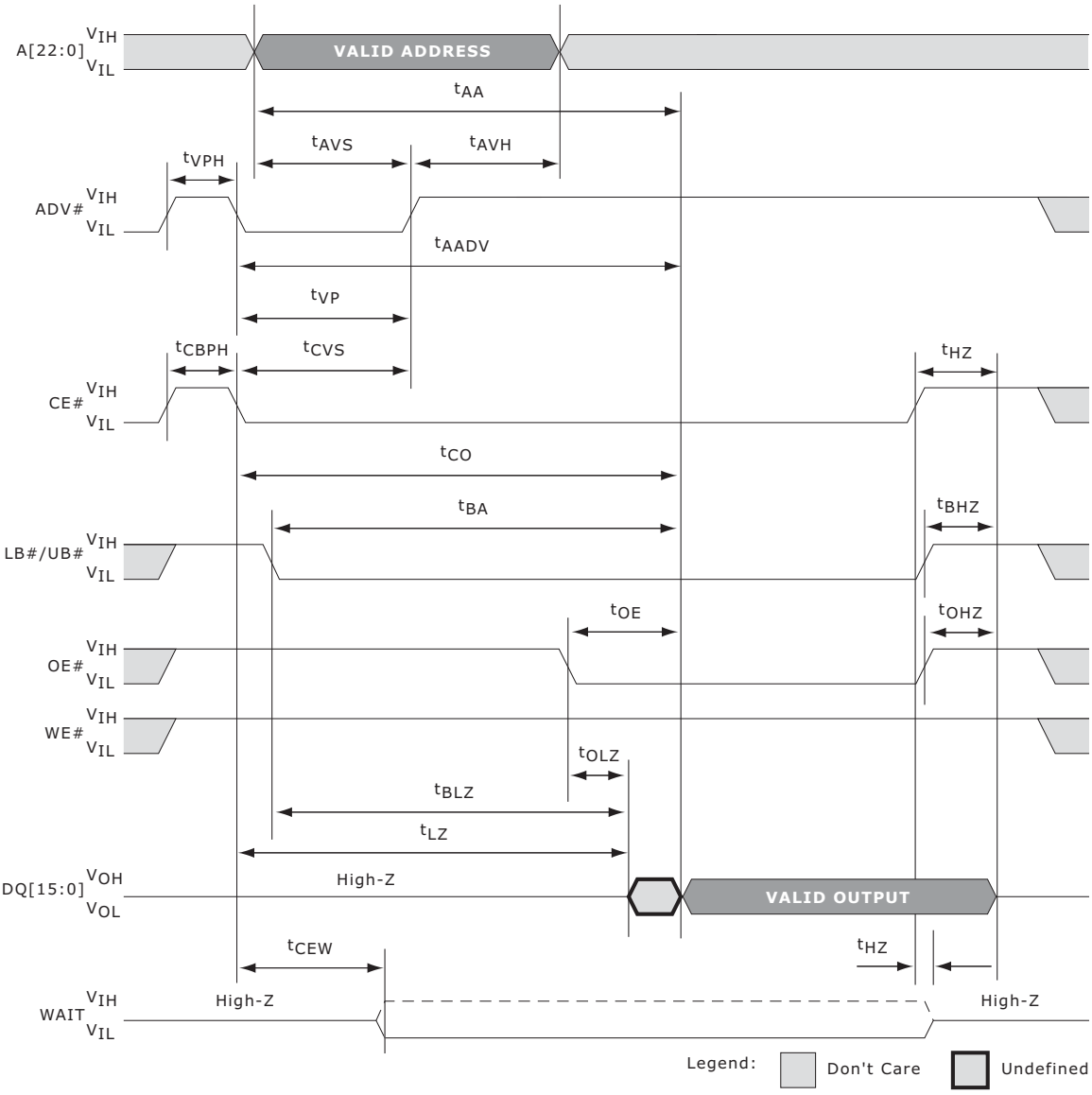


Figure 27.5 Asynchronous Read Using ADV#

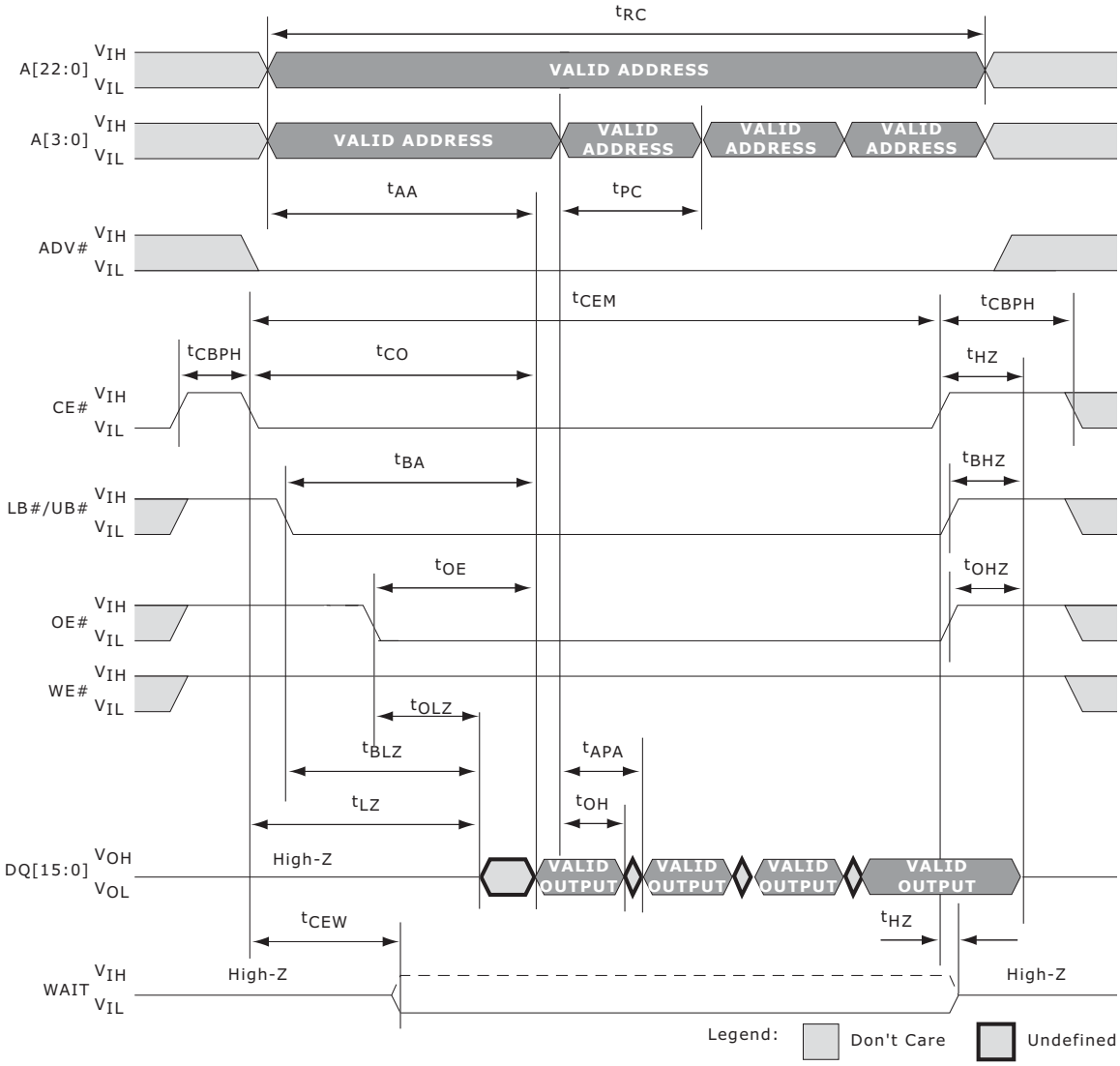
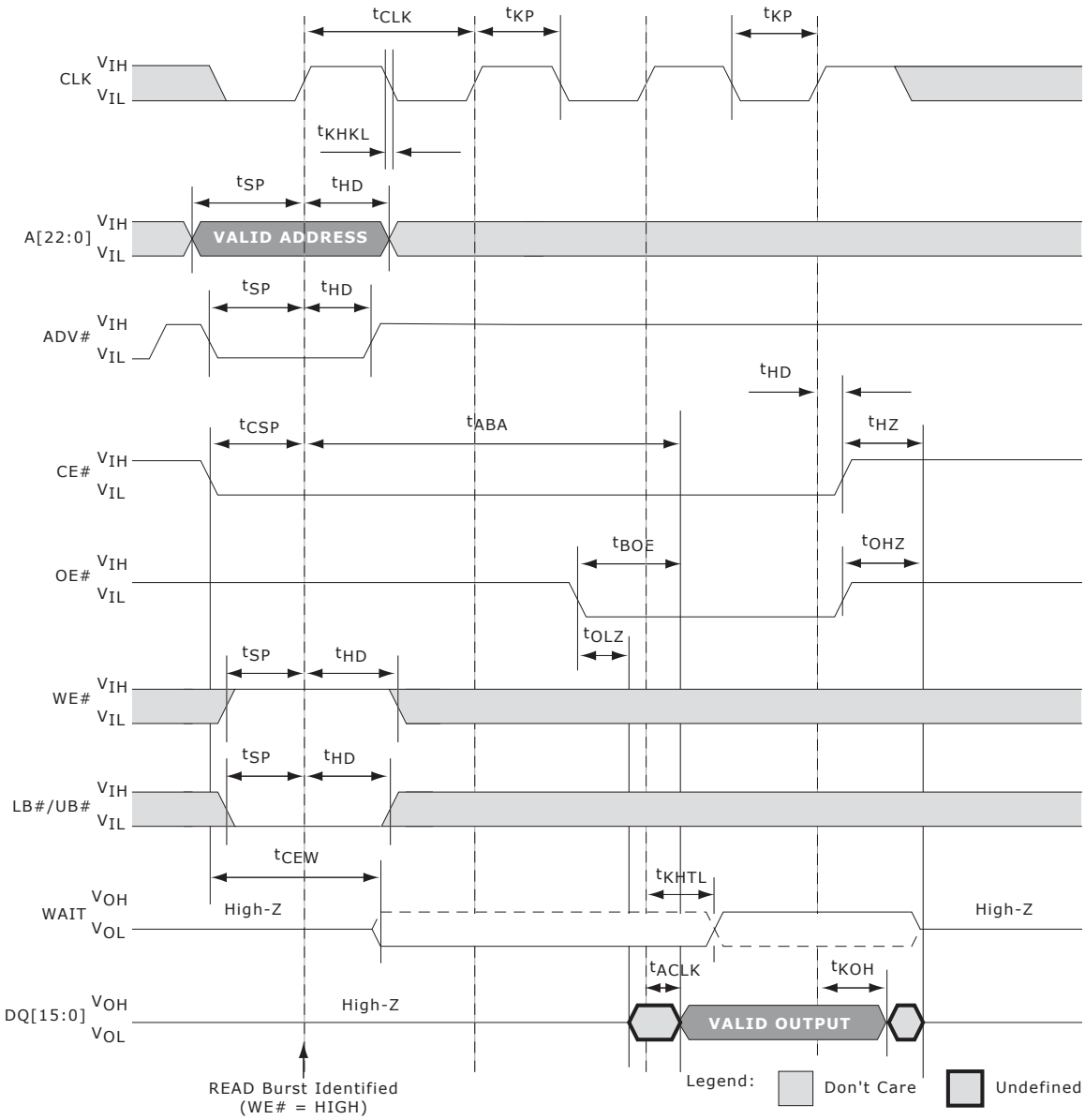
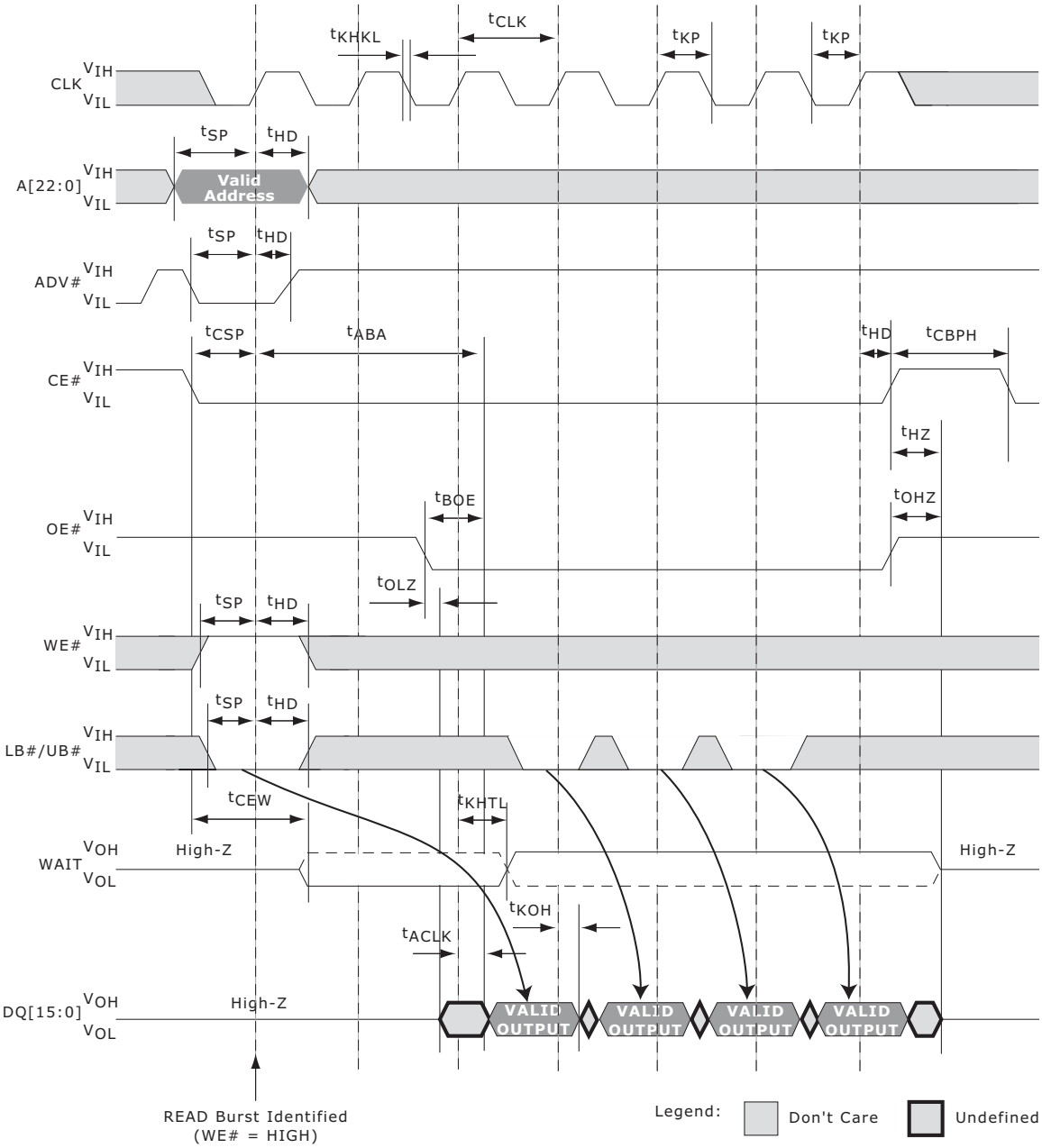


Figure 27.6 Page Mode Read



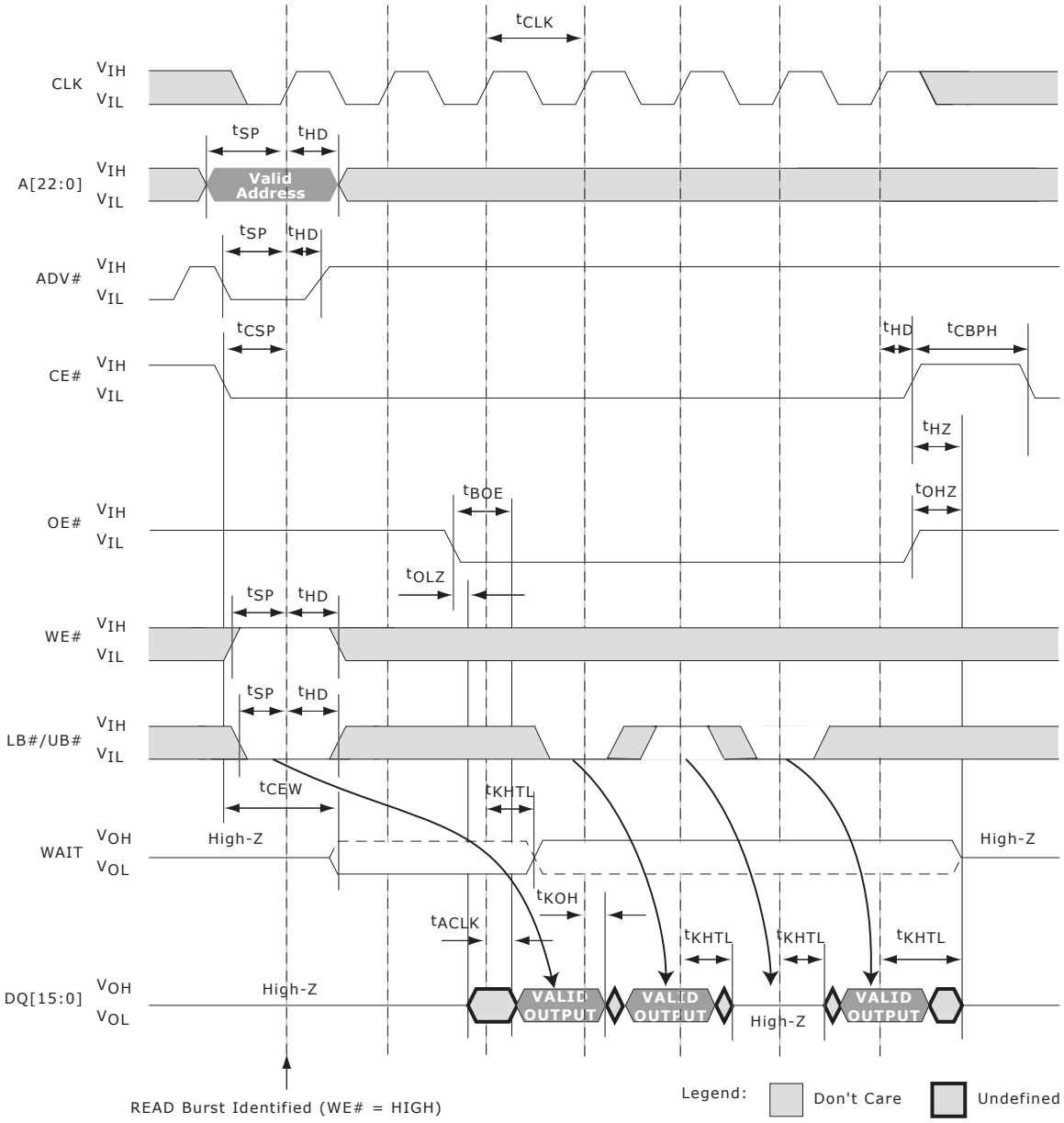
Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay. Clock rates below 50MHz (t_{CLK} > 20ns) are allowed as long as t_{CSP} specifications are met.*

Figure 27.7 Single-Access Burst Read Operation—Variable Latency



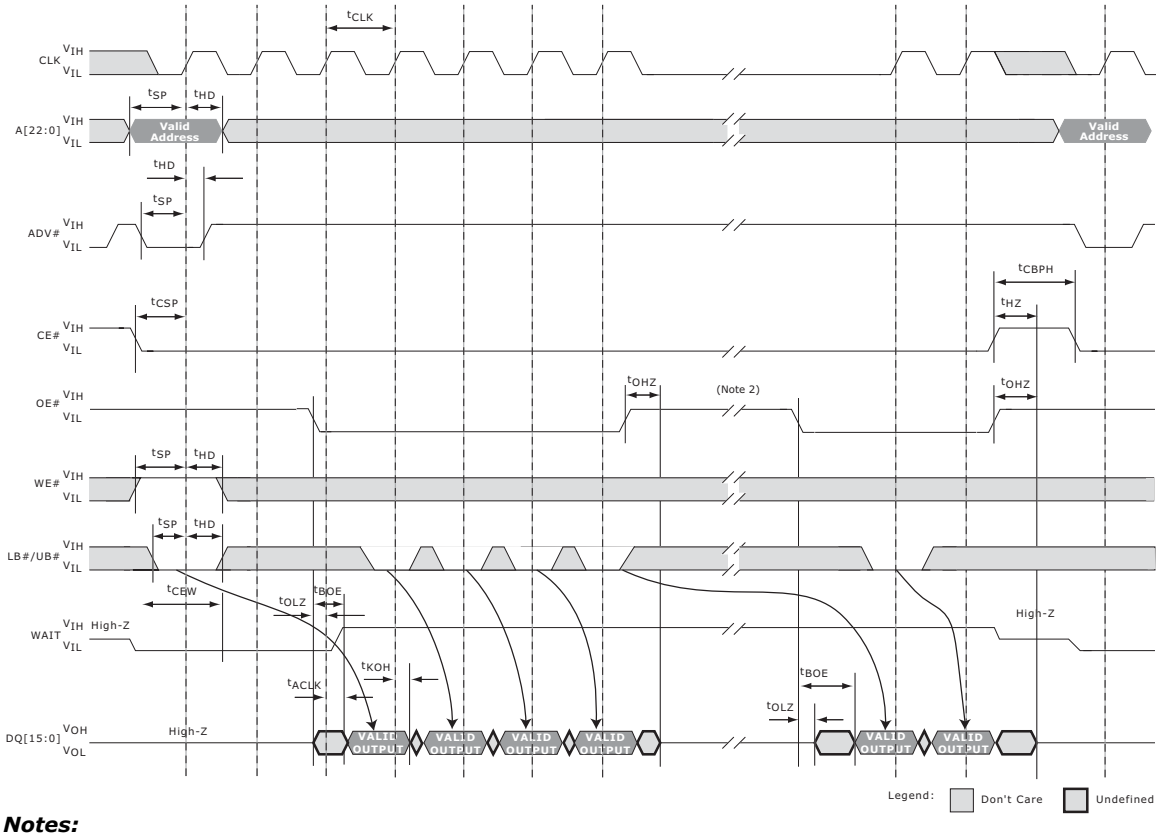
Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay. Clock rates below 50MHz (t_{CLK} > 20ns) are allowed as long as t_{CSP} specifications are met.*

Figure 27.8 Four-word Burst Read Operation—Variable Latency



Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*

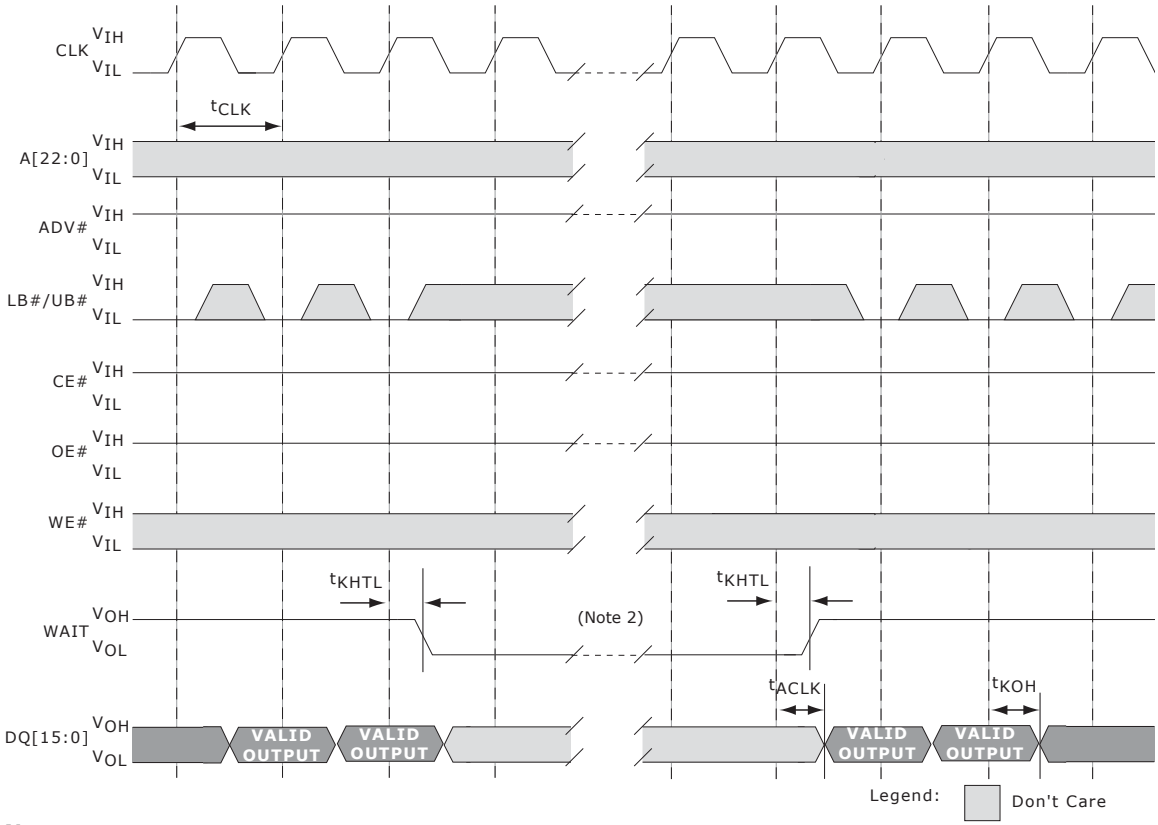
Figure 27.9 Four-Word Burst Read Operation (with LB#/UB#)



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *OE# can stay Low during burst suspend. If OE# is Low, DQ[15:0] will continue to output valid data.*

Figure 27.10 Refresh Collision During Write Operation



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *Wait will assert LC + 1 or 2LC + 1 cycles for variable latency (depending upon refresh status).*

Figure 27.11 Continuous Burst Read Showing an Output Delay with BCR[8] = 0 for End-of-Row Condition

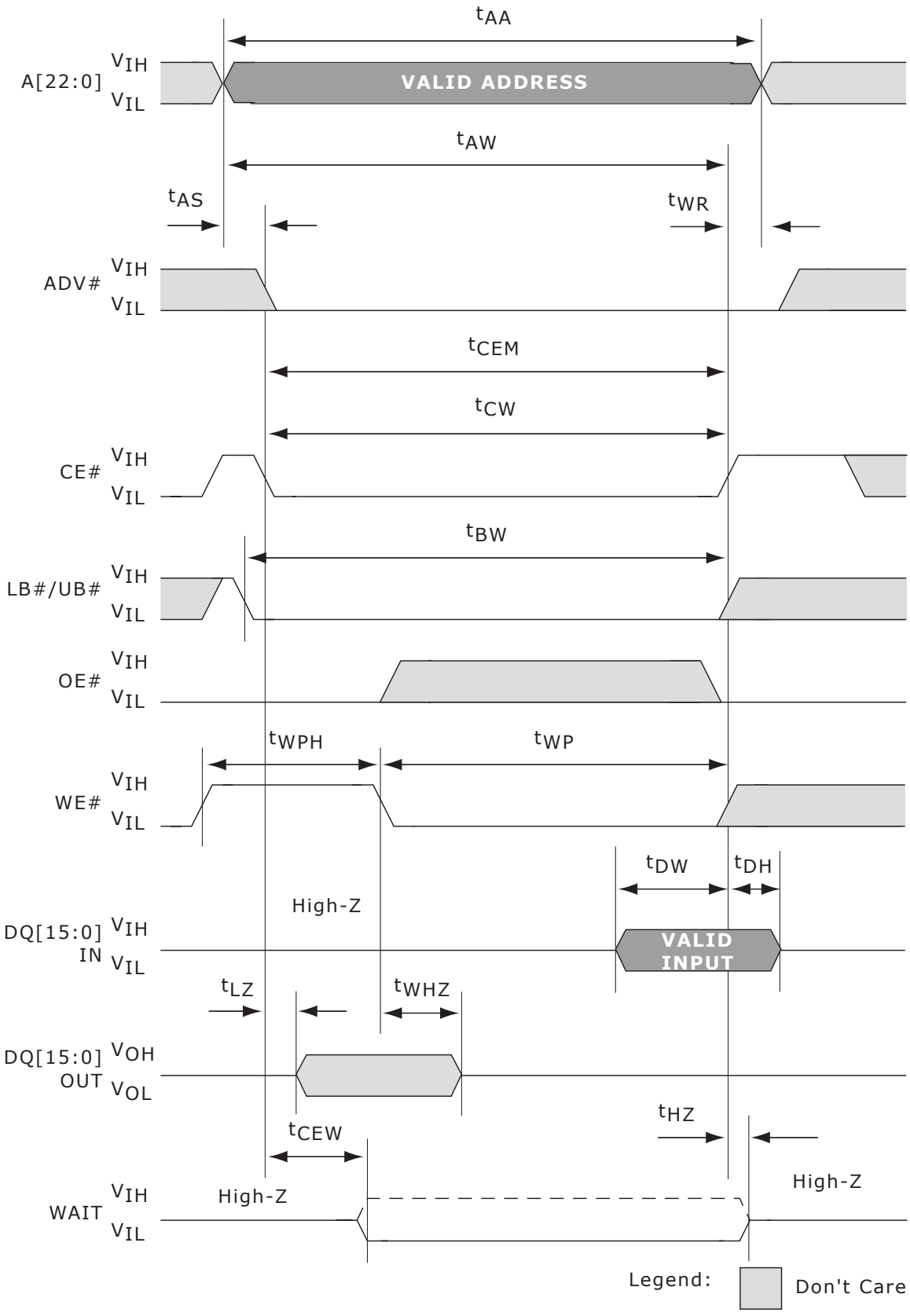


Figure 27.12 CE#-Controlled Asynchronous Write

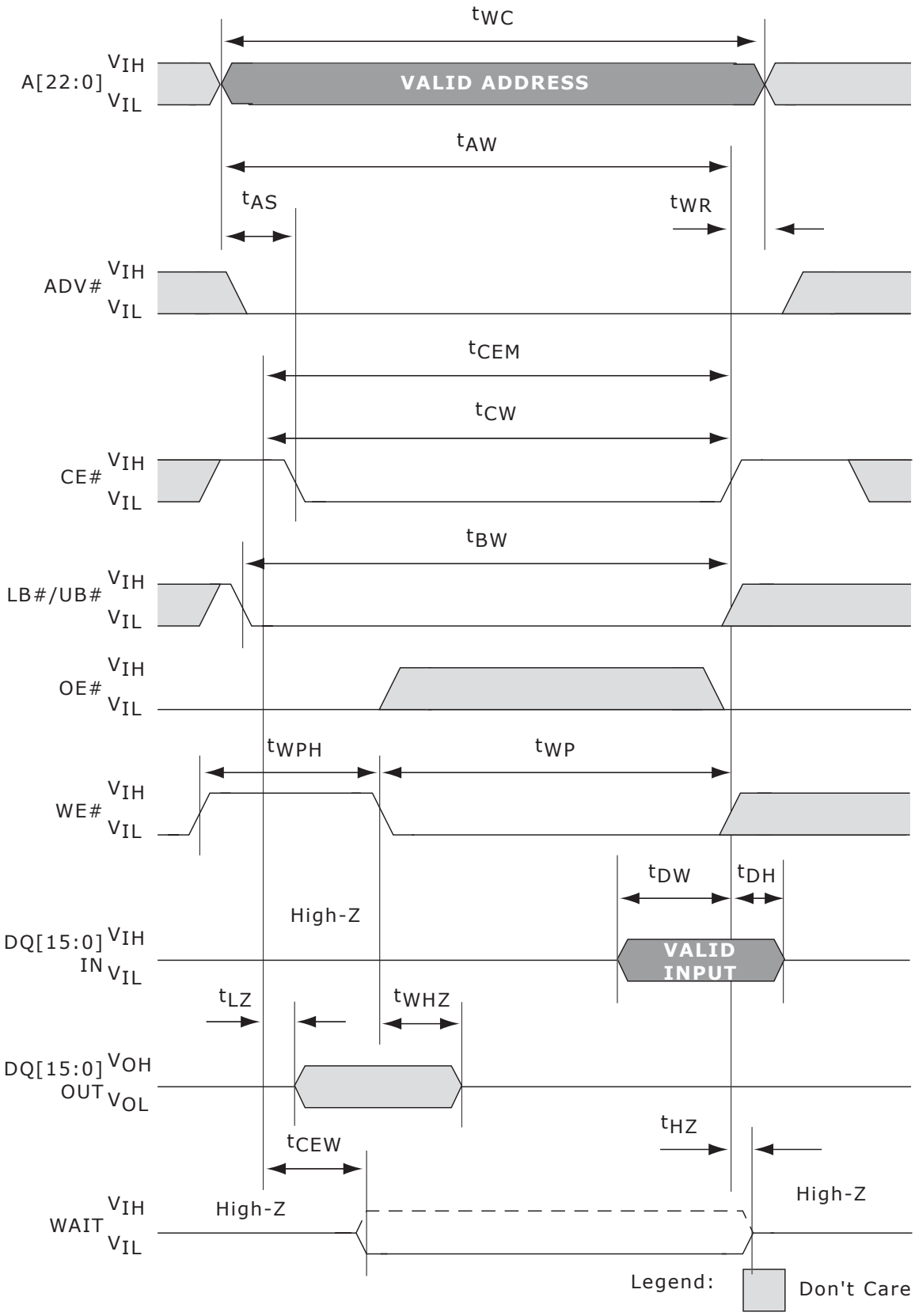


Figure 27.13 LB#/UB#-Controlled Asynchronous Write

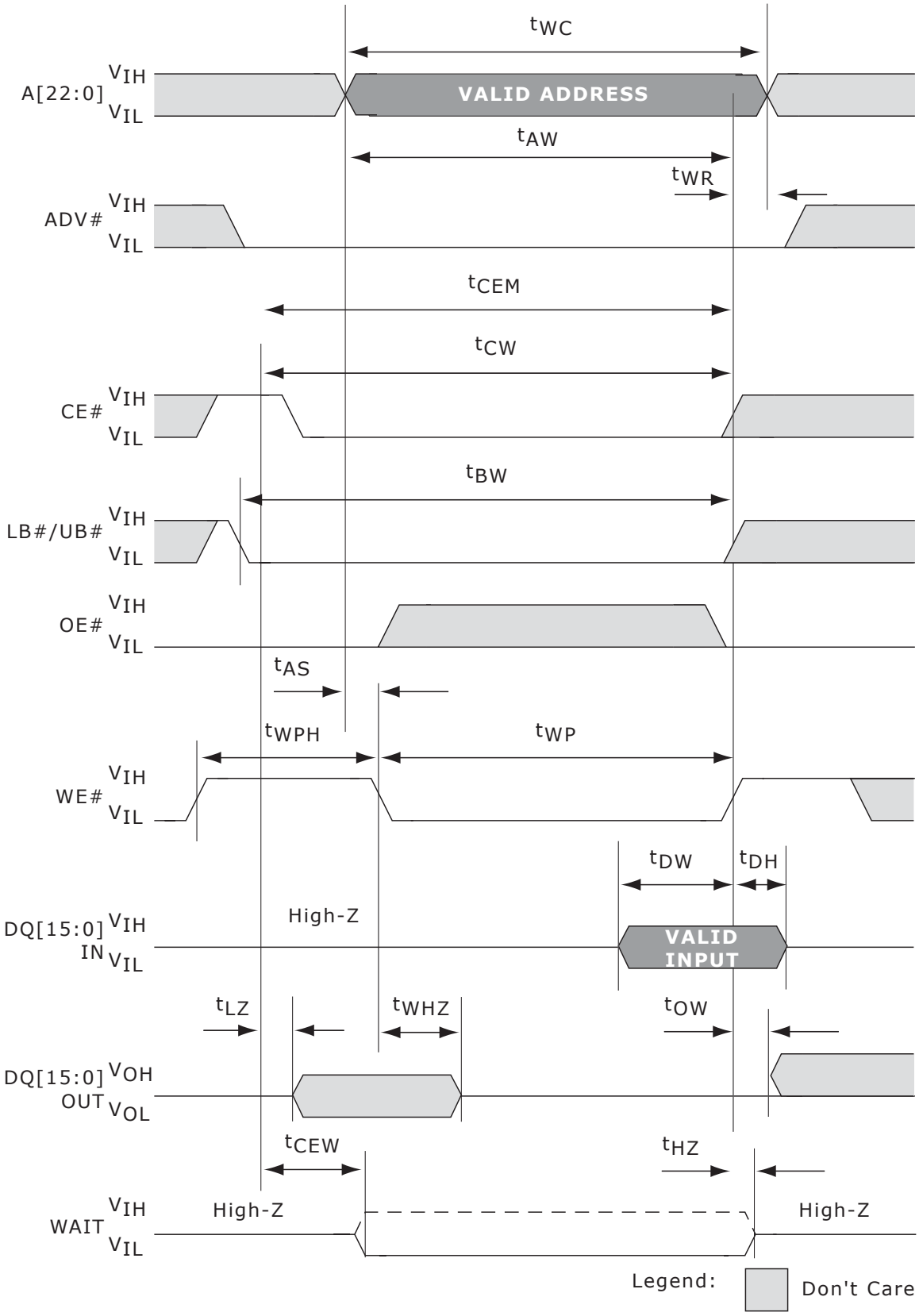


Figure 27.14 WE#-Controlled Asynchronous Write

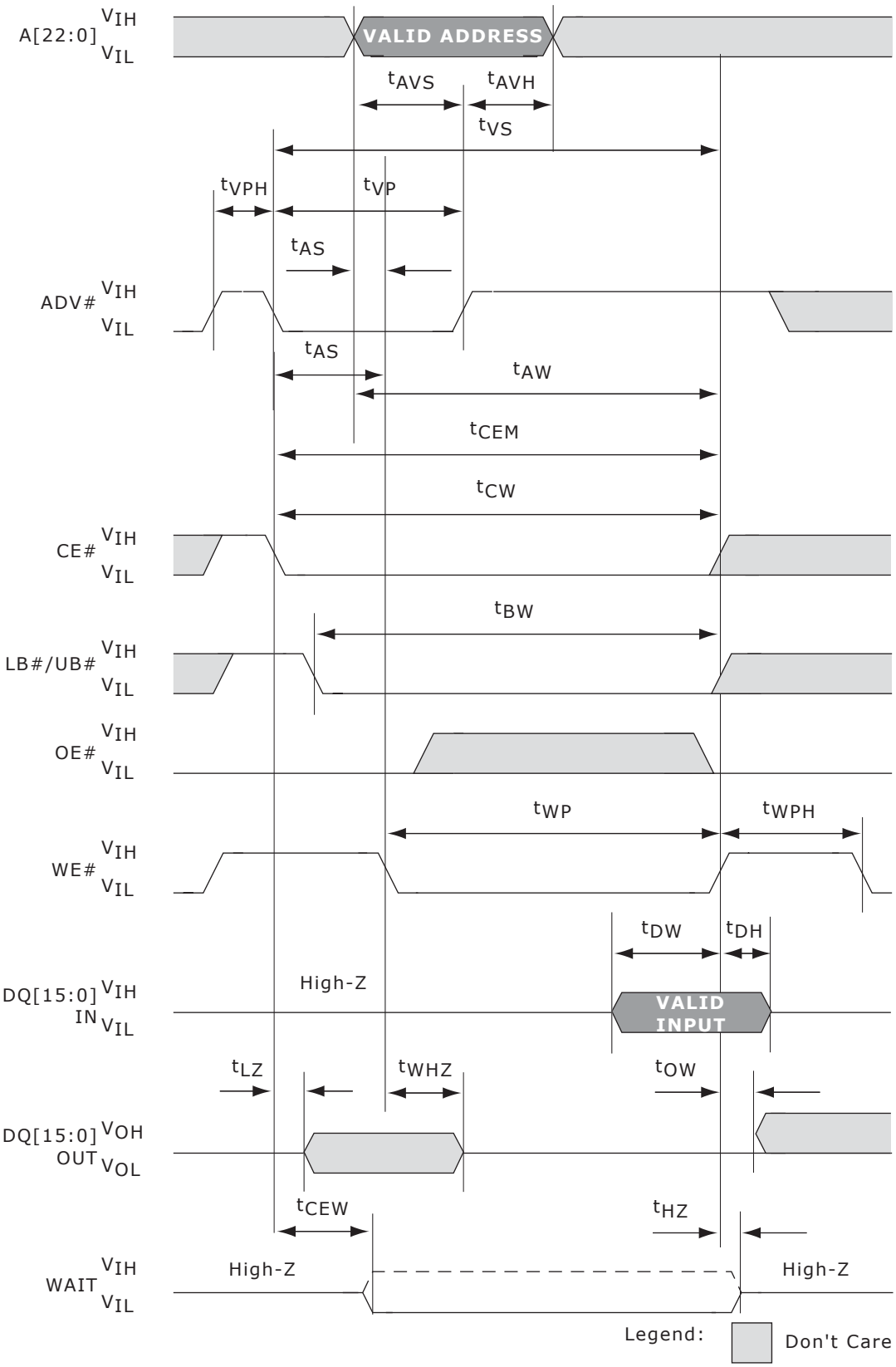
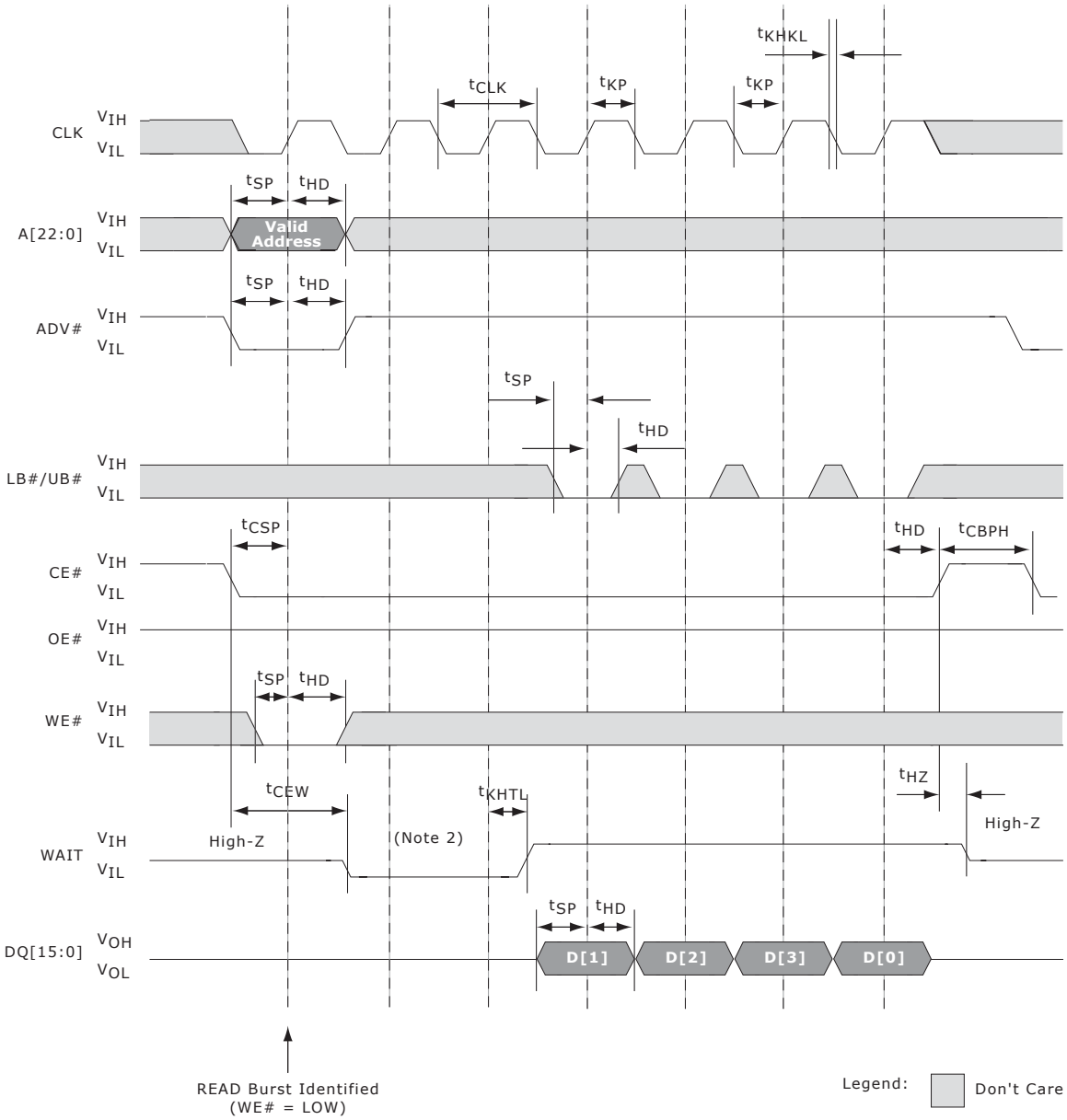
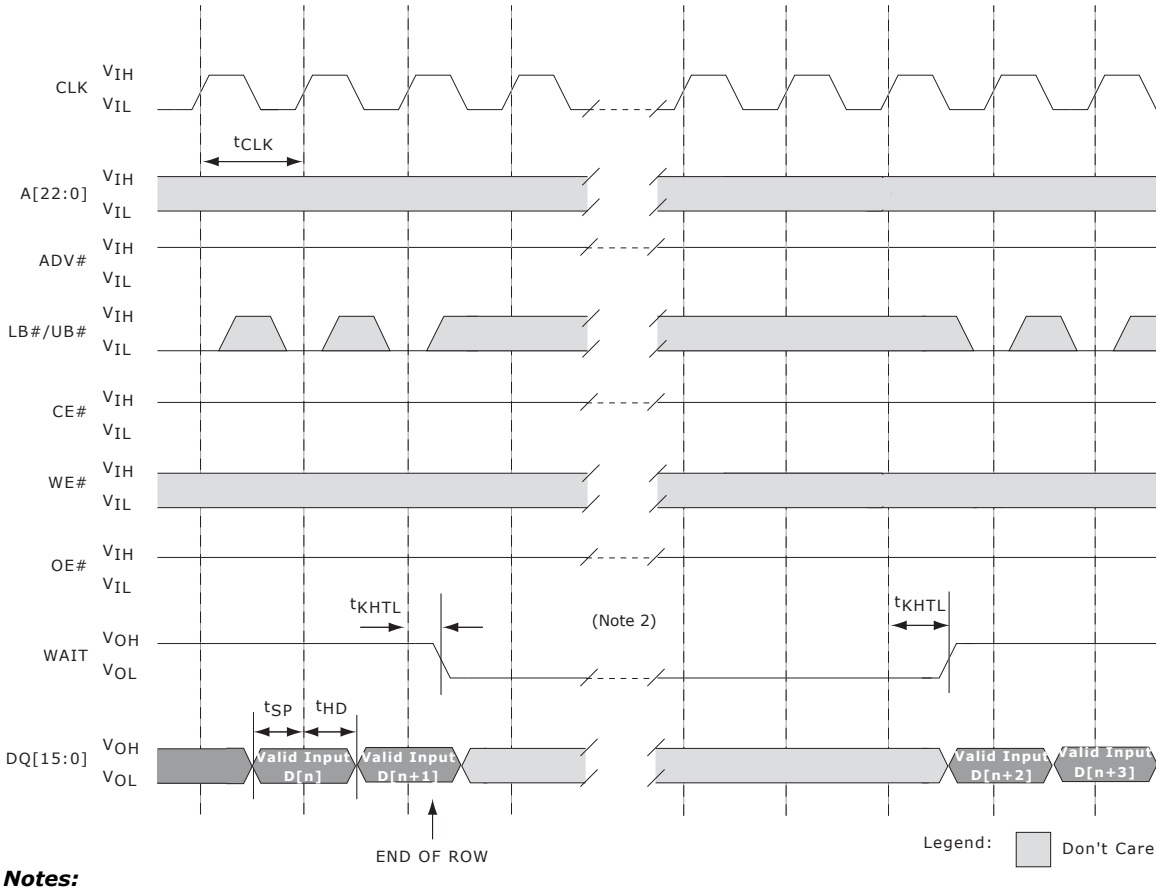


Figure 27.15 Asynchronous Write Using ADV#



Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay; burst length four; burst wrap enabled.*

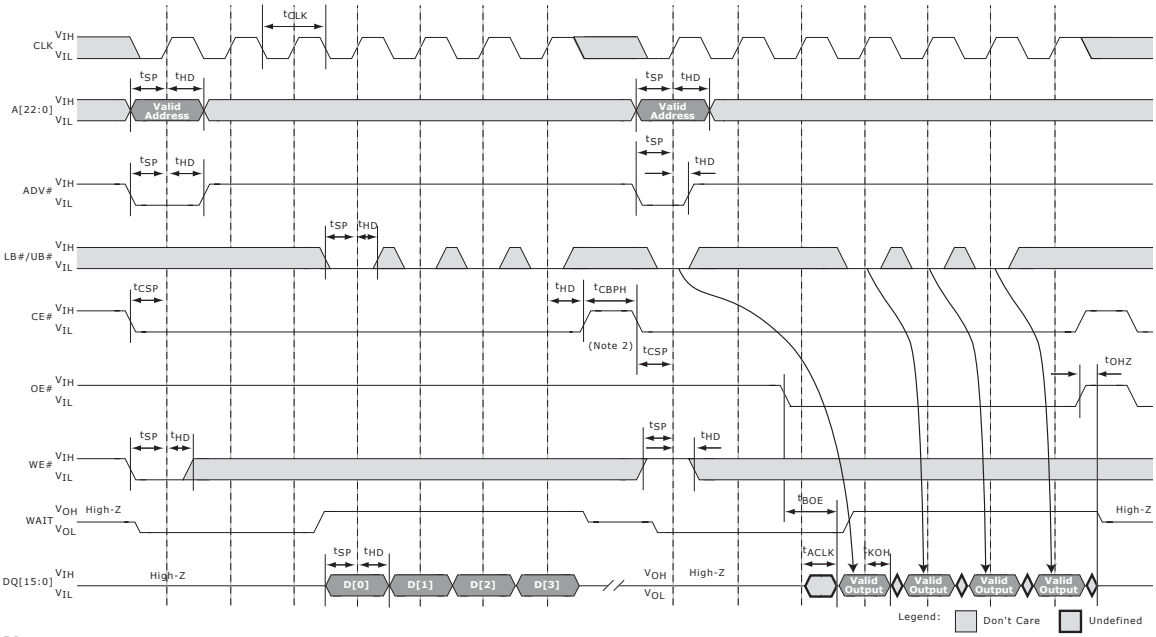
Figure 27.16 Burst Write Operation



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *Wait will assert LC + 1 or 2LC + 1 cycles for variable latency (depending upon refresh status).*

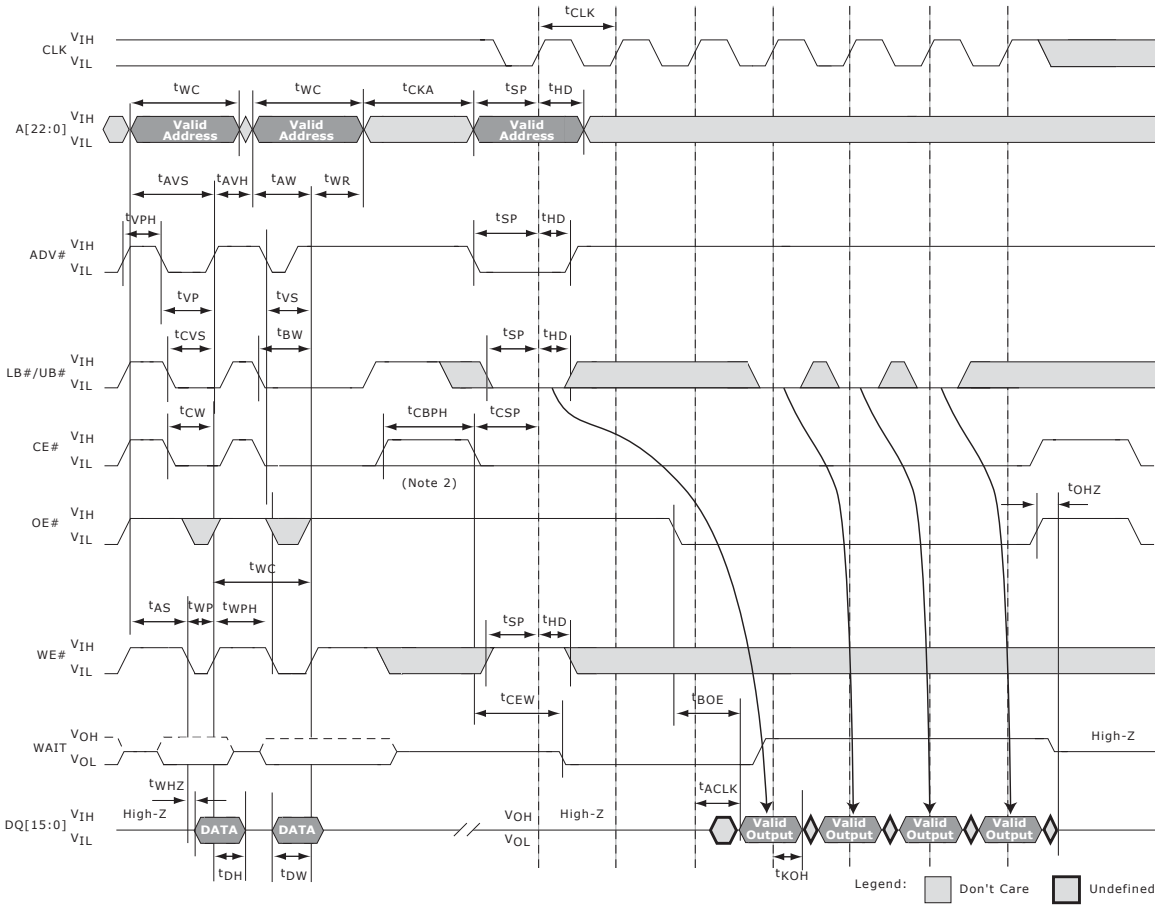
Figure 27.17 Continuous Burst Write Showing an Output Delay with BCR[8] = 0 for End-of-Row Condition



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *To allow self-refresh operations to occur between transactions, CE# must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation. CE# can stay Low between burst Read and burst Write operations.*

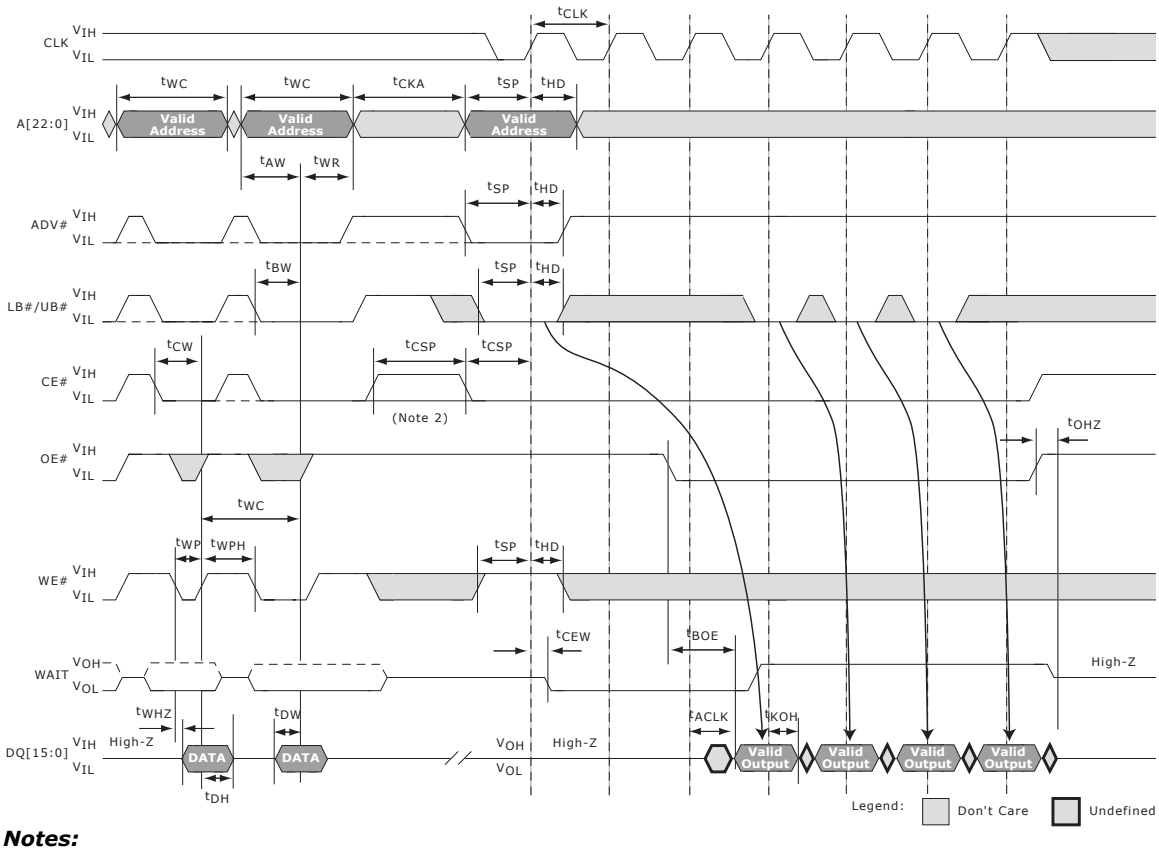
Figure 27.18 Burst Write Followed by Burst Read



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *When transitioning between asynchronous and variable-latency burst operations, CE# must go High. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation.*

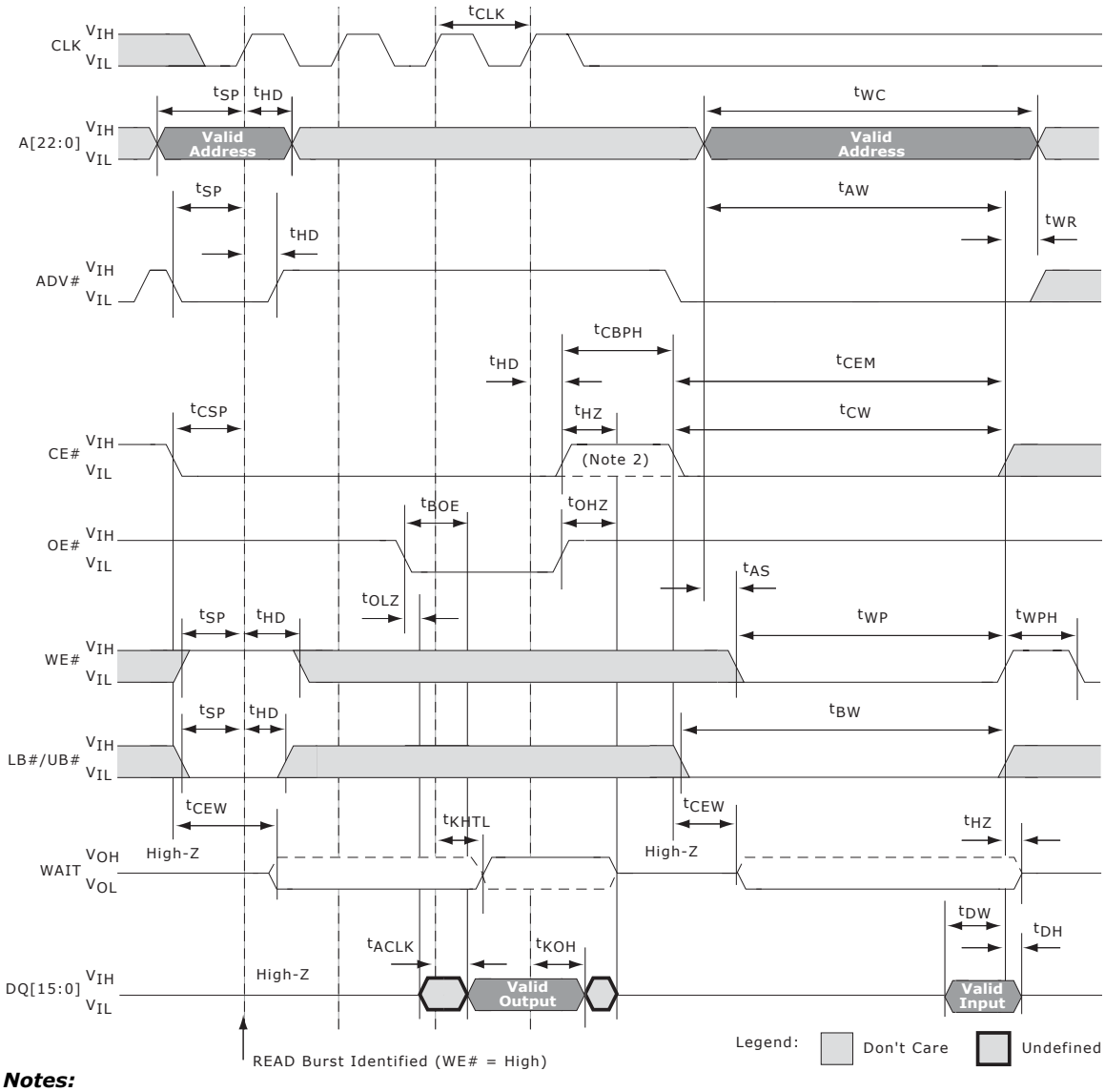
Figure 27.19 Asynchronous Write Followed by Burst Read



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *When transitioning between asynchronous and variable-latency burst operations, CE# must go High. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation.*

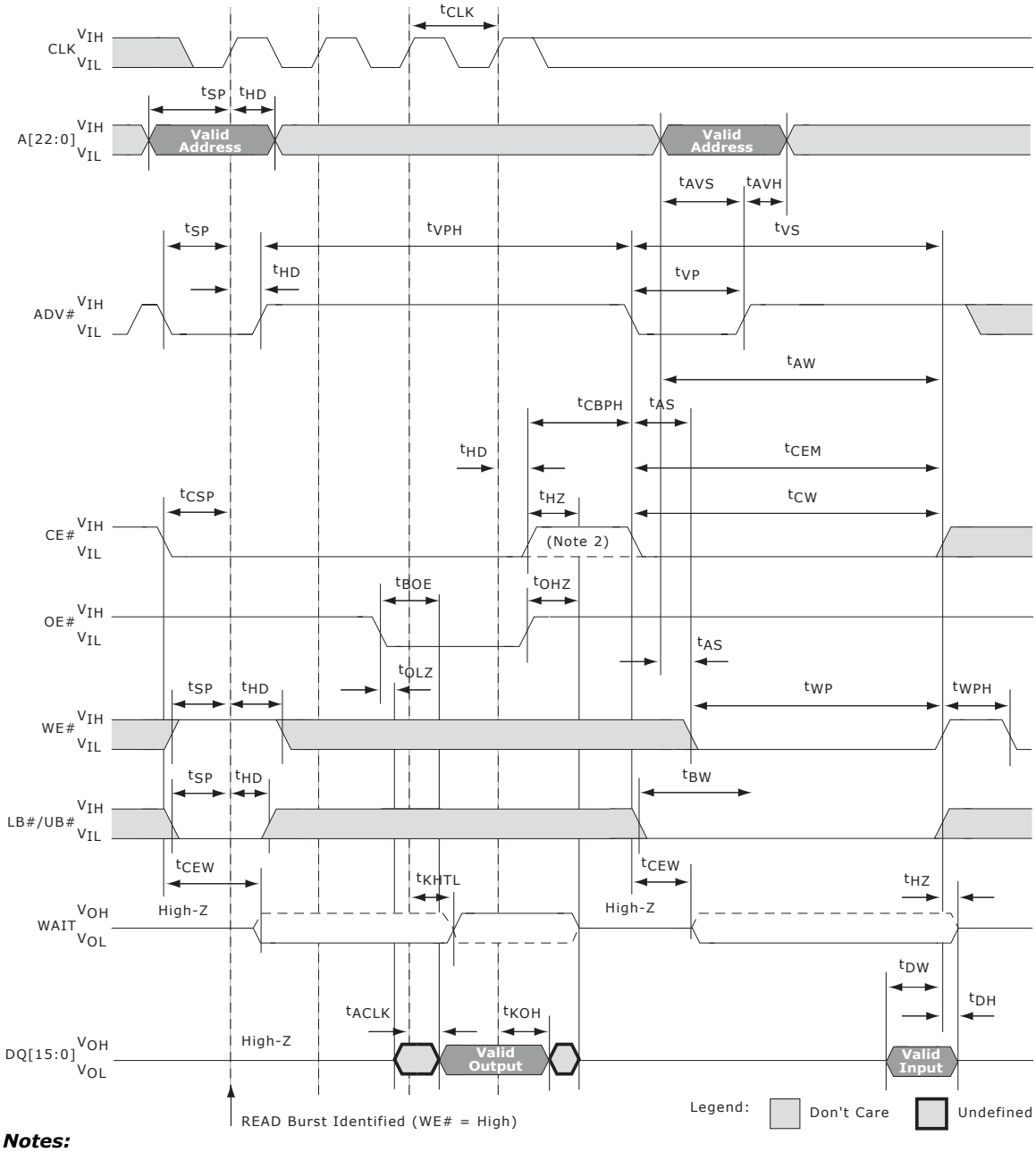
Figure 27.20 Asynchronous Write (ADV# Low) Followed By Burst Read



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *When transitioning between asynchronous and variable-latency burst operations, CE# must go High. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation.*

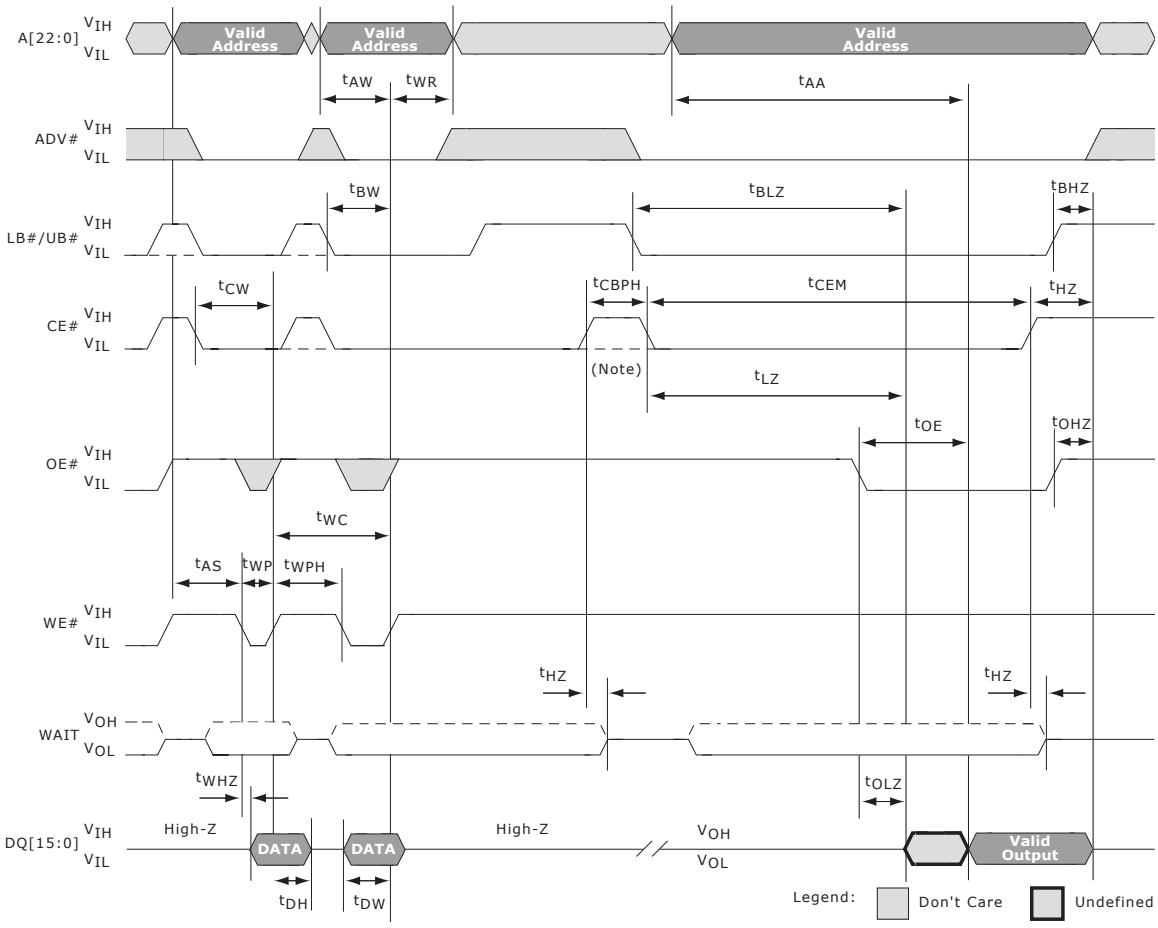
Figure 27.21 Burst Read Followed by Asynchronous Write (WE#-Controlled)



Notes:

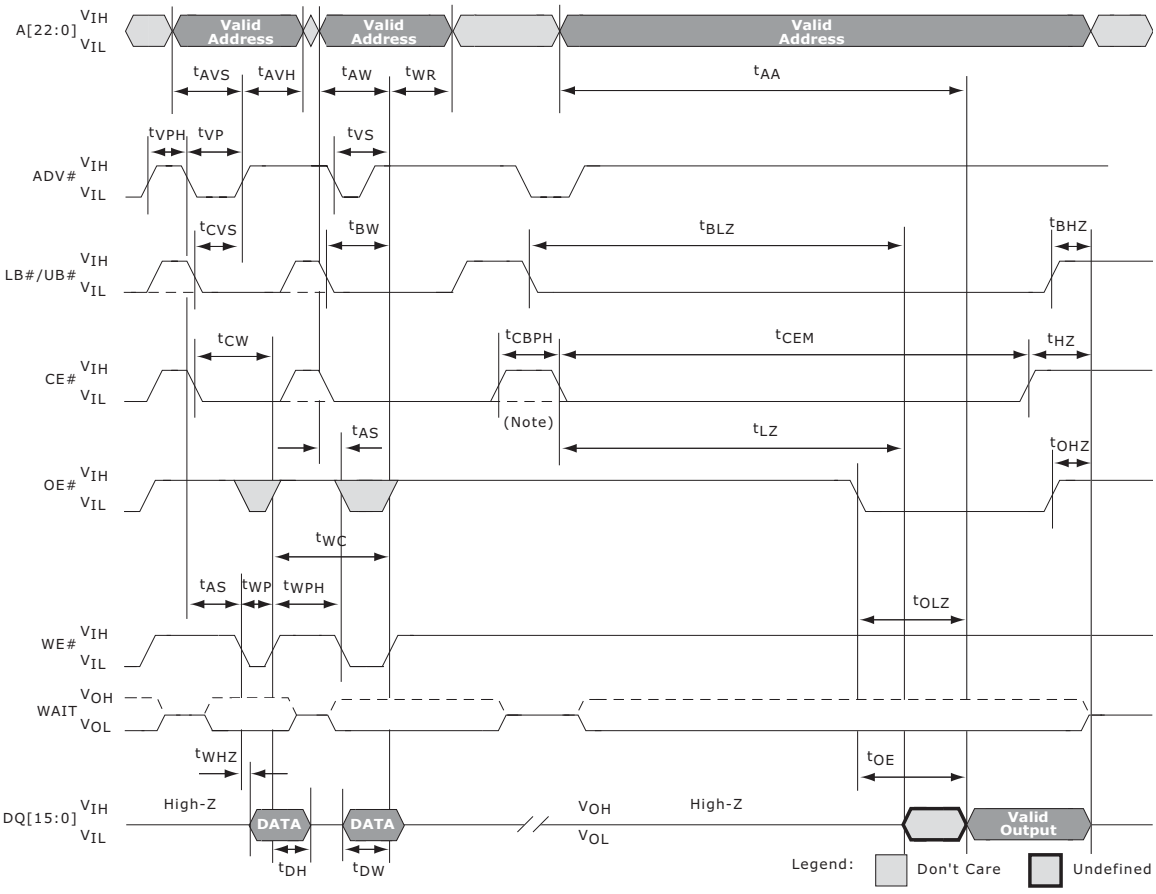
1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *When transitioning between asynchronous and variable-latency burst operations, CE# must go High. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation.*

Figure 27.22 Burst Read Followed by Asynchronous Write Using ADV#



Note: *CE# can stay Low when transitioning between asynchronous operations. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation.*

Figure 27.23 Asynchronous Write Followed by Asynchronous Read—ADV# Low



Note: *CE# can stay Low when transitioning between asynchronous operations. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation.*

Figure 27.24 Asynchronous Write Followed by Asynchronous Read

28 Revisions

Revision A0 (March 17, 2005)

Initial Release

Colophon

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