M36L0T8060T1
M36L0T8060B1

256 Mbit (16 Mb ×16, multiple bank, multilevel, burst) Flash memory and 64 Mbit PSRAM, 1.8 V core, 3 V I/O supply, multichip package

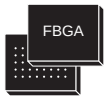
Features

Multichip package

- 1 die of 256 Mbit (16 Mb ×16, multiple bank, multilevel, burst) Flash memory
- 1 die of 64 Mbit (4 Mb ×16) Pseudo SRAM
- Supply voltage
  - V_{DDF} = 1.7 V to 1.95 V
  - V_{DDQF} = V_{CCP} = 2.7 V to 3.1 V
  - V_{PPF} = 9 V for fast program
- Electronic signature
  - Manufacturer code: 20h
  - Top device code M36L0T8060T1: 880Dh
  - Bottom device code M36L0T8060B1: 880Eh
- Package
  - ECOPACK®

Flash memory

- Synchronous/asynchronous read
  - Synchronous burst read mode: 52 MHz
  - Asynchronous page read mode
  - Random access: 85 ns
- Synchronous burst read suspend
- Programming time
  - 5 µs typical word program time using Buffer Enhanced Factory Program command
- Memory organization
  - Multiple bank memory array: 16 Mbit banks
  - Parameter blocks (top or bottom location)
- Dual operations
  - Program/erase in one bank while read in others
  - No delay between read and write operations
- 100 000 program/erase cycles per block



TFBGA88 (ZAQ)
8 x 10 mm

- Security
  - 64 bit unique device number
  - 2112 bit user programmable OTP cells
- Block locking
  - All blocks locked at power-up
  - Any combination of blocks can be locked with zero latency
  - $\overline{WP}_F$ for block lock-down
  - Absolute write protection with V_{PPF} = V_{SS}
- Common Flash interface (CFI)

PSRAM

- Access time: 65 ns
- Low standby current: 90 µA (T_A≤40 °C)
- Deep power-down current: 10 µA
- Byte control: $\overline{UB}$/$\overline{LB}$
- Compatible with standard LPSRAM
- Wide operating temperature
  - T_A = –30 to +85 °C
- Power-down modes
  - Deep power-down

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1 Description

The M36L0T8060T1 and M36L0T8060B1 combine two memory devices in a multichip package:

- a 256-Mbit, multiple bank Flash memory, the M30L0T8000T2 or M30L0T8000B2
- a 64-Mbit PSRAM, the M69KW096B

The M36L0T8060TB1 datasheet should be read in conjunction with the M30L0T8000x2 and M69KW096B datasheets, both available from any local STMicroelectronics distributor.

The memory is offered in a stacked TFBGA88 (8 × 10 mm, 8 × 10 ball array, 0.8 mm pitch) package. It is supplied with all the bits erased (set to '1').

Figure 1. Logic diagram

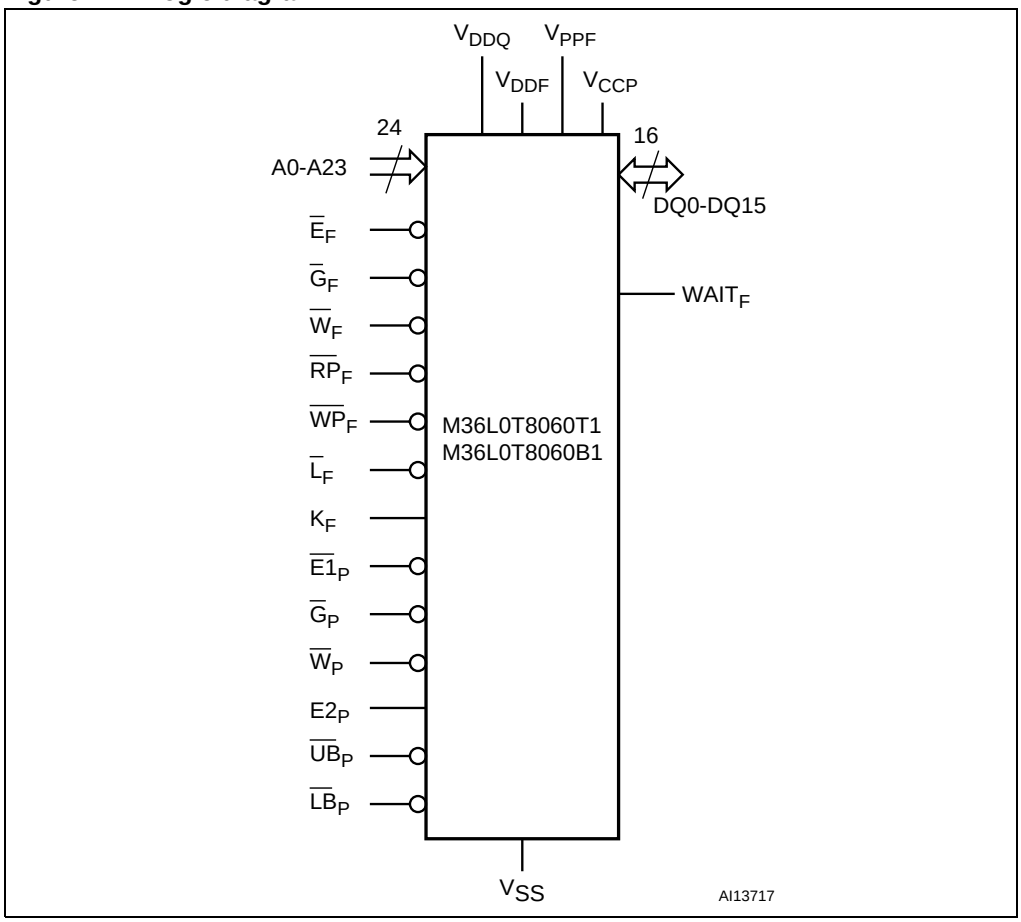
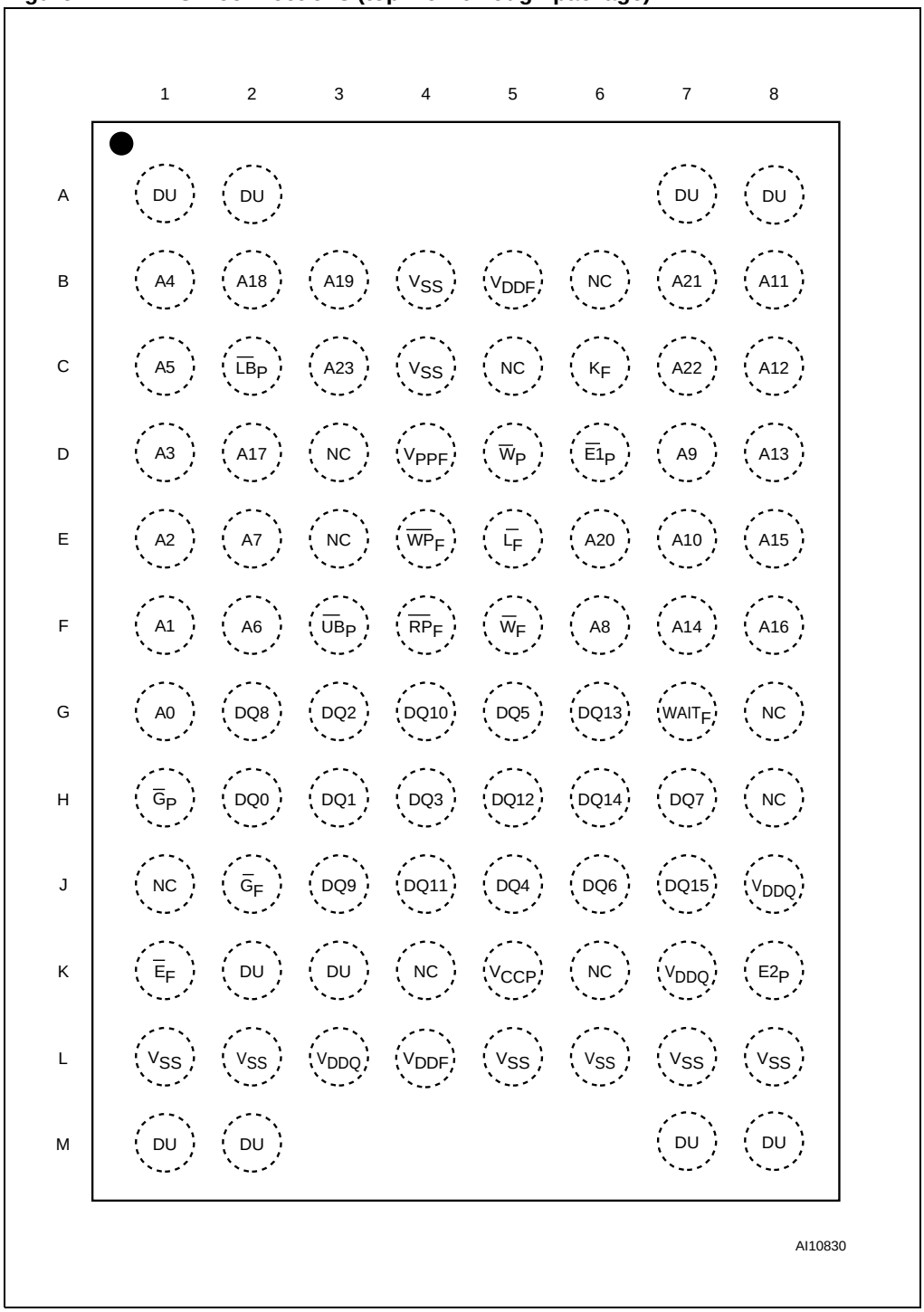


Table 1. Signal names

Signal name	Function	Direction
A0-A23[1]	Address	Input
DQ0-DQ15	Common data input/output	I/O
V_{DDF}	Flash memory power supply	Input
V_{DDQF}	Flash memory power supply for I/O buffers	Input
V_{PPF}	Flash optional supply voltage for fast program and erase	Input
V_{SS}	Ground	
V_{CCP}	PSRAM power supply	Input
NC	Not connected internally	
DU	Do not use as internally connected	
Flash memory signals		
$\overline{E}_F$	Chip Enable	Input
$\overline{G}_F$	Output Enable	Input
$\overline{W}_F$	Write Enable	Input
$\overline{RP}_F$	Reset	Input
$\overline{WP}_F$	Write Protect	Input
$\overline{L}_F$	Latch Enable	Input
K_F	Clock	Input
$WAIT_F$	Wait	Output
PSRAM signals		
$\overline{E1}_P$	Chip Enable	Input
$\overline{G}_P$	Output Enable	Input
$\overline{W}_P$	Write Enable	Input
$E2_P$	Chip Enable	Input
$\overline{UB}_P$	Upper Byte Enable	Input
$\overline{LB}_P$	Lower Byte Enable	Input

1. A22-A23 are only address inputs for the Flash memory component.

Figure 2. TFBGA connections (top view through package)



2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names* for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-A23)

Addresses A0-A21 are common inputs for the Flash memory and PSRAM components. The other lines (A23-A22) are only inputs for the Flash memory component.

The address inputs select the cells in the memory array to access during bus read operations. During bus write operations they control the commands sent to the command interface of the Flash memory Program/Erase Controller or they select the cells to be accessed in the PSRAM.

In the PSRAM these signals are also used during the set configuration register sequence

2.2 Data inputs/outputs (DQ0-DQ15)

In the Flash memory the data I/O output the data stored at the selected address during a bus read operation or input a command or the data to be programmed during a bus write operation.

For the PSRAM component, the upper byte data inputs/outputs (DQ8-DQ15) carry the data to or from the upper part of the selected address when Upper Byte Enable ($\overline{UB}_P$) is driven Low. The lower byte data inputs/outputs (DQ0-DQ7) carry the data to or from the lower part of the selected address when Lower Byte Enable ($\overline{LB}_P$) is driven Low. When both $\overline{UB}_P$ and $\overline{LB}_P$ are disabled, the data inputs/ outputs are high impedance.

2.3 Flash Chip Enable ($\overline{E}_F$)

The Flash Chip Enable input activates the control logic, input buffers, decoders and sense amplifiers of the Flash memory component. When Chip Enable is Low, V_{IL}, and Reset is High, V_{IH}, the device is in active mode. When Chip Enable is at V_{IH} the Flash memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

It is not allowed to set $\overline{E}_F$ to V_{IL}, $\overline{E1}_P$ to V_{IL} and $E2_P$ to V_{IH} at the same time.

2.4 Flash Output Enable ($\overline{G}_F$)

The Output Enable pin controls the data outputs during Flash memory bus read operations.

2.5 Flash Write Enable ($\overline{W}_F$)

The Write Enable input controls the bus write operation of the Flash memory's command interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable, whichever occurs first.

2.6 Flash Write Protect ($\overline{WP}_F$)

Write Protect is an input that provides additional hardware protection for each block. When Write Protect is Low, V_{IL}, lock-down is enabled and the protection status of the locked-down blocks cannot be changed. When Write Protect is at High, V_{IH}, lock-down is disabled and the locked-down blocks can be locked or unlocked. (See the lock status table in the M30L0T8000x2 datasheet).

2.7 Flash Reset ($\overline{RP}_F$)

The Reset input provides a hardware reset of the Flash memory. When Reset is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the reset supply current I_{DD2}. Refer to the M30L0T8000x2 datasheet for the value of I_{DD2}. After reset all blocks are in the locked state and the configuration register is reset. When Reset is at V_{IH}, the device is in normal operation. Upon exiting reset mode the device enters asynchronous read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

2.8 Flash Latch Enable ($\overline{L}_F$)

Latch Enable latches the A0-A23 address bits on its rising edge. The address latch is transparent when Latch Enable is at V_{IL} and it is inhibited when Latch Enable is at V_{IH}.

2.9 Flash Clock (K_F)

The clock input synchronizes the memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at V_{IL}. Clock is ignored during asynchronous read and in write operations.

2.10 Flash Wait ($WAIT_F$)

Wait is an output signal used during synchronous read to indicate whether the data on the output bus are valid. This output is high impedance when Chip Enable is at V_{IH}, Output Enable is at V_{IH}, or Reset is at V_{IL}. It can be configured to be active during the wait cycle or one data cycle in advance.

2.11 PSRAM Chip Enable ($\overline{E1}_P$)

When asserted (Low), the Chip Enable, $\overline{E1}_P$, activates the memory state machine, address buffers and decoders, allowing Read and Write operations to be performed. When de-asserted (High), all other pins are ignored and the device is automatically put in low-power standby mode.

It is not allowed to set $\overline{E}_F$ to V_{IL}, $\overline{E1}_P$ to V_{IL} and $E2_P$ to V_{IH} at the same time.

2.12 PSRAM Chip Enable ($E2_P$)

The Chip Enable, $E2_P$, puts the device in power-down mode (deep power-down, PAR and standby) when it is driven Low. Deep power-down mode is the lowest power mode.

It is not allowed to set $\overline{E}_F$ to V_{IL}, $\overline{E1}_P$ to V_{IL} and $E2_P$ to V_{IH} at the same time.

2.13 PSRAM Output Enable ($\overline{G}_P$)

The Output Enable, $\overline{G}_P$, provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus.

2.14 PSRAM Write Enable ($\overline{W}_P$)

The Write Enable, $\overline{W}_P$, controls the bus write operation of the PSRAM's command interface.

2.15 PSRAM Upper Byte Enable ($\overline{UB}_P$)

The Upper Byte Enable, $\overline{UB}_P$, gates the data on the upper byte data inputs/outputs (DQ8-DQ15) to or from the upper part of the selected address during a write or read operation.

2.16 PSRAM Lower Byte Enable ($\overline{LB}_P$)

The Lower Byte Enable, $\overline{LB}_P$, gates the data on the lower byte data inputs/outputs (DQ0-DQ7) to or from the lower part of the selected address during a write or read operation.

2.17 Flash V_{DDF} supply voltage

V_{DDF} provides the power supply to the internal core of the Flash memory. It is the main power supply for all Flash memory operations (read, program, and erase).

2.18 PSRAM V_{CCP} supply voltage

The V_{CCP} supply voltage supplies the power for all PSRAM operations (read, write, etc.) and for driving the refresh logic, even when the device is not being accessed.

2.19 Flash V_{DDQF} supply voltage

V_{DDQF} provides the power supply for the Flash I/O pins. This allows all outputs to be powered independently of the Flash memory core power supply, V_{DDF}.

2.20 Flash V_{PPF} program supply voltage

V_{PPF} is both a Flash memory control input and a Flash memory power supply pin. The two functions are selected by the voltage range applied to the pin.

If V_{PPF} is kept in a low voltage range (0 V to V_{DDQF}) V_{PPF} is seen as a control input. In this case a voltage lower than V_{PPLK} provides absolute protection against program or erase, while if V_{PPF} is within the V_{PP1} range these functions are enabled (see the M30L0T8000x2 datasheet for the relevant values). V_{PPF} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

If V_{PPF} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PPF} must be stable until the program/erase algorithm is completed.

2.21 V_{SS} ground

V_{SS} is the common ground reference for all voltage measurements in the Flash memory (core and I/O buffers) and PSRAM chips. It must be connected to the system ground.

Note: Each Flash memory device in a system should have their supply voltage (V_{DDF}) and the program supply voltage V_{PPF} decoupled with a 0.1 µF ceramic capacitor close to the pin (high-frequency, inherently-low inductance capacitors should be as close as possible to the package). See Figure 5: AC measurement load circuit. The PCB track widths should be sufficient to carry the required V_{PPF} program and erase currents.

3 Functional description

The PSRAM and Flash memory components have separate power supplies but share the same grounds. They are distinguished by three Chip Enable inputs: $\overline{E}_F$ for the Flash memory and $\overline{E1}_P$ and $E2_P$ for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is simultaneous read operations on the Flash memory and PSRAM components, which would result in a data bus contention. Therefore, it is recommended to put the other devices in the high impedance state when reading the selected device.

Figure 3. Functional block diagram

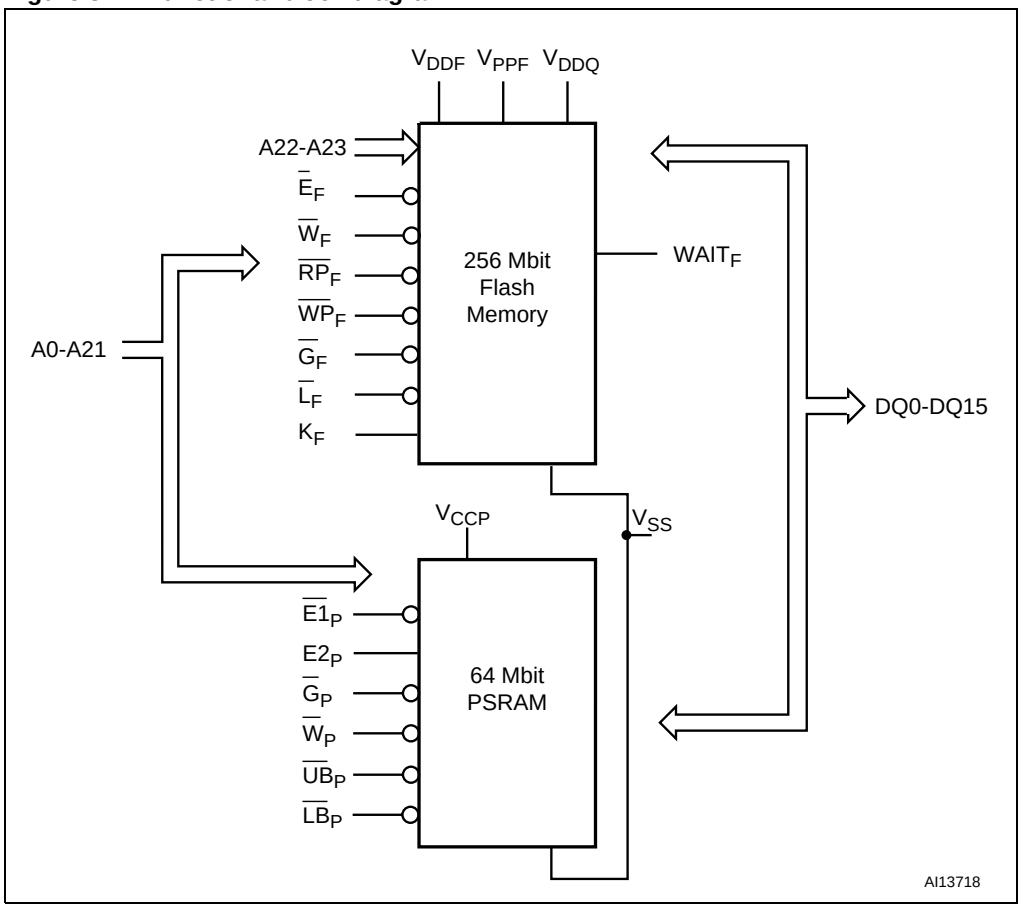


Table 2. Main operating modes(1)

Operation	$\overline{E}_F$	$\overline{G}_F$	$\overline{W}_F$	$\overline{L}_F$	$\overline{RP}_F$	$WAIT_F$(2)	$\overline{E1}_P$	$E2_P$	$\overline{W}_P$	$\overline{G}_P$	$\overline{LB}_P$	$\overline{UB}_P$	DQ0-DQ7	DQ8-DQ15
Flash read	V_{IL}	V_{IL}	V_{IH}	V_{IL}(3)	V_{IH}		PSRAM must be disabled.						Flash data out	
Flash write	V_{IL}	V_{IH}	V_{IL}	V_{IL}(3)	V_{IH}								Flash data in	
Flash address latch	V_{IL}	X	V_{IH}	V_{IL}	V_{IH}								Flash data out or Hi-Z(4)	
Flash output disable	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}	Hi-Z	Any PSRAM mode is allowed.						Hi-Z	
Flash standby	V_{IH}	X	X	X	V_{IH}	Hi-Z							Hi-Z	
Flash reset	X	X	X	X	V_{IL}	Hi-Z							Hi-Z	
PSRAM read(5)	The Flash memory must be disabled						V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Data output	Hi-Z
							V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Hi-Z	Data output
							V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Data output	Data output
PSRAM standby (deselected)	Any Flash mode is allowed.						V_{IH}	V_{IH}	X	X	X	X	Hi-Z	Hi-Z
PSRAM deep power-down(6)							X	V_{IL}	X	X	X	X	Hi-Z	Hi-Z
PSRAM write(5)	The Flash memory must be disabled						V_{IL}	V_{IH}	V_{IL}	V_{IH}(7)	V_{IL}	V_{IH}	Data input	Invalid
							V_{IL}	V_{IH}	V_{IL}	V_{IH}(7)	V_{IH}	V_{IL}	Invalid	Data input
							V_{IL}	V_{IH}	V_{IL}	V_{IH}(7)	V_{IL}	V_{IL}	Data input	Data input

1. X = 'don't care'
2. $WAIT_F$ signal polarity is configured using the Set Configuration Register command. See the M30L0T8000x2 datasheet for details.
3. $\overline{L}_F$ can be tied to V_{IH} if the valid address has been previously latched.
4. Depends on $\overline{G}_F$.
5. Address bits are either at V_{IL} or V_{IH} but must be valid before PSRAM read or write operation.
6. Power-down mode can be entered from standby state and all DQ pins are in High-Z state. Data retention depends on the power-down mode selected.
7. $\overline{G}_P$ can be V_{IL} during the write operation if the following conditions are satisfied:
   a. Write pulse is initiated by $\overline{E1}_P$ ($\overline{E1}_P$ controlled write timing), or cycle time of the previous operation cycle is satisfied;
   b. $\overline{G}_P$ stays V_{IL} during the entire write cycle.

4 Maximum ratings

Stressing the device above the ratings listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient operating temperature	–25	85	°C
T_{BIAS}	Temperature under bias	–25	85	°C
T_{STG}	Storage temperature	–55	125	°C
V_{IO}	Input or output voltage	–0.5	3.6	V
V_{DDF}	Flash memory core supply voltage	–0.2	2.5	V
V_{DDQF}	Flash memory input/output supply voltage	–0.2	3.8	V
V_{CCP}	PSRAM core supply voltage	–0.5	3.6	V
V_{PPF}	Flash program voltage	–0.2	10	V
I_O	Output short circuit current		100	mA
t_{VPPFH}	Time for V_{PPF} at V_{PPFH}		100	hours

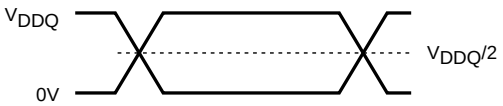
5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 4: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC measurement conditions

Parameter	Flash memory		PSRAM		Unit
	Min	Max	Min	Max	
V_{DDF} supply voltage	1.7	1.95	–	–	V
V_{CCP} supply voltage	–	–	2.7	3.1	V
V_{DDQF} supply voltage	2.7	3.1	–	–	V
V_{PPF} supply voltage (Factory environment)	8.5	9.5	–	–	V
V_{PPF} supply voltage (Application environment)	–0.4	V_{DDQF} +0.4	–	–	V
Load capacitance (C_L)	30		50		pF
Output circuit resistors (R_1, R_2)	16.7		16.7		kΩ
Input rise and fall times		5	5		ns
Input pulse voltages	0 to V_{DDQF}		0 to V_{CCP}		V
Input and output timing ref. voltages	$V_{DDQF}/2$		$V_{CCP}/2$		V

Figure 4. AC measurement I/O waveform



1. V_{DDQ} means $V_{DDQF} = V_{CCP}$.

Figure 5. AC measurement load circuit

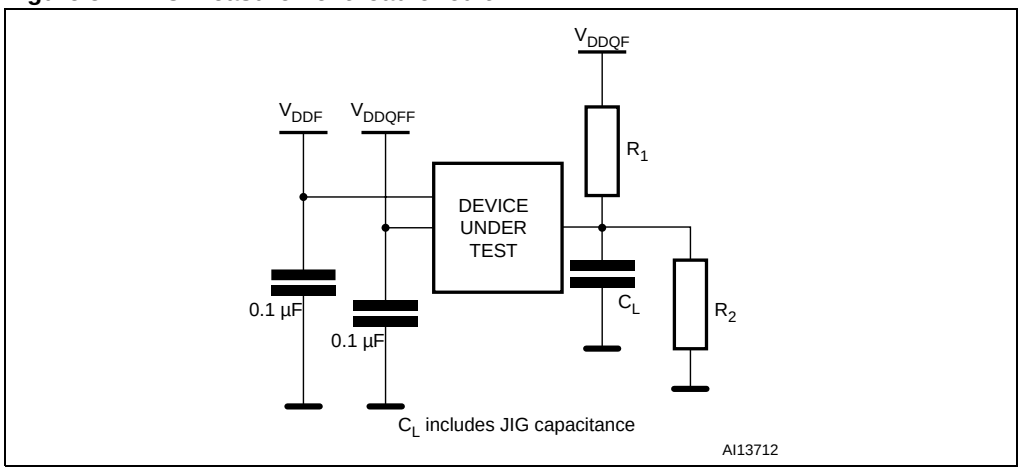


Table 5. Device capacitance(1)

Symbol	Parameter	Test condition	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		14	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V		20	pF

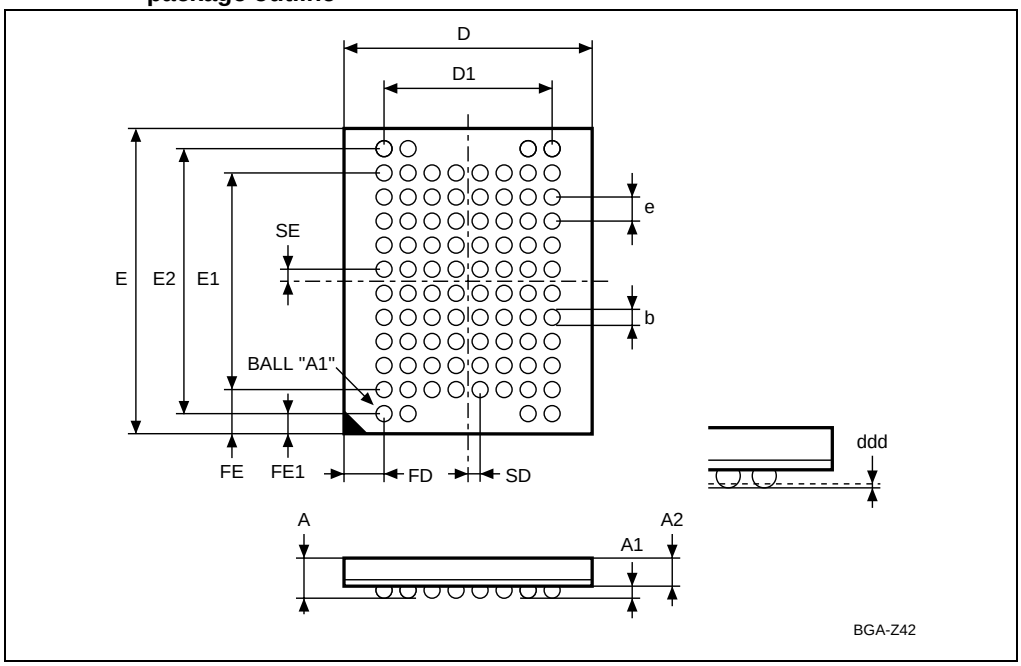
1. Sampled only, not 100% tested.

Please refer to the M30L0T8000x0 and M69KW096B datasheets for further DC and AC characteristic values and illustrations.

6 Package mechanical

ECOPACK® packages have a lead-free second-level interconnect. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark and specifications are available at www.st.com.

Figure 6. TFBGA88 8 × 10 mm, 8 × 10 ball array - 0.8 mm pitch, bottom view package outline



1. Drawing is not to scale.

Table 6. Stacked TFBGA88 8 × 10 mm - 8 × 10 active ball array, 0.8 mm pitch, package data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.200			0.0079	
A2	0.850			0.0335		
b	0.350	0.300	0.400	0.0138	0.0118	0.0157
D	8.000	7.900	8.100	0.3150	0.3110	0.3189
D1	5.600			0.2205		
ddd			0.100			0.0039
E	10.000	9.900	10.100	0.3937	0.3898	0.3976
E1	7.200			0.2835		
E2	8.800			0.3465		
e	0.800	–	–	0.0315	–	–
FD	1.200			0.0472		
FE	1.400			0.0551		
FE1	0.600			0.0236		
SD	0.400			0.0157		
SE	0.400			0.0157		

7 Part numbering

Table 7. Ordering information scheme

Example: M36 L 0 T 8 0 6 0 T 1 ZAQ T

Device type
M36 = multichip package (multiple Flash + RAM)

Flash 1 architecture
L = multilevel, multiple bank, burst mode

Flash 2 architecture
0 = no die

Operating voltage
T = V_{DDF} = 1.7 V to 1.95 V; V_{DDQF} = V_{CCP} = 2.7 V to 3.1 V

Flash 1 density
8 = 256 Mbits

Flash 2 density
0 = no die

RAM 1 density
6 = 64 Mbits

RAM 0 density
0 = no die

Parameter blocks location
T = top boot block Flash
B = bottom boot block Flash

Product version
1 = 90 nm Flash technology and multilevel design, 85 ns speeds;
0.13 µm RAM, 65 ns speed

Package
ZAQ = stacked TFBGA88 8 × 10 mm - 8 × 10 active ball array, 0.8 mm pitch

Option
E = ECOPACK® package, standard packing
F = ECOPACK® package, tape and reel packing

Devices are shipped from the factory with the memory content bits erased to ’1’. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the STMicroelectronics sales office nearest to you.

8 Revision history

Table 8. Document revision history

Date	Revision	Changes
15-Dec-2006	0.1	Initial release
25-Feb-2008	1	Datasheet promoted to full maturity.

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