Features

- 32-Mbit Flash and 4-Mbit/8-Mbit SRAM
- Single 66-ball 8 mm x 11 mm CBGA Package
- 2.7V to 3.3V Operating Voltage

Flash

- 2.7V to 3.3V Read/Write
- Access Time – 85, 90, 110 ns
- Sector Erase Architecture
  - Sixty-three 32K Word (64K Byte) Sectors with Individual Write Lockout
  - Eight 4K Word (8K Byte) Sectors with Individual Write Lockout
- Fast Word Program Time – 20 µs
- Fast Sector Erase Time – 200 ms
- Dual-plane Organization, Permitting Concurrent Read while Program/Erase
  - Memory Plane A: Eight 4K Word and Fifteen 32K Word Sectors
  - Memory Plane B: Forty-eight 32K Word Sectors
- Erase Suspend Capability
  - Supports Reading/Programming Data from Any Sector by Suspending Erase of Any Different Sector
- Low-power Operation
  - 25 mA Active
  - 10 µA Standby
- Data Polling, Toggle Bit, Ready/$\overline{Busy}$ for End of Program Detection
- VPP Pin for Accelerated Program/Erase Operations
- $\overline{RESET}$ Input for Device Initialization
- Sector Lockdown Support
- Top or Bottom Boot Block Configuration Available
- 128-bit Protection Register

SRAM

- 4-megabit (256K x 16)/8-megabit (512K x 16)
- 2.7V to 3.3V V_{CC}
- 70 ns Access Time
- Fully Static Operation and Tri-state Output
- 1.2V (Min) Data Retention
- Industrial Temperature Range

Device Number	Flash Boot Location	Flash Plane Architecture	SRAM Configuration
AT52BR3244	Bottom	24M + 8M	256K x 16
AT52BR3244T	Top	24M + 8M	256K x 16
AT52BR3248	Bottom	24M + 8M	512K x 16
AT52BR3248T	Top	24M + 8M	512K x 16

32-megabit
(2M x 16) Flash
+ 4-megabit
(256K x 16)/
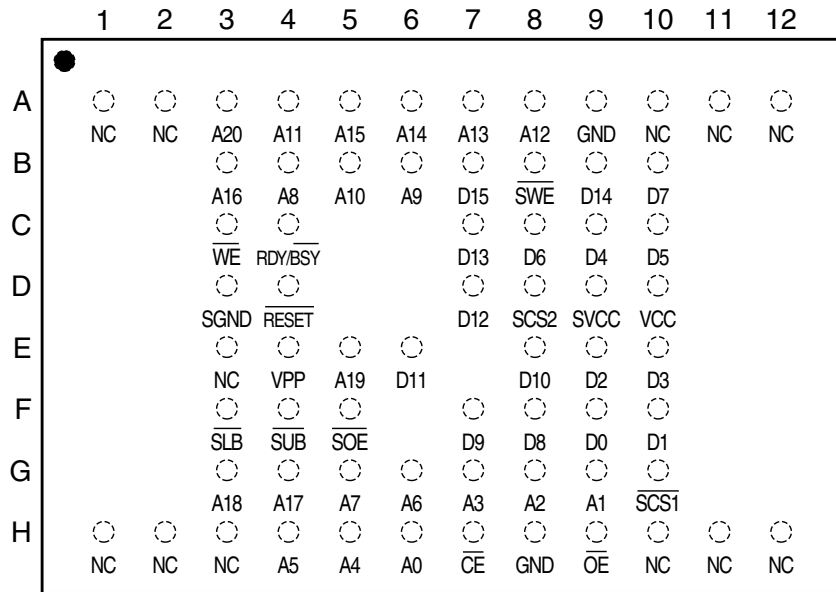8-megabit
(512K x 16)
SRAM
Stack Memory

AT52BR3244
AT52BR3244T
AT52BR3248
AT52BR3248T

Not Recommended for New Designs. New Designs Should Use AT52BR3224(T)/3228(T)

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AT52BR3244(T)/ AT52BR3248(T) (Top View)

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        1     2     3     4     5     6     7     8     9     10    11    12
  A    NC    NC    A20   A11   A15   A14   A13   A12   GND   NC    NC    NC
  B                A16   A8    A10   A9    D15   SWE   D14   D7
  C                WE    RDY/BSY            D13   D6    D4    D5
  D                SGND  RESET              D12   SCS2  SVCC  VCC
  E                NC    VPP   A19   D11          D10   D2    D3
  F                SLB   SUB   SOE         D9    D8    D0    D1
  G                A18   A17   A7    A6    A3    A2    A1    SCS1
  H    NC    NC    NC    A5    A4    A0    CE    GND   OE    NC    NC    NC
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Pin Configurations

Pin Name	Function
A0 - A20	Addresses
$\overline{CE}$	Flash Chip Enable
$\overline{OE}$	Flash Output Enable
$\overline{WE}$	Flash Write Enable
$\overline{RESET}$	Flash Reset
RDY/$\overline{BUSY}$	Flash READY/$\overline{BUSY}$ Output
VPP	Flash Power Supply for Accelerated Program/Erase Operations
VCC	Flash Power
GND	Flash Ground
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect
$\overline{SLB}$	SRAM Lower Byte
$\overline{SUB}$	SRAM Upper Byte
SVCC	SRAM Power
SGND	SRAM Ground
$\overline{SCS1}$	SRAM Chip Select 1
SCS2	SRAM Chip Select 2
$\overline{SWE}$	SRAM Write Enable
$\overline{SOE}$	SRAM Output Enable

AT52BR3244(T)/3248(T)

Description

The AT52BR3244(T) combines a 32-megabit Flash (2M x 16) and a 4-megabit SRAM in a stacked 66-ball CBGA package. The AT52BR3248(T) combines a 32-megabit Flash (2M x 16) and a 8-megabit SRAM in a stacked 66-ball CBGA package. The devices operate at 2.7V to 3.3V in the industrial temperature range. They use a 32-megabit Flash with dual plane architecture for concurrent read/write operations. It is organized as 24M + 8M for planes A and B, respectively. The 4-megabit SRAM is organized as 256K x 16, while the 8-megabit SRAM is organized as 512K x 16.

Block Diagram
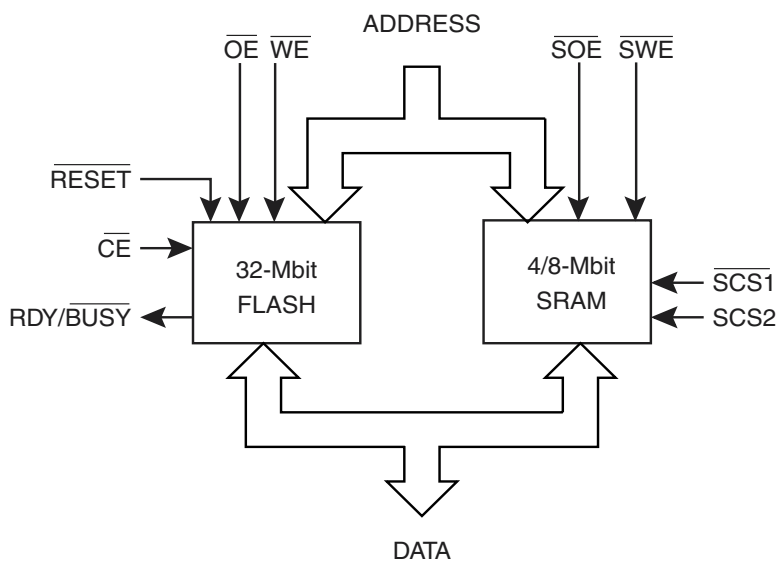
Absolute Maximum Ratings

Temperature under Bias .... -40°C to +85°C

Storage Temperature .... -55°C to +150°C

All Input Voltages
except V_{PP} and $\overline{RESET}$
(including NC Pins)
with Respect to Ground .... -0.2V to +3.3V

Voltage on V_{PP}
with Respect to Ground .... -0.2V to + 6.25V

Voltage on $\overline{RESET}$
with Respect to Ground .... -0.2V to +13.5V

All Output Voltages
with Respect to Ground .... -0.2V to +0.2V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT52BR3244(T)-85, -90	AT52BR3248(T)-85, -90
Operating Temperature (Case)	Industrial	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.3V	2.7V to 3.3V

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32-megabit Flash Description

The 32-megabit Flash memory is organized as 2,097,152 words of 16 bits each or 4,194,304 bytes of 8 bits each. The x16 data appears on I/O0 - I/O15; the x8 data appears on I/O0 - I/O7. The memory is divided into 71 sectors for erase operations. The device has $\overline{CE}$ and $\overline{OE}$ control signals to avoid any bus contention. This device can be read or reprogrammed using a single 2.7V power supply, making it ideally suited for in-system programming.

The device powers on in the read mode. Command sequences are used to place the device in other operation modes such as program and erase. The device has the capability to protect the data in any sector (see Sector Lockdown section).

The device is segmented into two memory planes. Reads from memory plane B may be performed even while program or erase functions are being executed in memory plane A and vice versa. This operation allows improved system performance by not requiring the system to wait for a program or erase operation to complete before a read is performed. To further increase the flexibility of the device, it contains an Erase Suspend feature. This feature will put the erase on hold for any amount of time and let the user read data from or program data to any of the remaining sectors within the same memory plane. There is no reason to suspend the erase operation if the data to be read is in the other memory plane. The end of a program or an erase cycle is detected by the Ready/$\overline{Busy}$ pin, $\overline{Data}$ Polling or by the toggle bit.

The VPP pin provides faster program/erase times. With V_{PP} at 5.0V or 12.0V, the program and erase operations are accelerated.

A six-byte command (Enter Single Pulse Program Mode) sequence to remove the requirement of entering the three-byte program sequence is offered to further improve programming time. After entering the six-byte code, only single pulses on the write control lines are required for writing into the device. This mode (Single Pulse Word Program) is exited by powering down the device, or by pulsing the $\overline{RESET}$ pin low for a minimum of 50 ns and then bringing it back to V_{CC}. Erase and Erase Suspend/Resume commands will not work while in this mode; if entered they will result in data being programmed into the device. It is not recommended that the six-byte code reside in the software of the final product but only exist in external programming code.

32-megabit Flash Memory Block Diagram
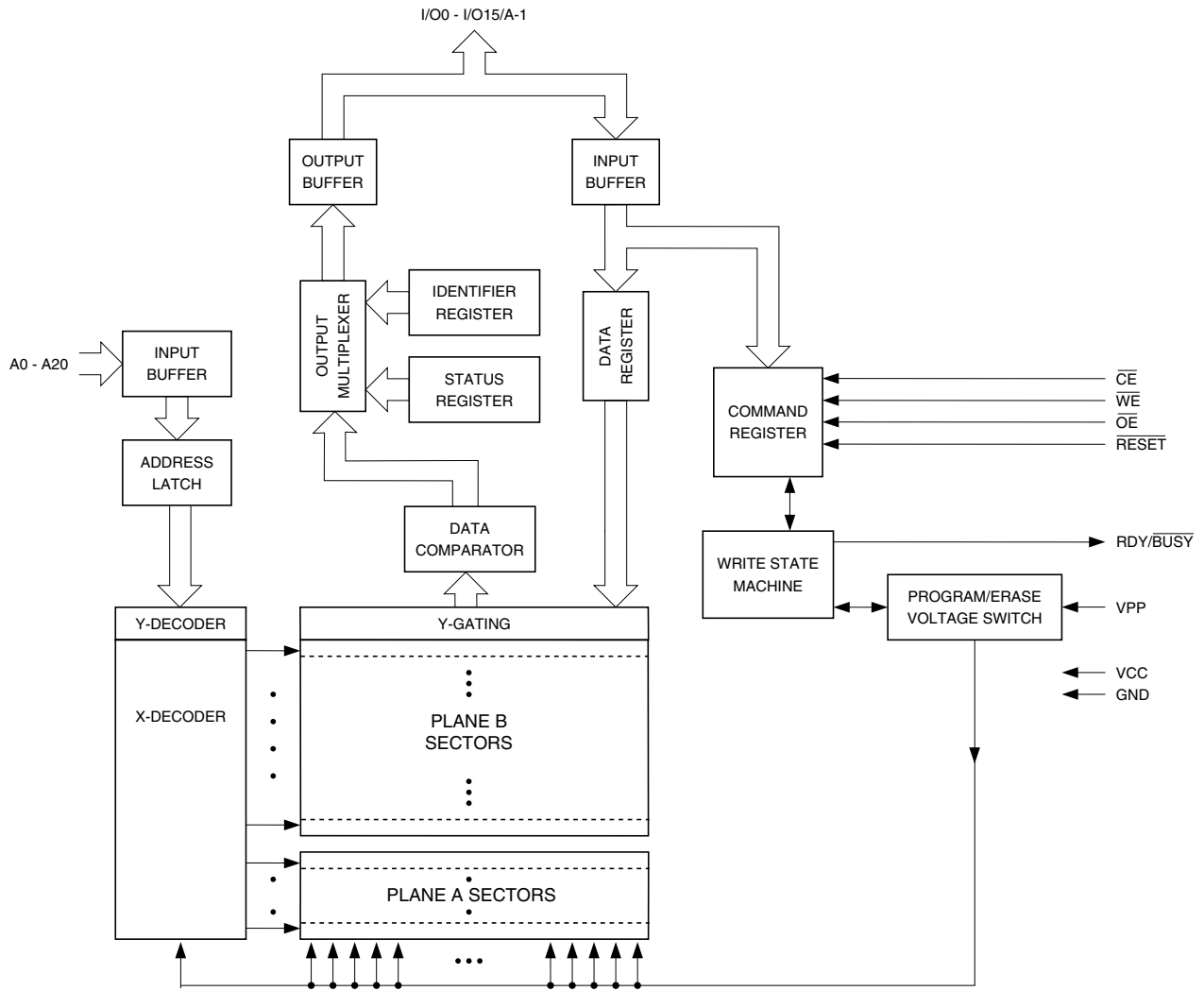
Device Operation

READ: The 32-megabit Flash is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins are asserted on the outputs. The outputs are put in the high-impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

COMMAND SEQUENCES: When the device is first powered on it will be reset to the read or standby mode, depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the Command Definitions table (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

RESET: A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{RESET}$ input halts the present device operation and puts the outputs of the device in a high-impedance state. When a high level is reasserted on the $\overline{RESET}$ pin, the device returns to the read or standby mode, depending upon the state of the control inputs.

ERASURE: Before a word can be reprogrammed, it must be erased. The erased state of memory bits is a logical "1". The entire device can be erased by using the Chip Erase command or individual sectors can be erased by using the Sector Erase command.

CHIP ERASE: The entire device can be erased at one time by using the six-byte chip erase software code. After the chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time to erase the chip is t_{EC}.

If the sector lockdown has been enabled, the chip erase will not erase the data in the sector that has been locked out; it will erase only the unprotected sectors. After the chip erase, the device will return to the read or standby mode.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into 71 sectors (SA0 - SA70) that can be individually erased. The Sector Erase command is a six-bus cycle operation. The sector address is latched on the falling $\overline{WE}$ edge of the sixth cycle while the 30H data input command is latched on the rising edge of $\overline{WE}$. The sector erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion. The maximum time to erase a section is t_{SEC}. When the sector programming lockdown feature is not enabled, the sector will erase (from the same Sector Erase command). An attempt to erase a sector that has been protected will result in the operation terminating in 2 µs.

WORD PROGRAMMING: Once a memory block is erased, it is programmed (to a logical "0") on a word-by-word basis. Programming is accomplished via the internal device command register and is a four-bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is completed after

the specified t_{BP} cycle time. The $\overline{Data}$ Polling feature or the Toggle Bit feature may be used to indicate the end of a program cycle.

VPP PIN: The circuitry of the 32-megabit Flash is designed so that the device can be programmed or erased from the V_{CC} power supply or from the VPP input pin. When V_{PP} is less than or equal to the VCC pin, the device selects the V_{CC} supply for programming and erase operations. When the VPP pin is greater than the V_{CC} supply, the device will select the V_{PP} input as the power supply for programming and erase operations. The device will allow for some variations between the V_{PP} input and the V_{CC} power supply in its selection of V_{CC} or V_{PP} for program or erase operations. If the VPP pin is within 0.3V of V_{CC} for 2.7V < V_{CC} < 3.3V, then the program or erase operations will use V_{CC} and disregard the V_{PP} input signal. When the V_{PP} signal is used to accelerate program and erase operations, the V_{PP} must be in the 5V ± 0.5V or 12V ± 0.5V range to ensure proper operation. The V_{pp} pin can be left unconnected.

SECTOR LOCKDOWN: Each sector has a programming lockdown feature. This feature prevents programming of data in the designated sectors once the feature has been enabled. These sectors can contain secure code that is used to bring up the system. Enabling the lockdown feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; any sector's usage as a write protected region is optional to the user.

At power-up or reset all sectors are unlocked. To activate the lockdown for a specific sector, the six-bus cycle Sector Lockdown command must be issued. Once a sector has been locked down, the contents of the sector is read-only and cannot be erased or programmed.

SECTOR LOCKDOWN DETECTION: A software method is available to determine if programming of a sector is locked down. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from address location 00002H within a sector will show if programming the sector is locked down. If the data on I/O0 is low, the sector can be programmed; if the data on I/O0 is high, the program lockdown feature has been enabled and the sector cannot be programmed. The software product identification exit code should be used to return to standard operation.

SECTOR LOCKDOWN OVERRIDE: The only way to unlock a sector that is locked down is through reset or power-up cycles. After power-up or reset, the content of a sector that is locked down can be erased and reprogrammed.

ERASE SUSPEND/ERASE RESUME: The Erase Suspend command allows the system to interrupt a sector erase operation and then program or read data from a different sector within the same plane. Since this device has a dual-plane architecture, there is no need to use the Erase Suspend feature while erasing a sector when you want to read data from a sector in the other plane. After the Erase Suspend command is given, the device requires a maximum time of 15 µs to suspend the erase operation. After the erase operation has been suspended, the plane that contains the suspended sector enters the erase-suspend-read mode. The system can then read data or program data to any other sector within the device. An address is not required during the Erase Suspend command. During a sector erase suspend, another sector cannot be erased. To resume the sector erase operation, the system must write the Erase Resume command. The Erase Resume command is a one-bus cycle command, which does require the plane address (determined by A20 - A19). The device also supports an erase suspend during a complete chip erase. While the chip erase is suspended, the user can read from any sector within the memory that is protected. The command sequence for a chip erase suspend and a sector erase suspend are the same.

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PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see "Operating Modes" on page 16 (for hardware operation) or "Software Product Identification Entry/Exit" on page 24. The manufacturer and device codes are the same for both modes.

128-BIT PROTECTION REGISTER: The 32-megabit Flash contains a 128-bit register that can be used for security purposes in system design. The protection register is divided into two 64-bit blocks. The two blocks are designated as block A and block B. The data in block A is non-changeable and is programmed at the factory with a unique number. The data in block B is programmed by the user and can be locked out such that data in the block cannot be reprogrammed. To program block B in the protection register, the four-bus cycle Program Protection Register command must be used as shown in the Command Definition table on page 10. To lock out block B, the four-bus cycle Lock Protection Register command must be used as shown in the Command Definition table. Data bit D0 must be one during the fourth bus cycle. All other data bits during the fourth bus cycle are don't cares. Please see the "Protection Register Addressing Table" on page 11 for the address locations in the protection register. To read the protection register, the Product ID Entry command is given followed by a normal read operation from an address within the protection register. After reading the protection register, the Product ID Exit command must be given prior to performing any other operation.

$\overline{\text{DATA}}$ POLLING: The Flash features $\overline{\text{Data}}$ Polling to indicate the end of a program cycle. During a program cycle an attempted read of the last word loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a "0" on I/O7. Once the program or erase cycle has completed, true data will be read from the device. $\overline{\text{Data}}$ Polling may begin at any time during the program cycle. Please see "Status Bit Table" on page 25 for more details.

TOGGLE BIT: In addition to $\overline{\text{Data}}$ Polling, the 32-megabit Flash provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the same memory plane will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

An additional toggle bit is available on I/O2, which can be used in conjunction with the toggle bit that is available on I/O6. While a sector is erase suspended, a read or a program operation from the suspended sector will result in the I/O2 bit toggling. Please see "Status Bit Table" on page 25 for more details.

RDY/$\overline{\text{BUSY}}$: An open-drain Ready/$\overline{\text{Busy}}$ output pin provides another method of detecting the end of a program or erase operation. RDY/$\overline{\text{BUSY}}$ is actively pulled low during the internal program and erase cycles and is released at the completion of the cycle. The open-drain connection allows for OR-tying of several devices to the same RDY/$\overline{\text{BUSY}}$ line.

HARDWARE DATA PROTECTION: The Hardware Data Protection feature protects against inadvertent programs to the Flash in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power-on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$

high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 2.7V to 3.3V power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to V_{CC} + 0.6V.

Command Definition in Hex[1]

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	555	AA	AAA[2]	55	555	80	555	AA	AAA	55	555	10
Sector Erase	6	555	AA	AAA	55	555	80	555	AA	AAA	55	SA[3][4]	30
Word Program	4	555	AA	AAA	55	555	A0	Addr	D_{IN}				
Enter Single Pulse Program Mode	6	555	AA	AAA	55	555	80	555	AA	AAA	55	555	A0
Single Pulse Word Program	1	Addr	D_{IN}										
Sector Lockdown	6	555	AA	AAA	55	555	80	555	AA	AAA	55	SA[3][4]	60
Erase Suspend	1	XXX	B0										
Erase Resume	1	PA[5]	30										
Product ID Entry	3	555	AA	AAA	55	555	90						
Product ID Exit[6]	3	555	AA	AAA	55	555	F0						
Product ID Exit[6]	1	XXX	F0										
Program Protection Register	4	555	AA	AAA	55	555	C0	Addr	D_{IN}				
Lock Protection Register - Block B	4	555	AA	AAA	55	555	C0	080	X0				
Status of Block B Protection	4	555	AA	AAA	55	555	90	80	D_{OUT}[7]				

Notes:
1. The DATA FORMAT shown for each bus cycle is as follows; I/O7 - I/O0 (Hex). In word operation I/O15 - I/O8 are Don't Care. The ADDRESS FORMAT shown for each bus cycle is as follows: A11 - A0 (Hex). Address A20 through A11 are Don't Care in the word mode. Address A20 through A11 and A-1 are Don't Care in the byte mode.
2. Since A11 is a Don't Care, AAA can be replaced with 2AA.
3. SA = sector address. Any word address within a sector can be used to designate the sector address (see pages 12-14 for details).
4. Once a sector is in the lockdown mode, data in the protected sector cannot be changed unless the chip is reset or power cycled.
5. PA is the plane address (A20 - A19).
6. Either one of the Product ID Exit commands can be used.
7. If data bit D1 is "0", block B is locked. If data bit D1 is "1", block B can be reprogrammed.

Absolute Maximum Ratings*

Temperature under Bias .... -55°C to +125°C
Storage Temperature .... -65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground ....-0.6V to +6.25V
All Output Voltages with Respect to Ground ....-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and V_{PP} with Respect to Ground ....-0.6V to +13.0V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Protection Register Addressing Table

Word	Use	Block	A7	A6	A5	A4	A3	A2	A1	A0
0	Factory	A	1	0	0	0	0	0	0	1
1	Factory	A	1	0	0	0	0	0	1	0
2	Factory	A	1	0	0	0	0	0	1	1
3	Factory	A	1	0	0	0	0	1	0	0
4	User	B	1	0	0	0	0	1	0	1
5	User	B	1	0	0	0	0	1	1	0
6	User	B	1	0	0	0	0	1	1	1
7	User	B	1	0	0	0	1	0	0	0

Note: 1.   All address lines not specified in the above table must be 0 when accessing the protection register, i.e., A20 - A8 = 0.

Bottom Boot 32-megabit Flash (24M + 8M) Sector Address Table

Plane	Sector	Size (Words)	x16 Address Range (A20 - A0)
A	SA0	4K	00000 - 00FFF
A	SA1	4K	01000 - 01FFF
A	SA2	4K	02000 - 02FFF
A	SA3	4K	03000 - 03FFF
A	SA4	4K	04000 - 04FFF
A	SA5	4K	05000 - 05FFF
A	SA6	4K	06000 - 06FFF
A	SA7	4K	07000 - 07FFF
A	SA8	32K	08000 - 0FFFF
A	SA9	32K	10000 - 17FFF
A	SA10	32K	18000 - 1FFFF
A	SA11	32K	20000 - 27FFF
A	SA12	32K	28000 - 2FFFF
A	SA13	32K	30000 - 37FFF
A	SA14	32K	38000 - 3FFFF
A	SA15	32K	40000 - 47FFF
A	SA16	32K	48000 - 4FFFF
A	SA17	32K	50000 - 57FFF
A	SA18	32K	58000 - 5FFFF
A	SA19	32K	60000 - 67FFF
A	SA20	32K	68000 - 6FFFF
A	SA21	32K	70000 - 77FFF
A	SA22	32K	78000 - 7FFFF
B	SA23	32K	80000 - 87FFF
B	SA24	32K	88000 - 8FFFF
B	SA25	32K	90000 - 97FFF
B	SA26	32K	98000 - 9FFFF
B	SA27	32K	A0000 - A7FFF
B	SA28	32K	A8000 - AFFFF
B	SA29	32K	B0000 - B7FFF
B	SA30	32K	B8000 - BFFFF
B	SA31	32K	C0000 - C7FFF
B	SA32	32K	C8000 - CFFFF
B	SA33	32K	D0000 - D7FFF
B	SA34	32K	D8000 - DFFFF
B	SA35	32K	E0000 - E7FFF
B	SA36	32K	E8000 - EFFFF

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Bottom Boot 32-megabit Flash (24M + 8M) Sector Address Table (Continued)

Plane	Sector	Size (Words)	x16 Address Range (A20 - A0)
B	SA37	32K	F0000 - F7FFF
B	SA38	32K	F8000 - FFFFF
B	SA39	32K	100000 - 107FFF
B	SA40	32K	108000 - 10FFFF
B	SA41	32K	110000 - 117FFF
B	SA42	32K	118000 - 11FFFF
B	SA43	32K	120000 - 127FFF
B	SA44	32K	128000 - 12FFFF
B	SA45	32K	130000 - 137FFF
B	SA46	32K	138000 - 13FFFF
B	SA47	32K	140000 - 147FFF
B	SA48	32K	148000 - 14FFFF
B	SA49	32K	150000 - 157FFF
B	SA50	32K	158000 - 15FFFF
B	SA51	32K	160000 - 167FFF
B	SA52	32K	168000 - 16FFFF
B	SA53	32K	170000 - 177FFF
B	SA54	32K	178000 - 17FFFF
B	SA55	32K	180000 - 187FFF
B	SA56	32K	188000 - 18FFFF
B	SA57	32K	190000 - 197FFF
B	SA58	32K	198000 - 19FFFF
B	SA59	32K	1A0000 - 1A7FFF
B	SA60	32K	1A8000 - 1AFFFF
B	SA61	32K	1B0000 - 1B7FFF
B	SA62	32K	1B8000 - 1BFFFF
B	SA63	32K	1C0000 - 1C7FFF
B	SA64	32K	1C8000 - 1CFFFF
B	SA65	32K	1D0000 - 1D7FFF
B	SA66	32K	1D8000 - 1DFFFF
B	SA67	32K	1E0000 - 1E7FFF
B	SA68	32K	1E8000 - 1EFFFF
B	SA69	32K	1F0000 -1F7FFF
B	SA70	32K	1F8000 - 1FFFF

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Top Boot 32-megabit Flash (24M + 8M) Sector Address Table

Plane	Sector	Size (Words)	x16 Address Range (A20 - A0)
B	SA0	32K	00000 - 07FFF
B	SA1	32K	08000 - 0FFFF
B	SA2	32K	10000 - 17FFF
B	SA3	32K	18000 - 1FFFF
B	SA4	32K	20000 - 27FFF
B	SA5	32K	28000 - 2FFFF
B	SA6	32K	30000 - 37FFF
B	SA7	32K	38000 - 3FFFF
B	SA8	32K	40000 - 47FFF
B	SA9	32K	48000 - 4FFFF
B	SA10	32K	50000 - 57FFF
B	SA11	32K	58000 - 5FFFF
B	SA12	32K	60000 - 67FFF
B	SA13	32K	68000 - 6FFFF
B	SA14	32K	70000 - 77FFF
B	SA15	32K	78000 - 7FFFF
B	SA16	32K	80000 - 87FFF
B	SA17	32K	88000 - 8FFFF
B	SA18	32K	90000 - 97FFF
B	SA19	32K	98000 - 9FFFF
B	SA20	32K	A0000 - A7FFF
B	SA21	32K	A8000 - AFFFF
B	SA22	32K	B0000 - B7FFF
B	SA23	32K	B8000 - BFFFF
B	SA24	32K	C0000 - C7FFF
B	SA25	32K	C8000 - CFFFF
B	SA26	32K	D0000 - D7FFF
B	SA27	32K	D8000 - DFFFF
B	SA28	32K	E0000 - E7FFF
B	SA29	32K	E8000 - EFFFF
B	SA30	32K	F0000 - F7FFF
B	SA31	32K	F8000 - FFFFF
B	SA32	32K	100000 - 107FFF
B	SA33	32K	108000 - 10FFFF
B	SA34	32K	110000 - 117FFF
B	SA35	32K	118000 - 11FFFF
B	SA36	32K	120000 - 127FFF

Top Boot 32-megabit Flash (24M + 8M) Sector Address Table (Continued)

Plane	Sector	Size (Words)	x16 Address Range (A20 - A0)
B	SA37	32K	128000 - 12FFFF
B	SA38	32K	130000 - 137FFF
B	SA39	32K	138000 - 13FFFF
B	SA40	32K	140000 - 147FFF
B	SA41	32K	148000 - 14FFFF
B	SA42	32K	150000 - 157FFF
B	SA43	32K	158000 - 15FFFF
B	SA44	32K	160000 - 167FFF
B	SA45	32K	168000 - 16FFFF
B	SA46	32K	170000 - 177FFF
B	SA47	32K	178000 - 17FFFF
A	SA48	32K	180000 - 187FFF
A	SA49	32K	188000 - 18FFFF
A	SA50	32K	190000 - 197FFF
A	SA51	32K	198000 - 19FFFF
A	SA52	32K	1A0000 - 1A7FFF
A	SA53	32K	1A8000 - 1AFFFF
A	SA54	32K	1B0000 - 1B7FFF
A	SA55	32K	1B8000 - 1BFFFF
A	SA56	32K	1C0000 - 1C7FFF
A	SA57	32K	1C8000 - 1CFFFF
A	SA58	32K	1D0000 - 1D7FFF
A	SA59	32K	1D8000 - 1DFFFF
A	SA60	32K	1E0000 - 1E7FFF
A	SA61	32K	1E8000 - 1EFFFF
A	SA62	32K	1F0000 - 1F7FFF
A	SA63	4K	1F8000 - 1F8FFF
A	SA64	4K	1F9000 - 1F9FFF
A	SA65	4K	1FA000 - 1FAFFF
A	SA66	4K	1FB000 - 1FBFFF
A	SA67	4K	1FC000 - 1FCFFF
A	SA68	4K	1FD000 - 1FDFFF
A	SA69	4K	1FE000 - 1FEFFF
A	SA70	4K	1FF000 - 1FFFFF

DC and AC Operating Range

		AT52BR3244(T)-85, 90	AT52BR3248(T)-85, 90
Operating Temperature (Case)	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.3V	2.7V to 3.3V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	V_{PP}	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Ai	D_{OUT}
Program/Erase[2]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PP}[6]	Ai	D_{IN}
Standby/Program Inhibit	V_{IH}	X[1]	X	V_{IH}	X	X	High-Z
Program Inhibit	X	X	V_{IH}	V_{IH}	X		
	X	V_{IL}	X	V_{IH}	X		
Output Disable	X	V_{IH}	X	V_{IH}	X		High-Z
Reset	X	X	X	V_{IL}	X	X	High-Z
Product Identification							
Hardware	V_{IL}	V_{IL}	V_{IH}	V_{IH}		A1 - A20 = V_{IL}, A9 = V_H[3], A0 = V_{IL}	Manufacturer Code[4]
						A1 - A20 = V_{IL}, A9 = V_H[3], A0 = V_{IH}	Device Code[4]
Software[5]				V_{IH}		A0 = V_{IL}, A1 - A20 = V_{IL}	Manufacturer Code[4]
						A0 = V_{IH}, A1 - A20 = V_{IL}	Device Code[4]

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC programming waveforms on page 23.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 001FH, Device Code: 00D8H - AT4952BR3244/3248;
   00D9H - AT52BR3244T/3248T.
5. See details under "Software Product Identification Entry/Exit" on page 24.
6. V_{PP} can be left unconnected or 0V ≤ V_{PP} ≤ 3.3V. For faster erase/program operations, V_{PP} can be set to 5.0V ± 0.5V or 12V ± 0.5V.

AT52BR3244(T)/3248(T)

DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		10	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		1	mA
I_{SB3}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}, V_{CC} = 2.85V		10	µA
I_{CC} [1]	V_{CC} Active Read Current	f = 5 MHz; I_{OUT} = 0 mA		30	mA
I_{CC1}	V_{CC} Programming Current (V_{PP} = V_{CC})			30	mA
I_{PP1}	V_{PP} Input Load Current	V_{PP} = 0V, V_{CC} = 3.0V		-10	µA
		V_{PP} = V_{CC} = 3.0V		50	µA
I_{CC2}	V_{CC} Programming Current (V_{PP} = 5.0V ± 0.5V)			30	mA
I_{PP2}	V_{PP} Programming Current (V_{PP} = 5.0V ± 0.5V)			25	mA
I_{CC3}	V_{CC} Programming Current (V_{PP} = 12.0V ± 0.5V)			30	mA
I_{PP3}	V_{PP} Programming Current (V_{PP} = 12.0V ± 0.5V)			40	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OL2}	Output Low Voltage	I_{OL} = 1.0 mA		0.20	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage	I_{OH} = -100 µA	2.5		V

Note: 1. In the erase mode, I_{CC} is 50 mA.

AC Read Characteristics

Symbol	Parameter	AT52BR3244(T)/3248(T)-85		AT52BR3244(T)/3248(T)-90		AT52BR3244(T)/3248(T)-110		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		85		90		110	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		85		90		110	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	40	0	40	0	40	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	25	0	25	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns
t_{RO}	$\overline{RESET}$ to Output Delay		600		600		600	ns

AC Read Waveforms[1][2][3][4]
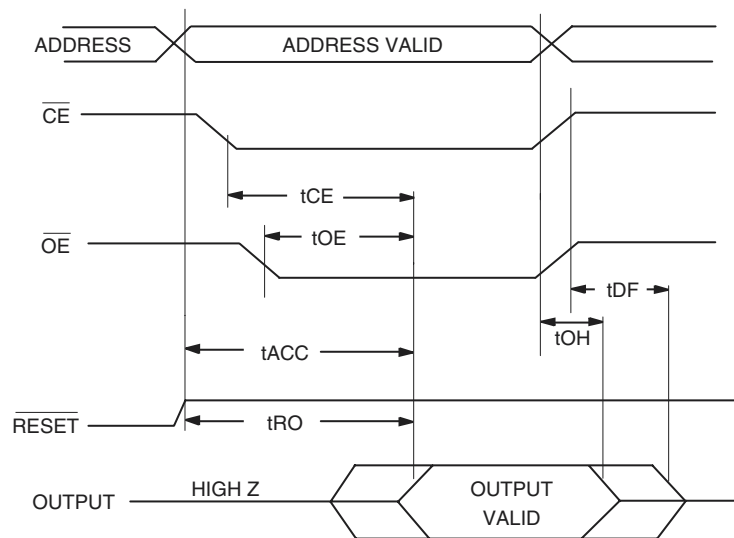
Notes: 1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (CL = 5 pF).
4. This parameter is characterized and is not 100% tested.

18   AT52BR3244(T)/3248(T)

Input Test Waveforms and Measurement Level

AC DRIVING LEVELS

2.4V

0.4V

1.5V

AC MEASUREMENT LEVEL

t_R, t_F < 5 ns

Output Test Load

3.3V

1.8K

OUTPUT PIN

1.3K

50 pF
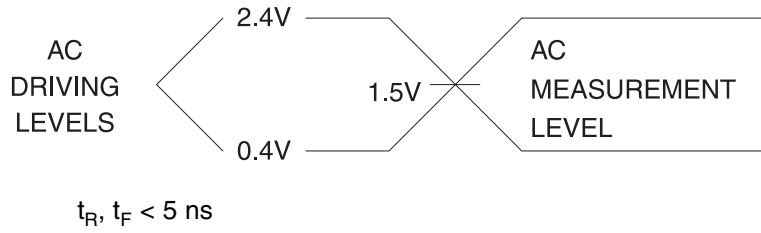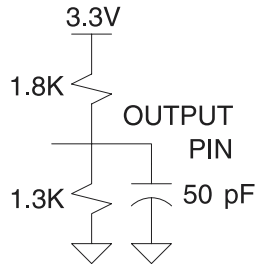
Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1.   This parameter is characterized and is not 100% tested.

AC Word Load Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	50		ns
t_{DS}	Data Setup Time	40		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	40		ns

AC Word Load Waveforms

$\overline{WE}$ Controlled
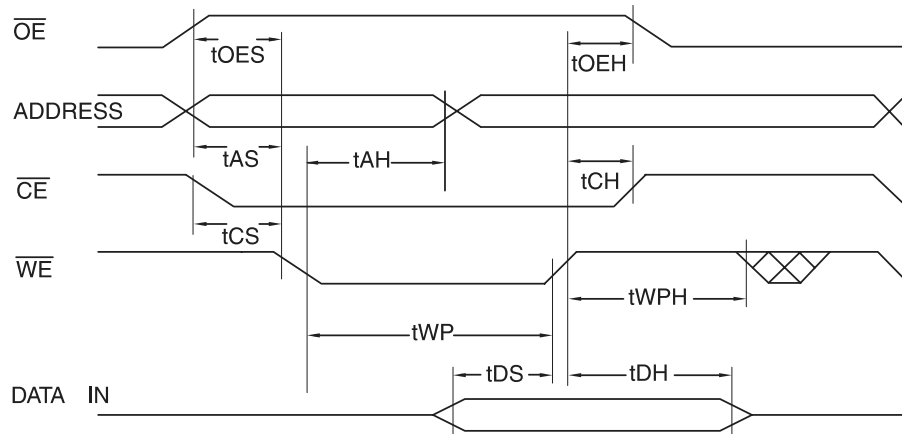
$\overline{CE}$ Controlled
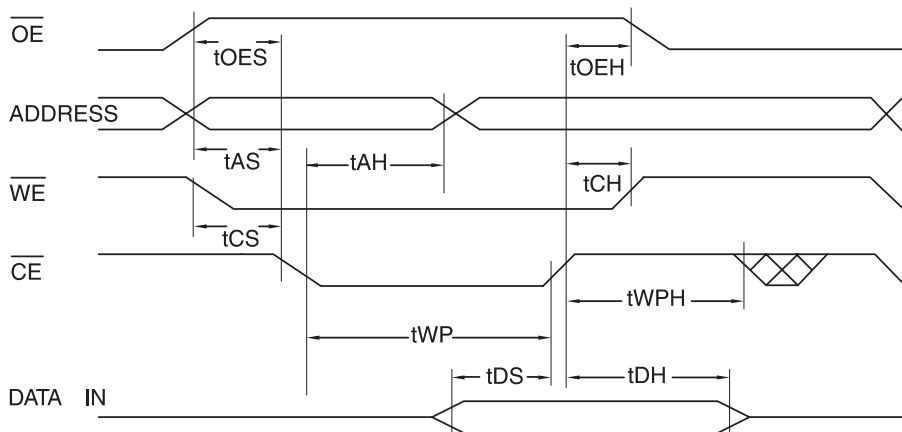
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Word Programming Time ($0V < V_{PP} < 4.5V$)		20	50	µs
t_{BPVPP}	Word Programming Time ($V_{PP} \geq 4.5V$)		10	25	µs
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Setup Time	40			ns
t_{DH}	Data Hold Time	10			ns
t_{WP}	Write Pulse Width	50			ns
t_{WPH}	Write Pulse Width High	40			ns
t_{WC}	Write Cycle Time	90			ns
$t_{SR/W}$	Latency between Read and Write Operations	0			ns
t_{RP}	$\overline{\text{Reset}}$ Pulse Width	500			ns
t_{RH}	$\overline{\text{Reset}}$ High Time before Read	200			ns
t_{EC}	Chip Erase Cycle Time ($V_{PP} < 4.5V$)			10	seconds
t_{ECVPP}	Chip Erase Cycle Time ($V_{PP} \geq 4.5V$)			5	seconds
t_{SEC}	Sector Erase Cycle Time ($V_{PP} < 4.5V$)		200	400	ms
t_{SECVPP}	Sector Erase Cycle Time ($V_{PP} \geq 4.5V$)		100	150	ms
t_{EPS}	Erase or Program Suspend Time			15	µs

## Program Cycle Waveforms
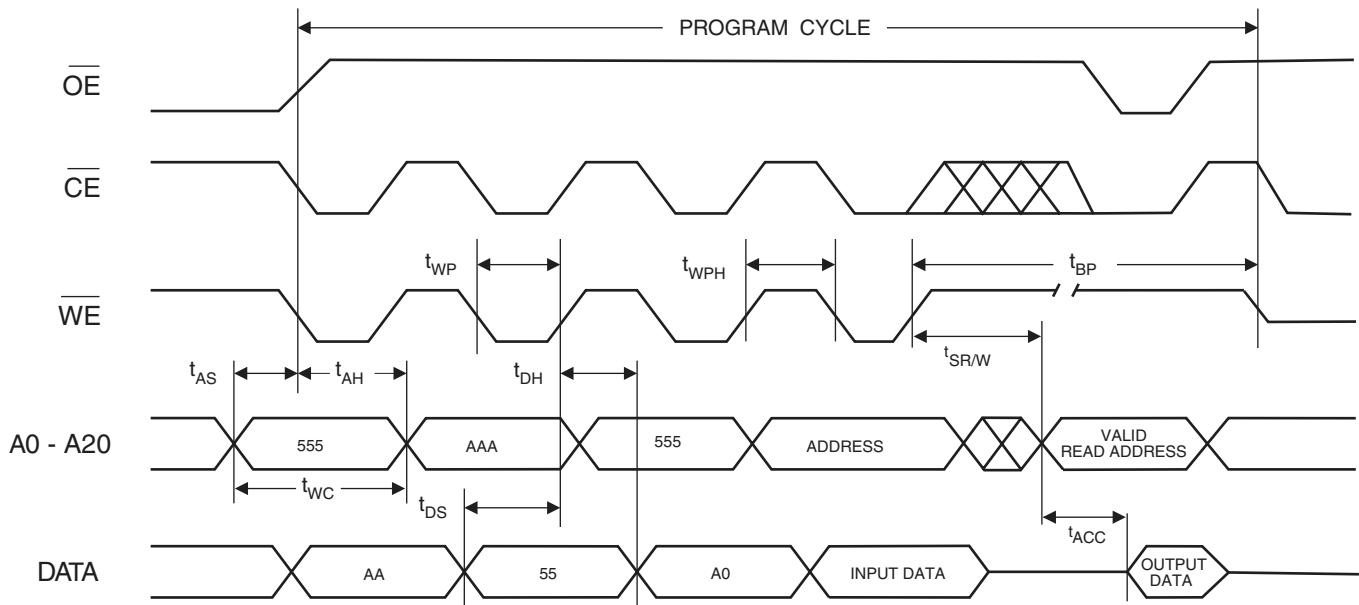
Sector or Chip Erase Cycle Waveforms
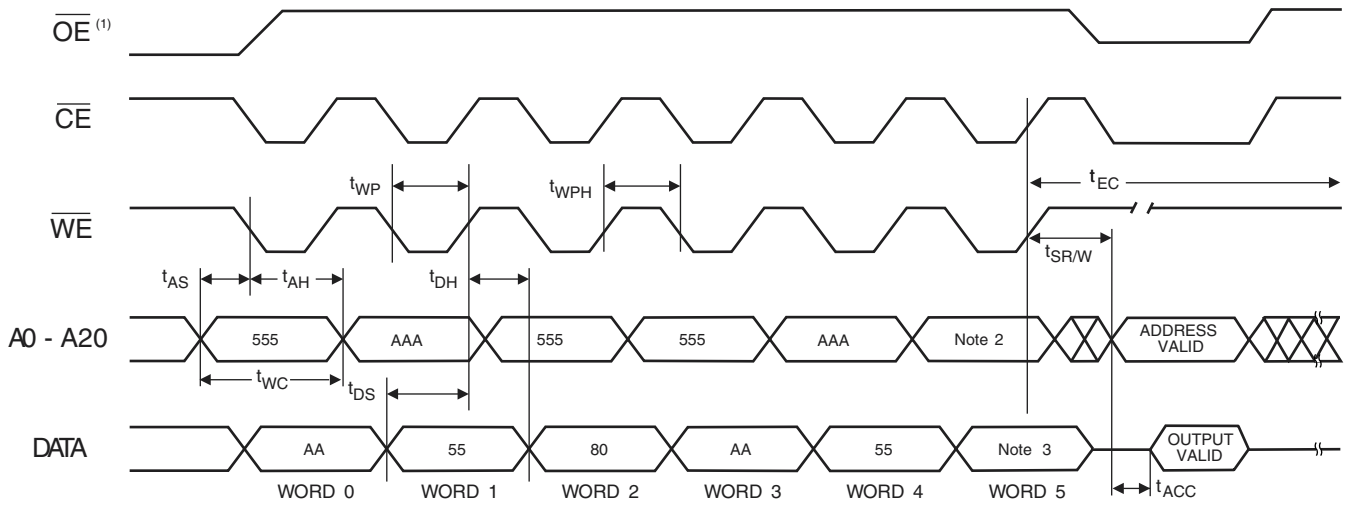
Notes: 1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
2. For chip erase, the address should be 555. For sector erase, the address depends on what sector is to be erased. (See note 3 under Command Definitions.)
3. For chip erase, the data should be 10H, and for sector erase, the data should be 30H.

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Data Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" on page 18.

Data Polling Waveforms
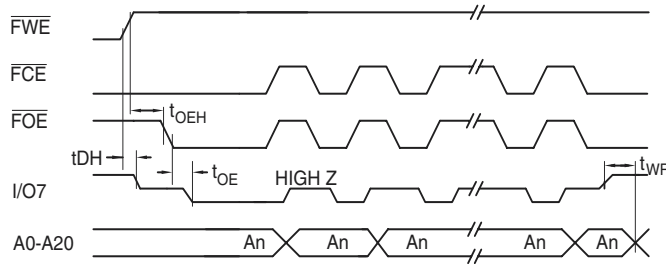
Toggle Bit Characteristics[1]

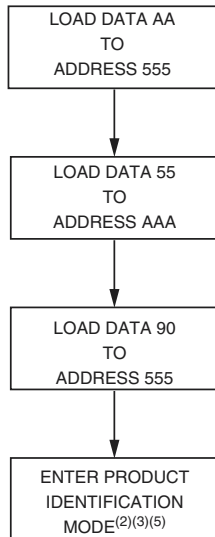| Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" on page 18.
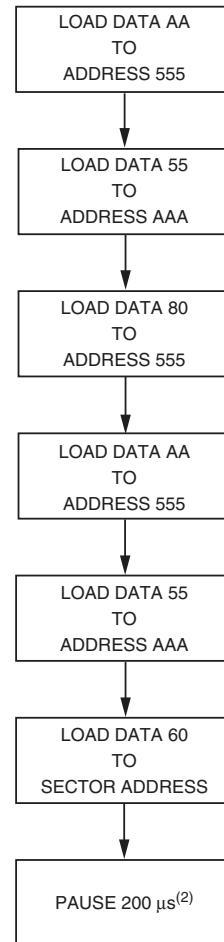
Toggle Bit Waveforms[1][2][3]
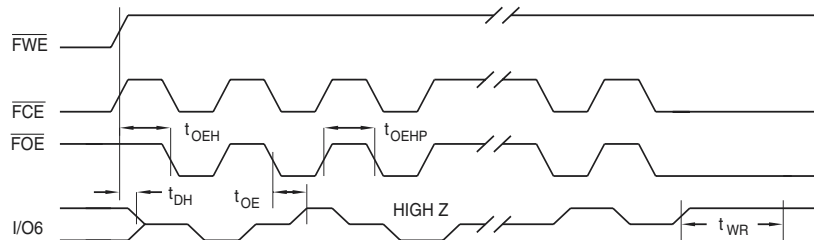
Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
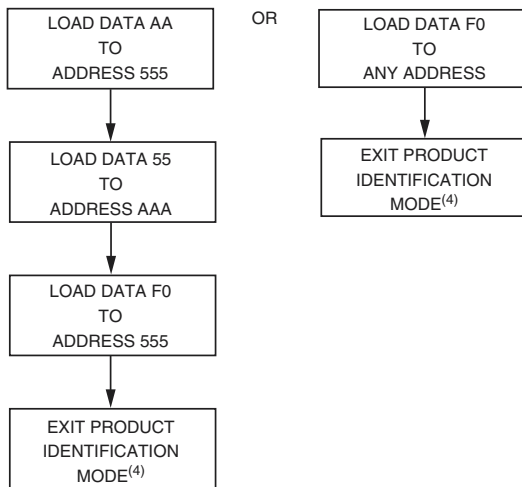3. Any address location may be used but the address should not vary.

Software Product Identification Entry[1]

```
LOAD DATA AA
TO
ADDRESS 555
      |
      v
LOAD DATA 55
TO
ADDRESS AAA
      |
      v
LOAD DATA 90
TO
ADDRESS 555
      |
      v
ENTER PRODUCT
IDENTIFICATION
MODE[2][3][5]
```

Software Product Identification Exit[1][6]

```
LOAD DATA AA           OR      LOAD DATA F0
TO                             TO
ADDRESS 555                    ANY ADDRESS
      |                             |
      v                             v
LOAD DATA 55                  EXIT PRODUCT
TO                            IDENTIFICATION
ADDRESS AAA                   MODE[4]
      |
      v
LOAD DATA F0
TO
ADDRESS 555
      |
      v
EXIT PRODUCT
IDENTIFICATION
MODE[4]
```

Notes: 1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
         Address Format: A11 - A0 (Hex) and A11 - A20 (Don't Care).
      2. A1 - A20 = V_{IL}. Manufacturer Code is read for A0 = V_{IL}; Device Code is read for A0 = V_{IH}. Additional Device Code is read for address 0003H
      3. The device does not remain in identification mode if powered down.
      4. The device returns to standard operation mode.
      5. Manufacturer Code: 001FH(x16) Device Code: 00D8H-AT52BR3244/3248; 00D9H-AT52BR3244T/3248T.
      6. Either one of the Product ID Exit commands can be used.

Sector Lockdown Enable Algorithm[1]

```
LOAD DATA AA
TO
ADDRESS 555
      |
      v
LOAD DATA 55
TO
ADDRESS AAA
      |
      v
LOAD DATA 80
TO
ADDRESS 555
      |
      v
LOAD DATA AA
TO
ADDRESS 555
      |
      v
LOAD DATA 55
TO
ADDRESS AAA
      |
      v
LOAD DATA 60
TO
SECTOR ADDRESS
      |
      v
PAUSE 200 µs[2]
```

Notes: 1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
         Address Format: A11 - A0 (Hex) and A11 - A20 (Don't Care).
      2. Sector Lockdown feature enabled.

Status Bit Table

Read Address In	Status Bit					
	I/O7		I/O6		I/O2	
	Plane A	**Plane B**	**Plane A**	**Plane B**	**Plane A**	**Plane B**
While						
Programming in Plane A	$\overline{\text{I/O7}}$	DATA	TOGGLE	DATA	1	DATA
Programming in Plane B	DATA	$\overline{\text{I/O7}}$	DATA	TOGGLE	DATA	1
Erasing in Plane A	0	DATA	TOGGLE	DATA	TOGGLE	DATA
Erasing in Plane B	DATA	0	DATA	TOGGLE	DATA	TOGGLE
Erase Suspended & Read Erasing Sector	1	1	1	1	TOGGLE	TOGGLE
Erase Suspended & Read Non-erasing Sector	DATA	DATA	DATA	DATA	DATA	DATA
Erase Suspended & Program Non-erasing Sector in Plane A	$\overline{\text{I/O7}}$	DATA	TOGGLE	DATA	TOGGLE	DATA
Erase Suspended & Program Non-erasing Sector in Plane B	DATA	$\overline{\text{I/O7}}$	DATA	TOGGLE	DATA	TOGGLE

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4-megabit SRAM Description

The 4-megabit SRAM is a high-speed, super low-power CMOS SRAM organized as 256K words by 16 bits. The SRAM uses high-performance full CMOS process technology and is designed for high-speed and low-power circuit technology. It is particularly well-suited for the high-density low-power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.2V.

Features

- **Fully Static Operation and Tri-state Output**
- **TTL Compatible Inputs and Outputs**
- **Battery Backup**
  - **1.2V (Min) Data Retention**

Voltage (V)	Speed (ns)	Operation Current/I_{CC} (mA) (Max)	Standby Current (µA) (Max)	Temperature (°C)
2.7 - 3.3	70	5	15	-40 - 85

Block Diagram

AT52BR3244(T)/3248(T)

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Absolute Maximum Ratings[1]

Symbol	Parameter	Rating	Unit
V_{IN}, V_{OUT}	Input/Output Voltage	-0.3 to 3.6	V
V_{CC}	Power Supply	-0.3 to 4.6	V
T_A	Operating Temperature	-40 to 85	°C
T_{STG}	Storage Temperature	-55 to 150	°C
P_D	Power Dissipation	1.0	W

Note: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

Truth Table

$\overline{SCS1}$	SCS2	$\overline{SWE}$	$\overline{SOE}$	$\overline{SLB}$[2]	$\overline{SUB}$[2]	Mode	I/O Pin I/O0 - I/O7	I/O Pin I/O8 - I/O15	Power
H[1]	X	X	X	X	X	Deselected	High-Z	High-Z	Standby
X[1]	L								
X	X			H	H				
L[1]	H	H	H	L	H	Output Disabled	High-Z	High-Z	Active
				H	L				
				L	L				
L	H	L	X	L	H	Write	D_{IN}	High-Z	Active
				H	L		High-Z	D_{IN}	
				L	L		D_{IN}	D_{IN}	
							D_{IN}	High-Z	
L	H	H	L	L	H	Read	D_{OUT}	High-Z	Active
				H	L		High-Z	D_{OUT}	
				L	L		D_{OUT}	D_{OUT}	
							D_{OUT}	High-Z	

Notes: 1. H = V_{IH}, L = V_{IL}, X = Don't Care (V_{IL} or V_{IH})
2. $\overline{SUB}$, $\overline{SLB}$ (Upper, Lower Byte Enable). These active LOW inputs allow individual bytes to be written or read. When $\overline{SLB}$ is LOW, data is written or read to the lower byte, I/O0 - I/O7. When $\overline{SUB}$ is LOW, data is written or read to the upper byte, I/O8 - I/O15.

Recommended DC Operating Condition

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	2.7	3.0	3.3	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2		V_{CC} + 0.3	V
V_{IL}[1]	Input Low Voltage	-0.31[1]		0.6	V

Note: 1. Undershoot: V_{IL} = -1.5V for pulse width less than 30 ns. Undershoot is sampled, not 100% tested.

DC Electrical Characteristics

T_A = -40°C to 85°C

Symbol	Parameter	Test Condition		Min	Typ[1]	Max	Unit
I_{LI}	Input Leakage Current	$V_{SS} < V_{IN} < V_{CC}$		-1		1	µA
I_{LO}	Output Leakage Current	$V_{SS} < V_{OUT} < V_{CC}$, $\overline{SCS1} = V_{IH}$ or SCS2=V_{IL} or $\overline{SOE} = V_{IH}$ or $\overline{SWE}$ = VIL or $\overline{SUB} = V_{IH}$, $\overline{SLB} = V_{IH}$		-1		1	µA
I_{CC}	Operating Power Supply Current	$\overline{SCS1} = V_{IL}$, SCS2=V_{IH}, $V_{IN} = V_{IH}$ or V_{IL}, $I_{I/O} = 0$ mA				5	mA
I_{CC1}	Average Operating Current	$\overline{SCS1} = V_{IL}$, SCS2 = V_{IH}, $V_{IN} = V_{IH}$ or V_{IL}, Cycle Time = Min 100% Duty, $I_{I/O} = 0$ mA				35	mA
		$\overline{SCS1} < 0.2V$, SCS2 > V_{CC} - 0.2V $V_{IN} < 0.2V$ or $V_{IN} > V_{CC}$ - 0.2V, Cycle Time = 1 µs 100% Duty, $I_{I/O} = 0$ mA				5	mA
I_{SB}	Standby Current (TTL Input)	$\overline{SCS1} = V_{IH}$ or SCS2 = V_{IL} or $\overline{SUB}$, $\overline{SLB} = V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL}				0.5	mA
I_{SB1}	Standby Current (CMOS Input)	$\overline{SCS1} > V_{CC}$ - 0.2V or SCS2 < V_{SS} + 0.2V or $\overline{SUB}$, $\overline{SLB} > V_{CC}$ - 0.2V $V_{IN} > V_{CC}$ - 0.2V or $V_{IN} < V_{SS}$ + 0.2V	SL		0.2	4	µA
			LL		0.2	15	µA
V_{OL}	Output Low	$I_{OL} = 0.1$ mA				0.4	V
V_{OH}	Output High	$I_{OH} = -0.1$ mA		2.4			V

Note: 1. Typical values are at $V_{CC} = 1.8V$ $T_A = 25°C$. Typical values are not 100% tested.

Capacitance[1]

(Temp = 25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max	Unit
C_{IN}	Input Capacitance (Add, $\overline{SCS1}$, SCS2, $\overline{SLB}$, $\overline{SUB}$, $\overline{SWE}$, $\overline{SOE}$)	$V_{IN} = 0$ V	8	pF
C_{OUT}	Output Capacitance (I/O)	$V_{I/O} = 0$ V	10	pF

Note: 1. These parameters are sampled and not 100% tested.

AC Characteristics
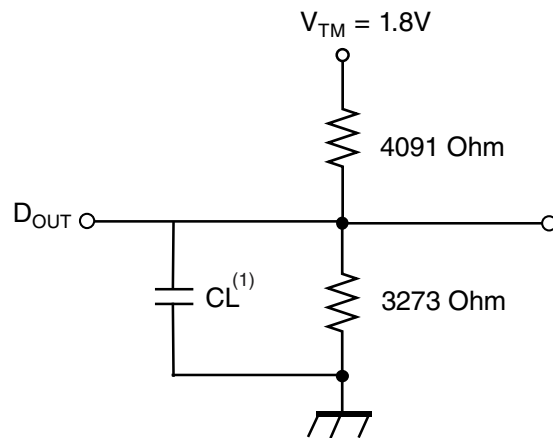
T_A = -40°C to 85°C, Unless Otherwise Specified

#	Symbol	Parameter	70 ns		Unit
			Min	Max	
1	t_{RC}	Read Cycle Time	70		ns
2	t_{AA}	Address Access Time		70	ns
3	t_{ACS}	Chip Select Access Time		70	ns
4	t_{OE}	Output Enable to Output Valid		35	ns
5	t_{BA}	$\overline{SLB}$, $\overline{SUB}$ Access Time		70	ns
6	t_{CLZ}	Chip Select to Output in Low Z	10		ns
7	t_{OLZ}	Output Enable to Output in Low Z	5		ns
8	t_{BLZ}	$\overline{SLB}$, $\overline{SUB}$ Enable to Output in Low Z	10		ns
9	t_{CHZ}	Chip Deselection to Output in High Z	0	30	ns
10	t_{OHZ}	Out Disable to Output in High Z	0	30	ns
11	t_{BHZ}	$\overline{SLB}$, $\overline{SUB}$ Disable to Output in High Z	0	30	ns
12	t_{OH}	Output Hold from Address Change	10		ns
13	t_{WC}	Write Cycle Time	70		ns
14	t_{CW}	Chip Selection to End of Write	60		ns
15	t_{AW}	Address Valid to End of Write	60		ns
16	t_{BW}	$\overline{SLB}$, $\overline{SUB}$ Valid to End of Write	60		ns
17	t_{AS}	Address Setup Time	0		ns
18	t_{WP}	Write Pulse Width	50		ns
19	t_{WR}	Write Recovery Time	0		ns
20	t_{WHZ}	Write to Output in High Z	0	20	ns
21	t_{DW}	Data to Write Time Overlap	30		ns
22	t_{DH}	Data Hold from Write Time	0		ns
23	t_{OW}	Output Active from End of Write	5		ns

AC Test Conditions

TA = -40°C to 85°C, Unless Otherwise Specified

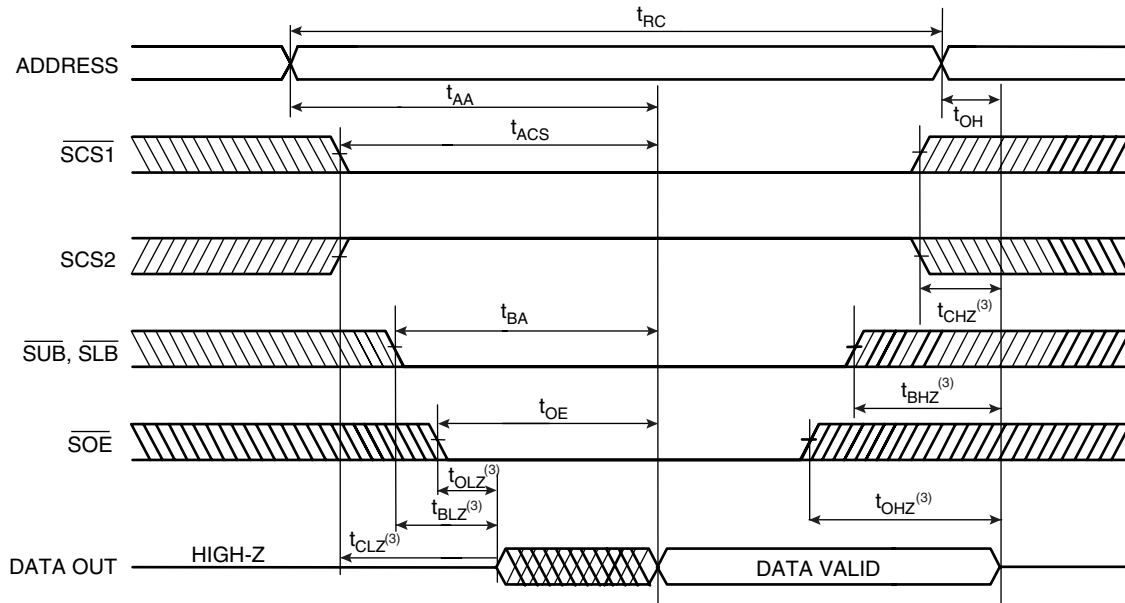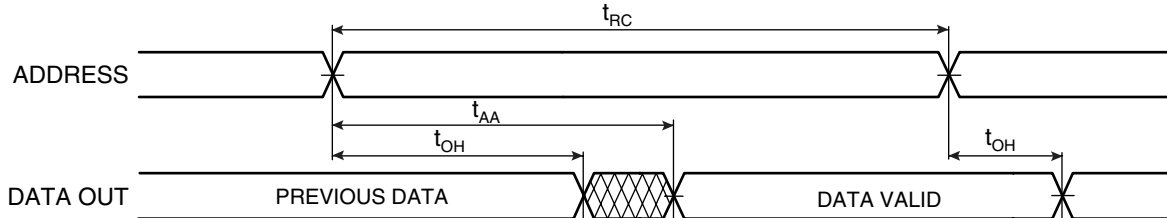| Parameter		Value
Input Pulse Level		0.4V to 2.2V
Input Rise and Fall Time		5 ns
Input and Output Timing Reference Level		1.5V
Output Load	CL = 5 pF + 1 TTL Load	CL = 5 pF + 1 TTL Load
	CL = 30 pF + 1 TTL Load	CL = 30 pF + 1 TTL Load

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AC Test Loads

Note: Including jig and scope capacitance.

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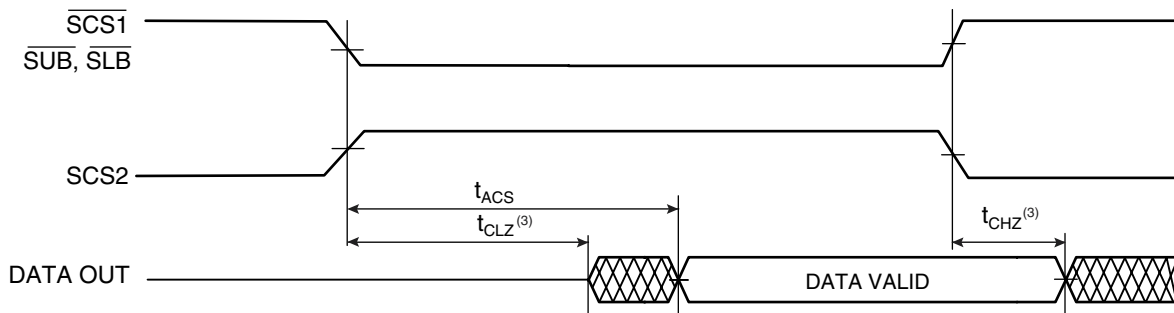## Timing Diagrams

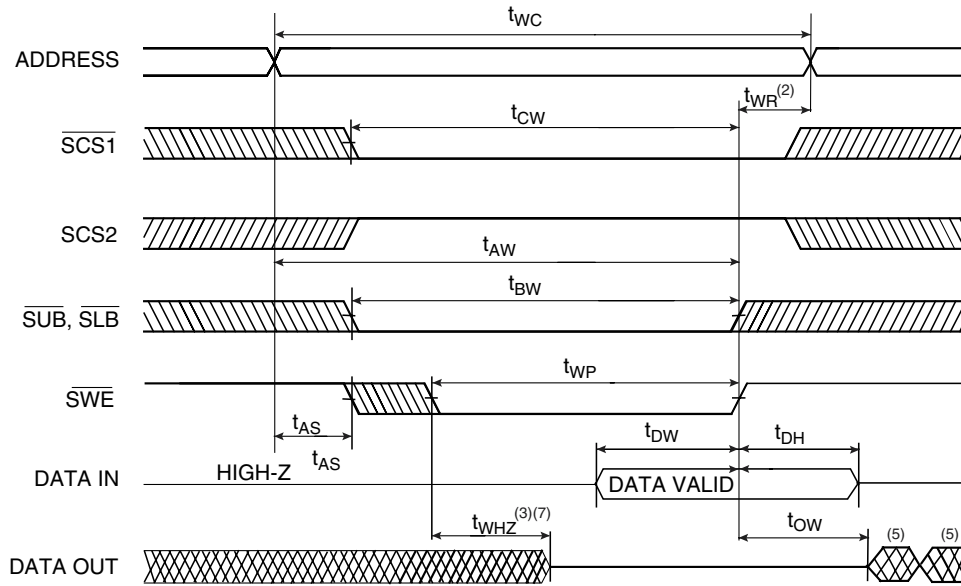### Read Cycle 1[(1),(4)]

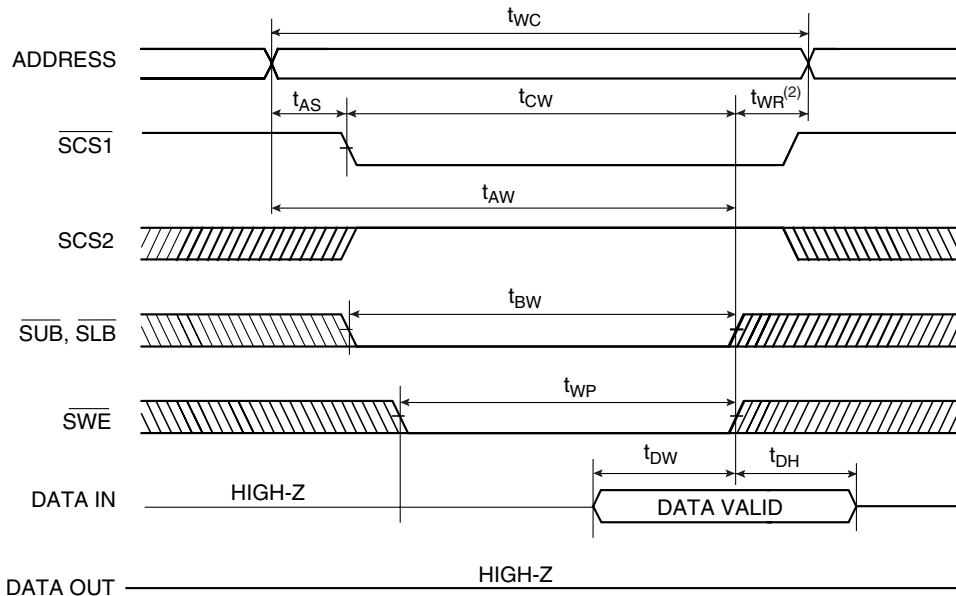### Read Cycle 2[(1),(2),(4)]

Read Cycle 3[(1),(2),(4)]

Notes: 1. Read Cycle occurs whenever a high on the $\overline{SWE}$ and $\overline{SOE}$ is low, while $\overline{SUB}$ and/or $\overline{SLB}$ and $\overline{SCS1}$ and SCS2 are in active status.
2. $\overline{SOE}$ = V_{IL}.
3. Transition is measured + 200 mV from steady state voltage. This parameter is sampled and not 100% tested.
4. $\overline{SCS1}$ in high for the standby, low for active. SCS2 in low for the standby, high for active. $\overline{SUB}$ and $\overline{SLB}$ in high for the standby, low for active.

Write Cycle 1 ($\overline{\text{SWE}}$ Controlled)[1],[4],[8]

ADDRESS

t_{WC}

SCS1

t_{CW} t_{WR}[2]

SCS2

t_{AW}

$\overline{\text{SUB}}$, $\overline{\text{SLB}}$

t_{BW}

$\overline{\text{SWE}}$

t_{WP}

t_{AS}

DATA IN   HIGH-Z t_{AS} DATA VALID t_{DW} t_{DH}

DATA OUT t_{WHZ}[3][7] t_{OW} (5)   (5)

Write Cycle 2 ($\overline{\text{SCS1}}$, SCS2 Controlled)[1],[4],[8]

ADDRESS

t_{WC}

SCS1 t_{AS} t_{CW} t_{WR}[2]

SCS2

t_{AW}

$\overline{\text{SUB}}$, $\overline{\text{SLB}}$

t_{BW}

$\overline{\text{SWE}}$

t_{WP}

DATA IN   HIGH-Z t_{DW} t_{DH} DATA VALID

DATA OUT   HIGH-Z

Notes: 1. A write occurs during the overlap of a low $\overline{\text{SWE}}$, a low $\overline{\text{SCS1}}$, a high SCS2 and a low $\overline{\text{SUB}}$ and/or $\overline{\text{SLB}}$.
2. t_{WR} is measured from the earlier of $\overline{\text{SCS1}}$, $\overline{\text{SLB}}$, $\overline{\text{SUB}}$, or $\overline{\text{SWE}}$ going high or SCS2 going low to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the $\overline{\text{SCS1}}$, $\overline{\text{SLB}}$ and $\overline{\text{SUB}}$ low transition and SCS2 high transition occur simultaneously with the $\overline{\text{SWE}}$ low transition or after the $\overline{\text{SWE}}$ transition, outputs remain in a high impedance state.
5. Q (data out) is the same phase with the write data of this write cycle.
6. Q (data out) is the read data of the next address.
7. Transition is measured + 200 mV from steady state. This parameter is sampled and not 100% tested.
8. $\overline{\text{SCS1}}$ in high for the standby, low for active SCS2 in low for the standby, high for active. $\overline{\text{SUB}}$ and $\overline{\text{SLB}}$ in high for the standby, low for active.
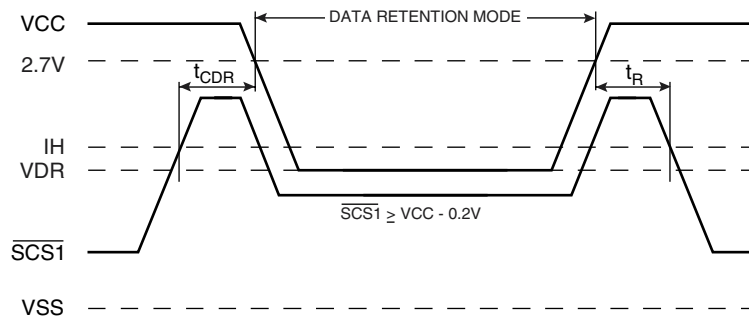
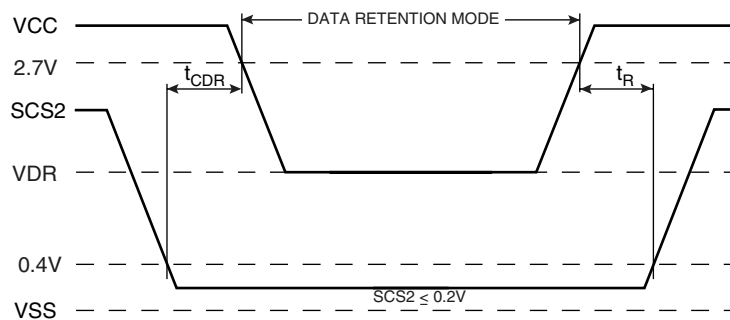## Data Retention Electric Characteristic

T_A = -40°C to 85°C

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{SCS1}$ > V_{CC} - 0.2V or SCS2 < V_{SS} + 0.2V or $\overline{SUB}$, $\overline{SLB}$ > V_{CC} - 0.2V V_{IN} > V_{CC} - 0.2V or V_{IN} < V_{SS} + 0.2V		1.2		3.3	V
I_{CCDR}	Data Retention Current	Vcc=1.5V, $\overline{SCS1}$ > V_{CC} - 0.2V or SCS2 < V_{SS} + 0.2V or $\overline{SUB}$, $\overline{SLB}$ > V_{CC} - 0.2V V_{IN} > V_{CC} - 0.2V or V_{IN} < V_{SS} + 0.2V	SL		0.1	2	µA
			LL		0.1	10	µA
tCDR	See Data Retention Timing Diagram	Chip Deselect to Data Retention Time		0			ns
tR	Operating Recovery Time		t_{RC}				

Note: 1. Typical values are under the condition of T_A = 25°C. Typical values are sampled and not 100% tested.

Data Retention Timing Diagram 1

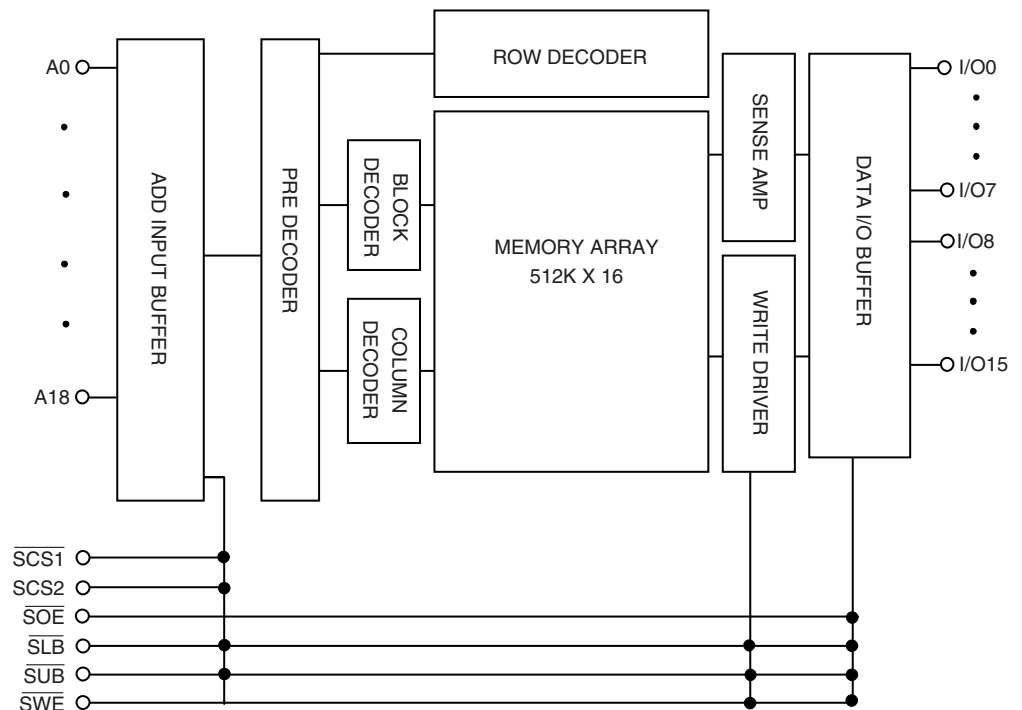## Data Retention Timing Diagram 2

8-megabit SRAM Description

The 8-megabit SRAM is a high-speed, super low-power CMOS SRAM organized as 512K words by 16 bits. The SRAM uses high-performance full CMOS process technology and is designed for high-speed and low-power circuit technology. It is particularly well-suited for the high-density low-power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.2V.

Features

- **Fully Static Operation and Tri-state Output**
- **TTL Compatible Inputs and Outputs**
- **Battery Backup**
    - **1.2V (Min) Data Retention**

Voltage (V)	Speed (ns)	Operation Current/I_{CC} (mA) (Max)	Standby Current (µA) (Max)	Temperature (°C)
2.7 - 3.3	70	5	15	-40 - 85

Block Diagram

AT52BR3244(T)/3248(T)

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Absolute Maximum Ratings[1]

Symbol	Parameter	Rating	Unit
V_{IN}, V_{OUT}	Input/Output Voltage	-0.3 to 3.6	V
V_{CC}	Power Supply	-0.3 to 4.6	V
T_A	Operating Temperature	-40 to 85	°C
T_{STG}	Storage Temperature	-55 to 150	°C
P_D	Power Dissipation	1.0	W

Note: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

Truth Table

$\overline{SCS1}$	SCS2	$\overline{SWE}$	$\overline{SOE}$	$\overline{SLB}$[2]	$\overline{SUB}$[2]	Mode	I/O0 - I/O7	I/O8 - I/O15	Power
H[1]	X	X	X	X	X	Deselected	High-Z	High-Z	Standby
X[1]	L			X	X				
X	X			H	H				
L[1]	H	H	H	L	H	Output Disabled	High-Z	High-Z	Active
				H	L				
				L	L				
L	H	L	X	L	H	Write	D_{IN}	High-Z	Active
				H	L		High-Z	D_{IN}	
				L	L		D_{IN}	D_{IN}	
							D_{IN}	High-Z	
L	H	H	L	L	H	Read	D_{OUT}	High-Z	Active
				H	L		High-Z	D_{OUT}	
				L	L		D_{OUT}	D_{OUT}	
							D_{OUT}	High-Z	

Notes: 1. H = V_{IH}, L = V_{IL}, X = Don't Care (V_{IL} or V_{IH}).
2. $\overline{SUB}$, $\overline{SLB}$ (Upper, Lower Byte Enable). These active LOW inputs allow individual bytes to be written or read. When $\overline{SLB}$ is LOW, data is written or read to the lower byte, I/O0 - I/O7. When $\overline{SUB}$ is LOW, data is written or read to the upper byte, I/O8 - I/O15.

Recommended DC Operating Condition

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	2.7	3.0	3.3	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2		V_{CC} + 0.3	V
V_{IL}[1]	Input Low Voltage	-0.31[1]		0.6	V

Note: 1. Undershoot: V_{IL} = -1.5V for pulse width less than 30 ns. Undershoot is sampled, not 100% tested.

DC Electrical Characteristics

T_A = -40°C to 85°C

Symbol	Parameter	Test Condition	Min	Typ[1]	Max	Unit
I_{LI}	Input Leakage Current	$V_{SS} < V_{IN} < V_{CC}$	-1		1	µA
I_{LO}	Output Leakage Current	$V_{SS} < V_{OUT} < V_{CC}$, $\overline{SCS1} = V_{IH}$ or SCS2=V_{IL} or $\overline{SOE} = V_{IH}$ or $\overline{SWE}$ = VIL or $\overline{SUB} = V_{IH}$, $\overline{SLB} = V_{IH}$	-1		1	µA
I_{CC}	Operating Power Supply Current	$\overline{SCS1} = V_{IL}$, SCS2=V_{IH}, $V_{IN} = V_{IH}$ or V_{IL}, $I_{I/O} = 0$ mA			5	mA
I_{CC1}	Average Operating Current	$\overline{SCS1} = V_{IL}$, SCS2 = V_{IH}, $V_{IN} = V_{IH}$ or V_{IL}, Cycle Time = Min 100% Duty, $I_{I/O} = 0$ mA			40	mA
		$\overline{SCS1} < 0.2V$, SCS2 > V_{CC} - 0.2V $V_{IN} < 0.2V$ or $V_{IN} > V_{CC}$ - 0.2V, Cycle Time = 1 µs 100% Duty, $I_{I/O} = 0$ mA			5	mA
I_{SB}	Standby Current (TTL Input)	$\overline{SCS1} = V_{IH}$ or SCS2 = V_{IL} or $\overline{SUB}$, $\overline{SLB} = V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL}			0.5	mA
I_{SB1}	Standby Current (CMOS Input)	$\overline{SCS1} > V_{CC}$ - 0.2V or SCS2 < V_{SS} + 0.2V or $\overline{SUB}$, $\overline{SLB} > V_{CC}$ - 0.2V $V_{IN} > V_{CC}$ - 0.2V or $V_{IN} < V_{SS}$ + 0.2V	LL		25	µA
V_{OL}	Output Low	$I_{OL} = 0.1$ mA			0.4	V
V_{OH}	Output High	$I_{OH} = -0.1$ mA	2.4			V

Note: 1. Typical values are at V_{CC} = 1.8V T_A = 25°C. Typical values are not 100% tested.

Capacitance[1]

(Temp = 25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max	Unit
C_{IN}	Input Capacitance (Add, $\overline{SCS1}$, SCS2, $\overline{SLB}$, $\overline{SUB}$, $\overline{SWE}$, $\overline{SOE}$)	$V_{IN} = 0$ V	8	pF
C_{OUT}	Output Capacitance (I/O)	$V_{I/O} = 0$ V	10	pF

Note: 1. These parameters are sampled and not 100% tested.

AC Characteristics

T_A = -40°C to 85°C, Unless Otherwise Specified

#	Symbol	Parameter	70 ns Min	70 ns Max	Unit
1	t_{RC}	Read Cycle Time	70		ns
2	t_{AA}	Address Access Time		70	ns
3	t_{ACS}	Chip Select Access Time		70	ns

AC Characteristics

T_A = -40°C to 85°C, Unless Otherwise Specified

#	Symbol	Parameter	70 ns		Unit
			Min	Max	
4	t_{OE}	Output Enable to Output Valid		35	ns
5	t_{BA}	$\overline{SLB}$, $\overline{SUB}$ Access Time		70	ns
6	t_{CLZ}	Chip Select to Output in Low Z	10		ns
7	t_{OLZ}	Output Enable to Output in Low Z	5		ns
8	t_{BLZ}	$\overline{SLB}$, $\overline{SUB}$ Enable to Output in Low Z	10		ns
9	t_{CHZ}	Chip Deselection to Output in High Z	0	30	ns
10	t_{OHZ}	Out Disable to Output in High Z	0	30	ns
11	t_{BHZ}	$\overline{SLB}$, $\overline{SUB}$ Disable to Output in High Z	0	30	ns
12	t_{OH}	Output Hold from Address Change	10		ns
13	t_{WC}	Write Cycle Time	70		ns
14	t_{CW}	Chip Selection to End of Write	60		ns
15	t_{AW}	Address Valid to End of Write	60		ns
16	t_{BW}	$\overline{SLB}$, $\overline{SUB}$ Valid to End of Write	60		ns
17	t_{AS}	Address Setup Time	0		ns
18	t_{WP}	Write Pulse Width	50		ns
19	t_{WR}	Write Recovery Time	0		ns
20	t_{WHZ}	Write to Output in High Z	0	20	ns
21	t_{DW}	Data to Write Time Overlap	30		ns
22	t_{DH}	Data Hold from Write Time	0		ns
23	t_{OW}	Output Active from End of Write	5		ns

AC Test Conditions

TA = -40°C to 85°C, Unless Otherwise Specified

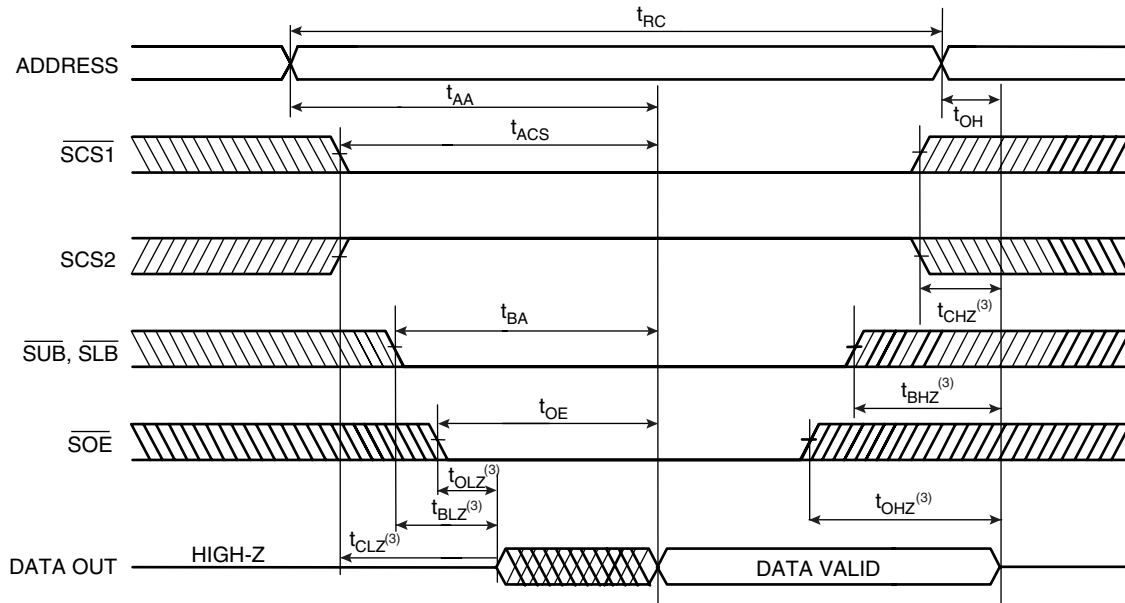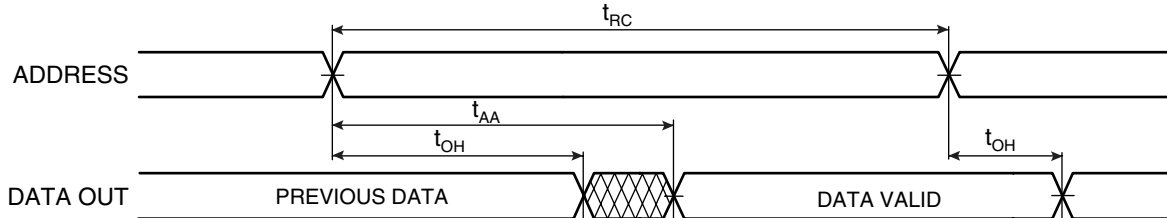| Parameter		Value
Input Pulse Level		0.4V to 2.2V
Input Rise and Fall Time		5 ns
Input and Output Timing Reference Level		1.5V
Output Load	CL = 5 pF + 1 TTL Load	CL = 5 pF + 1 TTL Load
	CL = 30 pF + 1 TTL Load	CL = 30 pF + 1 TTL Load

AC Test Loads

$V_{TM} = 2.8V$

1045 Ohm

D_{OUT}

$CL^{(1)}$

2048 Ohm

Note: Including jig and scope capacitance.

Timing Diagrams

Read Cycle 1[(1),(4)]

t_{RC}

ADDRESS

t_{AA}

t_{OH}

$\overline{SCS1}$

t_{ACS}

SCS2

t_{CHZ}[(3)]

t_{BA}

$\overline{SUB}$, $\overline{SLB}$

t_{BHZ}[(3)]

t_{OE}

$\overline{SOE}$

t_{OLZ}[(3)]

t_{BLZ}[(3)]

t_{OHZ}[(3)]

t_{CLZ}[(3)]

DATA OUT   HIGH-Z   DATA VALID

Read Cycle 2[(1),(2),(4)]

t_{RC}

ADDRESS

t_{AA}

t_{OH}

t_{OH}

DATA OUT   PREVIOUS DATA   DATA VALID

Read Cycle 3[(1),(2),(4)]

$\overline{SCS1}$
$\overline{SUB}$, $\overline{SLB}$

SCS2

t_{ACS}

t_{CLZ}[(3)]

t_{CHZ}[(3)]

DATA OUT   DATA VALID

Notes: 1. Read Cycle occurs whenever a high on the $\overline{SWE}$ and $\overline{SOE}$ is low, while $\overline{SUB}$ and/or $\overline{SLB}$ and $\overline{SCS1}$ and SCS2 are in active status.
2. $\overline{SOE}$ = V_{IL}.
3. Transition is measured + 200 mV from steady state voltage. This parameter is sampled and not 100% tested.
4. $\overline{SCS1}$ in high for the standby, low for active. SCS2 in low for the standby, high for active. $\overline{SUB}$ and $\overline{SLB}$ in high for the standby, low for active.

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Write Cycle 1 ($\overline{\text{SWE}}$ Controlled)[1],[4],[8]

```
                    t_WC
ADDRESS

                    t_CW              t_WR[2]
SCS1

                    t_AW
SCS2
                    t_BW
SUB, SLB

                    t_WP
SWE
        t_AS              t_DW    t_DH
        t_AS
DATA IN   HIGH-Z         DATA VALID

        t_WHZ[3][7]           t_OW
DATA OUT                          (5)  (5)
```

Write Cycle 2 ($\overline{\text{SCS1}}$, SCS2 Controlled)[1],[4],[8]

```
                    t_WC
ADDRESS

        t_AS        t_CW        t_WR[2]
SCS1

                    t_AW
SCS2
                    t_BW
SUB, SLB

                    t_WP
SWE
                        t_DW    t_DH
DATA IN   HIGH-Z         DATA VALID

DATA OUT         HIGH-Z
```

Notes: 1. A write occurs during the overlap of a low $\overline{\text{SWE}}$, a low $\overline{\text{SCS1}}$, a high SCS2 and a low $\overline{\text{SUB}}$ and/or $\overline{\text{SLB}}$.
2. t_{WR} is measured from the earlier of $\overline{\text{SCS1}}$, $\overline{\text{SLB}}$, $\overline{\text{SUB}}$, or $\overline{\text{SWE}}$ going high or SCS2 going low to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the $\overline{\text{SCS1}}$, $\overline{\text{SLB}}$ and $\overline{\text{SUB}}$ low transition and SCS2 high transition occur simultaneously with the $\overline{\text{SWE}}$ low transition or after the $\overline{\text{SWE}}$ transition, outputs remain in a high impedance state.
5. Q (data out) is the same phase with the write data of this write cycle.
6. Q (data out) is the read data of the next address.
7. Transition is measured + 200 mV from steady state. This parameter is sampled and not 100% tested.
8. $\overline{\text{SCS1}}$ in high for the standby, low for active SCS2 in low for the standby, high for active. $\overline{\text{SUB}}$ and $\overline{\text{SLB}}$ in high for the standby, low for active.
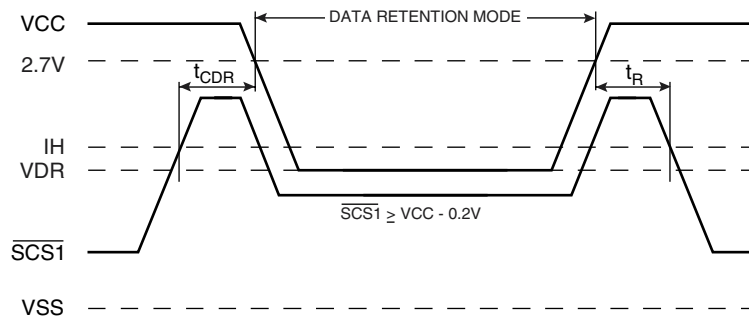
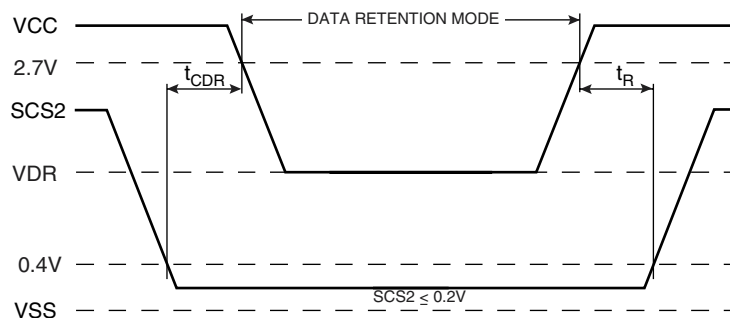## Data Retention Electric Characteristic

T_A = -40°C to 85°C

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{SCS1}$ > V_{CC} - 0.2V or SCS2 < V_{SS} + 0.2V or $\overline{SUB}$, $\overline{SLB}$ > V_{CC} - 0.2V V_{IN} > V_{CC} - 0.2V or V_{IN} < V_{SS} + 0.2V		1.2		3.3	V
I_{CCDR}	Data Retention Current	Vcc=1.5V, $\overline{SCS1}$ > V_{CC} - 0.2V or SCS2 < V_{SS} + 0.2V or $\overline{SUB}$, $\overline{SLB}$ > V_{CC} - 0.2V V_{IN} > V_{CC} - 0.2V or V_{IN} < V_{SS} + 0.2V	SL		0.1	2	µA
			LL		0.1	10	µA
tCDR	See Data Retention Timing Diagram	Chip Deselect to Data Retention Time		0			ns
tR	Operating Recovery Time		t_{RC}				

Note: 1. Typical values are under the condition of T_A = 25°C. Typical values are sampled and not 100% tested.

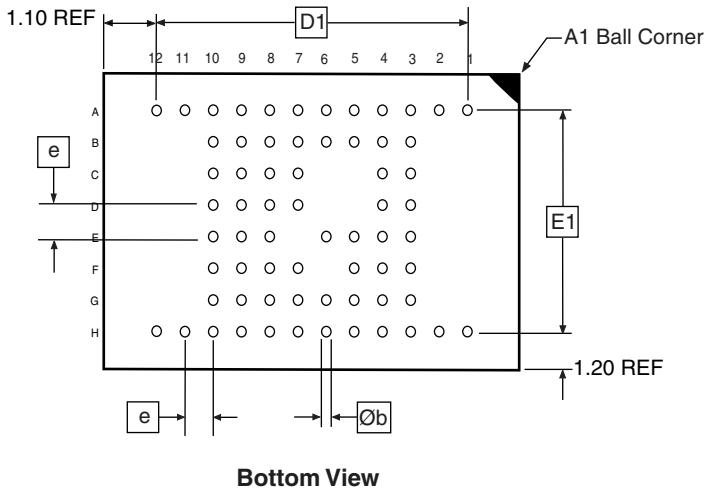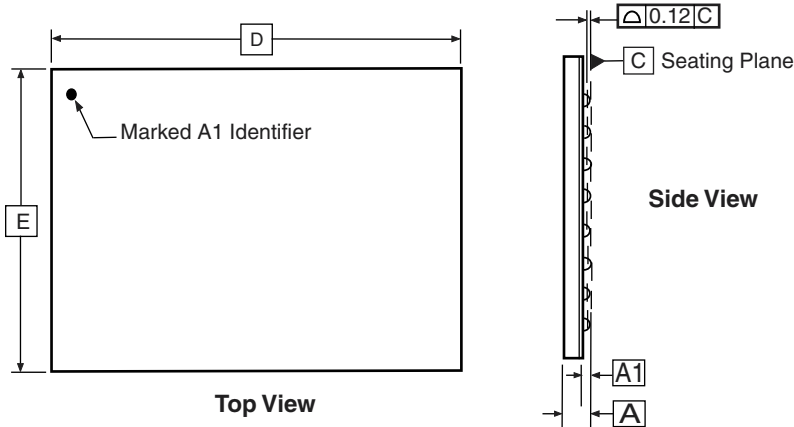## Data Retention Timing Diagram 1

Data Retention Timing Diagram 2

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Ordering Information

t_{ACC} (ns)	Ordering Code	Flash Boot Block	Flash Plane Architecture	SRAM	Package	Operation Range
85	AT52BR3244-85CI	Bottom	24M + 8M	256K x 16	66C4	Industrial (-40° to 85°C)
90	AT52BR3244-90CI	Bottom	24M + 8M	256K x 16	66C4	Industrial (-40° to 85°C)
110	AT52BR3244-11CI	Bottom	24M + 8M	256K x 16	66C4	Industrial (-40° to 85°C)
85	AT52BR3244T-85CI	Top	24M + 8M	256K x 16	66C4	Industrial (-40° to 85°C)
90	AT52BR3244T-90CI	Top	24M + 8M	256K x 16	66C4	Industrial (-40° to 85°C)
110	AT52BR3244T-11CI	Top	24M + 8M	256K x 16	66C4	Industrial (-40° to 85°C)
85	AT52BR3248-85CI	Bottom	24M + 8M	512K x 16	66C4	Industrial (-40° to 85°C)
90	AT52BR3248-90CI	Bottom	24M + 8M	512K x 16	66C4	Industrial (-40° to 85°C)
85	AT52BR3248T-85CI	Top	24M + 8M	512K x 16	66C4	Industrial (-40° to 85°C)
90	AT52BR3248T-90CI	Top	24M + 8M	512K x 16	66C4	Industrial (-40° to 85°C)

Package Type	
66C4	66-ball, Plastic Chip-size Ball Grid Array Package (CBGA)

Packaging Information

66C4 – CBGA

Side View

Top View

Marked A1 Identifier

0.12 C

C Seating Plane

A1

A

Bottom View

1.10 REF

D1

12 11 10 9 8 7 6 5 4 3 2 1

A1 Ball Corner

E1

1.20 REF

e

Øb

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.25	–	–	
D	10.90	11.00	11.10	
D1	8.80 TYP			
E	7.90	8.00	8.10	
E1	5.60 TYP			
e	0.80 TYP			
Øb	0.40 TYP			

08/29/01

		TITLE	DRAWING NO.	REV.
AMEL	2325 Orchard Parkway San Jose, CA 95131	**66C4**, 66-ball (12 x 8 Array), 11 x 8 x 1.2 mm Body, 0.8 mm Ball Pitch Chip-scale Ball Grid Array Package (CBGA)	66C4	A

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