

M/A-COM

GaAs MMIC VSAT Power Amplifier, 2W 5.9 - 6.4 GHz



Features

• High Linear Gain: 30 dB Typ.

High Saturated Output Power: +33 dBm Typ.
High Power Added Efficiency: 26% Typ.

- 50Ω Input/Output Broadband Matched
- High Performance Ceramic Bolt Down Package

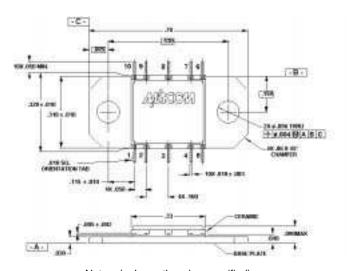
Description

M/A-COM's AM42-0040 is a three-stage MMIC power amplifier in a ceramic bolt down style hermetic package. The AM42-0040 employs an internally matched monolithic chip with internally decoupled Gate and Drain bias networks. The AM42-0040 is designed to be operated from a constant current Drain supply. By varying the Gate bias voltage, the saturated output power performance of this device can be tailored for various applications.

The AM42-0040 is designed for use as an output stage or driver amplifier for C-band VSAT transmitter systems. This amplifier employs a fully monolithic chip and requires a minimum of external components.

M/A-COM's AM42-0040 is fabricated using a mature 0.5 micron GaAs MESFET process. The process features full chip passivation for increased performance and reliability. These amplifiers are 100% RF tested to ensure compliance to performance specifications.

CR-15



Notes: (unless otherwise specified)

1. Dimensions are in inches.

2. Tolerance: .XXX = ± 0.005
.XX = ± 0.010

Ordering Information

Part Number	Package
AM42-0040	Ceramic Bolt Down Package

Electrical Specifications: $T_A = +25$ °C, $V_{DD} = +9V$, V_{GG} adjusted for $I_{DD} = 1050$ mA, Frequency = 5.9 to 6.4 GHz

Parameter	Abby.	Test Conditions	Units	Min.	Тур.	Max.
						Wax.
Linear Gain	G _L	P _{IN} ≤ -10 dBm	dB	27	30	
Input VSWR	VSWR _{IN}	P _{IN} ≤ -10 dBm	_	_	2.3:1	2.7:1
Output VSWR	VSWR _{OUT}	P _{IN} ≤ -10 dBm		_	3.0:1	
Output Power	P _{SAT}	P_{IN} = +10 dBm, I_{DD} =1050 mA Typ.	dBm	31.7	33.0	34.3
Output Power vs. Frequency	P _{SAT}	P_{IN} = +10 dBm, I_{DD} =1050 mA Typ.	dB	_	1.0	1.5
Output Power vs. Temperature	P _{SAT}	P_{IN} = +10 dBm, I_{DD} =1050 mA Typ.	dB	_	±0.4	_
(with respect to T _A =+25°C)		$T_A = -40$ °C to +70°C				
Drain Bias Current	I _{DD}	P _{IN} = +10 dBm	mA	900	1050	1100
Gate Bias Voltage	V_{GG}	P_{IN} = +10 dBm, I_{DD} =1050 mA Typ.	V	-2.4	-1.2	-0.4
Gate Bias Current	I_{GG}	P_{IN} = +10 dBm, I_{DD} =1050 mA Typ.	mA	_	5	20
Thermal Resistance	θ_{JC}	25°C Heat Sink	°C/W	_	5.6	_
Second Harmonic	f ₂	P_{IN} = +10 dBm, I_{DD} =1050 mA Typ.	dBc	_	-35	_
Third Harmonic	f ₃	P_{IN} = +10 dBm, I_{DD} =1050 mA Typ.	dBc	_	-45	_

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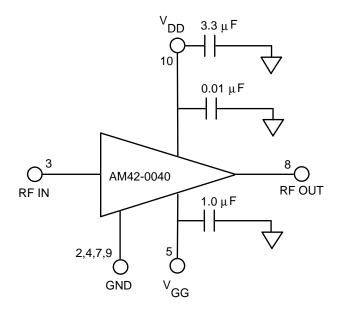


Absolute Maximum Ratings^{1,2,3,4}

Parameter	Absolute Maximum
Input Power	+23 dBm
V_{DD}	+12 Volts
V_{GG}	-3 Volts
V_{DD} - V_{GG}	12 Volts
I _{DD}	1700 mA
Channel Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

- 1. Exceeding any one or a combination of these limits may cause permanent damage.
- 2. Case Temperature $(T_c) = +25$ °C.
- 3. Nominal bias is obtained by first connecting -2.4 volts to pin 5 ($V_{\rm GG}$), followed by connecting +9 volts to pin 10 ($V_{\rm DD}$). Note sequence. Adjust $V_{\rm GG}$ for a drain current of 1050 mA typical.
- RF ground and thermal interface is the flange (case bottom).
 Adequate heat sinking is required.
- 5. No dc supply voltage will appear at the RF ports.
- 6. The dc resistance at the input and output ports is a short circuit. No voltage is allowed on these ports.
- 7. For optimum $\rm IP_3$ performance, the $\rm V_{DD}$ bypass capacitors should be placed within 0.5 inches of the $\rm V_{DD}$ leads.

Typical Bias Configuration^{4,5,6,7}



Pin Configuration

Pin No.	Pin Name	Description
1	N/C	No Connection
2	GND	DC and RF Ground
3	RF In	RF Input
4	GND	DC and RF Ground
5	V_{GG}	Gate Supply
6	N/C	No Connection
7	GND	DC and RF Ground
8	RF Out	RF Output
9	GND	DC and RF Ground
10	V_{DD}	Drain Supply



Typical Performance @ +25°C

