Am42BDS6408H

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with “Am” and “MBM”. To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **30491** Revision **A** Amendment **+3** Issue Date **October 23, 2003**

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ADVANCE INFORMATION

Am42BDS6408H

Am29BDS640H 64 Megabit (4 M x 16-Bit) Stacked MultiChip Package (MCP) Flash Memory and SRAM
CMOS 1.8 Volt-only Simultaneous Read/Write, Burst Mode Flash Memory, and 8 Mbit (512 K x 16-Bit) SRAM

FLASH DISTINCTIVE CHARACTERISTICS

ARCHITECTURAL ADVANTAGES

- **Single 1.8 volt read, program and erase (1.65 to 1.95 volt)**
- **Manufactured on 0.13 µm process technology**
- **VersatileIO™ (V_{IO}) Feature**
  - — Device generates data output voltages and tolerates data input voltages as determined by the voltage on the V_{IO} pin
  - — 1.8V compatible I/O signals
  - — Contact factory for availability of 1.5V compatible I/O signals
- **Simultaneous Read/Write operation**
  - — Data can be continuously read from one bank while executing erase/program functions in other bank
  - — Zero latency between read and write operations
  - — Four bank architecture: 8Mb/24Mb/24Mb/8Mb
- **Programable Burst Interface**
  - — 2 Modes of Burst Read Operation
  - — Linear Burst: 8, 16, and 32 words with wrap-around
  - — Continuous Sequential Burst
- **SecSi™ (Secured Silicon) Sector region**
  - — Up to 128 words accessible through a command sequence
  - — Up to 64 factory-locked words
  - — Up to 64 customer-lockable words
- **Sector Architecture**
  - — Sixteen 4 Kword sectors and one hundred twenty-six 32 Kword sectors
  - — Banks A and D each contain eight 4 Kword sectors and fifteen 32 Kword sectors; Banks B and C each contain forty-eight 32 Kword sectors
  - — Sixteen 4 Kword boot sectors: eight at the top of the address range and eight at the bottom of the address range
- **Minimum 1 million erase cycle guarantee per sector**
- **20-year data retention at 125°C**
  - — Reliable operation for the life of the system
- **89-ball FBGA package**

PERFORMANCE CHARCTERISTICS

- **Read access times at 66/54 MHz (C_L=30 pF)**
  - — Burst access times of 11/13.5 ns at industrial temperature range
  - — Synchronous latency of 56/69 ns
  - — Asynchronous random access times of 45/50/55 ns
- **Power dissipation (typical values, C_L = 30 pF)**
  - — Burst Mode Read: 10 mA
  - — Simultaneous Operation: 25 mA
  - — Program/Erase: 15 mA
  - — Standby mode: 0.2 µA

HARDWARE FEATURES

- **Handshaking feature**
  - — Provides host system with minimum possible latency by monitoring RDY
  - — Reduced Wait-state handshaking option further reduces initial access cycles required for burst accesses beginning on even addresses
- **Hardware reset input (RESET#)**
  - — Hardware method to reset the device for reading array data
- **WP# input**
  - — Write protect (WP#) function allows protection of the four highest and four lowest 4 kWord boot sectors, regardless of sector protect status
- **Persistent Sector Protection**
  - — A command sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector
  - — Sectors can be locked and unlocked in-system at V_{CC} level
- **Password Sector Protection**
  - — A sophisticated sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector using a user-defined 64-bit password
- **ACC input: Acceleration function reduces programming time; all sectors locked when ACC = V_{IL}**

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Refer to AMD's Website (www.amd.com) for the latest information.

- **CMOS compatible inputs, CMOS compatible outputs**
- **Low V_{CC} write inhibit**

SOFTWARE FEATURES

- **Supports Common Flash Memory Interface (CFI)**
- **Software command set compatible with JEDEC 42.4 standards**
  - — Backwards compatible with Am29F and Am29LV families
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program and erase operation completion
- **Erase Suspend/Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Unlock Bypass Program command**
  - — Reduces overall programming time when issuing multiple program command sequences
- **Burst Suspend/Resume**
  - — Suspends a burst operation to allow system use of the address and data bus, than resumes the burst at the previous state

SRAM FEATURES

- **Power dissipation**
  - — Operating: 10 mA typical
  - — Standby: 2 µA
- **CE1s# and CE2 Chip Select**
- **Power down features using CE1s# and CE2s**
- **Data retention supply voltage: 1.0 to 2.2 volt**
- **Byte data control: LB# (DQ7-DQ0), UB#s (DQ15-DQ8)**

GENERAL DESCRIPTION

The Am29BDS640H is a 64 Mbit, 1.8 Volt-only, simultaneous Read/Write, Burst Mode Flash memory device, organized as 4,194,304 words of 16 bits each. This device uses a single V_{CC} of 1.65 to 1.95 V to read, program, and erase the memory array. A 12.0-volt V_{HH} on ACC may be used for faster program performance if desired.

At 66 MHz, the device provides a burst access of 11 ns at 30 pF with a latency of 56 ns at 30 pF.At 54 MHz, the device provides a burst access of 13.5 ns at 30 pF with a latency of 69ns at 30 pF. The device operates within the industrial temperature range of -40°C to +85°C. The device is offered in the 64-ball FBGA package.

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into four banks. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The device is divided as shown in the following table:

Bank	Quantity	Size
A	8	4 Kwords
	15	32 Kwords
B	48	32 Kwords
C	48	32 Kwords
D	15	32 Kwords
	8	4 Kwords

The VersatileIO™ (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{IO} pin.

The device uses Chip Enable (CE#), Write Enable (WE#), Address Valid (AVD#) and Output Enable (OE#) to control asynchronous read and write operations. For burst operations, the device additionally requires Ready (RDY), and Clock (CLK). This implementation allows easy interface with minimal glue logic to a wide range of microprocessors/microcontrollers for high performance read operations.

The burst read mode feature gives system designers flexibility in the interface to the device. The user can preset the burst length and wrap through the same memory space, or read the flash array in continuous mode.

The clock polarity feature provides system designers a choice of active clock edges, either rising or falling. The active clock edge initiates burst accesses and determines when data will be output.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the SecSi Sector area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read boot-up firmware from the Flash memory device.

The host system can detect whether a program or erase operation is complete by using the device status bit DQ7 (Data# Polling) and DQ6/DQ2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The device also offers two types of data protection at the sector level. When at V_{IL}, **WP#** locks the four highest and four lowest boot sectors.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunnelling. The data is programmed using hot electron injection.

TABLE OF CONTENTS

PRODUCT SELECTOR GUIDE

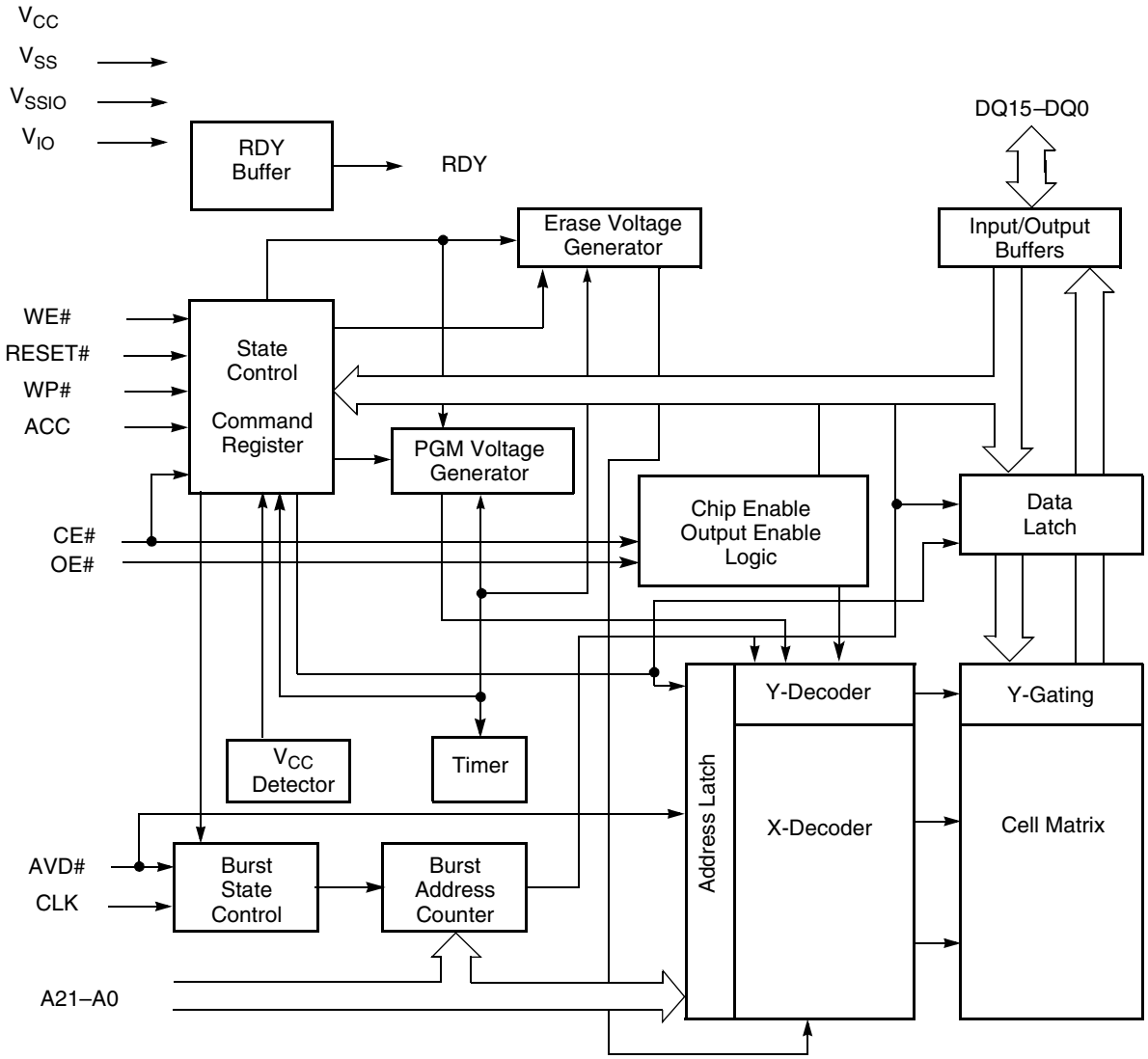
Part Number			Am42BDS6408H			
Burst Frequency			66 MHz		54 MHz	
Speed Option		V_{CC}, V_{IO} = 1.65 – 1.95 V	E8, E9	E3, E4	D8, D9	D3, D4
FLASH	Max Initial Synchronous Access Time, ns (T_{IACC}) Reduced Wait-state Handshaking; Even Address		56	56	69	69
	Max Initial Synchronous Access Time, ns (T_{IACC}) Reduced Wait-state Handshaking; Odd Address; or Standard Handshaking		71	71	87.5	87.5
	Max Burst Access Time, ns (T_{BACC})		11		13.5	
	Max Asynchronous Access Time, ns (T_{ACC})		50	50	55	55
	Max CE# Access Time, ns (T_{CE})					
	Max OE# Access Time, ns (T_{OE})		11		13.5	
SRAM	Max Access time, ns (t_{ACC})		70	55	70	55
	Max CE# Access time, ns (t_{CE})		70	55	70	55
	Max OE# Access, ns (t_{OE})		35	25	35	25

Note: *Speed Options ending in "8" and "6" indicate the "reduced wait-state handshaking" option, which speeds initial synchronous accesses for even addresses.*

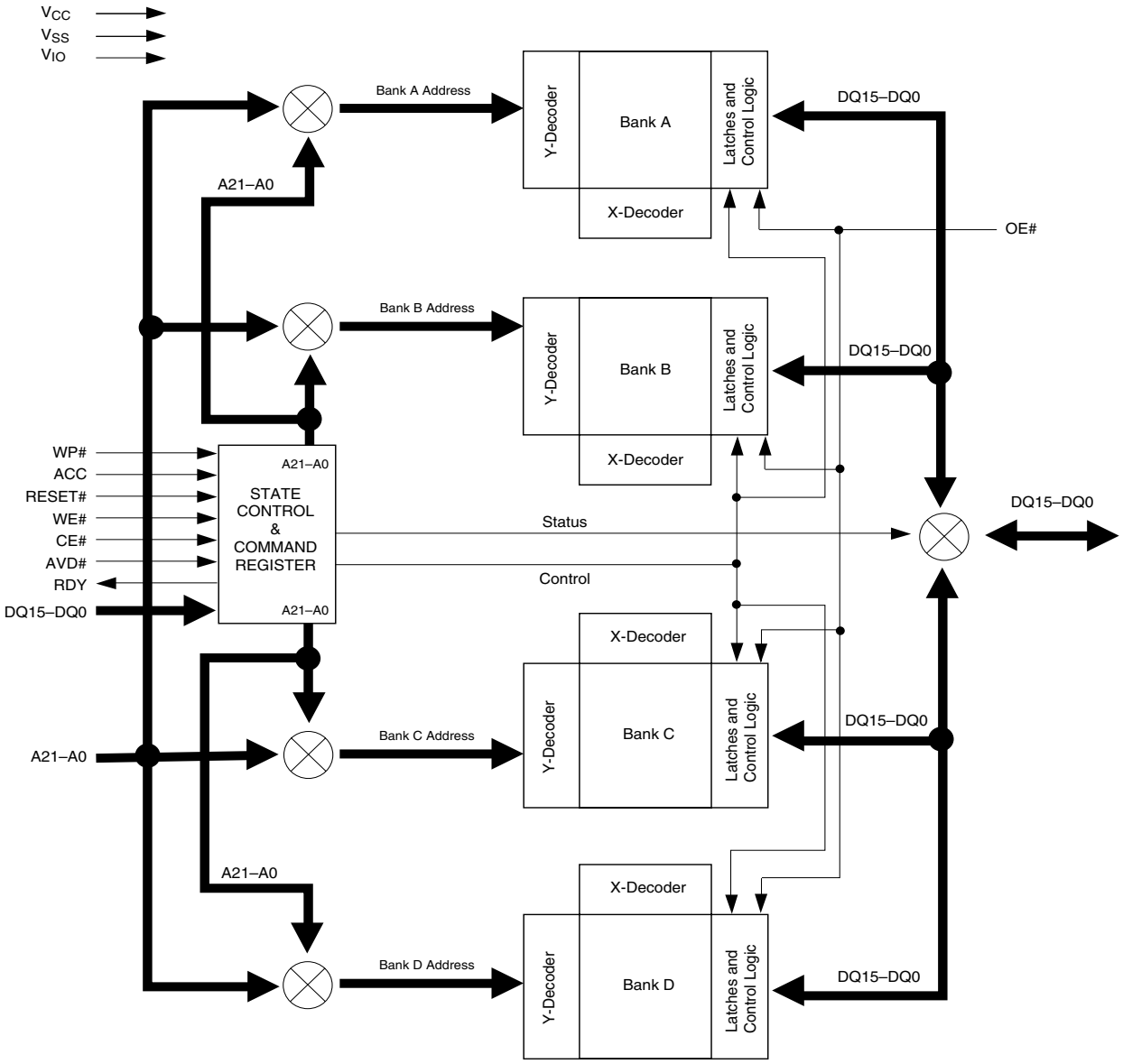
Speed Options ending in "9" and "7" indicate the "standard handshaking" option.

See the AC Characteristics section of this datasheet for full specifications.

FLASH MEMORY BLOCK DIAGRAM

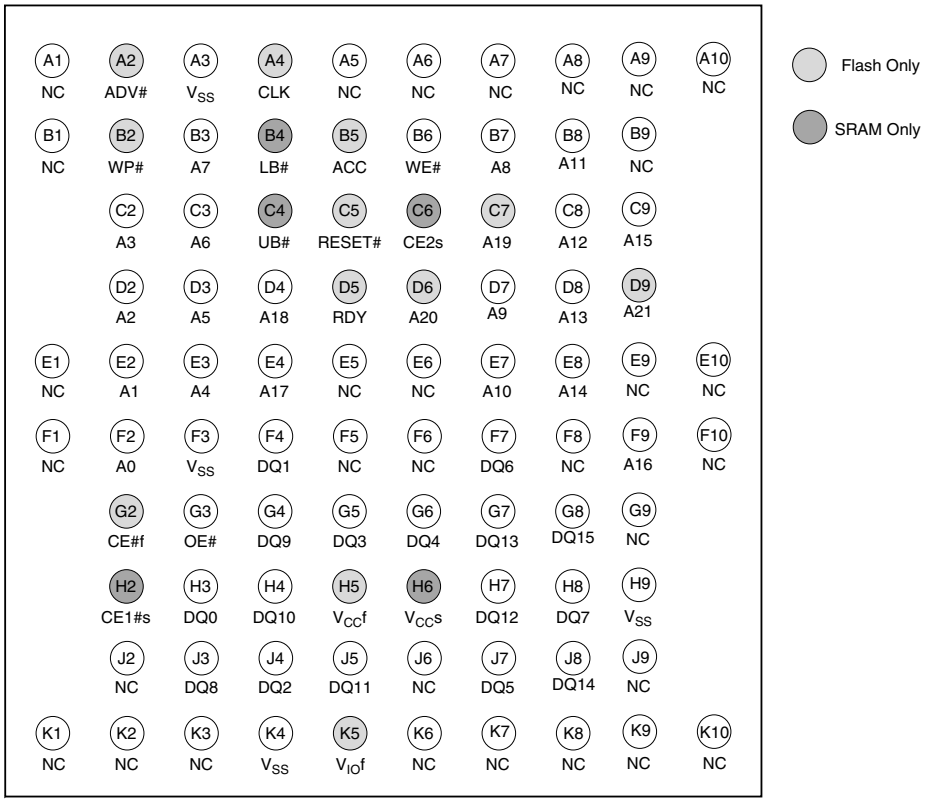


BLOCK DIAGRAM OF SIMULTANEOUS OPERATION CIRCUIT



CONNECTION DIAGRAM

89-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



Special Handling Instructions for FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN DESCRIPTION

A18–A0 = 19 Address Inputs (Common)

A21–A19 = 3 Address Inputs (Flash)

DQ15–DQ0 = 16 Data Inputs/Outputs (Common)

CE#f = Chip Enable (Flash)

CE1#s = Chip Enable 1 (SRAM)

CE2s = Chip Enable 2 (SRAM)

OE# = Output Enable (Common)

WE# = Write Enable (Common)

UB#s = Upper Byte Control (SRAM)

LB#s = Lower Byte Control (SRAM)

RESET# = Hardware Reset Pin, Active Low

V_{CC}f = Flash 1.8 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)

V_{IO}f = Input & Output Buffer Power Supply must be tied to V_{CC}.

V_{CC}s = SRAM Power Supply

V_{SSIO}f = Output Buffer Ground

V_{SS} = Device Ground (Common)

NC = Pin Not Connected Internally

RDY = Ready output; indicates the status of the Burst read. Low = data not valid at expected time. High = data valid.

CLK = CLK is not required in asynchronous mode. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter.

AVD# = Address Valid input. Indicates to device that the valid address is present on the address inputs (A21–A0).

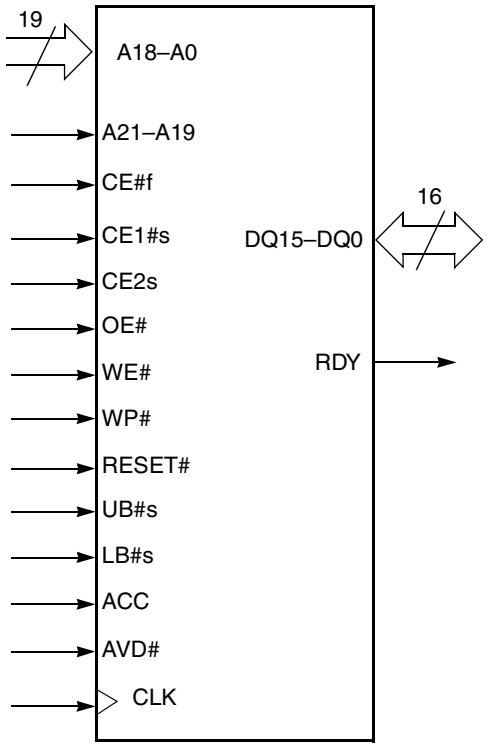
Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched.

High = device ignores address inputs

WP# = Hardware write protect input. At V_{IL}, disables program and erase functions in the two outermost sectors. Should be at V_{IH} for all other conditions.

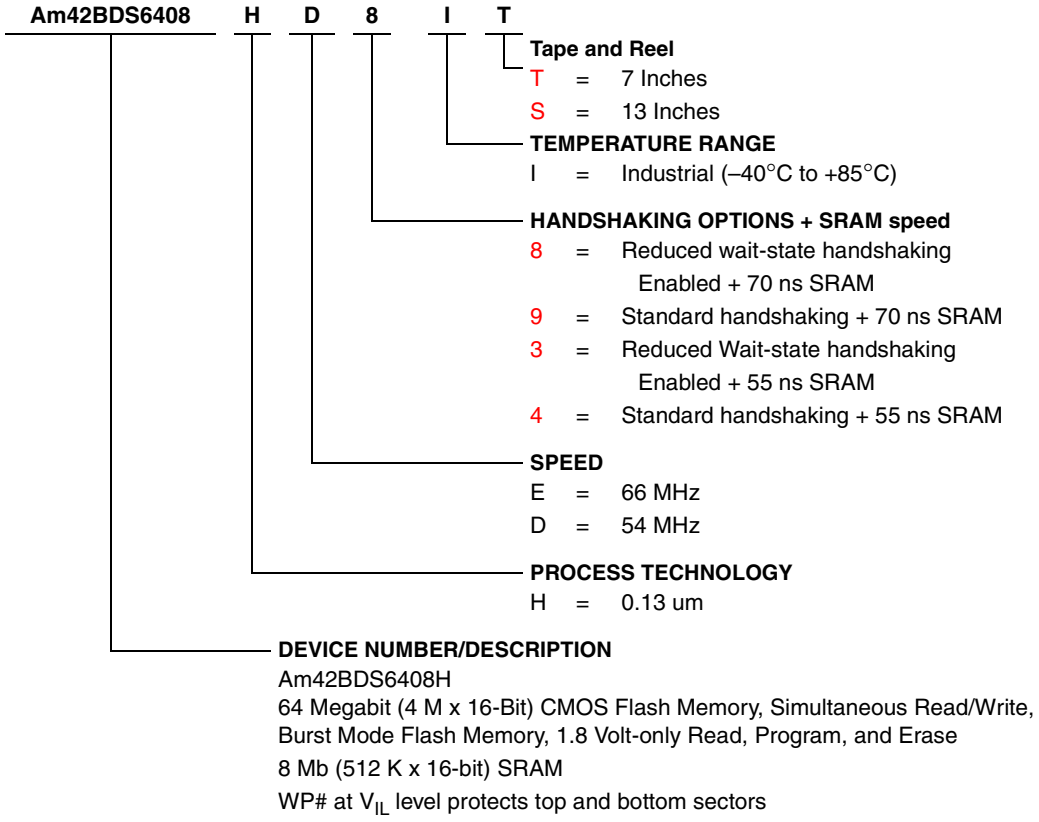
ACC = At V_{ID}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, locks all sectors. Should be at V_{IH} for all other conditions.

LOGIC SYMBOL



ORDERING INFORMATION

The order number (Valid Combination) is formed by the following:



Valid Combinations		Package Marking	Flash Burst Frequency (MHz)	SRAM Speed (ns)
Order Number				
Am42BDS6408HE8	I	M420000070	66	70
Am42BDS6408HE9		M420000071		
Am42BDS6408HD8		M420000072	54	
Am42BDS6408HD9		M420000073		
Am42BDS6408HE3		M420000074	66	55
Am42BDS6408HE4		M420000075		
Am42BDS6408HD3		M420000076	54	
Am42BDS6408HD4		M420000077		

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: *For the Am29BDS640H, the last digit of the speed grade specifies the V_{IO} range of the device. Speed options ending in "8" and "9" (e.g., D8, D9) indicate a 1.8 Volt V_{IO} range.*

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operations

Operation	CE#	OE#	WE#	A21–0	DQ15–0	RESET#	CLK (See Note)	AVD#
Asynchronous Read - Addresses Latched	L	L	H	Addr In	I/O	H	X	⌐↑
Asynchronous Read - Addresses Steady State	L	L	H	Addr In	I/O	H	X	L
Asynchronous Write	L	H	L	Addr In	I/O	H	X	L
Synchronous Write	L	H	L	Addr In	I/O	H	⌐↑	⌐↑
Standby (CE#)	H	X	X	HIGH Z	HIGH Z	H	X	X
Hardware Reset	X	X	X	HIGH Z	HIGH Z	L	X	X
Burst Read Operations								
Load Starting Burst Address	L	X	H	Addr In	X	H	↑	⌐
Advance Burst to next address with appropriate Data presented on the Data Bus	L	L	H	HIGH Z	Burst Data Out	H	↑	H
Terminate current Burst read cycle	H	X	H	HIGH Z	HIGH Z	H	↑	X
Terminate current Burst read cycle via RESET#	X	X	H	HIGH Z	HIGH Z	L	X	X
Terminate current Burst read cycle and start new Burst read cycle	L	X	H	HIGH Z	I/O	H	↑	⌐

Legend: *L = Logic 0, H = Logic 1, X = Don't Care, S = Stable Logic 0 or 1 but no transitions.*

Note: *Default active edge of CLK is the rising edge.*

VersatileIO™ (V_{IO}) Control

The VersatileIO™ (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{IO} pin.

Requirements for Asynchronous Read Operation (Non-Burst)

To read data from the memory array, the system must first assert a valid address on A21–A0, while driving AVD# and CE# to V_{IL}. WE# should remain at V_{IH}. The rising edge of AVD# latches the address. The data will appear on DQ15–DQ0. Since the memory array is divided into four banks, each bank remains enabled for read access until the command register contents are altered.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the outputs. The output enable access time (t_{OE}) is the delay from the falling edge of OE# to valid data at the output.

The internal state machine is set for reading array data in asynchronous mode upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

Requirements for Synchronous (Burst) Read Operation

The device is capable of continuous sequential burst operation and linear burst operation of a preset length.

When the device first powers up, it is enabled for asynchronous read operation.

Prior to entering burst mode, the system should determine how many wait states are desired for the initial word (t_{IACC}) of each burst access, what mode of burst operation is desired, which edge of the clock will be the active clock edge, and how the RDY signal will transition with valid data. The system would then write the configuration register command sequence. See "Set Configuration Register Command Sequence" section on page 30 and "Command Definitions" section on page 30 for further details.

Once the system has written the "Set Configuration Register" command sequence, the device is enabled for synchronous reads only.

The initial word is output t_{IACC} after the active edge of the first CLK cycle. Subsequent words are output t_{BACC} after the active edge of each successive clock cycle, which automatically increments the internal address counter. Note that the device has a fixed internal address boundary that occurs every 64 words, starting at address 00003Fh. During the time the device is outputting data at this fixed internal address boundary (address 00003Fh, 00007Fh, 0000BFh, etc.), a two cycle latency occurs before data appears for the next address (address 000040h, 000080h, 0000C0h, etc.). The RDY output indicates this condition to the system by pulsing low. For standard handshaking devices, there is no two cycle latency between 3Fh and 40h (or offset from these values by a multiple of 64) if the latched address was 3Eh or 3Fh (or offset from these values by a multiple of 64). See Figure 43, "Latency with Boundary Crossing," on page 76.

For reduced wait-state handshaking devices, if the address latched is 3Eh or 3Fh (or offset from these values by a multiple of 64) two additional cycle latency occurs prior to the initial access and the two cycle latency between 3Fh and 40h (or offset from these values by a multiple of 64) will not occur.

The device will continue to output sequential burst data, wrapping around to address 000000h after it reaches the highest addressable memory location, until the system drives CE# high, RESET# low, or AVD# low in conjunction with a new address. See Table 1, "Device Bus Operations," on page 12.

If the host system crosses the bank boundary while reading in burst mode, and the device is not programming or erasing, a two-cycle latency will occur as described above in the subsequent bank. If the host system crosses the bank boundary while the device is programming or erasing, the device will provide read status information. The clock will be ignored. After the host has completed status reads, or the device has completed the program or erase operation, the host can restart a burst operation using a new address and AVD# pulse.

If the clock frequency is less than 6 MHz during a burst mode operation, additional latencies will occur. RDY indicates the length of the latency by pulsing low.

8-, 16-, and 32-Word Linear Burst with Wrap Around

The remaining three modes are of the linear wrap around design, in which a fixed number of words are read from consecutive addresses. In each of these modes, the burst addresses read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode (see Table 2.)

Table 2. Burst Address Groups

Mode	Group Size	Group Address Ranges
8-word	8 words	0-7h, 8-Fh, 10-17h,...
16-word	16 words	0-Fh, 10-1Fh, 20-2Fh,...
32-word	32 words	00-1Fh, 20-3Fh, 40-5Fh,...

As an example: if the starting address in the 8-word mode is 39h, the address range to be read would be 38-3Fh, and the burst sequence would be 39-3A-3B-3C-3D-3E-3F-38h-etc. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group. In a similar fashion, the 16-word and 32-word Linear Wrap modes begin their burst sequence on the starting address written to the device, and then wrap back to the first address in the selected address group. **Note that in these three burst read modes the address pointer does not cross the boundary that occurs every 64 words; thus, no wait states are inserted (except during the initial access).**

The RDY pin indicates when data is valid on the bus. The devices can wrap through a maximum of 128 words of data (8 words up to 16 times, 16 words up to 8 times, or 32 words up to 4 times) before requiring a new synchronous access (latching of a new address).

Burst Suspend/Resume

The Burst Suspend/Resume feature allows the system to temporarily suspend a synchronous burst operation during the initial access (before data is available) or after the device is outputting data. When the burst operation is suspended, any previously latched internal data and the current state are retained.

Burst Suspend requires CE# to be asserted, WE# de-asserted, and the initial address latched by AVD# or the CLK edge. Burst Suspend occurs when OE# is de-asserted. See Figure 18, "Reduced Wait-state Handshake Burst Suspend/Resume at an even address," on page 57, Figure 19, "Reduced Wait-state Handshake Burst Suspend/Resume at an odd address," on page 57, Figure 20, "Reduced Wait-state

Handshake Burst Suspend/Resume at address 3Eh (or offset from 3Eh)," on page 58, Figure 21, "Reduced Wait-state Handshake Burst Suspend/Resume at address 3Fh (or offset from 3Fh by a multiple of 64)," on page 58, Figure 22, "Standard Handshake Burst Suspend prior to Initial Access," on page 59, Figure 23, "Standard Handshake Burst Suspend at or after Inital Access," on page 59, Figure 24, "Standard Handshake Burst Suspend at address 3Fh (starting address 3Dh or earlier)," on page 60, Figure 25, "Standard Handshake Burst Suspend at address 3Eh/3Fh (without a valid Initial Access)," on page 60, and Figure 26, "Standard Handshake Burst Suspend at address 3Eh/3Fh (with 1 Access CLK)," on page 61.

Burst plus Burst Suspend should not last longer than t_{RCC} without re-latching an address or crossing an address boundary. To resume the burst access, OE# must be re-asserted. The next active CLK edge will resume the burst sequence where it had been suspended. See, Figure 27, "Read Cycle for Continuous Suspend," on page 61.

The RDY pin is only controlled by CE#. RDY will remain active and is not placed into a high-impedance state when OE# is de-asserted.

Configuration Register

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, active clock edge, RDY configuration, and synchronous mode active.

Reduced Wait-state Handshaking Option

The device can be equipped with a reduced wait-state handshaking feature that allows the host system to simply monitor the RDY signal from the device to determine when the initial word of burst data is ready to be read. The host system should use the programmable wait state configuration to set the number of wait states for optimal burst mode operation. The initial word of burst data is indicated by the rising edge of RDY after OE# goes low.

The presence of the reduced wait-state handshaking feature may be verified by writing the autoselect command sequence to the device. See "Autoselect Command Sequence" for details.

For optimal burst mode performance on devices without the reduced wait-state handshaking option, the host system must set the appropriate number of wait states in the flash device depending on clock frequency and the presence of a boundary crossing. See "Set Configuration Register Command Sequence" section on page 30 section for more information. The device will automatically delay RDY and data by one additional clock cycle when the starting address is odd.

The autoselect function allows the host system to determine whether the flash device is enabled for reduced wait-state handshaking. See the "Autoselect Command Sequence" section for more information.

Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in another bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 46, "Back-to-Back Read/Write Cycle Timings," on page 79 shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the DC Characteristics table for read-while-program and read-while-erase current specifications.

Writing Commands/Command Sequences

The device has the capability of performing an asynchronous or synchronous write operation. While the device is configured in Asynchronous read it is able to perform Asynchronous write operations only. CLK is ignored in the Asynchronous programming mode. When in the Synchronous read mode configuration, the device is able to perform both Asynchronous and Synchronous write operations. CLK and WE# address latch is supported in the Synchronous programming mode. During a synchronous write operation, to write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive AVD# and CE# to V_{IL}, and OE# to V_{IH} when providing an address to the device, and drive WE# and CE# to V_{IL}, and OE# to V_{IH} when writing commands or data. During an asynchronous write operation, the system must drive CE# and WE# to V_{IL} and OE# to V_{IH} when providing an address, command, and data. Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE#. The asynchronous and synchronous programing operation is independent of the Set Device Read Mode bit in the Configuration Register (see Table 15, "Configuration Register," on page 33).

The device features an Unlock Bypass mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 10, "Sector Address Table," on page 26 indicates the address space that each sector occupies. The device address space is divided into four banks: Banks B and C contain only 32 Kword sectors, while Banks A and D contain both 4 Kword boot sectors in addition to 32 Kword sectors. A

"bank address" is the address bits required to uniquely select a bank. Similarly, a "sector address" is the address bits required to uniquely select a sector.

I_{CC2} in the "DC Characteristics" section on page 49 represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. ACC is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this input, the device automatically enters the aforementioned Unlock Bypass mode and uses the higher voltage on the input to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the ACC input returns the device to normal operation. Note that sectors must be unlocked prior to raising ACC to V_{HH}. *Note that the ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, the ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result*.

When at V_{IL}, ACC locks all sectors. ACC should be at V_{IH} for all other conditions.

Table 3. Am42BDS6408H Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector	A21–A12	Sector/ Sector Block Size
SA0	0000000000	4 Kwords
SA1	0000000001	4 Kwords
SA2	0000000010	4 Kwords
SA3	0000000011	4 Kwords
SA4	0000000100	4 Kwords
SA5	0000000101	4 Kwords
SA6	0000000110	4 Kwords
SA7	0000000111	4 Kwords
SA8	0000001XXX	32 Kwords
SA9	0000010XXX	32 Kwords
SA10	0000011XXX	32 Kwords
SA11–SA14	00001XXXXX	128 (4x32) Kwords
SA15–SA18	00010XXXXX	128 (4x32) Kwords
SA19–SA22	00011XXXXX	128 (4x32) Kwords
SA23-SA26	00100XXXXX	128 (4x32) Kwords
SA27-SA30	00101XXXXX	128 (4x32) Kwords
SA31-SA34	00110XXXXX	128 (4x32) Kwords
SA35-SA38	00111XXXXX	128 (4x32) Kwords
SA39-SA42	01000XXXXX	128 (4x32) Kwords
SA43-SA46	01001XXXXX	128 (4x32) Kwords
SA47-SA50	01010XXXXX	128 (4x32) Kwords
SA51–SA54	01011XXXXX	128 (4x32) Kwords
SA55–SA58	01100XXXXX	128 (4x32) Kwords
SA59–SA62	01101XXXXX	128 (4x32) Kwords
SA63–SA66	01110XXXXX	128 (4x32) Kwords
SA67–SA70	01111XXXXX	128 (4x32) Kwords
SA71–SA74	10000XXXXX	128 (4x32) Kwords
SA75–SA78	10001XXXXX	128 (4x32) Kwords
SA79–SA82	10010XXXXX	128 (4x32) Kwords
SA83–SA86	10011XXXXX	128 (4x32) Kwords
SA87–SA90	10100XXXXX	128 (4x32) Kwords
SA91–SA94	10101XXXXX	128 (4x32) Kwords
SA95–SA98	10110XXXXX	128 (4x32) Kwords
SA99–SA102	10111XXXXX	128 (4x32) Kwords
SA103–SA106	11000XXXXX	128 (4x32) Kwords
SA107–SA110	11001XXXXX	128 (4x32) Kwords
SA111–SA114	11010XXXXX	128 (4x32) Kwords
SA115–SA118	11011XXXXX	128 (4x32) Kwords
SA119–SA122	11100XXXXX	128 (4x32) Kwords
SA123–SA126	11101XXXXX	128 (4x32) Kwords
SA127–SA130	11110XXXXX	128 (4x32) Kwords
SA131	1111100XXX	32 Kwords
SA132	1111101XXX	32 Kwords
SA133	1111110XXX	32 Kwords
SA134	1111111000	4 Kwords
SA135	1111111001	4 Kwords
SA136	1111111010	4 Kwords
SA137	1111111011	4 Kwords
SA138	1111111100	4 Kwords
SA139	1111111101	4 Kwords
SA140	1111111110	4 Kwords
SA141	1111111111	4 Kwords

Sector/Sector Block Protection and Unprotection

The hardware sector protection feature disables both programming and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection can be implemented via two methods.

(Note: For the following discussion, the term “sector” applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Table 3, “Am42BDS6408H Boot Sector/Sector Block Addresses for Protection/Unprotection,” on page 16

Sector Protection

The Am42BDS6408H features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

Persistent Sector Protection

A command sector protection method that replaces the old 12 V controlled protection method.

Password Sector Protection

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted

WP# Hardware Protection

A write protect pin that can prevent program or erase operations in the outermost sectors.

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

Selecting a Sector Protection Mode

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used. If the customer decides to continue using the Persistent Sector Protection method, they must set the **Persistent Sector Protection Mode Locking Bit**. This will permanently set the part to op-

erate only using Persistent Sector Protection. If the customer decides to use the password method, they must set the **Password Mode Locking Bit**. This will permanently set the part to operate only using password sector protection.

It is important to remember that setting either the **Persistent Sector Protection Mode Locking Bit** or the **Password Mode Locking Bit** permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit has been set. **It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone.** This is so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at the factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See "Autoselect Command Sequence" section on page 33 for details.

Persistent Sector Protection

The Persistent Sector Protection method replaces the old 12 V controlled protection method while at the same time enhancing flexibility by providing three different sector protection states:

- **Persistently Locked**—A sector is protected and cannot be changed.
- **Dynamically Locked**—The sector is protected and can be changed by a simple command
- **Unlocked**—The sector is unprotected and can be changed by a simple command

In order to achieve these states, three types of "bits" are going to be used:

Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to a maximum four sectors ("Am42BDS6408H Boot Sector/Sector Block Addresses for Protection/Unprotection" section on page 16). All 4 Kbyte boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility. Each PPB is individually modifiable through the **PPB Program Command**.

Note: If a PPB requires erasure, all of the sector PPBs must first be preprogrammed prior to PPB erasing. All PPBs erase in parallel, unlike programming where individual PPBs are programmable. It is the responsibility of the user to perform the preprogramming operation. Otherwise, an already erased sector PPBs has the potential of being over-erased. There is no hardware mechanism to prevent sector PPBs over-erasure.

Persistent Protection Bit Lock (PPB Lock)

A global volatile bit. When set to "1", the PPBs cannot be changed. When cleared ("0"), the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

Dynamic Protection Bit (DYB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYBs is "0". Each DYB is individually modifiable through the DYB Write Command.

When the parts are first shipped, the PPBs are cleared. The DYBs and PPB Lock are defaulted to power up in the cleared state – meaning the PPBs are changeable.

When the device is first powered on the DYBs power up cleared (sectors not protected). The Protection State for each sector is determined by the logical OR of the PPB and the DYB related to that sector. For the sectors that have the PPBs cleared, the DYBs control whether or not the sector is protected or unprotected. By issuing the DYB Write command sequences, the DYBs will be set or cleared, thus placing each sector in the protected or unprotected state. These are the so-called **Dynamic Locked or Unlocked** states. They are called dynamic states because it is very easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DYBs maybe set or cleared as often as needed.

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles because they are Non-Volatile. Individual PPBs are set with a command but must all be cleared as a group through a complex sequence of program and erasing commands. The PPBs are also limited to 100 erase cycles.

The PBB Lock bit adds an additional level of protection. Once all PPBs are programmed to the desired settings, the PPB Lock may be set to "1". Setting the PPB Lock disables all program and erase commands to the Non-Volatile PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle. System boot code can determine if any changes to the

PPB are needed e.g. to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock to disable any further changes to the PPBs during system operation.

The WP# write protect pin adds a final level of hardware protection to the four highest and four lowest 4 Kbyte sectors (SA0 - SA3, SA138 - SA141 for a dual boot). When this pin is low it is not possible to change the contents of these four sectors. These sectors generally hold system boot code. So, the WP# pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Write command sequence is all that is necessary. The DYB write command for the dynamic sectors switch the DYBs to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock bit must be disabled by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB lock bit once again will lock the PPBs, and the device operates normally again.

Note: to achieve the best protection, it's recommended to execute the PPB lock bit set command early in the boot code, and protect the boot code by holding WP# = V_{IL}.

Table 4. Sector Protection Schemes

DYB	PPB	PPB Lock	Sector State
0	0	0	Unprotected—PPB and DYB are changeable
0	0	1	Unprotected—PPB not changeable, DYB is changeable
0	1	0	Protected—PPB and DYB are changeable
1	0	0	
1	1	0	
0	1	1	Protected—PPB not changeable, DYB is changeable
1	0	1	
1	1	1	

Table 4 contains all possible combinations of the DYB, PPB, and PPB lock relating to the status of the sector.

In summary, if the PPB is set, and the PPB lock is set, the sector is protected and the protection can not be removed until the next power cycle clears the PPB lock. If the PPB is cleared, the sector can be dynamically locked or unlocked. The DYB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs after which the device returns to read mode without having erased the protected sector.

The programming of the DYB, PPB, and PPB lock for a given sector can be verified by writing a DYB/PPB/PPB lock verify command to the device.

Persistent Sector Protection Mode Locking Bit

Like the password mode locking bit, a Persistent Sector Protection mode locking bit exists to guarantee that the device remain in software sector protection. Once set, the Persistent Sector Protection locking bit prevents programming of the password protection mode locking bit. This guarantees that a hacker could not place the device in password protection mode.

Password Protection Mode

The Password Sector Protection Mode method allows an even higher level of security than the Persistent Sector Protection Mode. There are two main differences between the Persistent Sector Protection and the Password Sector Protection Mode:

- When the device is first powered on, or comes out of a reset cycle, the PPB Lock bit is set to the **locked state**, rather than cleared to the unlocked state.
- The only means to clear the PPB Lock bit is by writing a unique **64-bit Password** to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

The password is stored in a **one-time programmable (OTP)** region of the flash memory. Once the Password Mode Locking Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear the PPB Lock bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-pro-

grammed password. If they match, the PPB Lock bit is cleared, and the PPBs can be altered. If they do not match, the flash device does nothing. There is a built-in 2 µs delay for each "password check." This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

Password and Password Mode Locking Bit

In order to select the Password sector protection scheme, the customer must first program the password. AMD recommends that the password be somehow correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

1. It permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.
2. It also disables *all further commands* to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Locking Bit, there will be no way to clear the PPB Lock bit.

The Password Mode Locking Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Mode Locking Bit is not erasable. Once Password Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands (see "Password Program Command" section on page 37 and "Password Verify Command" section on page 37). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

Persistent Protection Bit Lock

The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Lock Bit is also set, after a hardware reset (RESET# asserted) or a power-up reset the ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a "1".

If the Password Mode Locking Bit is not set, including Persistent Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is set by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

High Voltage Sector Protection

Sector protection and unprotection may also be implemented using programming equipment. The procedure requires high voltage (V_{ID}) to be placed on the RESET# pin. Refer to Figure 2, "In-System Sector Protection/ Sector Unprotection Algorithms," on page 21 for details on this procedure. Note that for sector unprotect, all unprotected sectors must be first protected prior to the first sector write cycle. Once the Password Mode Locking bit or Persistent Protection Locking bit are set, the high voltage sector protect/unprotect capability is disabled.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# inputs are both held at $V_{CC} \pm 0.2$ V. The device requires standard access time (t_{CE}) for read access, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the "DC Characteristics" section on page 49 represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. While in asynchronous mode, the device automatically enables this mode when addresses remain stable for t_{ACC} + 60 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. While in synchronous mode, the device automatically enables this mode when either the first active CLK level is greater than t_{ACC} or the CLK runs slower than 5 MHz. Note that a new burst operation is required to provide new data.

I_{CC6} in the "DC Characteristics" section on page 49 represents the automatic sleep mode current specification.

RESET#: Hardware Reset Input

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, resets the configuration register, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.2$ V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.2$ V, the standby current will be greater.

RESET# may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

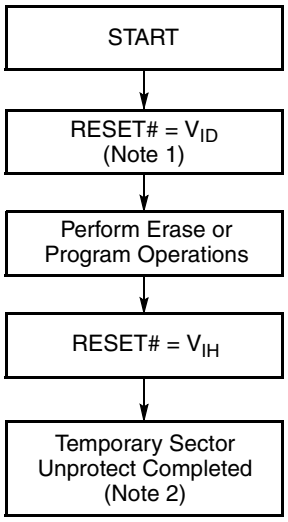
If RESET# is asserted during a program or erase operation, the device requires a time of t_{READY} (during Embedded Algorithms) before the device is ready to read data again. If RESET# is asserted when a program or erase operation is not executing, the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after RESET# returns to V_{IH}.

Refer to the "AC Characteristics" section on page 64 for RESET# parameters and to Figure 30, "Reset Timings," on page 64 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state.

Figure 1. Temporary Sector Unprotect Operation



Notes:

1. *All protected sectors unprotected (If WP# = V_{IL}, outermost boot sectors will remain protected).*
2. *All previously protected sectors are protected once again.*

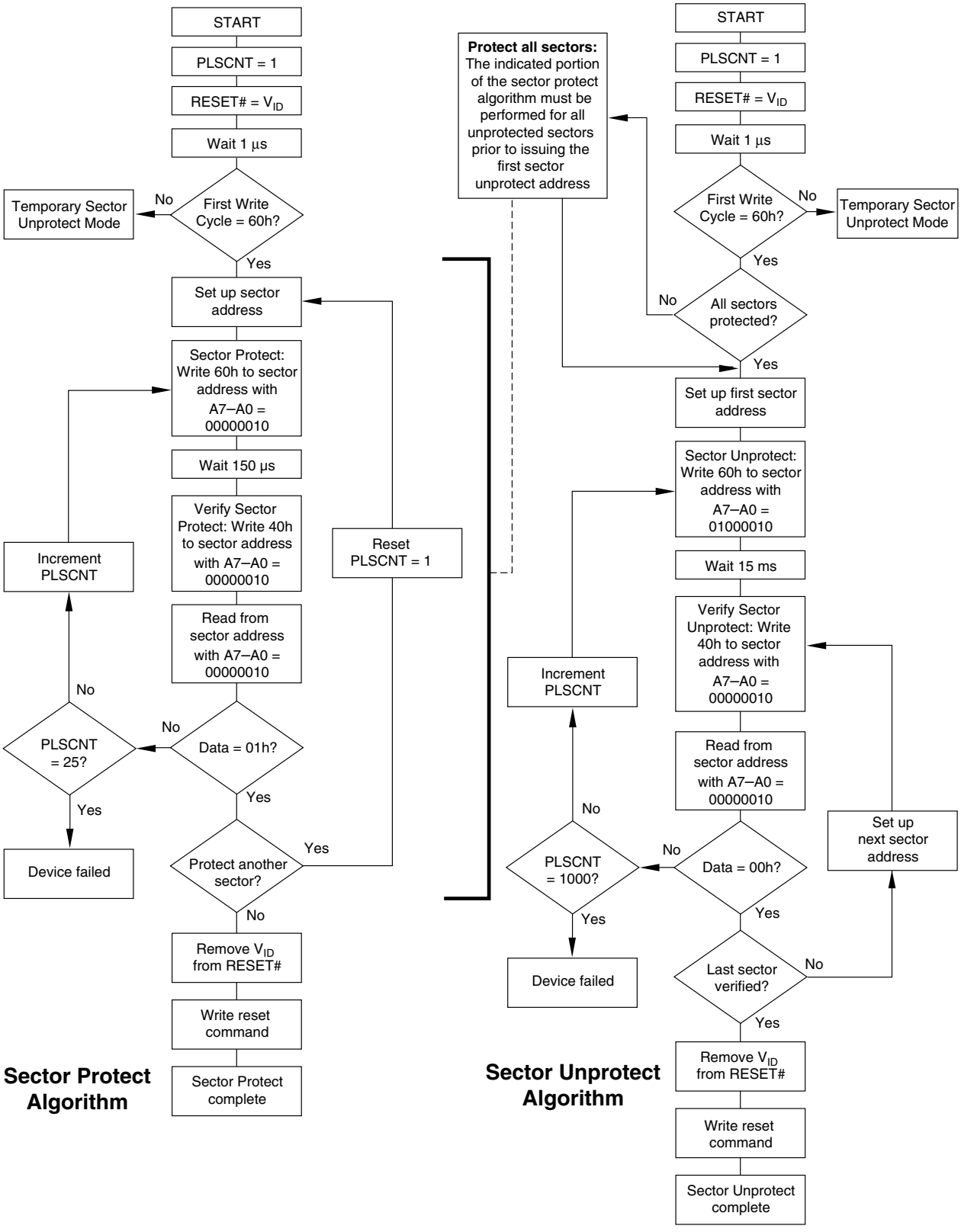


Figure 2. In-System Sector Protection/ Sector Unprotection Algorithms

SecSi™ (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN) The 128-word SecSi sector is divided into 64 factory-lockable words that can be programmed and locked by the customer. The SecSi sector is located at addresses 000000h-00007Fh in both Persistent Protection mode and Password Protection mode. It uses indicator bits (DQ6, DQ7) to indicate the factory-locked and customer-locked status of the part.

The system accesses the SecSi Sector through a command sequence (see "Enter SecSi™ Sector/Exit SecSi Sector Command Sequence"). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space.

Factory-Locked Area (64 words)

The factory-locked area of the SecSi Sector (000000h-00003Fh) is locked when the part is shipped, whether or not the area was programmed at the factory. The SecSi Sector Factory-locked Indicator Bit (DQ7) is permanently set to a "1". AMD offers the ExpressFlash service to program the factory-locked area with a random ESN, a customer-defined code, or any combination of the two. Because only AMD can program and protect the factory-locked area, this method ensures the security of the ESN once the product is shipped to the field. Contact an AMD representative for details on using AMD's ExpressFlash service.

Table 5. SecSi™ Sector Addresses

	Sector Size	Address Range
Am42BDS6408H	128 words	000000h–00007Fh
Factory-Locked Area	64 words	000000h-00003Fh
Customer-Lockable Area	64 words	000040h-00007Fh

Customer-Lockable Area (64 words)

The customer-lockable area of the SecSi Sector (000040h-00007Fh) is shipped unprotected, which allows the customer to program and optionally lock the area as appropriate for the application. The SecSi Sector Customer-locked Indicator Bit (DQ6) is shipped as "0" and can be permanently locked to "1" by issuing the SecSi Protection Bit Program Command. The SecSi Sector can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the SecSi Sector.

The Customer-lockable SecSi Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter SecSi Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the SecSi Sector Region without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.
- Write the three-cycle Enter SecSi Sector Secure Region command sequence, and then use the alternate method of sector protection described in the High Voltage Sector Protection section.

Once the SecSi Sector is locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing the remainder of the array.

The SecSi Sector lock must be used with caution since, once locked, there is no procedure available for unlocking the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

SecSi Sector Protection Bits

The SecSi Sector Protection Bits prevent programming of the SecSi Sector memory area. Once set, the SecSi Sector memory area contents are non-modifiable.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 16, "Command Definitions," on page 40 for command definitions).

The device offers two types of data protection at the sector level:

- The PPB and DYB associated command sequences disables or re-enables both program and erase operations in any sector or sector group.
- When WP# is at V_{IL}, the four outermost sectors are locked.
- When ACC is at V_{IL}, all sectors are locked.

The following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting the four outermost sectors. This function is provided by the WP# pin and overrides the previously discussed Sector Protection/Unprotection method.

If the system asserts V_{IL} on the WP# pin, the device disables program and erase functions in the eight "outermost" 4 Kword boot sectors.

If the system asserts V_{IH} on the WP# pin, the device reverts to whether sectors 0–3 and 138–141 were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected using the method described in "PPB Program Command" section on page 38.

Note that the WP# pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = RESET# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 6-9. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 6-9. The system must write the reset command to return the device to the autoselect mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the AMD site at the following URL:
http://www.amd.com/flash/cfi.

Alternatively, contact an AMD representative for copies

Table 6. CFI Query Identification String

Addresses	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string "QRY"
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 7. System Interface String

Addresses	Data	Description
1Bh	0017h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0019h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0004h	Typical timeout per single byte/word write 2^N µs
20h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	0009h	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0004h	Max. timeout for byte/word write 2^N times typical
24h	0000h	Max. timeout for buffer write 2^N times typical
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 8. Device Geometry Definition

Addresses	Data	Description
27h	0017h	Device Size = 2^N byte
28h 29h	0001h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0000h 0000h	Max. number of bytes in multi-byte write = 2^N (00h = not supported)
2Ch	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	007Dh 0000h 0000h 0001h	Erase Block Region 2 Information
35h 36h 37h 38h	0007h 0000h 0020h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information

Table 9. Primary Vendor-Specific Extended Query

Addresses	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	0031h	Major version number, ASCII
44h	0033h	Minor version number, ASCII
45h	000Ch	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Technology (Bits 5-2) 0011 = 0.13 µm
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0000h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0007h	Sector Protect/Unprotect scheme 07 = Advanced Sector Protection
4Ah	0077h	Simultaneous Operation Number of Sectors in all banks except boot block
4Bh	0001h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page, 04 = 16 Word Page
4Dh	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0001h	Top/Bottom Boot Sector Flag 01h = Dual Boot Device, 02h = Bottom Boot Device, 03h = Top Boot Device
50h	0000h	Program Suspend. 00h = not supported
57h	0004h	Bank Organization: X = Number of banks
58h	0017h	Bank A Region Information. X = Number of sectors in bank
59h	0030h	Bank B Region Information. X = Number of sectors in bank
5Ah	0030h	Bank C Region Information. X = Number of sectors in bank
5Bh	0017h	Bank D Region Information. X = Number of sectors in bank

Table 10. Sector Address Table

Bank	Sector	Sector Size	Address Range
Bank D	SA0	4 Kwords	000000h-000FFFh
	SA1	4 Kwords	001000h-001FFFh
	SA2	4 Kwords	002000h-002FFFh
	SA3	4 Kwords	003000h-003FFFh
	SA4	4 Kwords	004000h-004FFFh
	SA5	4 Kwords	005000h-005FFFh
	SA6	4 Kwords	006000h-006FFFh
	SA7	4 Kwords	007000h-007FFFh
	SA8	32 Kwords	008000h-00FFFFh
	SA9	32 Kwords	010000h-017FFFh
	SA10	32 Kwords	018000h-01FFFFh
	SA11	32 Kwords	020000h-027FFFh
	SA12	32 Kwords	028000h-02FFFFh
	SA13	32 Kwords	030000h-037FFFh
	SA14	32 Kwords	038000h-03FFFFh
	SA15	32 Kwords	040000h-047FFFh
	SA16	32 Kwords	048000h-04FFFFh
	SA17	32 Kwords	050000h-057FFFh
	SA18	32 Kwords	058000h-05FFFFh
	SA19	32 Kwords	060000h-067FFFh
	SA20	32 Kwords	068000h-06FFFFh
	SA21	32 Kwords	070000h-077FFFh
	SA22	32 Kwords	078000h-07FFFFh
Bank C	SA23	32 Kwords	080000h-087FFFh
	SA24	32 Kwords	088000h-08FFFFh
	SA25	32 Kwords	090000h-097FFFh
	SA26	32 Kwords	098000h-09FFFFh
	SA27	32 Kwords	0A0000h-0A7FFFh
	SA28	32 Kwords	0A8000h-0AFFFFh
	SA29	32 Kwords	0B0000h-0B7FFFh
	SA30	32 Kwords	0B8000h-0BFFFFh
	SA31	32 Kwords	0C0000h-0C7FFFh
	SA32	32 Kwords	0C8000h-0CFFFFh
	SA33	32 Kwords	0D0000h-0D7FFFh
	SA34	32 Kwords	0D8000h-0DFFFFh
	SA35	32 Kwords	0E0000h-0E7FFFh
	SA36	32 Kwords	0E8000h-0EFFFFh
	SA37	32 Kwords	0F0000h-0F7FFFh
	SA38	32 Kwords	0F8000h-0FFFFFh

Bank	Sector	Sector Size	Address Range
Bank C	SA39	32 Kwords	100000h-107FFFh
	SA40	32 Kwords	108000h-10FFFFh
	SA41	32 Kwords	110000h-117FFFh
	SA42	32 Kwords	118000h-11FFFFh
	SA43	32 Kwords	120000h-127FFFh
	SA44	32 Kwords	128000h-12FFFFh
	SA45	32 Kwords	130000h-137FFFh
	SA46	32 Kwords	138000h-13FFFFh
	SA47	32 Kwords	140000h-147FFFh
	SA48	32 Kwords	148000h-14FFFFh
	SA49	32 Kwords	150000h-157FFFh
	SA50	32 Kwords	158000h-15FFFFh
	SA51	32 Kwords	160000h-167FFFh
	SA52	32 Kwords	168000h-16FFFFh
	SA53	32 Kwords	170000h-177FFFh
	SA54	32 Kwords	178000h-17FFFFh
	SA55	32 Kwords	180000h-187FFFh
	SA56	32 Kwords	188000h-18FFFFh
	SA57	32 Kwords	190000h-197FFFh
	SA58	32 Kwords	198000h-19FFFFh
	SA59	32 Kwords	1A0000h-1A7FFFh
	SA60	32 Kwords	1A8000h-1AFFFFh
	SA61	32 Kwords	1B0000h-1B7FFFh
	SA62	32 Kwords	1B8000h-1BFFFFh
	SA63	32 Kwords	1C0000h-1C7FFFh
	SA64	32 Kwords	1C8000h-1CFFFFh
	SA65	32 Kwords	1D0000h-1D7FFFh
	SA66	32 Kwords	1D8000h-1DFFFFh
	SA67	32 Kwords	1E0000h-1E7FFFh
	SA68	32 Kwords	1E8000h-1EFFFFh
	SA69	32 Kwords	1F0000h-1F7FFFh
	SA70	32 Kwords	1F8000h-1FFFFFh

Bank	Sector	Sector Size	Address Range
Bank B	SA71	32 Kwords	200000h-207FFFh
	SA72	32 Kwords	208000h-20FFFFh
	SA73	32 Kwords	210000h-217FFFh
	SA74	32 Kwords	218000h-21FFFFh
	SA75	32 Kwords	220000h-227FFFh
	SA76	32 Kwords	228000h-22FFFFh
	SA77	32 Kwords	230000h-237FFFh
	SA78	32 Kwords	238000h-23FFFFh
	SA79	32 Kwords	240000h-247FFFh
	SA80	32 Kwords	248000h-24FFFFh
	SA81	32 Kwords	250000h-257FFFh
	SA82	32 Kwords	258000h-25FFFFh
	SA83	32 Kwords	260000h-267FFFh
	SA84	32 Kwords	268000h-26FFFFh
	SA85	32 Kwords	270000h-277FFFh
	SA86	32 Kwords	278000h-27FFFFh
	SA87	32 Kwords	280000h-287FFFh
	SA88	32 Kwords	288000h-28FFFFh
	SA89	32 Kwords	290000h-297FFFh
	SA90	32 Kwords	298000h-29FFFFh
	SA91	32 Kwords	2A0000h-2A7FFFh
	SA92	32 Kwords	2A8000h-2AFFFFh
	SA93	32 Kwords	2B0000h-2B7FFFh
	SA94	32 Kwords	2B8000h-2BFFFFh
	SA95	32 Kwords	2C0000h-2C7FFFh
	SA96	32 Kwords	2C8000h-2CFFFFh
	SA97	32 Kwords	2D0000h-2D7FFFh
	SA98	32 Kwords	2D8000h-2DFFFFh
	SA99	32 Kwords	2E0000h-2E7FFFh
	SA100	32 Kwords	2E8000h-2EFFFFh
	SA101	32 Kwords	2F0000h-2F7FFFh
	SA102	32 Kwords	2F8000h-2FFFFFh

Bank	Sector	Sector Size	Address Range
Bank B	SA103	32 Kwords	300000h-307FFFh
	SA104	32 Kwords	308000h-30FFFFh
	SA105	32 Kwords	310000h-317FFFh
	SA106	32 Kwords	318000h-31FFFFh
	SA107	32 Kwords	320000h-327FFFh
	SA108	32 Kwords	328000h-32FFFFh
	SA109	32 Kwords	330000h-337FFFh
	SA110	32 Kwords	338000h-33FFFFh
	SA111	32 Kwords	340000h-347FFFh
	SA112	32 Kwords	348000h-34FFFFh
	SA113	32 Kwords	350000h-357FFFh
	SA114	32 Kwords	358000h-35FFFFh
	SA115	32 Kwords	360000h-367FFFh
	SA116	32 Kwords	368000h-36FFFFh
	SA117	32 Kwords	370000h-377FFFh
	SA118	32 Kwords	378000h-37FFFFh
Bank A	SA119	32 Kwords	380000h-387FFFh
	SA120	32 Kwords	388000h-38FFFFh
	SA121	32 Kwords	390000h-397FFFh
	SA122	32 Kwords	398000h-39FFFFh
	SA123	32 Kwords	3A0000h-3A7FFFh
	SA124	32 Kwords	3A8000h-3AFFFFh
	SA125	32 Kwords	3B0000h-3B7FFFh
	SA126	32 Kwords	3B8000h-3BFFFFh
	SA127	32 Kwords	3C0000h-3C7FFFh
	SA128	32 Kwords	3C8000h-3CFFFFh
	SA129	32 Kwords	3D0000h-3D7FFFh
	SA130	32 Kwords	3D8000h-3DFFFFh
	SA131	32 Kwords	3E0000h-3E7FFFh
	SA132	32 Kwords	3E8000h-3EFFFFh
	SA133	32 Kwords	3F0000h-3F7FFFh
	SA134	4 Kwords	3F8000h-3F8FFFh
	SA135	4 Kwords	3F9000h-3F9FFFh
	SA136	4 Kwords	3FA000h-3FAFFFh
	SA137	4 Kwords	3FB000h-3FBFFFh
	SA138	4 Kwords	3FC000h-3FCFFFh
	SA139	4 Kwords	3FD000h-3FDFFFh
	SA140	4 Kwords	3FE000h-3FEFFFh
	SA141	4 Kwords	3FF000h-3FFFFFh

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 16, "Command Definitions," on page 40 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data in asynchronous mode. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. After completing a programming operation in the Erase Suspend mode, the system may once again read array data from any non-erase-suspended sector within the same bank. See the "Erase Suspend/Erase Resume Commands" section on page 36 for more information.

The system must issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the "Reset Command" section on page 33 for more information.

See also "Requirements for Asynchronous Read Operation (Non-Burst)" section on page 12 and "Requirements for Synchronous (Burst) Read Operation" section on page 12 for more information. The Asynchronous Read and Synchronous/Burst Read tables provide the read parameters, and Figure 13, "CLK Synchronous Burst Mode Read (rising active CLK)," on page 54, Figure 15, "Synchronous Burst Mode Read," on page 55, and Figure 28, "Asynchronous Mode Read with Latched Addresses," on page 63 show the timings.

Set Configuration Register Command Sequence

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, active clock edge, RDY configuration, and synchronous mode active. The configuration register must be set before the device will enter burst mode.

The configuration register is loaded with a three-cycle command sequence. The first two cycles are standard unlock sequences. On the third cycle, the data should be C0h, address bits A11–A0 should be 555h, and address bits A19–A12 set the code to be latched. The device will power up or after a hardware reset with the default setting, which is in asynchronous mode. The register must be set before the device can enter synchronous mode. The configuration register can not be changed during device operations (program, erase, or sector lock).

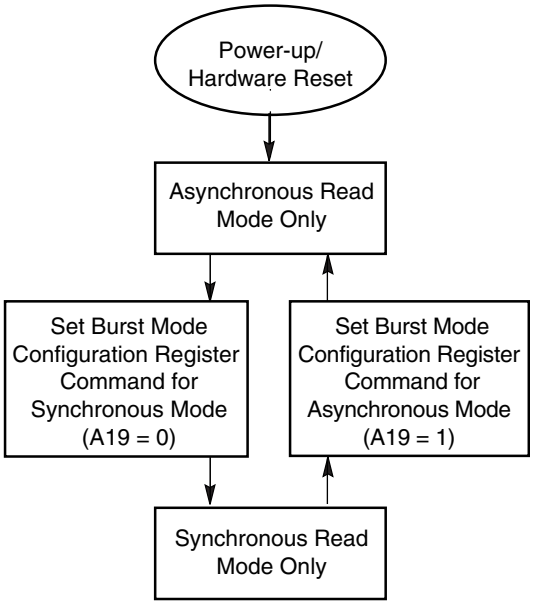


Figure 3. Synchronous/Asynchronous State Diagram

Read Mode Setting

On power-up or hardware reset, the device is set to be in asynchronous read mode. This setting allows the system to enable or disable burst mode during system operations. Address A19 determines this setting: "1" for asynchronous mode, "0" for synchronous mode.

Programmable Wait State Configuration

The programmable wait state feature informs the device of the number of clock cycles that must elapse after AVD# is driven active before data will be available. This value is determined by the input frequency of the device. Address bits A14–A12 determine the setting (see Table 11, "Programmable Wait State Settings," on page 31).

The wait state command sequence instructs the device to set a particular number of clock cycles for the initial access in burst mode. The number of wait states that should be programmed into the device is directly related to the clock frequency.

Table 11. Programmable Wait State Settings

A14	A13	A12	Total Initial Access Cycles
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	7 (default)
1	1	0	Reserved
1	1	1	Reserved

Notes:

1. *Upon power-up or hardware reset, the default setting is seven wait states.*
2. *RDY will default to being active with data when the Wait State Setting is set to a total initial access cycle of 2.*

It is recommended that the wait state command sequence be written, even if the default wait state value is desired, to ensure the device is set as expected. A hardware reset will set the wait state to the default setting.

Reduced Wait-state Handshaking Option

If the device is equipped with the reduced wait-state handshaking option, the host system should set address bits A14–A12 to 010 for the system/device to execute at maximum speed.

Table 12 describes the typical number of clock cycles (wait states) for various conditions.

Table 12. Wait States for Reduced wait-state Handshaking

V_{IO} = 1.8 V			
System Frequency Range	**Even Initial Address**	**Odd Initial Address**	**Device Speed Rating**
6–22 MHz	2	2	D (54 MHz)
22–28 MHz	2	3	
28–43 MHz	3	4	
43–54 MHz	4	5	
6–28 MHz	2	2	E (66 MHz)
28–35 MHz	2	3	
35–53 MHz	3	4	
53–66 MHz	4	5	

V_{IO} = 1.5 V			
System Frequency Range	**Even Initial Address**	**Odd Initial Address**	**Device Speed Rating**
6–18 MHz	2	2	D (54 MHz)
18–22 MHz	2	3	
22–33 MHz	3	4	
33–45 MHz	4	5	
45–54 MHz	5	6	
6–23 MHz	2	2	E (66 MHz)
23–28 MHz	2	3	
28–42 MHz	3	4	
42–56 MHz	4	5	
56–66 MHz	5	6	

Notes:

1. *If the latched address is 3Eh or 3Fh (or an address offset from either address by a multiple of 64), add two access cycles to the values listed.*
2. *In the 8-, 16-, and 32-word burst modes, the address pointer does not cross 64-word boundaries (3Fh, or addresses offset from 3Fh by a multiple of 64).*
3. *Typical initial access cycles may vary depending on system margin requirements.*

Standard Handshaking Option

For optimal burst mode performance on devices with the standard handshaking option, the host system must set the appropriate number of wait states in the flash device depending on the clock frequency.

Table 13 describes the typical number of clock cycles (wait states) for various conditions with A14-A12 set to 101.

Table 13. Wait States for Standard Handshaking

Conditions at Address	Typical No. of Clock Cycles after AVD# Low
Initial address	7
Initial address is 3E or 3Fh (or offset from these addresses by a multiple of 64) and is at boundary crossing*	7

** In the 8-, 16- and 32-word burst read modes, the address pointer does not cross 64-word boundaries (addresses which are multiples of 3Fh).*

The autoselect function allows the host system to determine whether the flash device is enabled for handshaking. See the "Autoselect Command Sequence" section on page 33 for more information.

Read Mode Configuration

The device supports four different read modes: continuous mode, and 8, 16, and 32 word linear wrap around modes. A continuous sequence begins at the starting address and advances the address pointer until the burst operation is complete. If the highest address in the device is reached during the continuous burst read mode, the address pointer wraps around to the lowest address.

For example, an eight-word linear read with wrap around begins on the starting address written to the device and then advances to the next 8 word boundary. The address pointer then returns to the 1st word after the previous eight word boundary, wrapping through the starting location. The sixteen- and thirty-two linear wrap around modes operate in a fashion similar to the eight-word mode.

Table 14 shows the address bits and settings for the four read modes.

Table 14. Read Mode Settings

Burst Modes	Address Bits	
	A16	A15
Continuous	0	0
8-word linear wrap around	0	1
16-word linear wrap around	1	0
32-word linear wrap around	1	1

Note: *Upon power-up or hardware reset the default setting is continuous.*

Burst Active Clock Edge Configuration

By default, the device will deliver data on the rising edge of the clock after the initial synchronous access time. Subsequent outputs will also be on the following rising edges, barring any delays. The device can be set so that the falling clock edge is active for all synchronous accesses. Address bit A17 determines this setting; "1" for rising active, "0" for falling active.

RDY Configuration

By default, the device is set so that the RDY pin will output V_{OH} whenever there is valid data on the outputs. The device can be set so that RDY goes active one data cycle before active data. Address bit A18 determines this setting; "1" for RDY active with data, "0" for RDY active one clock cycle before valid data. In asynchronous mode, RDY is an open-drain output.

Configuration Register

Table 15 shows the address bits that determine the configuration register settings for various device functions.

Table 15. Configuration Register

Address Bit	Function	Settings (Binary)
A19	Set Device Read Mode	0 = Synchronous Read (Burst Mode) Enabled 1 = Asynchronous Mode (default)
A18	RDY	0 = RDY active one clock cycle before data 1 = RDY active with data (default)
A17	Clock	0 = Burst starts and data is output on the falling edge of CLK 1 = Burst starts and data is output on the rising edge of CLK (default)
A16 A15	Read Mode	Synchronous Mode 00 = Continuous (default) 01 = 8-word linear with wrap around 10 = 16-word linear with wrap around 11 = 32-word linear with wrap around
A14 A13 A12	Programmable Wait State	000 = Data is valid on the 2th active CLK edge after AVD# transition to V_{IH} 001 = Data is valid on the 3th active CLK edge after AVD# transition to V_{IH} 010 = Data is valid on the 4th active CLK edge after AVD# transition to V_{IH} 011 = Data is valid on the 5th active CLK edge after AVD# transition to V_{IH} 100 = Data is valid on the 6th active CLK edge after AVD# transition to V_{IH} 101 = Data is valid on the 7th active CLK edge after AVD# transition to V_{IH} (default) 110 = Reserved 111 = Reserved

Note: *Device will be in the default state upon power-up or hardware reset.*

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins (prior to the third cycle). This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 16, "Command Definitions," on page 40 shows the address and data requirements. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. No subsequent data will be made available if the autoselect data is read in synchronous mode. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence. Read commands to other banks will return data from the array. The following table describes the address requirements for the various autoselect functions, and the resulting data. BA represents the bank address, and

SA represents the sector address. The device ID is read in three cycles.

Description	Address	Read Data
Manufacturer ID	(BA) + 00h	0001h
Device ID, Word 1	(BA) + 01h	227Eh
Device ID, Word 2	(BA) + 0Eh	221Eh
Device ID, Word 3	(BA) + 0Fh	2201h
Sector Protection Verification	(SA) + 02h	0001 (locked), 0000 (unlocked)
Indicator Bits	(BA) + 03h	DQ15 - DQ8 = 0 DQ7: Factory Lock Bit 1 = Locked, 0 = Not Locked DQ6: Customer Lock Bit 1 = Locked, 0 = Not Locked DQ5: Handshake Bit 1 = Reduced Wait-state Handshake, 0 = Standard Handshake

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

Enter SecSi™ Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. The SecSi Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Table 16, "Command Definitions," on page 40 shows the address and data requirements for both command sequences.

Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 16, "Command Definitions," on page 40 shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by monitoring DQ7 or DQ6/DQ2. Refer to the "Write Operation Status" section on page 43 for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from "0" back to a "1." Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bit to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

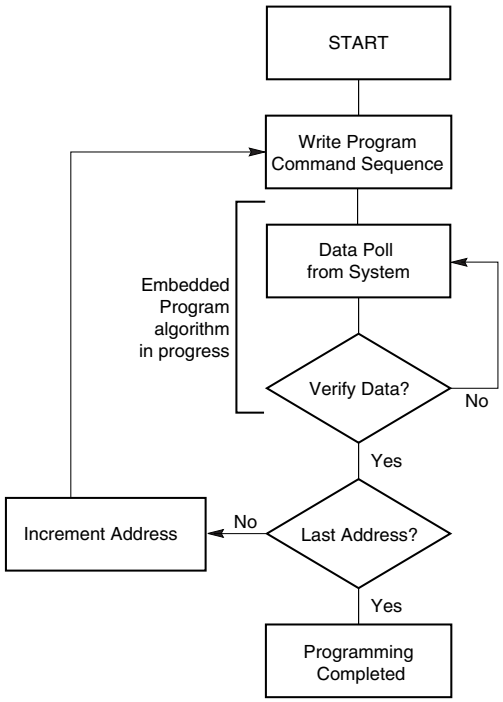
Unlock Bypass Command Sequence

The unlock bypass feature allows the system to primarily program to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. The host system may also initiate the chip erase and sector erase sequences in the unlock bypass mode. The erase command sequences are four cycles in length instead of six cycles. Table 16, "Command Definitions," on page 40 shows the requirements for the unlock bypass command sequences.

During the unlock bypass mode, only the Read, Unlock Bypass Program, Unlock Bypass Sector Erase, Unlock Bypass Chip Erase, and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need only contain the data 00h. The bank then returns to the read mode.

The device offers accelerated program operations through the ACC input. When the system asserts V_{HH} on this input, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the ACC input to accelerate the operation.

Figure 4, "Program Operation," on page 35 illustrates the algorithm for the program operation. Refer to the Erase/Program Operations table in the AC Characteristics section for parameters, and Figure 31, "Asynchronous Program Operation Timings: AVD# Latched Addresses," on page 66 and Figure 33, "Synchronous Program Operation Timings: WE# Latched Addresses," on page 68 for timing diagrams.



Note: *See Table 16 for program command sequence.*

Figure 4. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 16, "Command Definitions," on page 40 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6/DQ2. Refer to the "Write Operation Status" section on page 43 for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

The host system may also initiate the chip erase command sequence while the device is in the unlock bypass mode. The command sequence is two cycles cycles in length instead of six cycles. See Table 16, "Command Definitions," on page 40 for details on the unlock bypass command sequences.

Figure 5, "Erase Operation," on page 37 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations table in the AC Characteristics section for parameters and timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 16, "Command Definitions," on page 40 shows the address and data requirements for the sector erase command sequence.

The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of no less than 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted.

The interrupts can be re-enabled after the last Sector Erase command is written. Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode. The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See "DQ3: Sector Erase Timer" section on page 46.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7 or DQ6/DQ2 in the erasing bank. Refer to the "Write Operation Status" section on page 43 for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

The host system may also initiate the sector erase command sequence while the device is in the unlock bypass mode. The command sequence is four cycles cycles in length instead of six cycles.

Figure 5, "Erase Operation," on page 37 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations table in the Figure , "AC Characteristics," on page 65 for parameters and timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the minimum 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

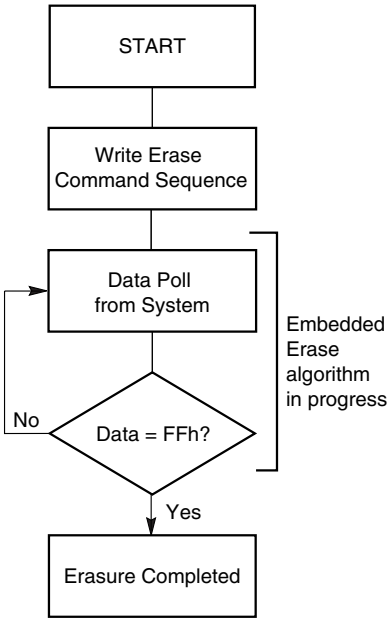
After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Figure , "Write Operation Status," on page 43 for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. Refer to the "Write Operation Status" section on page 43 for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the "Am42BDS6408H Boot Sector/Sector Block Addresses for Protection/Unprotection" section on page 16 and "Autoselect Command Sequence" section on page 33 for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command

are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



Notes:

1. *See Table 16 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 5. Erase Operation

Password Program Command

The Password Program Command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. 4 Password Program commands are required to program the password. The user must enter the unlock cycle, password program command (38h) and the program address/data for each portion of the password when programming. There are no provisions for entering the 2-cycle unlock cycle, the password program command, and all the password data. There is no special addressing order required for programming the password. Also, when the password is undergoing programming, Simultaneous Operation is disabled. Read operations to any memory location will return the programming status. Once programming is complete, the user must issue a Read/Reset command to return the device to normal operation. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent verification. The Password Program Command is only capable of programming “0”s. Programming a “1” after a cell is programmed as a “0” results in a time-out by the Embedded Program Algorithm™ with the cell remaining as a “0”. The password is all F’s when shipped from the factory. All 64-bit password combinations are valid as a password.

Password Verify Command

The Password Verify Command is used to verify the Password. The Password is verifiable only when the Password Mode Locking Bit is not programmed. If the Password Mode Locking Bit is programmed and the user attempts to verify the Password, the device will always drive all F’s onto the DQ data bus.

Also, the device will not operate in Simultaneous Operation when the Password Verify command is executed. Only the password is returned regardless of the bank address. The lower two address bits (A1–A0) are valid during the Password Verify. Writing the Read/Reset command returns the device back to normal operation.

Password Protection Mode Locking Bit Program Command

The Password Protection Mode Locking Bit Program Command programs the Password Protection Mode Locking Bit, which prevents further verifies or updates to the Password. When the Password Protection Mode Locking Bit is undergoing programming, Simultaneous Operation is disabled. Once programmed, the Password Protection Mode Locking Bit cannot be erased! If the Password Protection Mode Locking Bit is verified as program without margin, the Password Protection Mode Locking Bit Program command can be executed to improve the program margin. Once the Password Protection Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit program circuitry is disabled, thereby forcing the device to remain in the Password Protection mode. Exiting the Mode Locking Bit Program command is accomplished by writing the Read/Reset command.

Persistent Sector Protection Mode Locking Bit Program Command

The Persistent Sector Protection Mode Locking Bit Program Command programs the Persistent Sector Protection Mode Locking Bit, which prevents the Password Mode Locking Bit from ever being programmed. If the Persistent Sector Protection Mode Locking Bit is verified as programmed without margin, the Persistent Sector Protection Mode Locking Bit Program Command should be reissued to improve program margin. By disabling the program circuitry of the Password Mode Locking Bit, the device is forced to remain in the Persistent Sector Protection mode of operation, once this bit is set. Exiting the Persistent Protection Mode Locking Bit Program command is accomplished by writing the Read/Reset command. When the Persistent Sector Protection Mode Locking Bit is undergoing programming, Simultaneous Operation is disabled.

SecSi Sector Protection Bit Program Command

The SecSi Sector Protection Bit Program Command programs the SecSi Sector Protection Bit, which prevents the SecSi sector memory from being cleared. If the SecSi Sector Protection Bit is verified as programmed without margin, the SecSi Sector Protection Bit Program Command should be reissued to improve program margin. Exiting the V_{CC}-level SecSi Sector Protection Bit Program Command is accomplished by writing the Read/Reset command.

PPB Lock Bit Set Command

The PPB Lock Bit Set command is used to set the PPB Lock bit if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set, it cannot be cleared unless the device is taken through a power-on clear or the Password Unlock command is executed. Upon setting the PPB Lock Bit, the PPBs are latched into the DYBs. If the Password Mode Locking Bit is set, the PPB Lock Bit status is reflected as set, even after a power-on reset cycle. Exiting the PPB Lock Bit Set command is accomplished by writing the Read/Reset command, only while in the Persistent Sector Protection Mode.

DYB Write Command

The DYB Write command is used to set or clear a DYB for a given sector. The high order address bits (A21–A12) are issued at the same time as the code 01h or 00h on DQ7-DQ0. All other DQ data bus pins are ignored during the data write cycle. The DYBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. The DYBs are cleared at power-up or hardware reset. Exiting the DYB Write command is accomplished by writing the Read/Reset command.

Password Unlock Command

The Password Unlock command is used to clear the PPB Lock Bit so that the PPBs can be unlocked for modification, thereby allowing the PPBs to become accessible for modification. The exact password must be entered in order for the unlocking function to occur. This command cannot be issued any faster than 2 µs at a time to prevent a hacker from running through the all 64-bit combinations in an attempt to correctly match a password. If the command is issued before the 2 µs execution window for each portion of the unlock, the command will be ignored.

The Password Unlock function is accomplished by writing Password Unlock command and data to the device to perform the clearing of the PPB Lock Bit. The password is 64 bits long, so the user must write the Password Unlock command 4 times. A1 and A0 are used for matching. Writing the Password Unlock command is not address order specific. The lower address A1–A0= 00, the next Password Unlock command is to A1–A0= 01, then to A1–A0= 10, and finally to A1–A0= 11.

Once the Password Unlock command is entered for all four words, the RDY pin goes LOW indicating that the device is busy. Approximately 1uSec is required for each portion of the unlock. Once the first portion of the password unlock completes (RDY is not driven and DQ6 does not toggle when read), the Password Unlock command is issued again, only this time with the next part of the password. Four Password Unlock commands are required to successfully clear the PPB Lock Bit. As with the first Password Unlock command, the RDY signal goes LOW and reading the device results in the DQ6 pin toggling on successive read operations until complete. It is the responsibility of the microprocessor to keep track of the number of Password Unlock commands, the order, and when to read the PPB Lock bit to confirm successful password unlock. In order to relock the device into the Password Mode, the PPB Lock Bit Set command can be re-issued.

PPB Program Command

The PPB Program command is used to program, or set, a given PPB. Each PPB is individually programmed (but is bulk erased with the other PPBs). The specific sector address (A21–A12) are written at the same time as the program command 60h with A6 = 0. If the PPB Lock Bit is set and the corresponding PPB is set for the sector, the PPB Program command will not execute and the command will time-out without programming the PPB.

After programming a PPB, two additional cycles are needed to determine whether the PPB has been programmed with margin. If the PPB has been programmed without margin, the program command should be reissued to improve the program margin.

The PPB Program command does not follow the Embedded Program algorithm.

All PPB Erase Command

The All PPB Erase command is used to erase all PPBs in bulk. There is no means for individually erasing a specific PPB. Unlike the PPB program, no specific sector address is required. However, when the PPB erase command is written (60h) and A6 = 1, all Sector PPBs are erased in parallel. If the PPB Lock Bit is set the ALL PPB Erase command will not execute and the command will time-out without erasing the PPBs. After erasing the PPBs, two additional cycles are needed to determine whether the PPB has been erased with margin. If the PPBs has been erased with-

out margin, the erase command should be reissued to improve the program margin.

It is the responsibility of the user to preprogram all PPBs prior to issuing the All PPB Erase command. If the user attempts to erase a cleared PPB, over-erasure may occur making it difficult to program the PPB at a later time. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.

DYB Write Command

The DYB Write command is used for setting the DYB, which is a volatile bit that is cleared at hardware reset. There is one DYB per sector. If the PPB is set, the sector is protected regardless of the value of the DYB. If the PPB is cleared, setting the DYB to a 1 protects the sector from programs or erases. Since this is a volatile bit, removing power or resetting the device will clear the DYBs.

PPB Status Command

The programming of the PPB for a given sector can be verified by writing a PPB status verify command to the device.

PPB Lock Bit Status Command

The programming of the PPB Lock Bit for a given sector can be verified by writing a PPB Lock Bit status verify command to the device.

DYB Status Command

The programming of the DYB for a given sector can be verified by writing a DYB Status command to the device.

Command Definitions

Table 16. Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 1–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Asynchronous Read (Note 7)		1	RA	RD												
Reset (Note 8)		1	XXX	F0												
Autoselect (Note 9)	Manufacturer ID	4	555	AA	2AA	55	(BA) 555	90	(BA) X00	0001						
	Device ID	6	555	AA	2AA	55	(BA) 555	90	(BA) X01	227E	(BA) X0E	221E	(BA) X0F	2201		
	Sector Lock Verify (Note 10)	4	555	AA	2AA	55	(SA) 555	90	(SA) X02	(Note 10)						
	Indicator Bits (Note 11)	4	555	AA	2AA	55	(BA) 555	90	(BA) X03	(Note 11)						
Program		4	555	AA	2AA	55	555	A0	PA	Data						
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10		
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30		
Erase Suspend (Note 14)		1	BA	B0												
Erase Resume (Note 15)		1	BA	30												
Set Configuration Register (Note 16)		3	555	AA	2AA	55	(CR) 555	C0								
CFI Query (Note 17)		1	55	98												
Unlock Bypass Mode	Unlock Bypass Entry	3	555	AA	2AA	55	555	20								
	Unlock Bypass Program (Notes 12, 13)	2	XX	A0	PA	PD										
	Unlock Bypass Sector Erase (Notes 12, 13)	2	XX	80	SA	30										
	Unlock Bypass Erase (Notes 12, 13)	2	XX	80	XXX	10										
	Unlock Bypass CFI (Notes 12, 13)	1	XX	98												
	Unlock Bypass Reset	2	XX	90	XXX	00										
Sector Protection Command Definitions																
SecSi Sector	SecSi Sector Entry	3	555	AA	2AA	55	555	88								
	SecSi Sector Exit	4	555	AA	2AA	55	555	90	XX	00						
	SecSi Protection Bit Program (Notes 18, 19, 21)	6	555	AA	2AA	55	555	60	(SA) OW	68	(SA) OW	48	OW	RD (0)		
Password Protection	Password Program (Notes 18, 23)	4	555	AA	2AA	55	555	38	XX0	PD0						
									XX1	PD1						
									XX2	PD2						
									XX3	PD3						
	Password Verify	4	555	AA	2AA	55	555	C8	XX0	PD0						
									XX1	PD1						
									XX2	PD2						
									XX3	PD3						
	Password Unlock (Note 23)	7	555	AA	2AA	55	555	28	XX0	PD0	XX1	PD1	XX2	PD2	XX3	PD3

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 1–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
PPB Commands	PPB Program (Notes 18, 19, 21)	6	555	AA	2AA	55	555	60	(SA) + WP	68	(SA) + WP	48	XX	RD (0)		
	All PPB Erase (Notes 18, 19, 22, 24)	6	555	AA	2AA	55	555	60	WP	60	WP	40	XX	RD (0)		
	PPB Status (Note 25)	4	555	AA	2AA	55	(BA) 555	90	(SA) X02	RD (0)						
PPB Lock Bit	PPB Lock Bit Set	3	555	AA	2AA	55	555	78								
	PPB Lock Bit Status (Note 19)	4	555	AA	2AA	55	(BA) 555	58	SA	RD (1)						
DYB	DYB Write	4	555	AA	2AA	55	555	48	SA	X1						
	DYB Erase	4	555	AA	2AA	55	555	48	SA	X0						
	DYB Status	4	555	AA	2AA	55	(BA) 555	58	SA	RD (0)						
Password Protection Mode Locking Bit Program (Notes 18, 19, 21)		6	555	AA	2AA	55	555	60	PL	68	PL	48	PL	RD (0)		
Persistent Protection Mode Locking Bit Program (Notes 18, 19, 21)		6	555	AA	2AA	55	555	60	SL	68	SL	48	SL	RD (0)		
Password Protection Mode Locking Bit Read (Notes 18, 19, 21)		4	555	AA	2AA	55	555	60	PL	RD (0)						
Persistent Protection Mode Locking Bit Read (Notes 18, 19, 21)		4	555	AA	2AA	55	555	60	SL	RD (0)						

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the rising edge of the AVD# pulse or active edge of CLK which ever comes first.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A21–A12 uniquely select any sector.

BA = Address of the bank (A21, A20, A19) that is being switched to autoselect mode, is in bypass mode, or is being erased.

SLA = Address of the sector to be locked. Set sector address (SA) and either A6 = 1 for unlocked or A6 = 0 for locked.

CR = Configuration Register address bits A19–A12.

OW = Address (A7–A0) is (00011010).

PD3–PD0 = Password Data. PD3–PD0 present four 16 bit combinations that represent the 64-bit Password

PWA = Password Address. Address bits A1 and A0 are used to select each 16-bit portion of the 64-bit entity.

PWD = Password Data.

PL = Address (A7-A0) is (00001010)

RD(0) = DQ0 protection indicator bit. If protected, DQ0 = 1, if unprotected, DQ0 = 0.

RD(1) = DQ1 protection indicator bit. If protected, DQ1 = 1, if unprotected, DQ1 = 0.

SL = Address (A7-A0) is (00010010)

WD= Write Data. See "Configuration Register" definition for specific write data

WP = Address (A7-A0) is (00000010)

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the following, all bus cycles are write cycle: read cycle, fourth through sixth cycles of the Autoselect commands, fourth cycle of the configuration register verify and password verify commands, and any cycle reading at RD(0) and RD(1).*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD, PD, WD, PWD, and PD3-PD0.*
5. *Unless otherwise noted, address bits A21–A12 are don't cares.*
6. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.*
7. *No unlock or command cycles required when bank is reading array data.*
8. *The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information) or performing sector lock/unlock.*
9. *The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address. See the Autoselect Command Sequence section for more information.*
10. *The data is 0000h for an unlocked sector and 0001h for a locked sector*
11. *DQ15 - DQ8 = 0, DQ7: Factory Lock Bit (1 = Locked, 0 = Not Locked), DQ6: Customer Lock Bit (1 = Locked, 0 = Not Locked), DQ5: Handshake Bit (1 = Reduced wait-state Handshake, 0 = Standard Handshake), DQ4 - DQ0 = 0*
12. *The Unlock Bypass command sequence is required prior to this command sequence.*
13. *The Unlock Bypass Reset command is required to return to reading array data when the bank is in the unlock bypass mode.*

14. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
15. *The Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*
16. *See "Set Configuration Register Command Sequence" for details.*
17. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
18. *The Reset command returns the device to reading the array.*
19. *Regardless of CLK and AVD# interaction or Control Register bit 15 setting, command mode verifies are always asynchronous read operations.*
20. *ACC must be at V_{HH} during the entire operation of this command*
21. *The fourth cycle programs the addressed locking bit. The fifth and sixth cycles are used to validate whether the bit has been fully programmed. If DQ0 (in the sixth cycle) reads 0, the program command must be issued and verified again.*
22. *The fourth cycle erases all PPBs. The fifth and sixth cycles are used to validate whether the bits have been fully erased. If DQ0 (in the sixth cycle) reads 1, the erase command must be issued and verified again.*
23. *The entire four bus-cycle sequence must be entered for each portion of the password.*
24. *Before issuing the erase command, all PPBs should be programmed in order to prevent over-erasure of PPBs.*
25. *In the fourth cycle, 01h indicates PPB set; 00h indicates PPB not set.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 18, "Write Operation Status," on page 47 and the following subsections describe the function of these bits. DQ7 and DQ6 each offers a method for determining whether a program or erase operation is complete or in progress.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

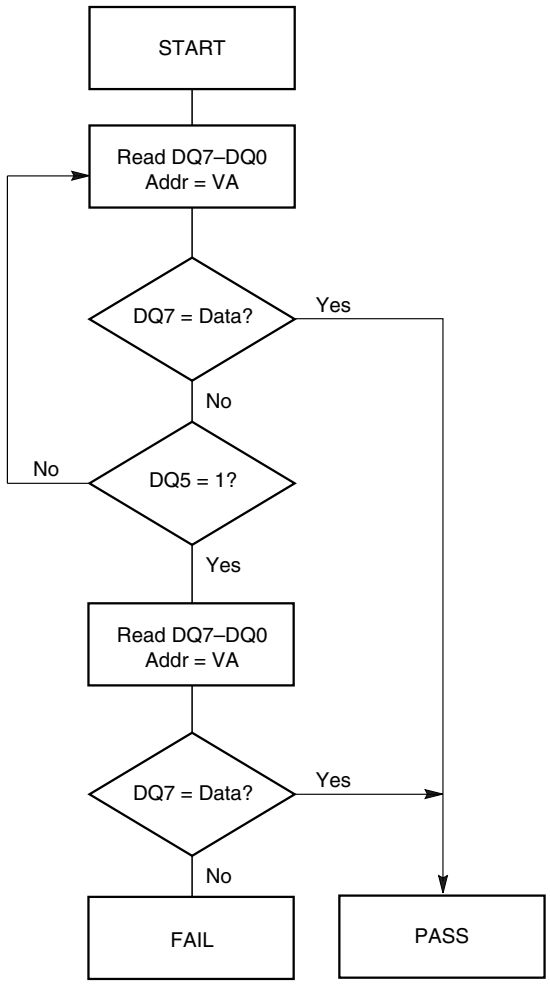
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6-DQ0 may be still invalid. Valid data on DQ7-DQ0 will appear on successive read cycles.

Table 18, "Write Operation Status," on page 47 shows the outputs for Data# Polling on DQ7. Figure 6, "Data# Polling Algorithm," on page 43 shows the Data# Polling algorithm. Figure 37, "Data# Polling Timings (During Embedded Algorithm)," on page 72 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 6. Data# Polling Algorithm

RDY: Ready

The RDY is a dedicated output that, when the device is configured in the Synchronous mode, indicates (when at logic low) the system should wait 1 clock cycle before expecting the next word of data. The RDY pin is only controlled by CE#. Using the RDY Configuration Command Sequence, RDY can be set so that a logic low indicates the system should wait 2 clock cycles before expecting valid data.

The following conditions cause the RDY output to be low: during the initial access (in burst mode), and after the boundary that occurs every 64 words beginning with the 64th address, 3Fh.

When the device is configured in Asynchronous Mode, the RDY is an open-drain output pin which indicates whether an Embedded Algorithm is in progress or completed. The RDY status is valid after the rising edge of the final WE# pulse in the command sequence.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is in high impedance (Ready), the device is in the read mode, the standby mode, or in the erase-suspend-read mode. Table 18, “Write Operation Status,” on page 47 shows the outputs for RDY.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address in the same bank, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

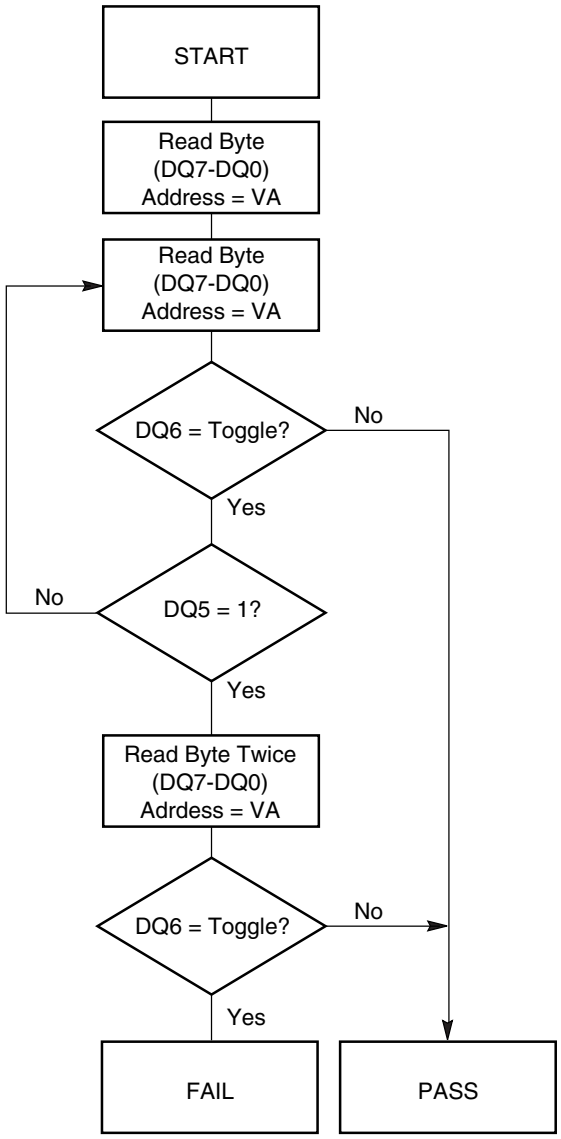
The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 ms after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

See the following for additional information: Figure 7, “Toggle Bit Algorithm,” on page 45, “DQ6: Toggle Bit I” on page 44, Figure 38, “Toggle Bit Timings (During Embedded Algorithm),” on page 72 (toggle bit timing diagram), and Table 17, “DQ6 and DQ2 Indications,” on page 46.

Toggle Bit I on DQ6 requires either OE# or CE# to be de-asserted and reasserted to show the change in state.



Note: *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.*

Figure 7. Toggle Bit Algorithm

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 17, "DQ6 and DQ2 Indications," on page 46 to compare outputs for DQ2 and DQ6.

See the following for additional information: Figure 7, "Toggle Bit Algorithm," on page 45, "DQ6: Toggle Bit I" on page 44, Figure 38, "Toggle Bit Timings (During Embedded Algorithm)," on page 72, and Table 17, "DQ6 and DQ2 Indications," on page 46.

Table 17. DQ6 and DQ2 Indications

If device is	and the system reads	then DQ6	and DQ2
programming,	at any address,	toggles,	does not toggle.
actively erasing,	at an address within a sector selected for erasure,	toggles,	also toggles.
	at an address within sectors *not* selected for erasure,	toggles,	does not toggle.
erase suspended,	at an address within a sector selected for erasure,	does not toggle,	toggles.
	at an address within sectors *not* selected for erasure,	returns array data,	returns array data. The system can read from any sector not selected for erasure.
programming in erase suspend	at any address,	toggles,	is not applicable.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 7, "Toggle Bit Algorithm," on page 45 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (Figure 7, "Toggle Bit Algorithm," on page 45).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." Only an erase operation can change a "0" back to a "1." Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also "Sector Erase Command Sequence" on page 35.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the

device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 18 shows the status of DQ3 relative to the other status bits.

Table 18. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RDY (Note 5)
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read (Note 4)	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	High Impedance
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	High Impedance
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.*
4. *The system may read either asynchronously or synchronously (burst) while in erase suspend.*
5. *The RDY pin acts a dedicated output to indicate the status of an embedded erase or program operation is in progress. This is available in the Asynchronous mode only.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –65°C to +125°C

Voltage with Respect to Ground:
All Inputs and I/Os except
as noted below (Note 1). . . . . –0.5 V to V_{IO} + 0.5 V

V_{CC} (Note 1). . . . . –0.5 V to +2.5 V

V_{IO} . . . . . –0.5 V to +2.5 V

A9, RESET#, ACC (Note 1) . . . . . –0.5 V to +12.5 V

Output Short Circuit Current (Note 3) . . . . . 100 mA

Notes:

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, inputs or I/Os may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 8. Maximum DC voltage on input or I/Os is V_{CC} + 0.5 V. During voltage transitions outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 9.*
2. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
3. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

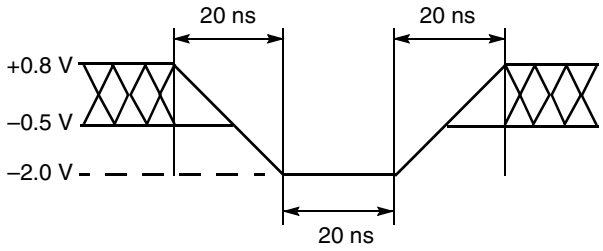


Figure 8. Maximum Negative Overshoot Waveform

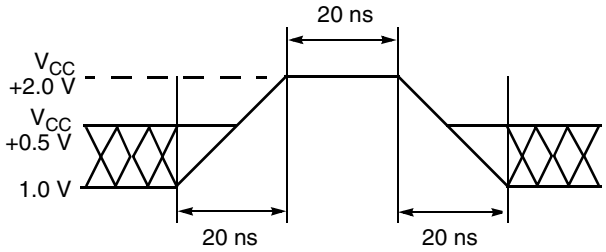


Figure 9. Maximum Positive Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

Supply Voltages

V_{CC} Supply Voltages . . . . . +1.65 V to +1.95 V

. . . . . V_{CC} >= V_{IO} - 100mV

V_{IO} Supply Voltages: . . . . . +1.65 V to +1.95 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

CMOS COMPATIBLE

Parameter	Description	Test Conditions Note: 1 & 2		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$max				±1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$max				±1	µA
I_{CCB}	V_{CC} Active burst Read Current	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 8	54 MHz		9	17	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 16	54 MHz		8	15.5	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = Continuous	54 MHz		7	14	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 8			50	200	µA
I_{IO1}	V_{IO} Non-active Output	OE# = V_{IH}			0.2	10	µA
I_{CC1}	V_{CC} Active Asynchronous Read Current (Note 3)	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}	10 MHz		TBD	TBD	mA
			5 MHz		12	16	mA
			1 MHz		3.5	5	mA
I_{CC2}	V_{CC} Active Write Current (Note 4)	CE# = V_{IL}, OE# = V_{IH}, ACC = V_{IH}			15	40	mA
I_{CC3}	V_{CC} Standby Current (Note 5)	CE# = RESET# = V_{CC} ± 0.2 V			1	40	µA
I_{CC4}	V_{CC} Reset Current	RESET# = V_{IL}, CLK = V_{IL}			1	40	µA
I_{CC5}	V_{CC} Active Current (Read While Write)	CE# = V_{IL}, OE# = V_{IH}			25	60	mA
I_{CC6}	V_{CC} Sleep Current	CE# = V_{IL}, OE# = V_{IH}			1	40	µA
I_{ACC}	Accelerated Program Current (Note 6)	CE# = V_{IL}, OE# = V_{IH}, V_{ACC} = 12.0 ± 0.5 V	V_{ACC}		7	15	mA
			V_{CC}		5	10	mA
V_{IL}	Input Low Voltage	V_{IO} = 1.8 V		–0.4		0.4	V
		V_{IO} = 1.5 V		TBD		TBD	
V_{IH}	Input High Voltage	V_{IO} = 1.8 V		V_{IO} – 0.4		V_{IO} + 0.4	
		V_{IO} = 1.5 V		TBD		TBD	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, $V_{IO} = V_{CC} = V_{CC\ min}$				0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{IO} = V_{CC} = V_{CC\ min}$		V_{IO} – 0.1			V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 1.8		11.5		12.5	V
V_{HH}	Voltage for Accelerated Program			11.5		12.5	V
V_{LKO}	Low V_{CC} Lock-out Voltage			1.0		1.4	V

Note:

1. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
2. *$V_{IO} = V_{CC}$*
3. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
4. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
5. *Device enters automatic sleep mode when addresses are stable for t_{ACC} + 60 ns. Typical sleep mode current is equal to I_{CC3}.*
6. *Total current during accelerated programming is the sum of V_{ACC} and V_{CC} currents.*

SRAM DC AND OPERATING CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}	–1.0		1.0	µA
I_{LO}	Output Leakage Current	CE1#s = V_{IH}, CE2s = V_{IL} or OE# = V_{IH} or WE# = V_{IL}, V_{IO}= V_{SS} to V_{CC}	–1.0		1.0	µA
I_{CC}	Operating Power Supply Current	I_{IO} = 0 mA, CE1#s = V_{IL}, CE2s = WE# = V_{IH}, V_{IN} = V_{IH} or V_{IL}			5	mA
$I_{CC1}s$	Average Operating Current	Cycle time = 1 µs, 100% duty, I_{IO} = 0 mA, CE1#s ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V		1	5	mA
$I_{CC2}s$	Average Operating Current	Cycle time = Min., I_{IO} = 0 mA, 100% duty, CE1#s = V_{IL}, CE2s = V_{IH}, V_{IN} = V_{IL} = or V_{IH}		8	15	mA
V_{OL}	Output Low Voltage	I_{OL} = 0.1 mA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = –0.1 mA	1.4			V
I_{SB1}	Standby Current (CMOS)	CE1#s ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V (CE1#s controlled) or CE2 ≤ 0.2 V (CE2s controlled), CIOs = V_{SS} or V_{CC}, Other input = 0 ~ V_{CC}		2	25	µA
V_{IL}	Input Low Voltage		–0.2 (Note 2)		0.4	V
V_{IH}	Input High Voltage		1.4		V_{CC}+0.2 (Note 3)	V

Notes:

1. *Typical values measured at V_{CC} = 2.0 V, T_A = 25°C. Not 100% tested.*
2. *Undershoot is –1.0 V when pulse width ≤ 20 ns.*
3. *Overshoot is V_{CC} + 1.0 V when pulse width ≤ 20 ns.*
4. *Overshoot and undershoot are sampled, not 100% tested.*

TEST CONDITIONS

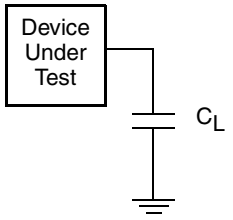


Figure 10. Test Setup

Table 19. Test Specifications

Test Condition	All Speed Options	Unit
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–V_{IO}	V
Input timing measurement reference levels	$V_{IO}/2$	V
Output timing measurement reference levels	$V_{IO}/2$	V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

SWITCHING WAVEFORMS

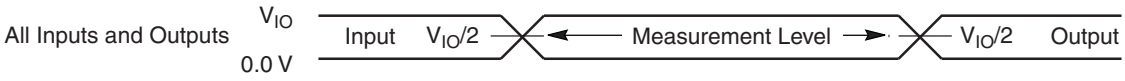


Figure 11. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

V_{CC} Power-up

Parameter	Description	Test Setup	Speed	Unit
t_{VCS}	V_{CC} Setup Time	Min	50	µs
t_{VIOS}	V_{IO} Setup Time	Min	50	µs
t_{RSTH}	RESET# Low Hold Time	Min	50	µs

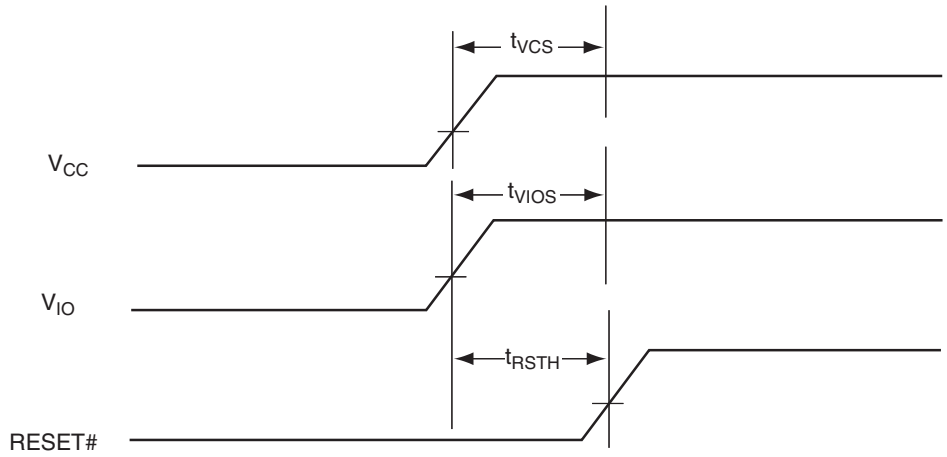


Figure 12. V_{CC} Power-up Diagram

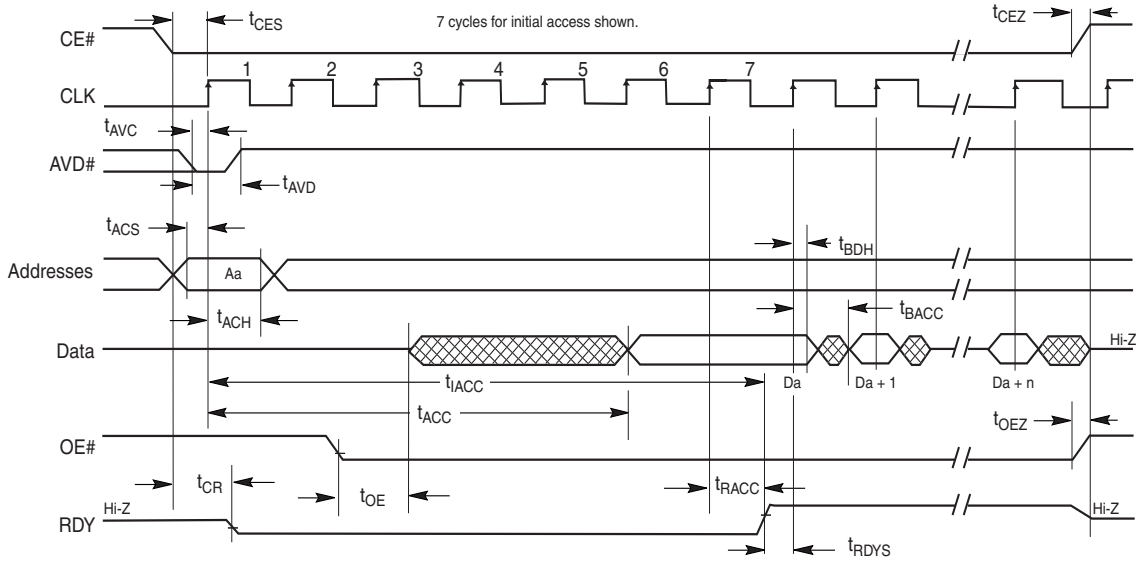
Synchronous/Burst Read (V_{IO} = 1.8 V)

Parameter		Description		E6, E7, E8, E9 (66 MHz)	D6, D7, D8, D9 (54 MHz)	Unit
JEDEC	Standard					
	t_{IACC}	Latency (Even address in Reduced wait-state Handshake mode)	Max	56	69	ns
	t_{IACC}	Latency (Standard Handshake or Odd address in Reduced wait-state Handshake mode	Max	71	87.5	ns
	t_{BACC}	Burst Access Time Valid Clock to Output Delay	Max	11	13.5	ns
	t_{ACS}	Address Setup Time to CLK (Note 1)	Min	4	5	ns
	t_{ACH}	Address Hold Time from CLK (Note 1)	Min	6	7	ns
	t_{BDH}	Data Hold Time from Next Clock Cycle	Min	3	4	ns
	t_{CR}	Chip Enable to RDY Valid	Max	11	13.5	ns
	t_{OE}	Output Enable to Output Valid	Max	11	13.5	ns
	t_{CEZ}	Chip Enable to High Z	Max	8	10	ns
	t_{OEZ}	Output Enable to High Z	Max	8	10	ns
	t_{CES}	CE# Setup Time to CLK	Min	4	5	ns
	t_{RDYS}	RDY Setup Time to CLK	Min	4	5	ns
	t_{RACC}	Ready Access Time from CLK	Max	11	13.5	ns
	t_{AAS}	Address Setup Time to AVD# (Note 1)	Min	4	5	ns
	t_{AAH}	Address Hold Time to AVD# (Note 1)	Min	6	7	ns
	t_{CAS}	CE# Setup Time to AVD#	Min	0		ns
	t_{AVC}	AVD# Low to CLK	Min	4	5	ns
	t_{AVD}	AVD# Pulse	Min	10	12	ns
	t_{ACC}	Access Time	Max	50	55	ns
	t_{CKA}	CLK to access resume	Max	11	13.5	ns
	t_{CKZ}	CLK to High Z	Max	8	10	ns
	t_{OES}	Output Enable Setup Time	Min	4	5	ns
	t_{RCC}	Read cycle for continuous suspend	Max	1		ms

Notes:

1. *Addresses are latched on the first of either the active edge of CLK or the rising edge of AVD#.*
2. *Please contact AMD for availability of V_{IO} = 1.5 V devices.*

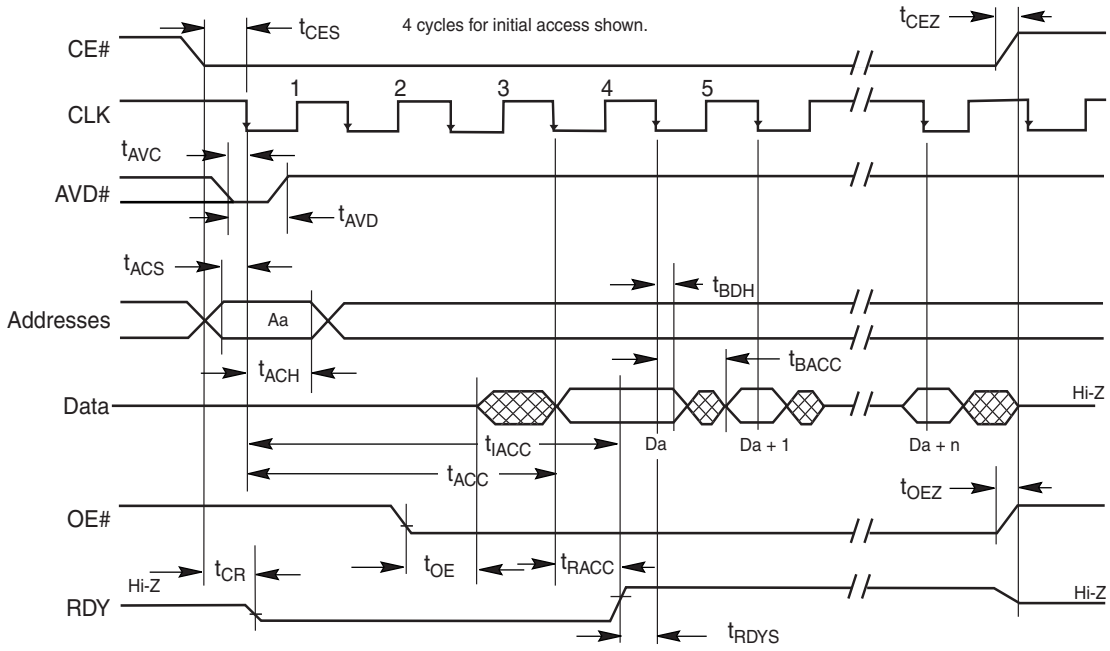
AC CHARACTERISTICS



Notes:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles.*
2. *If any burst address occurs at a 64-word boundary, two additional clock cycle are inserted, and is indicated by RDY.*
3. *The device is in synchronous mode.*

Figure 13. CLK Synchronous Burst Mode Read (rising active CLK)

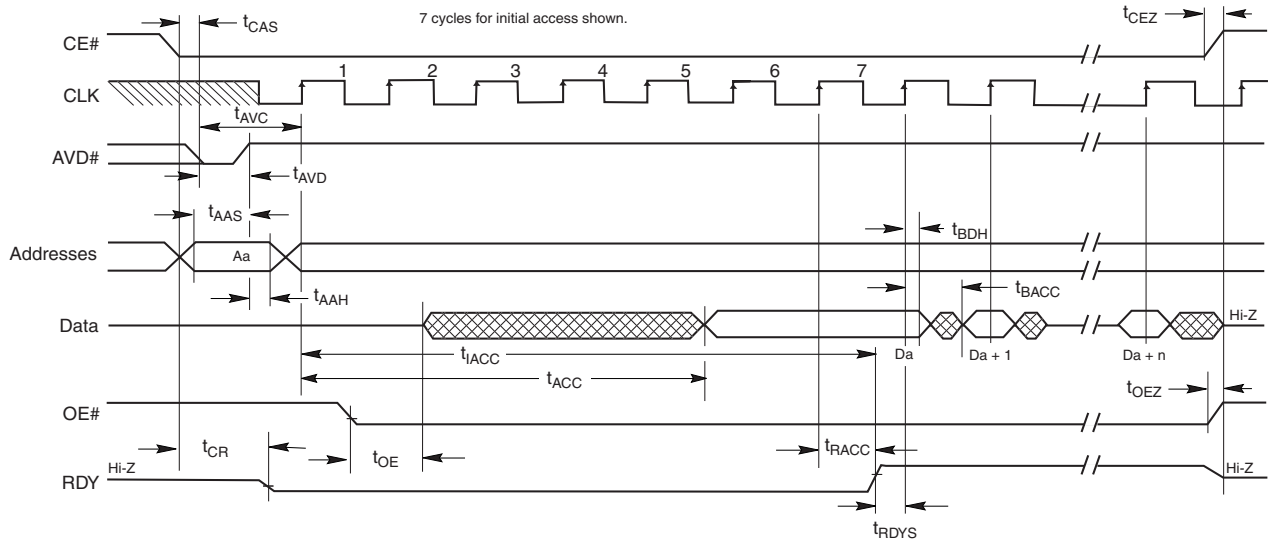


Notes:

1. *Figure shows total number of wait states set to four cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active falling edge.*
2. *If any burst address occurs at a 64-word boundary, two additional clock cycle are inserted, and is indicated by RDY.*
3. *The device is in synchronous mode.*

Figure 14. CLK Synchronous Burst Mode Read (Falling Active Clock)

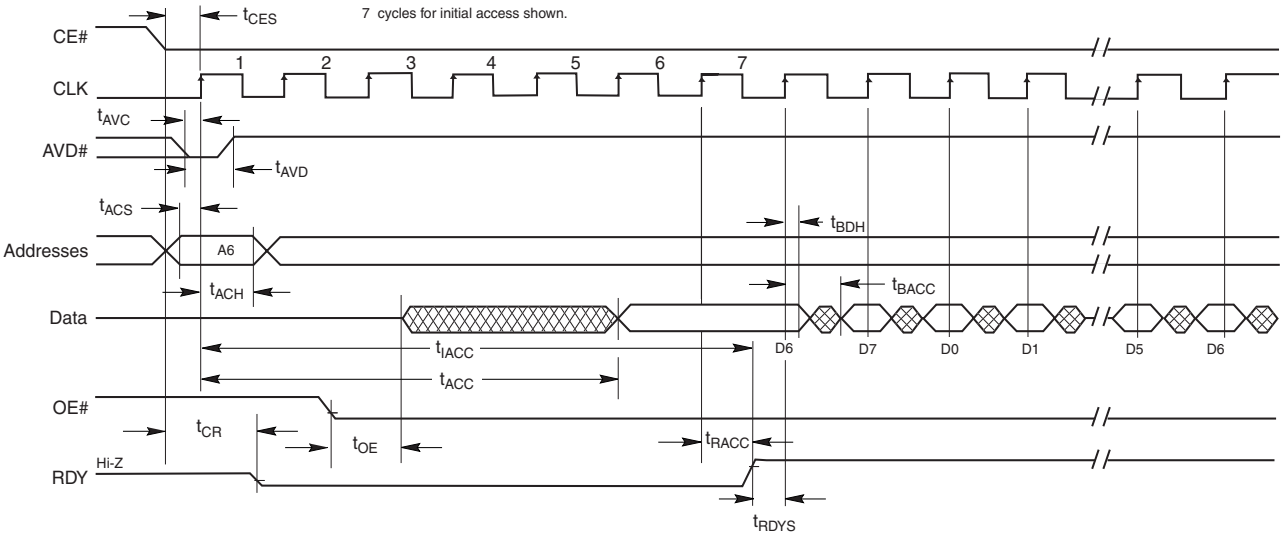
AC CHARACTERISTICS



Notes:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active rising edge.*
2. *If any burst address occurs at a 64-word boundary, two additional clock cycle are inserted, and is indicated by RDY.*
3. *The device is in synchronous mode.*

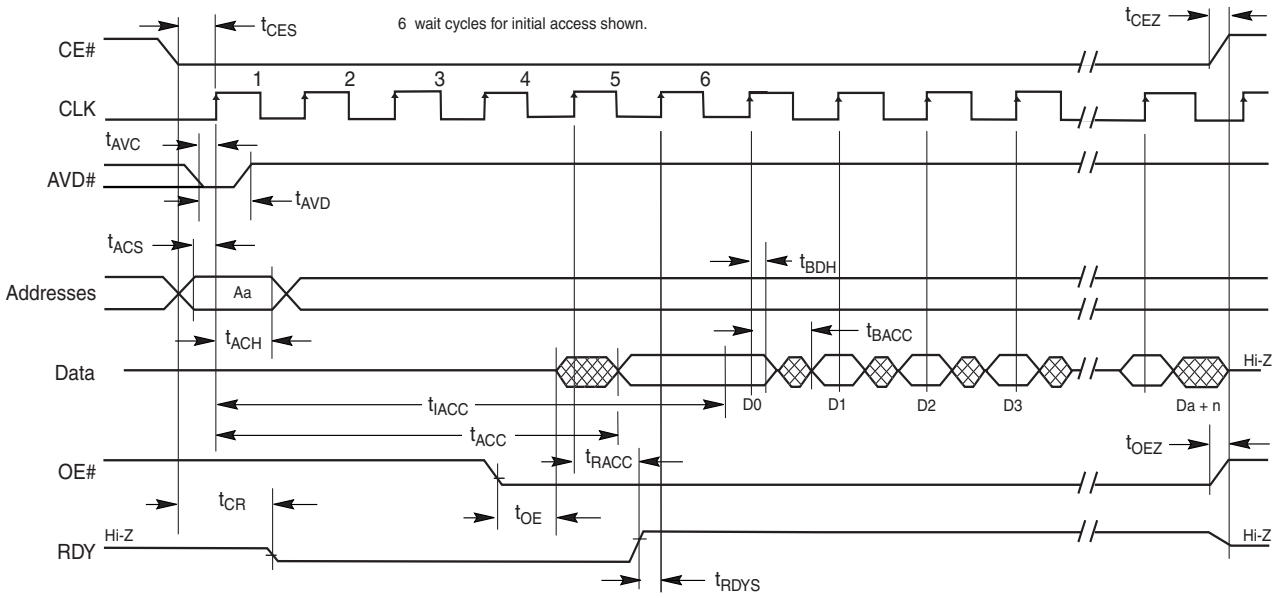
Figure 15. Synchronous Burst Mode Read



Note: *Figure assumes 7 wait states for initial access and automatic detect synchronous read. D0–D7 in data waveform indicate the order of data within a given 8-word address range, from lowest to highest. Starting address in figure is the 7th address in range (A6). See "Requirements for Synchronous (Burst) Read Operation". The Set Configuration Register command sequence has been written with A18=1; device will output RDY with valid data.*

Figure 16. 8-word Linear Burst with Wrap Around

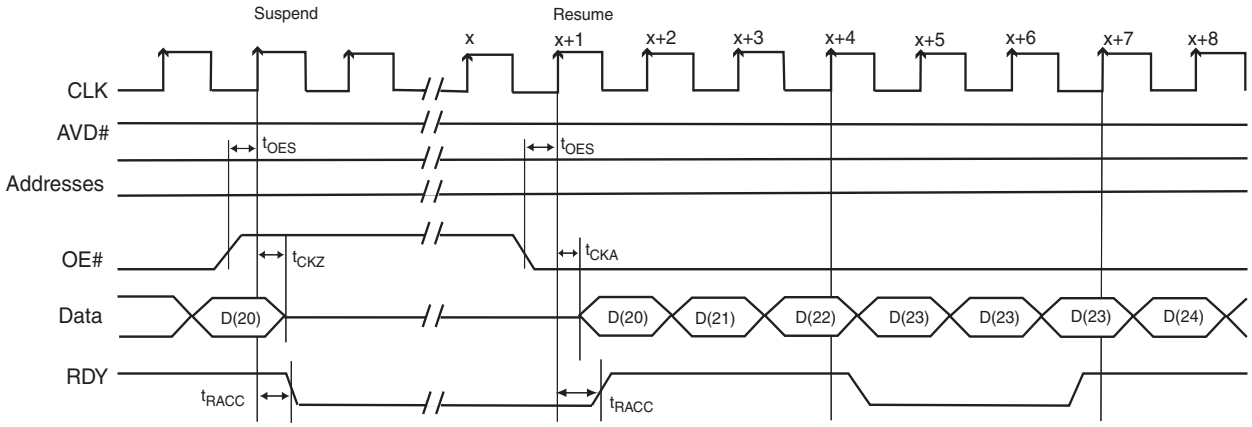
AC CHARACTERISTICS



Note: *Figure assumes 6 wait states for initial access and synchronous read. The Set Configuration Register command sequence has been written with A18=0; device will output RDY one cycle before valid data.*

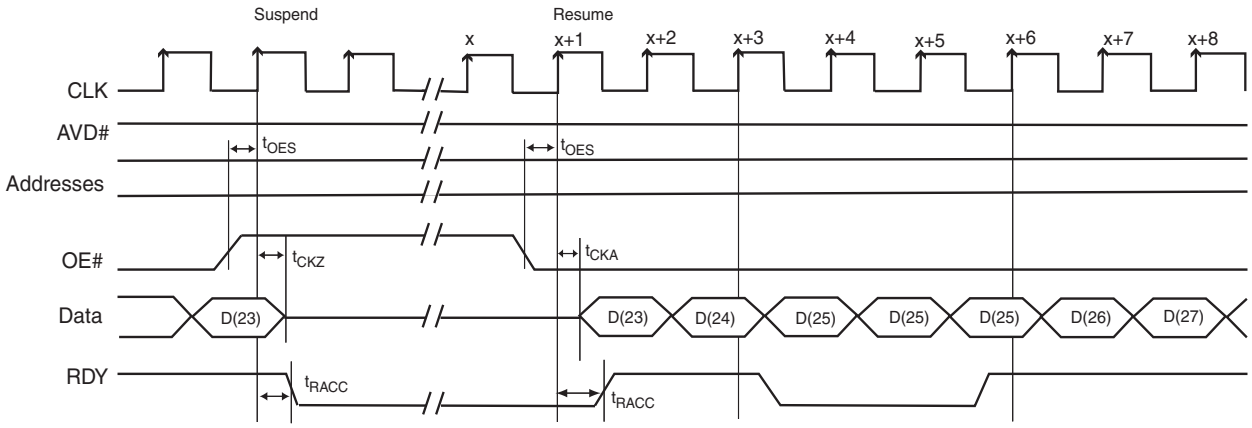
Figure 17. Linear Burst with RDY Set One Cycle Before Data

AC CHARACTERISTICS



Note: *Figure is for any even address other than 3Eh (or multiple thereof).*

Figure 18. Reduced Wait-state Handshake Burst Suspend/Resume at an even address



Note: *Figure is for any odd address other than 3Fh (or multiple thereof).*

Figure 19. Reduced Wait-state Handshake Burst Suspend/Resume at an odd address

AC CHARACTERISTICS

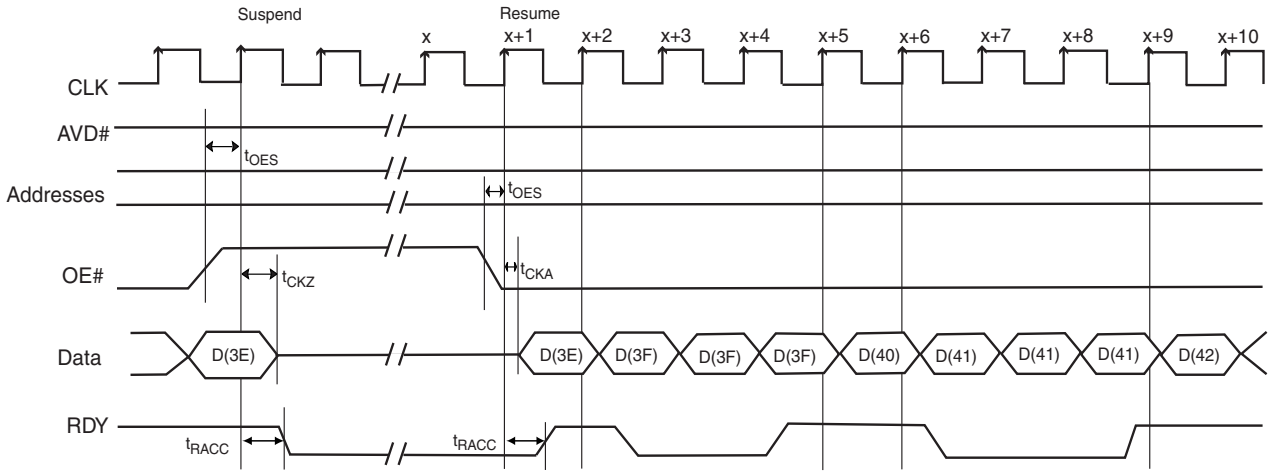


Figure 20. Reduced Wait-state Handshake Burst Suspend/Resume at address 3Eh (or offset from 3Eh)

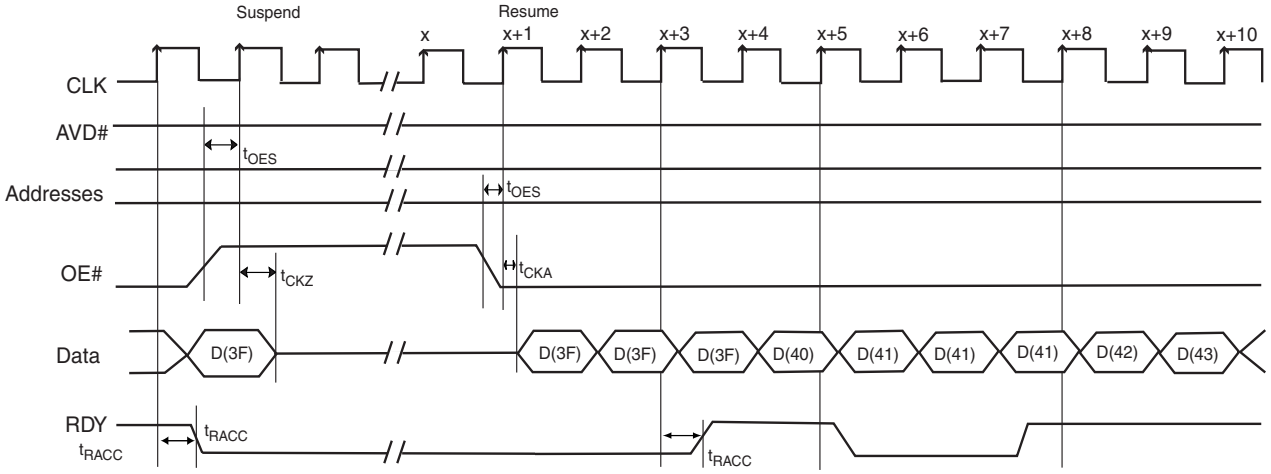
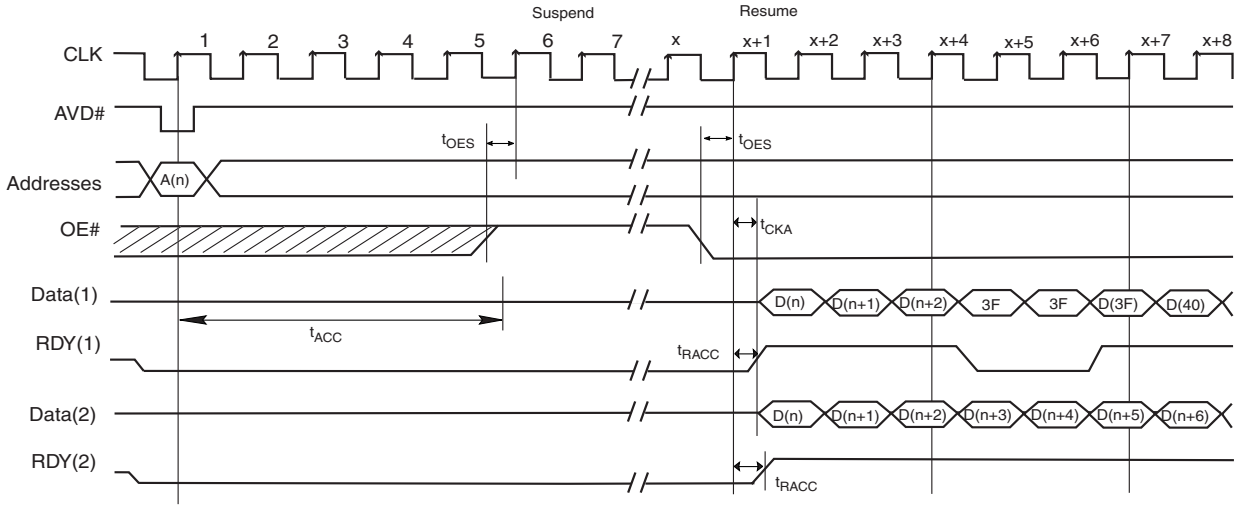


Figure 21. Reduced Wait-state Handshake Burst Suspend/Resume at address 3Fh (or offset from 3Fh by a multiple of 64)

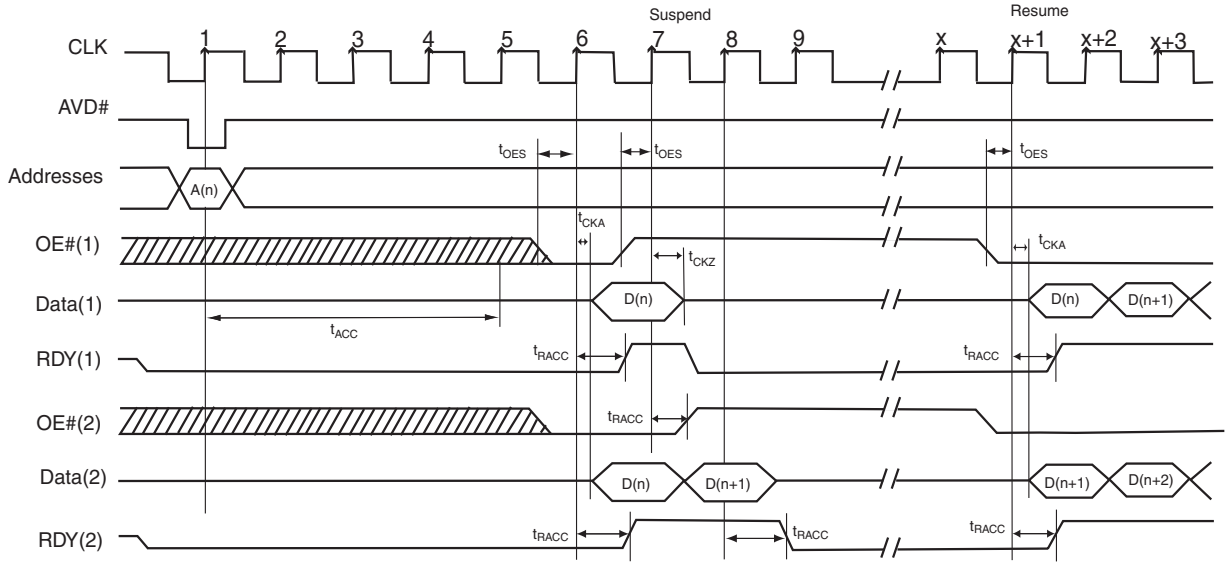
AC CHARACTERISTICS



Note: *Figure assumes 6 wait states for initial access and synchronous read. The Set Configuration Register command sequence has been written with A18=0; device will output RDY with valid data.*
1) RDY goes low during the two-cycle latency during a boundary crossing.

2) RDY stays high when a burst sequence crosses no boundaries.

Figure 22. Standard Handshake Burst Suspend prior to Initial Access

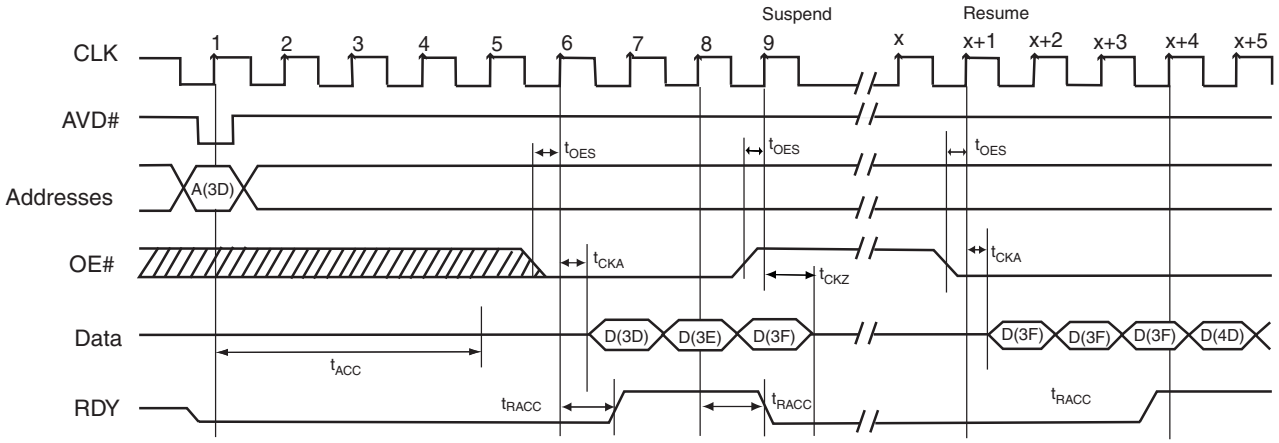


Note: *Figure assumes 6 wait states for initial access and synchronous read. The Set Configuration Register command sequence has been written with A18=0; device will output RDY with valid data.*
1) Burst suspend during the initial synchronous access

2) Burst suspend after one clock cycle following the initial synchronous access

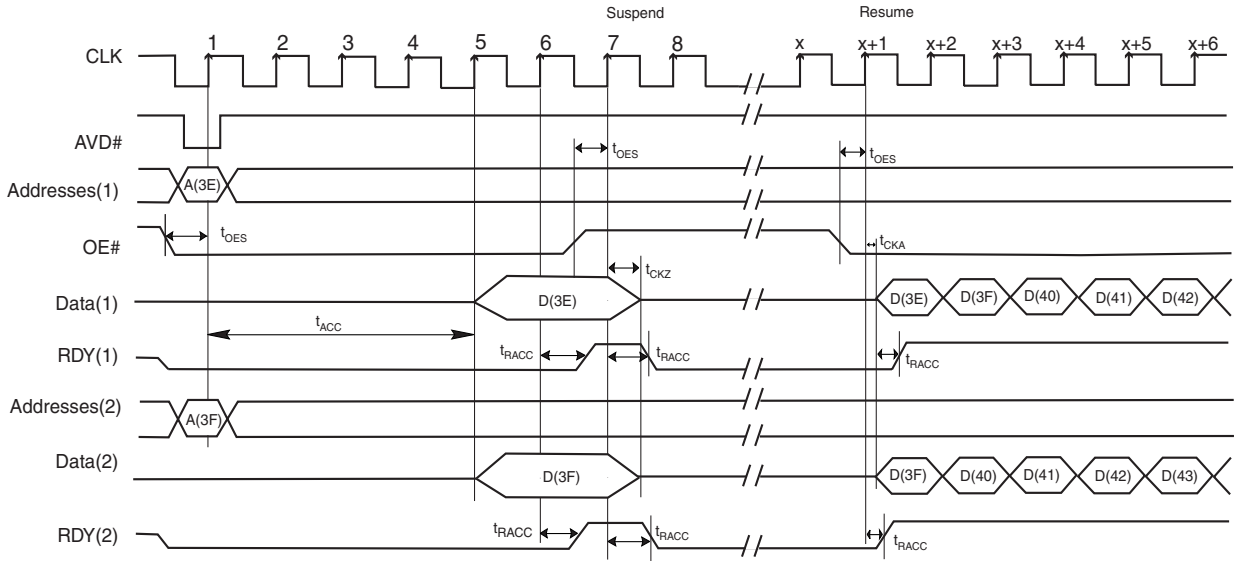
Figure 23. Standard Handshake Burst Suspend at or after Inital Access

AC CHARACTERISTICS



Note: *Figure assumes 6 wait states for initial access and synchronous read. The Set Configuration Register command sequence has been written with A18=0; device will output RDY with valid data.*

Figure 24. Standard Handshake Burst Suspend at address 3Fh (starting address 3Dh or earlier)

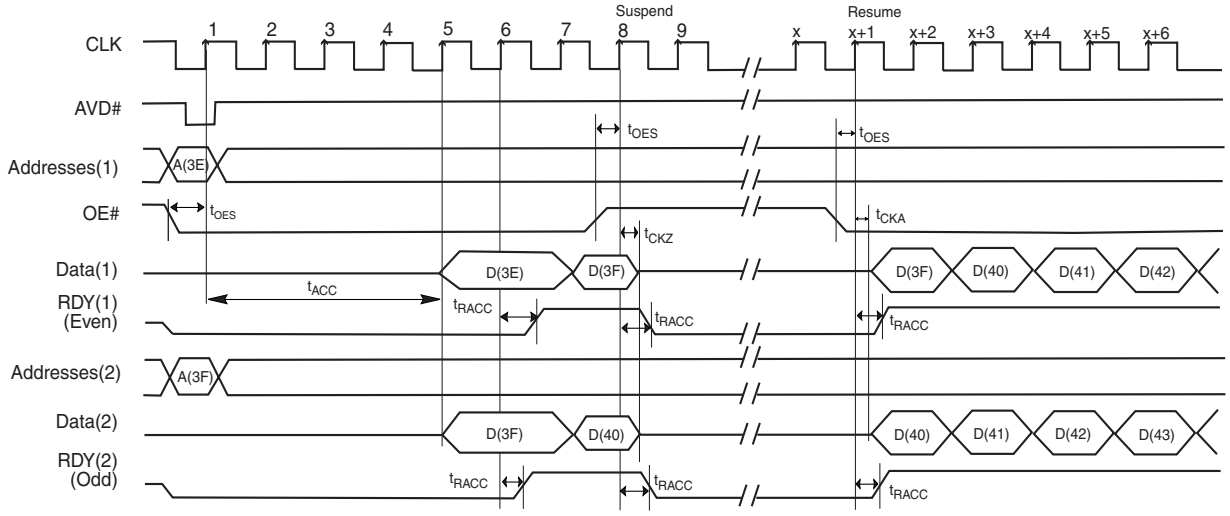


Note: *Figure assumes 6 wait states for initial access and synchronous read. The Set Configuration Register command sequence has been written with A18=0; device will output RDY with valid data.*
1) Address is 3Eh or offset by a multiple of 64 (40h)

2) Address is 3Fh or offset by a multiple of 64 (40h)

Figure 25. Standard Handshake Burst Suspend at address 3Eh/3Fh (without a valid Initial Access)

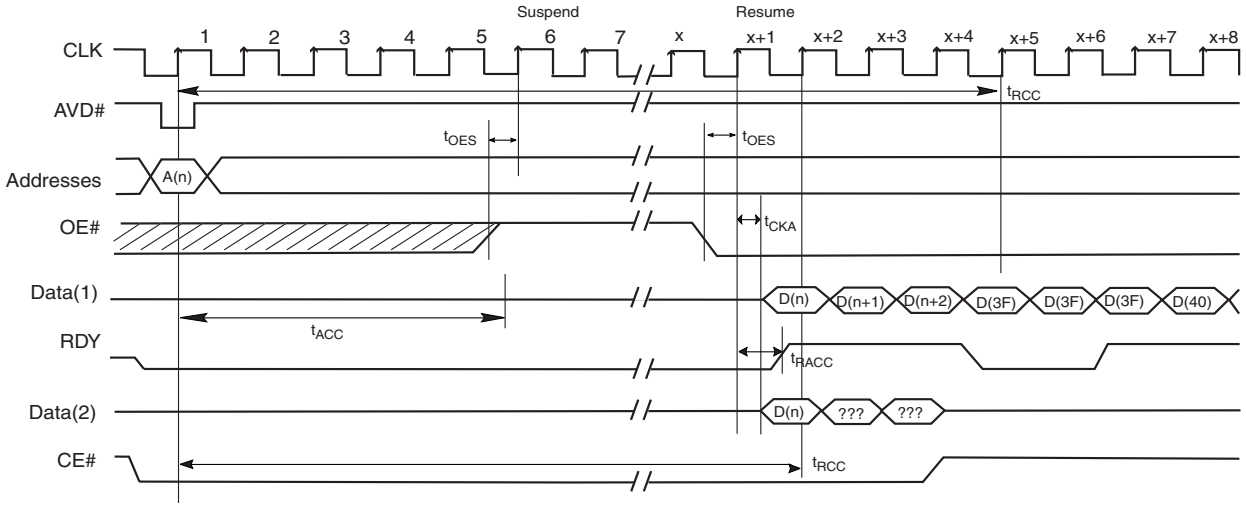
AC CHARACTERISTICS



Note: *Figure assumes 6 wait states for initial access and synchronous read. The Set Configuration Register command sequence has been written with A18=0; device will output RDY with valid data.*
1) Address 3Eh or offset by a multiple of 64 (40h)

2) Address is 3Fh or offset by a multiple of 64 (40h)

Figure 26. Standard Handshake Burst Suspend at address 3Eh/3Fh (with 1 Access CLK)



Note: *Figure assumes 6 wait states for initial access and synchronous read. The Set Configuration Register command sequence has been written with A18=0; device will output RDY with valid data.*
1) Device crosses a page boundary prior to t_{RCC}

2) Device neither crosses a page boundary nor latches a new address prior to t_{RCC}

Figure 27. Read Cycle for Continuous Suspend

AC CHARACTERISTICS

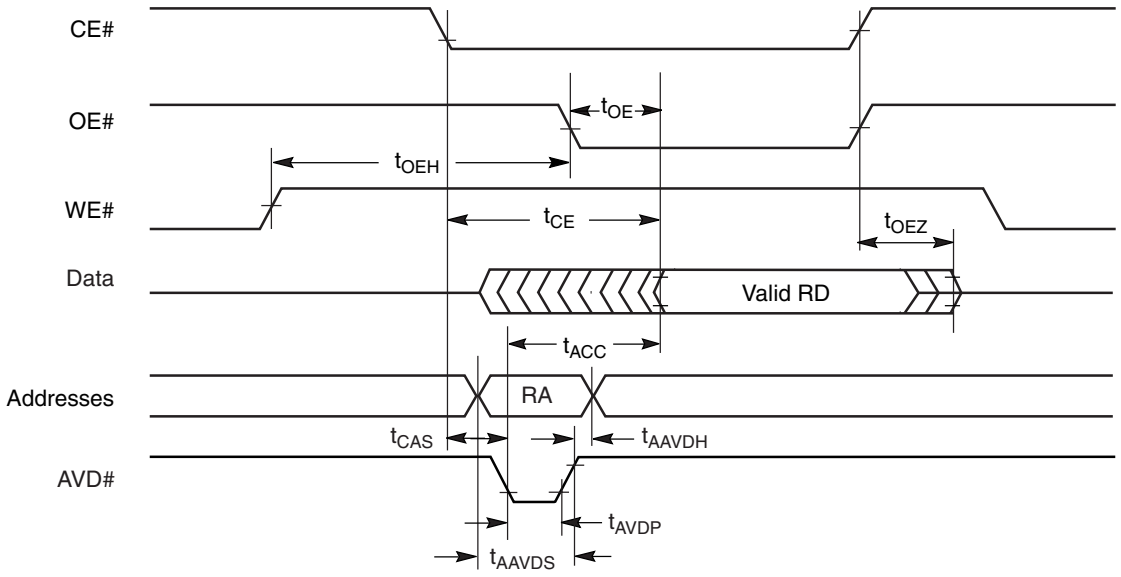
Asynchronous Mode Read (V_{IO} = 1.8 V)

Parameter		Description			E3, E4, E8, E9 (66 MHz)	D6, D7, D8, D9 (54 MHz)	Unit
JEDEC	Standard						
	t_{CE}	Access Time from CE# Low		Max	50	TBD	ns
	t_{ACC}	Asynchronous Access Time (Note 1)		Max	50	TBD	ns
	t_{AVDP}	AVD# Low Time		Min	10	12	ns
	t_{AAVDS}	Address Setup Time to Rising Edge of AVD		Min	4	5	ns
	t_{AAVDH}	Address Hold Time from Rising Edge of AVD		Min	6	7	ns
	t_{OE}	Output Enable to Output Valid		Max	11	13.5	ns
	t_{OEH}	Output Enable Hold Time	Read	Min	0		ns
			Toggle and Data# Polling	Min	8	10	ns
	t_{OEZ}	Output Enable to High Z (Note 2)		Max	8	10	ns
	t_{CAS}	CE# Setup Time to AVD#		Min	0		ns

Notes:

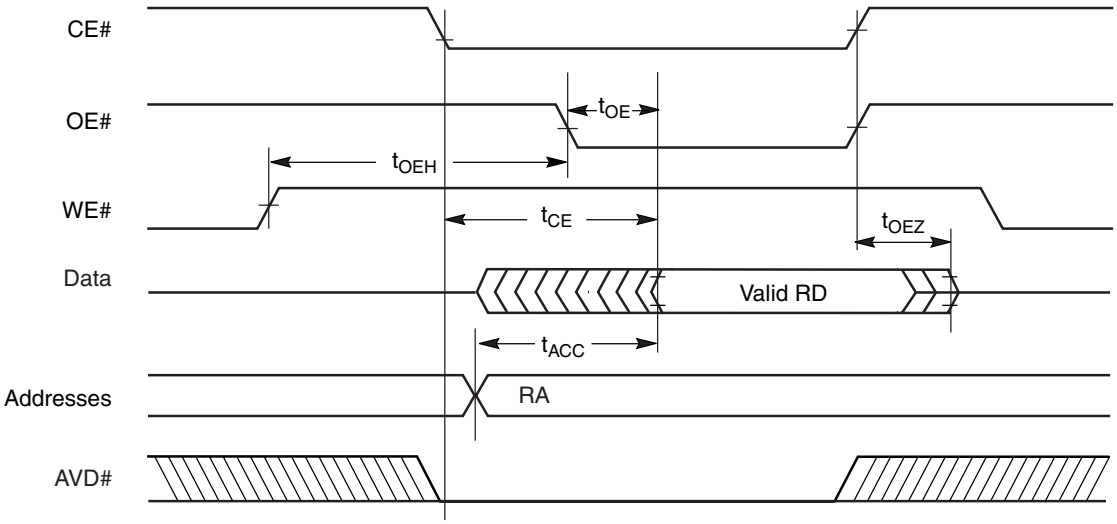
1. *Asynchronous Access Time is from the last of either stable addresses or the falling edge of AVD#.*
2. *Not 100% tested.*

AC CHARACTERISTICS



Note: *RA = Read Address, RD = Read Data.*

Figure 28. Asynchronous Mode Read with Latched Addresses



Note: *RA = Read Address, RD = Read Data.*

Figure 29. Asynchronous Mode Read

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	200	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs

Note: *Not 100% tested.*

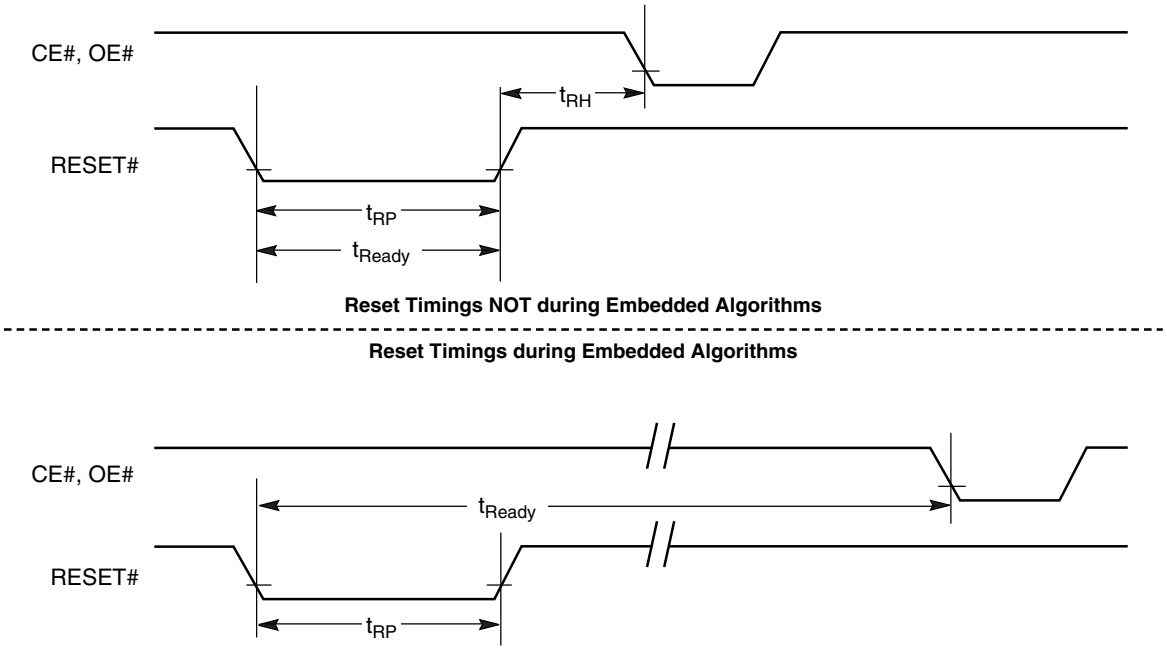


Figure 30. Reset Timings

AC CHARACTERISTICS

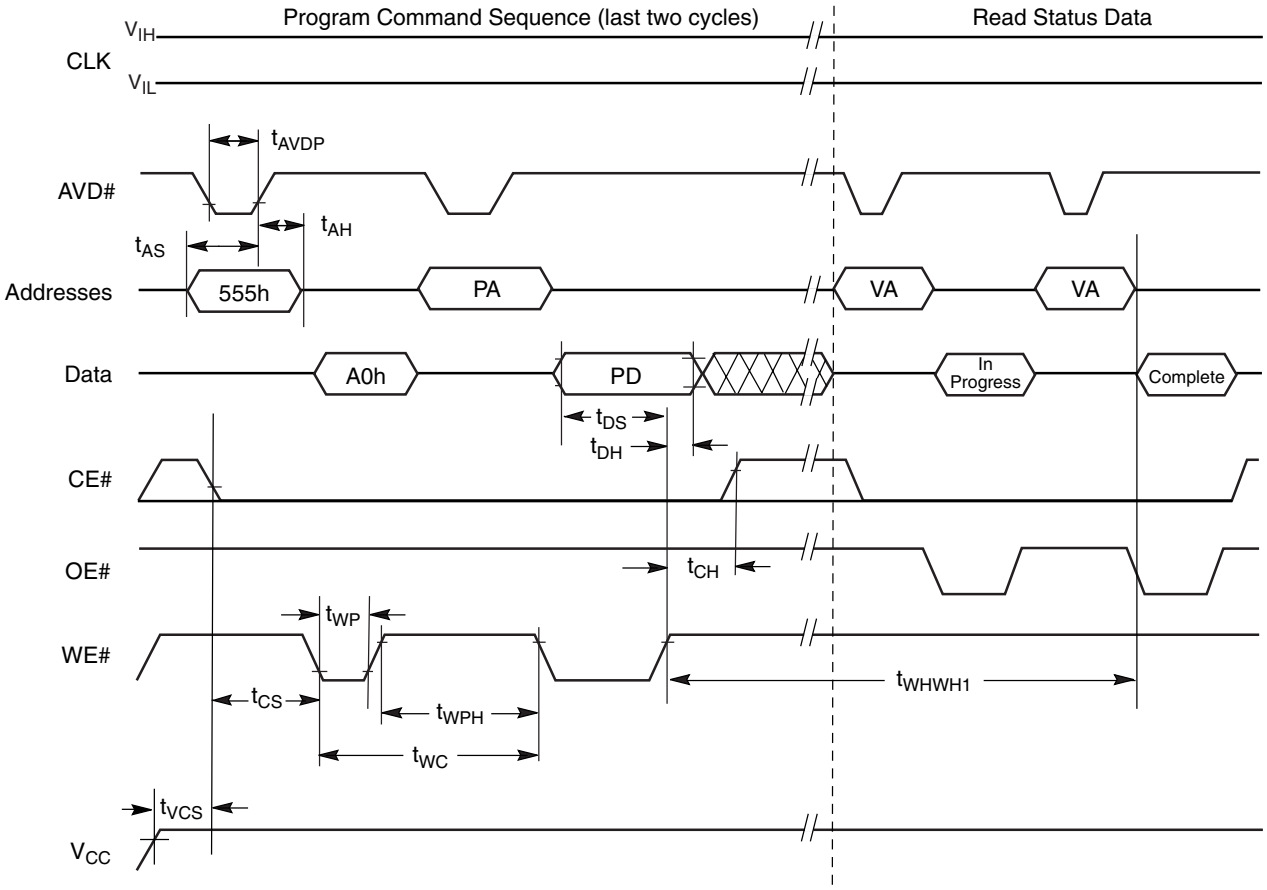
Erase/Program Operations (V_{IO} = 1.8 V)

Parameter		Description			E6, E7, E8, E9 (66 MHz)	D6, D7, D8, D9 (54 MHz)	Unit
JEDEC	Standard						
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	50	55	ns
t_{AVWL}	t_{AS}	Address Setup Time (Notes 2, 3)	Synchronous	Min	4	5	ns
			Asynchronous		0		
t_{WLAX}	t_{AH}	Address Hold Time (Notes 2, 3)	Synchronous	Min	6	7	ns
			Asynchronous		20	20	
	t_{AVDP}	AVD# Low Time		Min	10	12	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	20	45	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write		Min	0		ns
	t_{CAS}	CE# Setup Time to AVD#		Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	20	30	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	20	20	ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 4)		Typ	9		µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation (Note 4)		Typ	4		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Notes 4, 5)		Typ	0.4		sec
		Chip Erase Operation (Notes 4, 5)			54		
	t_{VID}	V_{ACC} Rise and Fall Time		Min	500		ns
	t_{VIDS}	V_{ACC} Setup Time (During Accelerated Programming)		Min	1		µs
	t_{VCS}	V_{CC} Setup Time		Min	50		µs
t_{ELWL}	t_{CS}	CE# Setup Time to WE#		Min	0		ns
	t_{AVSW}	AVD# Setup Time to WE#		Min	4	5	ns
	t_{AVHW}	AVD# Hold Time to WE#		Min	4	5	ns
	t_{ACS}	Address Setup Time to CLK (Notes 2, 3)		Min	4	5	ns
	t_{ACH}	Address Hold Time to CLK (Notes 2, 3)		Min	6	7	ns
	t_{AVHC}	AVD# Hold Time to CLK		Min	4	5	ns
	t_{CSW}	Clock Setup Time to WE#		Min	5		ns

Notes:

1. *Not 100% tested.*
2. *Asynchronous mode allows the Asynchronous program operation only. Synchronous mode allows both Asynchronous and Synchronous program operation.*
3. *In asynchronous program operation timing, addresses are latched on the falling edge of WE# or rising edge of AVD#. In synchronous program operation timing, addresses are latched on the first of either the falling edge of WE# or the active edge of CLK.*
4. *See the "Erase and Programming Performance" section for more information.*
5. *Does not include the preprogramming time.*

AC CHARACTERISTICS

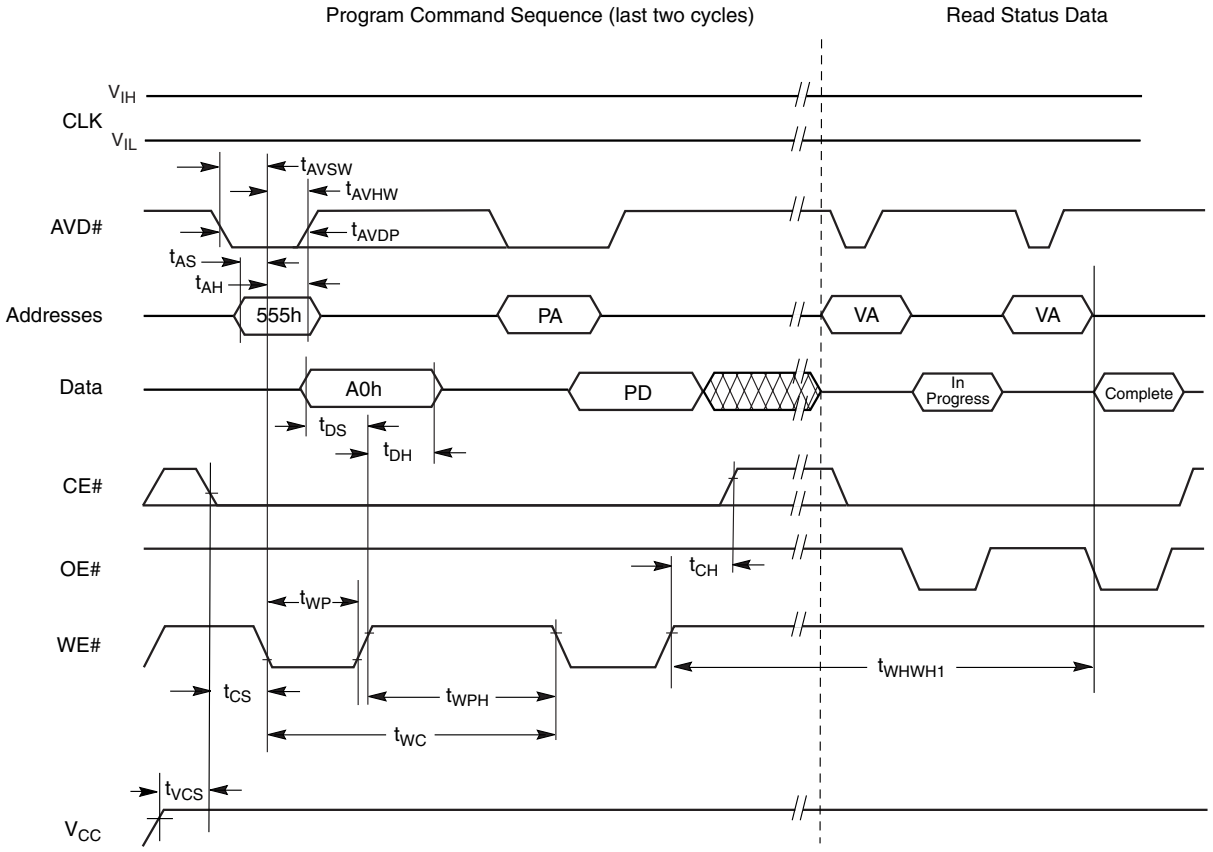


Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A21–A12 are don't care during command sequence unlock cycles.*
4. *CLK can be either V_{IL} or V_{IH}.*
5. *The Asynchronous programming operation is independent of the Set Device Read Mode bit in the Configuration Register.*

Figure 31. Asynchronous Program Operation Timings: AVD# Latched Addresses

AC CHARACTERISTICS

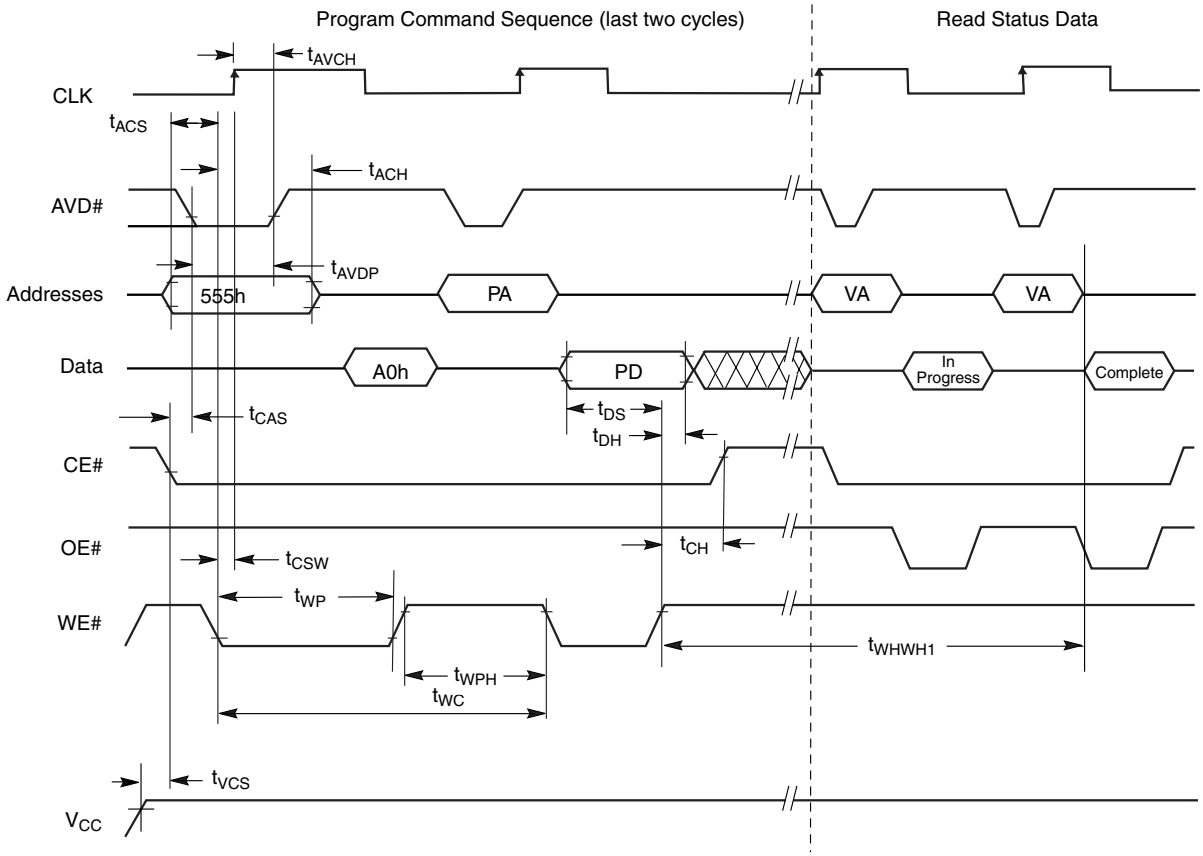


Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A21–A12 are don't care during command sequence unlock cycles.*
4. *CLK can be either V_{IL} or V_{IH}.*
5. *The Asynchronous programming operation is independent of the Set Device Read Mode bit in the Configuration Register.*

Figure 32. Asynchronous Program Operation Timings: WE# Latched Addresses

AC CHARACTERISTICS

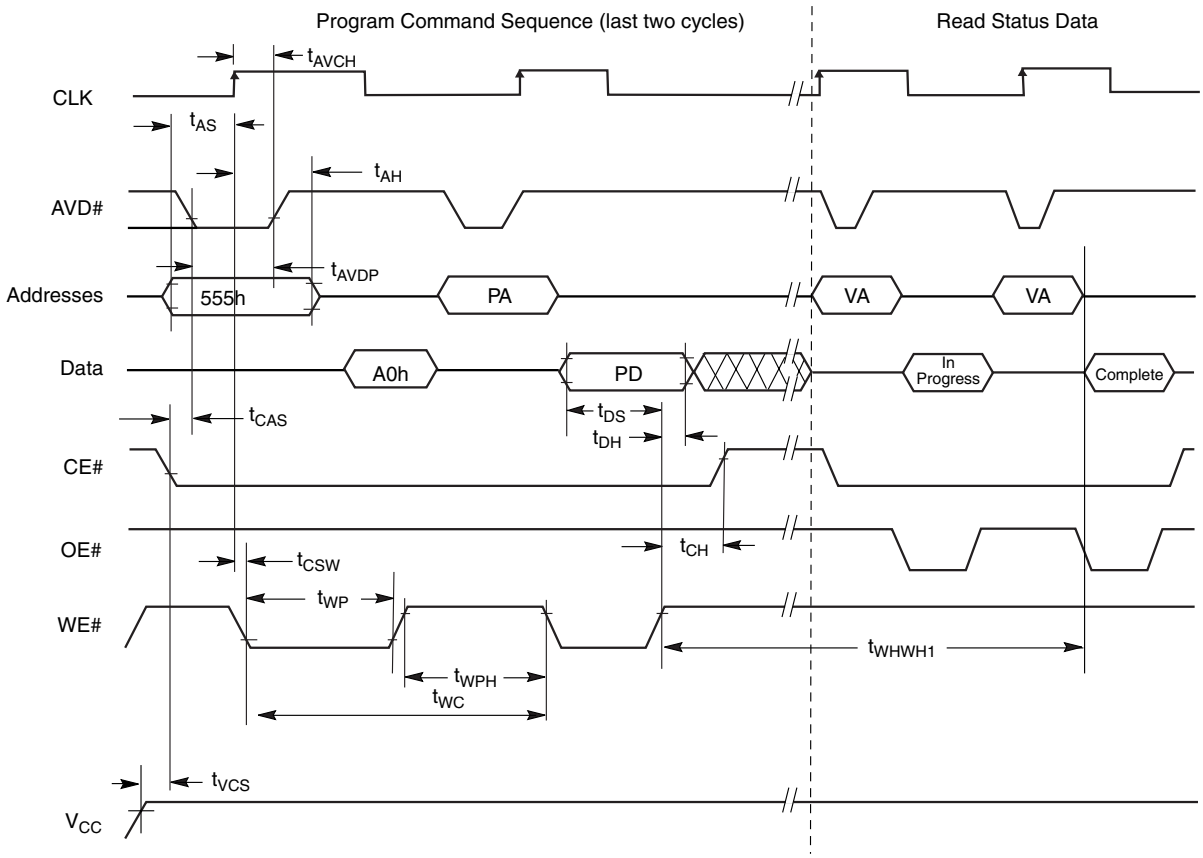


Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A21–A12 are don't care during command sequence unlock cycles.*
4. *Addresses are latched on the first of either the rising edge of AVD# or the active edge of CLK.*
5. *Either CE# or AVD# is required to go from low to high in between programming command sequences.*
6. *The Synchronous programming operation is dependent of the Set Device Read Mode bit in the Configuration Register. The Configuration Register must be set to the Synchronous Read Mode.*

Figure 33. Synchronous Program Operation Timings: WE# Latched Addresses

AC CHARACTERISTICS



Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A21–A12 are don't care during command sequence unlock cycles.*
4. *Addresses are latched on the first of either the rising edge of AVD# or the active edge of CLK.*
5. *Either CE# or AVD# is required to go from low to high in between programming command sequences.*
6. *The Synchronous programming operation is dependent of the Set Device Read Mode bit in the Configuration Register. The Configuration Register must be set to the Synchronous Read Mode.*

Figure 34. Synchronous Program Operation Timings: CLK Latched Addresses

AC CHARACTERISTICS

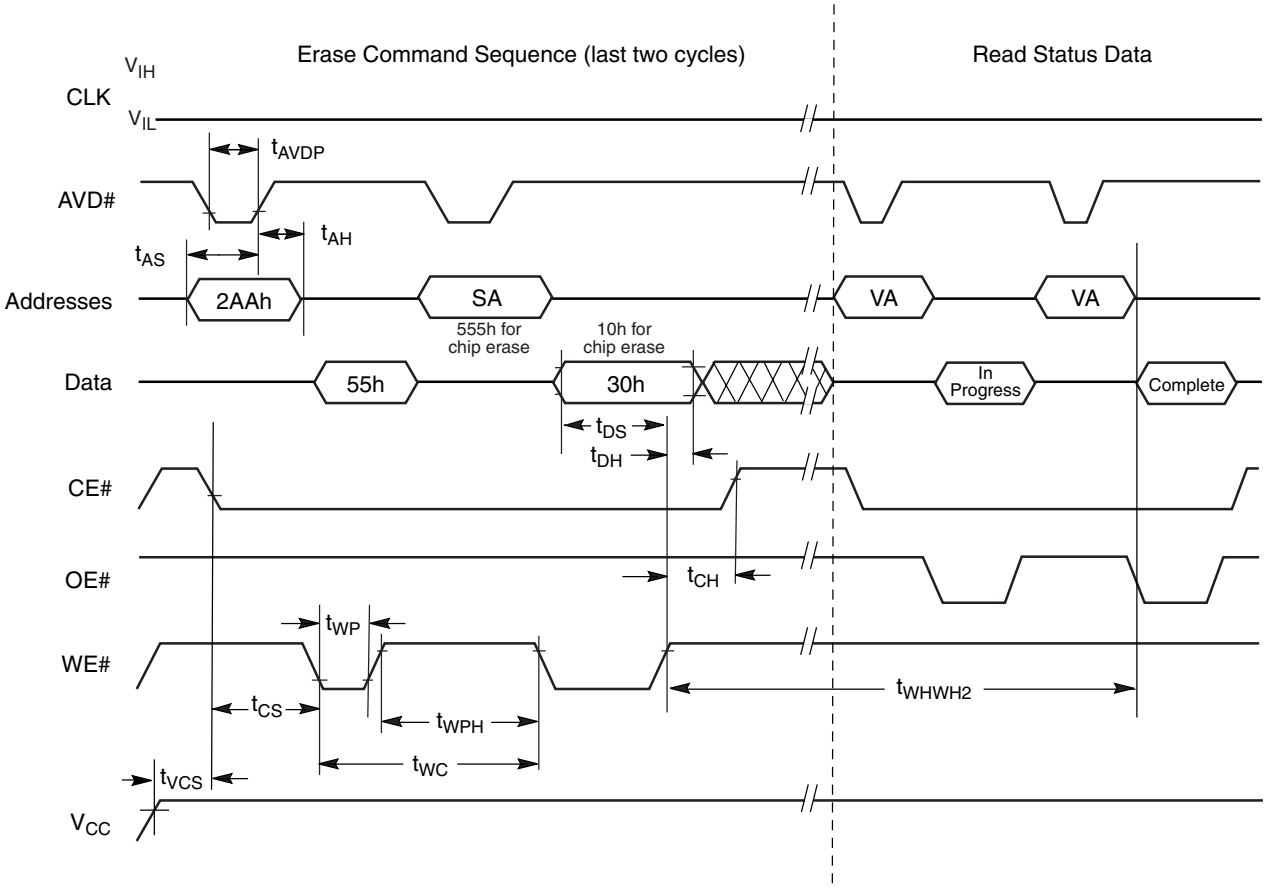
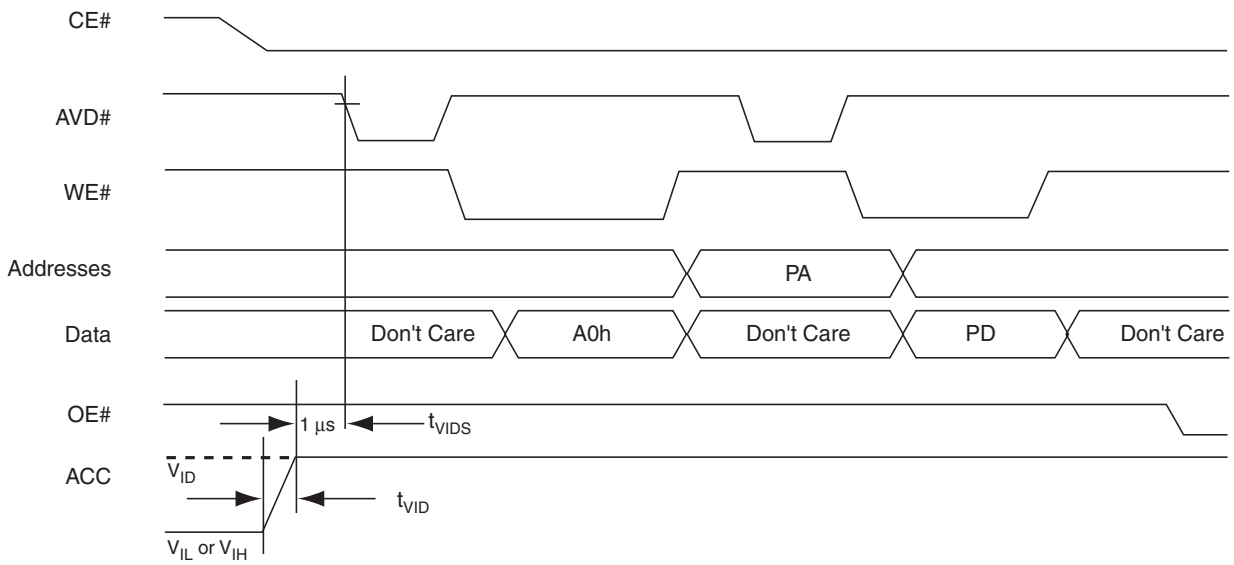


Figure 35. Chip/Sector Erase Command Sequence

Notes:

1. *SA is the sector address for Sector Erase.*
2. *Address bits A21–A12 are don't cares during unlock cycles in the command sequence.*

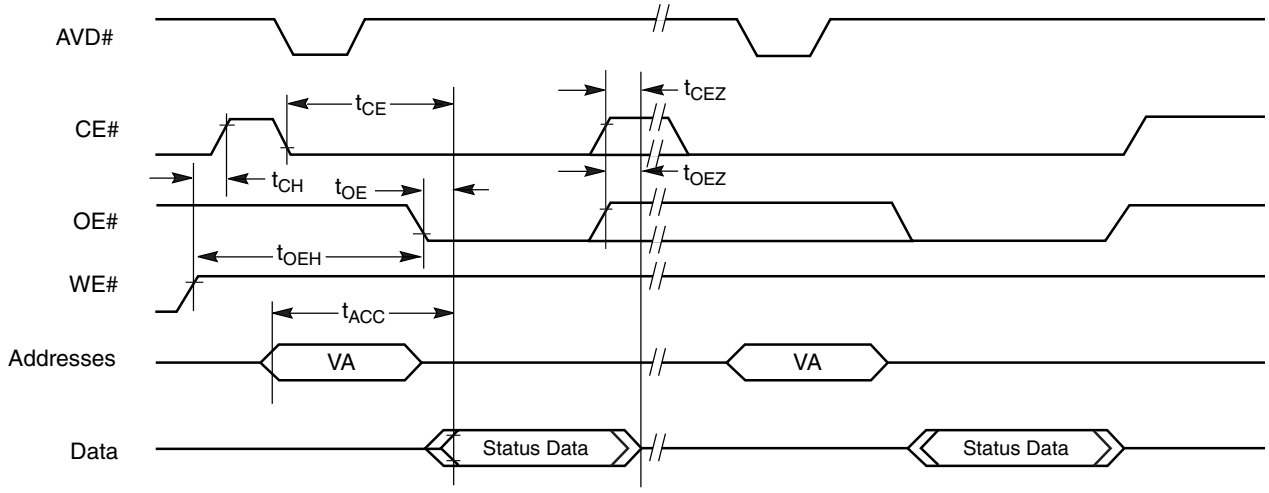
AC CHARACTERISTICS



Note: *Use setup and hold times from conventional program operation.*

Figure 36. Accelerated Unlock Bypass Programming Timing

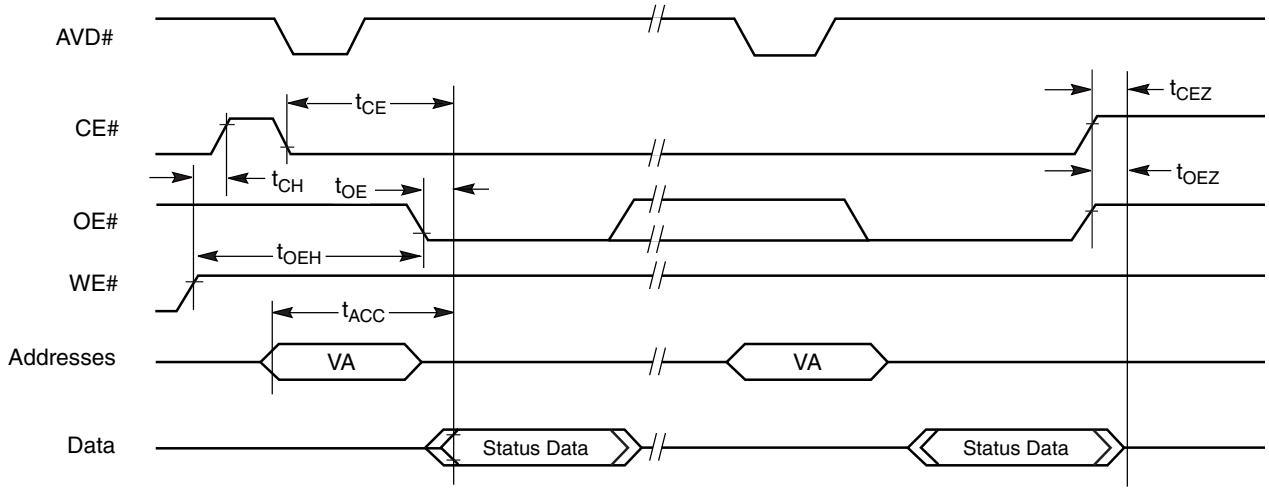
AC CHARACTERISTICS



Notes:

1. *Status reads in figure are shown as asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, and Data# Polling will output true data.*
3. *While in Asynchronous mode, RDY will be low while the device is in embedded erase or programming mode.*

Figure 37. Data# Polling Timings (During Embedded Algorithm)

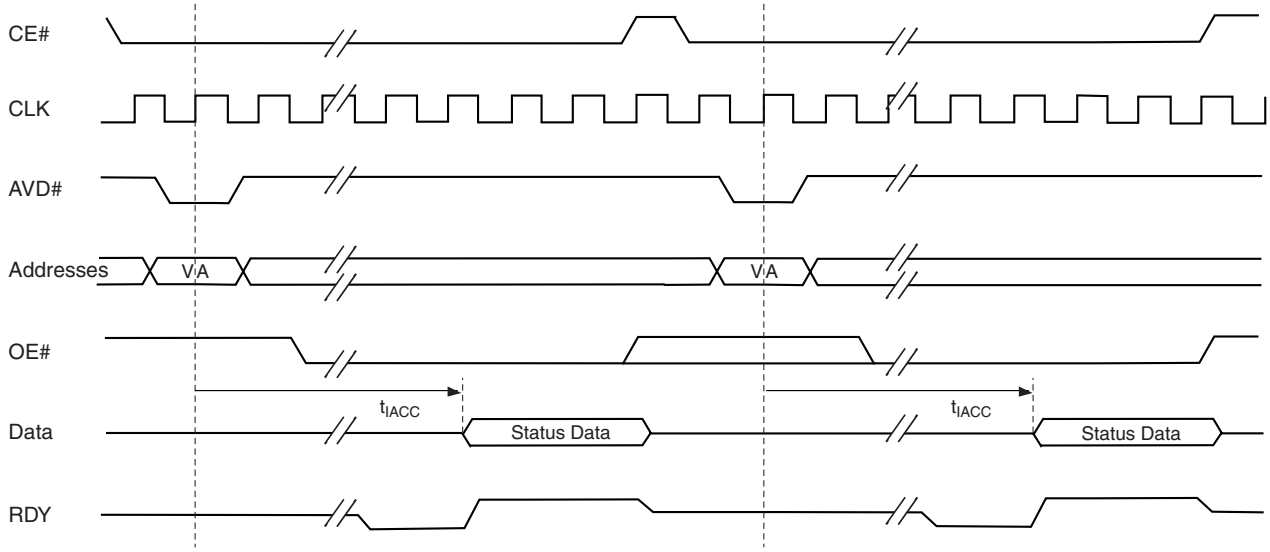


Notes:

1. *Status reads in figure are shown as asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.*
3. *While in Asynchronous mode, RDY will be low while the device is in embedded erase or programming mode.*

Figure 38. Toggle Bit Timings (During Embedded Algorithm)

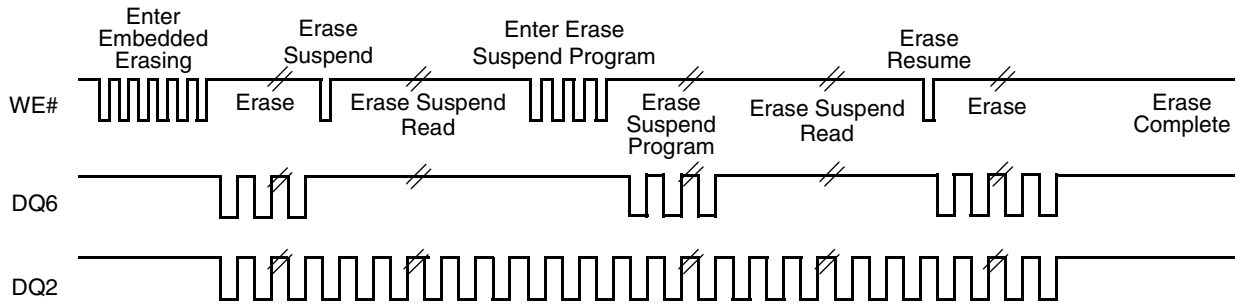
AC CHARACTERISTICS



Notes:

1. *The timings are similar to synchronous read timings.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.*
3. *RDY is active with data (A18 = 0 in the Configuration Register). When A18 = 1 in the Configuration Register, RDY is active one clock cycle before data.*

Figure 39. Synchronous Data Polling Timings/Toggle Bit Timings



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 40. DQ2 vs. DQ6

AC CHARACTERISTICS

Temporary Sector Unprotect

Parameter					
JEDEC	Std	Description		All Speed Options	Unit
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min	250	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RDY High for Temporary Sector Unprotect	Min	4	µs

Note: *Not 100% tested.*

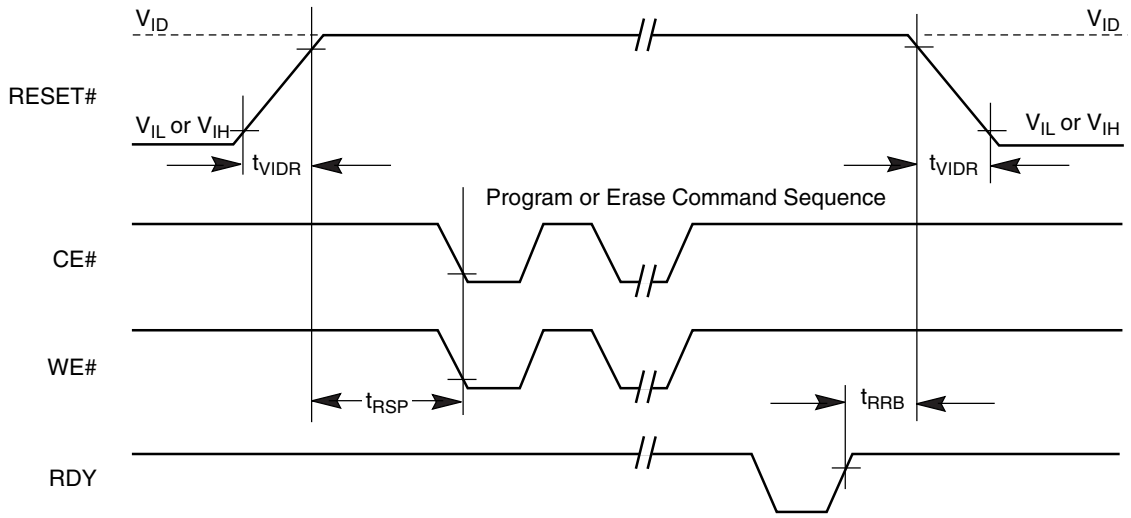
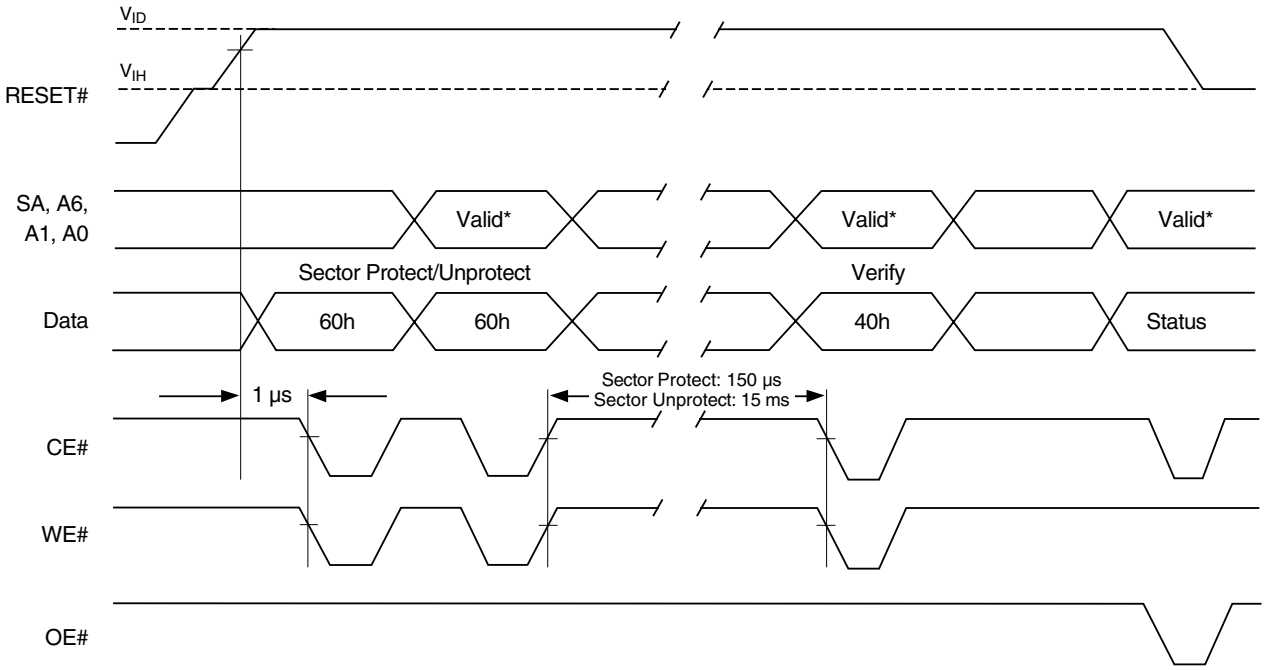


Figure 41. Temporary Sector Unprotect Timing Diagram

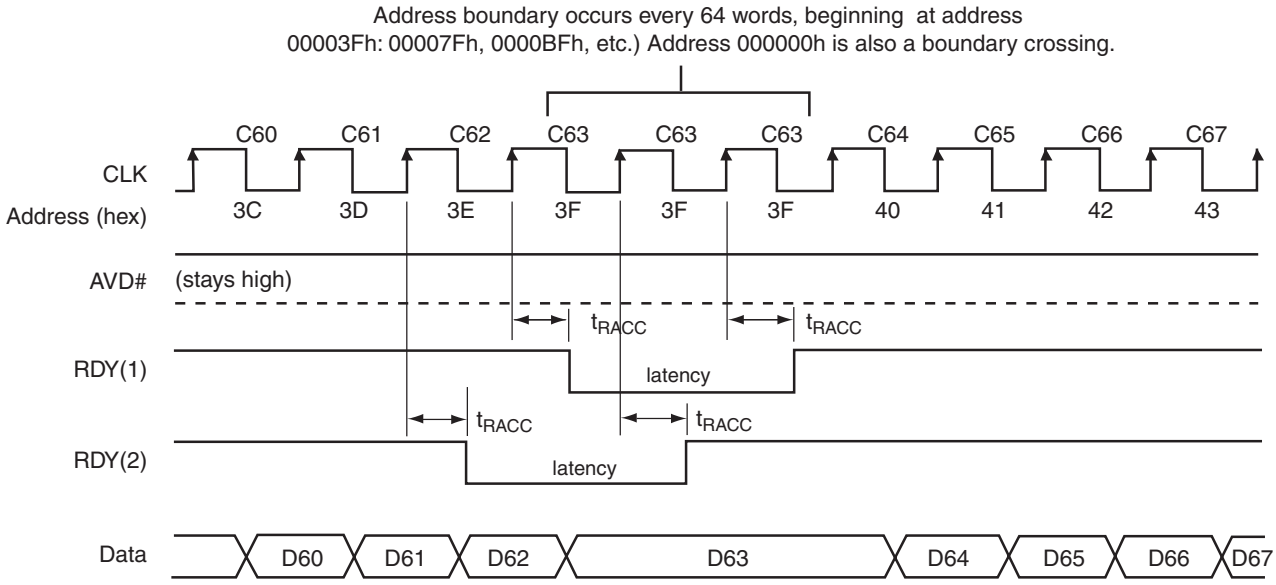
AC CHARACTERISTICS



* *For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

Figure 42. Sector/Sector Block Protect and Unprotect Timing Diagram

AC CHARACTERISTICS)

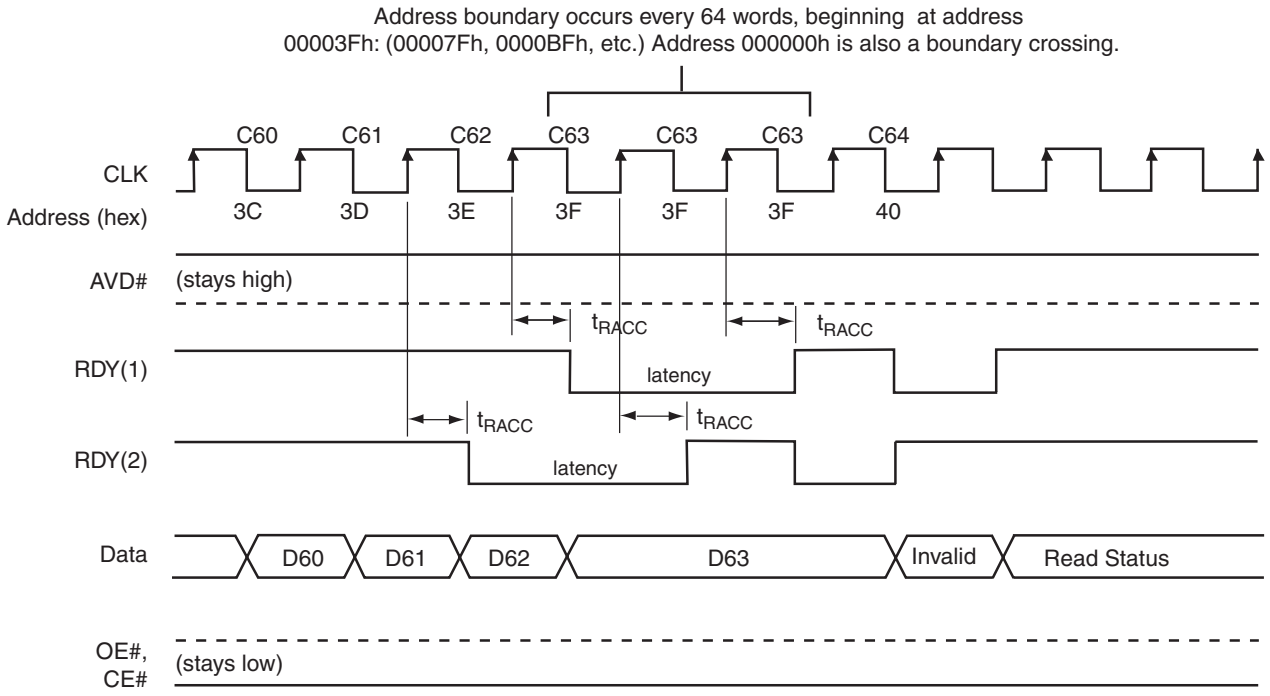


Notes:

1. *RDY active with data (A18 = 0 in the Configuration Register).*
2. *RDY active one clock cycle before data (A18 = 1 in the Configuration Register).*
3. *Cxx indicates the clock that triggers Dxx on the outputs; for example, C60 triggers D60. Figure shows the device not crossing a bank in the process of performing an erase or program.*
4. *If the starting address latched in is either 3Eh or 3Fh (or some 64 multiple of either), there is no additional 2 cycle latency at the boundary crossing.*

Figure 43. Latency with Boundary Crossing

AC CHARACTERISTICS

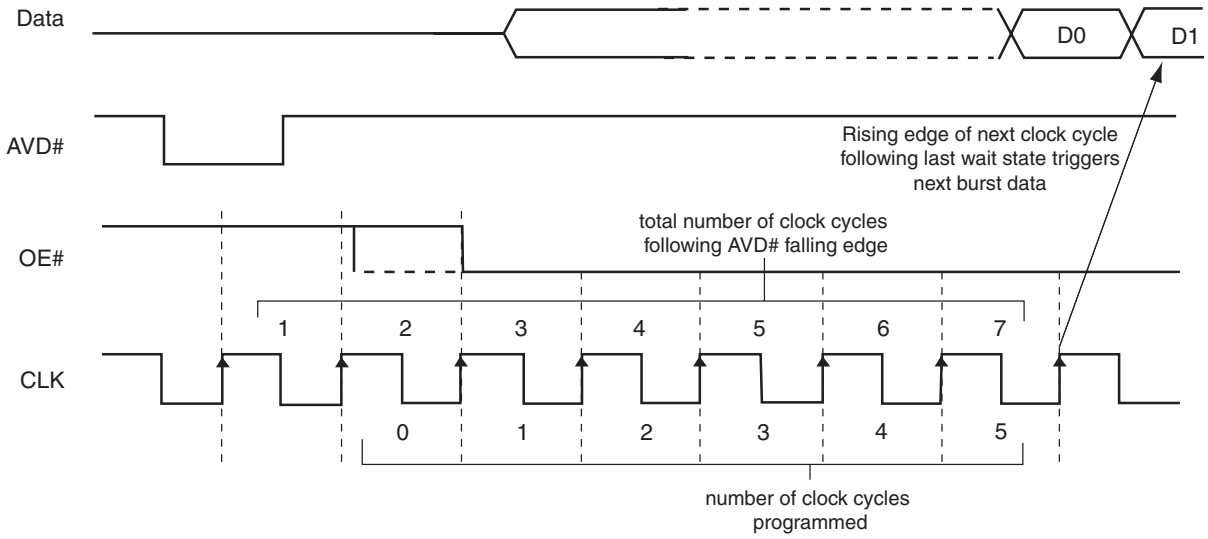


Notes:

1. *RDY active with data (A18 = 0 in the Configuration Register).*
2. *RDY active one clock cycle before data (A18 = 1 in the Configuration Register).*
3. *Cxx indicates the clock that triggers Dxx on the outputs; for example, C60 triggers D60. Figure shows the device crossing a bank in the process of performing an erase or program.*

Figure 44. Latency with Boundary Crossing into Program/Erase Bank

AC CHARACTERISTICS

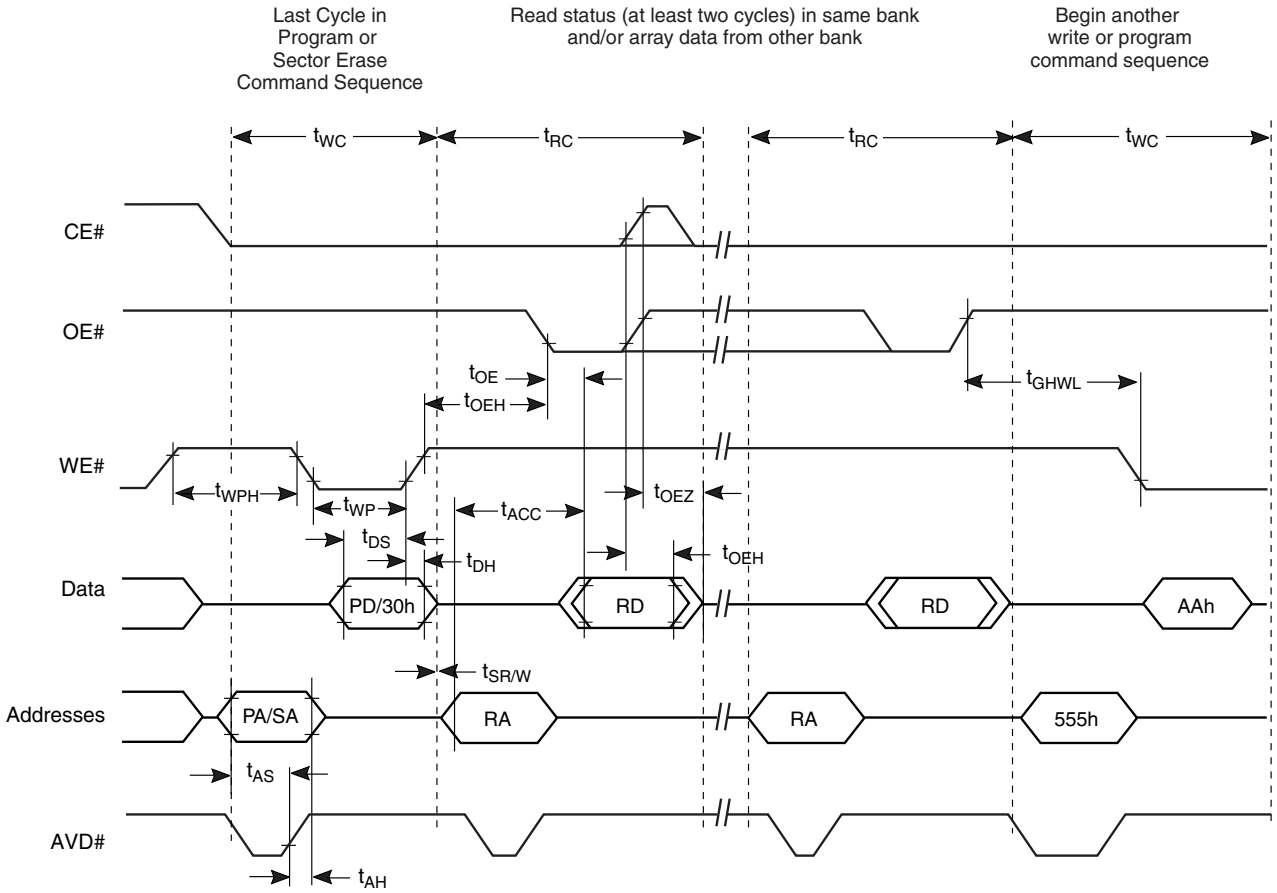


Wait State Decoding Addresses:
A14, A13, A12 = "111" ⇒ Reserved
A14, A13, A12 = "110" ⇒ Reserved
A14, A13, A12 = "101" ⇒ 5 programmed, 7 total
A14, A13, A12 = "100" ⇒ 4 programmed, 6 total
A14, A13, A12 = "011" ⇒ 3 programmed, 5 total
A14, A13, A12 = "010" ⇒ 2 programmed, 4 total
A14, A13, A12 = "001" ⇒ 1 programmed, 3 total
A14, A13, A12 = "000" ⇒ 0 programmed, 2 total

Note: *Figure assumes address D0 is not at an address boundary, active clock edge is rising, and wait state is set to "101".*

Figure 45. Example of Wait States Insertion

AC CHARACTERISTICS



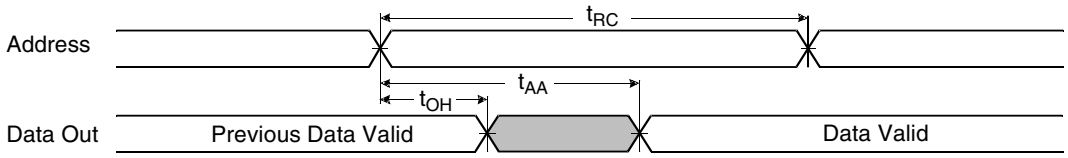
Note: *Breakpoints in waveforms indicate that system may alternately read array data from the "non-busy bank" while checking the status of the program or erase operation in the "busy" bank. The system should read status twice to ensure valid information.*

Figure 46. Back-to-Back Read/Write Cycle Timings

SRAM AC CHARACTERISTICS

Read Cycle

Parameter Symbol	Description		E6, E7, D6, D7	E8, E9, D8, D9	Unit
t_{RC}	Read Cycle Time	Min	55	70	ns
t_{AA}	Address Access Time	Max	55	70	ns
t_{CO1}, t_{CO2}	Chip Enable to Output	Max	55	70	ns
t_{OE}	Output Enable Access Time	Max	25	35	ns
t_{BA}	LB#s, UB#s to Access Time	Max	55	70	ns
t_{LZ1}, t_{LZ2}	Chip Enable (CE1#s Low and CE2s High) to Low-Z Output	Min	10		ns
t_{BLZ}	UB#, LB# Enable to Low-Z Output	Min	10		ns
t_{OLZ}	Output Enable to Low-Z Output	Min	5		ns
t_{HZ1}, t_{HZ2}	Chip Disable to High-Z Output	Max	25		ns
t_{BHZ}	UB#s, LB#s Disable to High-Z Output	Max	25		ns
t_{OHZ}	Output Disable to High-Z Output	Max	25		ns
t_{OH}	Output Data Hold from Address Change	Min	10		ns



Note: *CE1#s = OE# = V_{IL}, CE2s = WE# = V_{IH}, UB#s and/or LB#s = V_{IL}*

Figure 47. SRAM Read Cycle—Address Controlled

SRAM AC CHARACTERISTICS

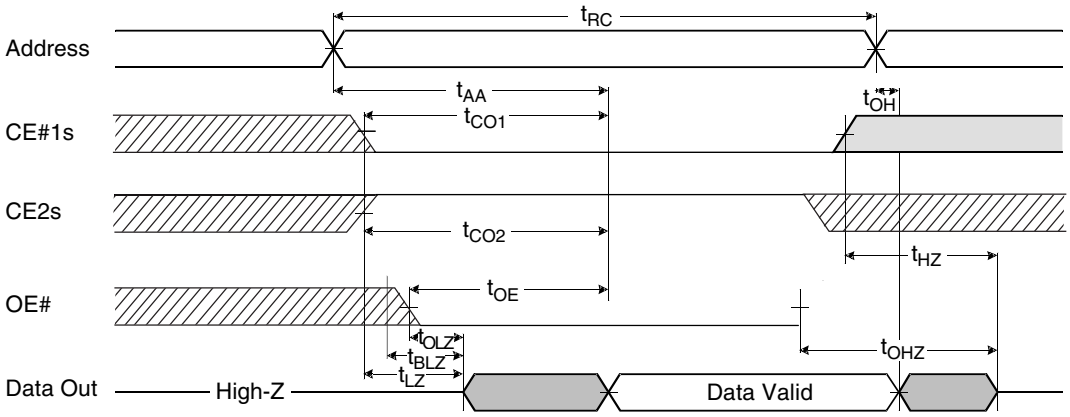


Figure 48. SRAM Read Cycle

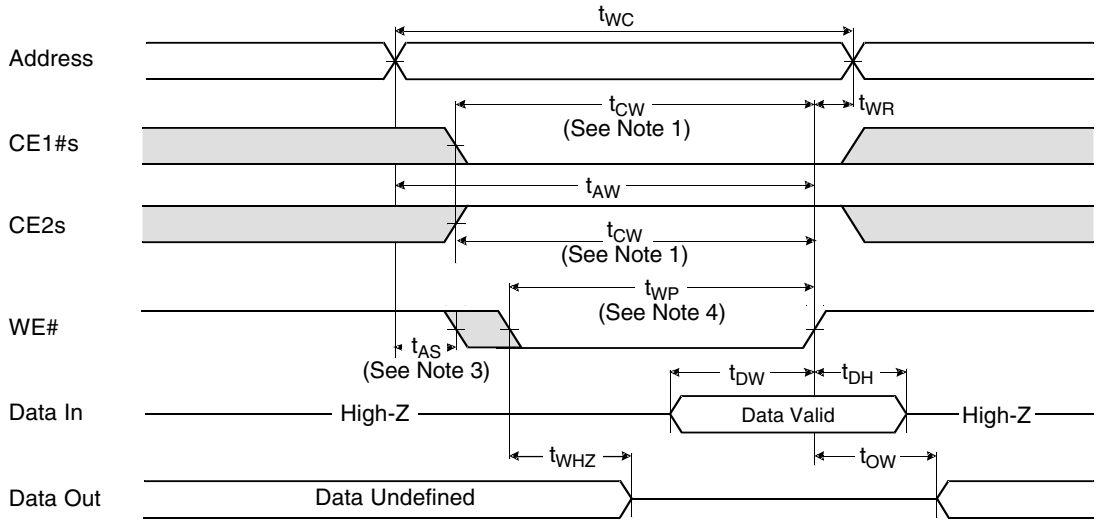
Notes:

1. *WE# = V_{IH}.*
2. *t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.*
3. *At any given temperature and voltage condition, t_{HZ} (Max.) is less than t_{LZ} (Min.) both for a given device and from device to device interconnection.*

SRAM AC CHARACTERISTICS

Write Cycle

Parameter Symbol	Description		E6, E7, D6, D7	E8, E9, D8, D9	Unit
t_{WC}	Write Cycle Time	Min	55	70	ns
t_{Cw}	Chip Enable to End of Write	Min	45	60	ns
t_{AS}	Address Setup Time	Min	0		ns
t_{AW}	Address Valid to End of Write	Min	45	60	ns
t_{BW}	UB#s, LB#s to End of Write	Min	45	60	ns
t_{WP}	Write Pulse Time	Min	45	50	ns
t_{WR}	Write Recovery Time	Min	0		ns
t_{WHZ}	Write to Output High-Z	Min	0		ns
		Max	20		
t_{DW}	Data to Write Time Overlap	Min	30		ns
t_{DH}	Data Hold from Write Time	Min	0		ns
t_{OW}	End Write to Output Low-Z	min	5		ns

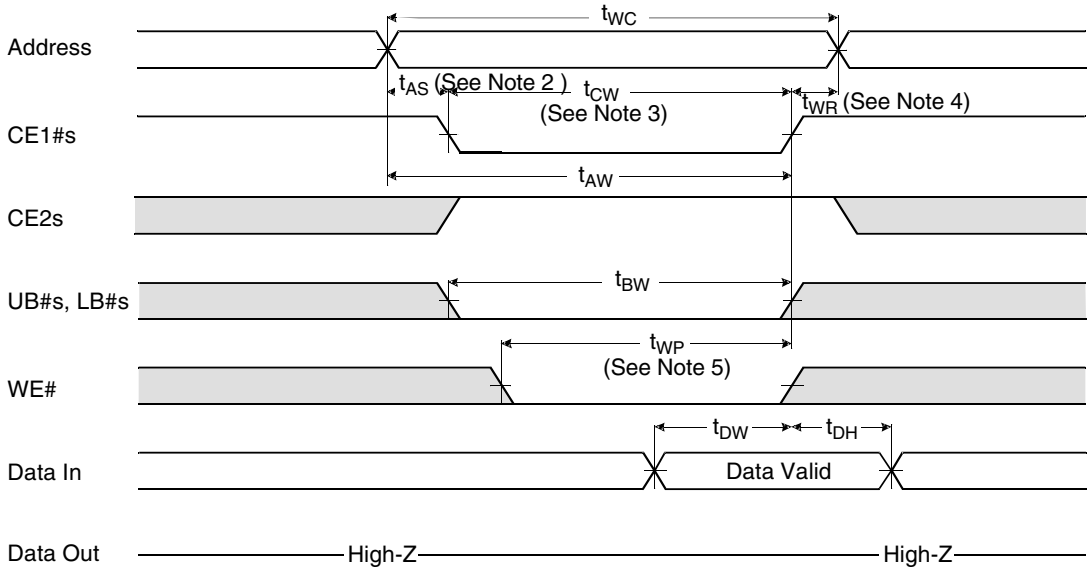


Notes:

1. *WE# controlled.*
2. *t_{CW} is measured from CE1#s going low to the end of write.*
3. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CE1#s or WE# going high.*
4. *t_{AS} is measured from the address valid to the beginning of write.*
5. *A write occurs during the overlap (t_{WP}) of low CE#1 and low WE#. A write begins when CE1#s goes low and WE# goes low when asserting UB#s or LB#s for a single byte operation or simultaneously asserting UB#s and LB#s for a double byte operation. A write ends at the earliest transition when CE1#s goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

Figure 49. SRAM Write Cycle—WE# Control

SRAM AC CHARACTERISTICS

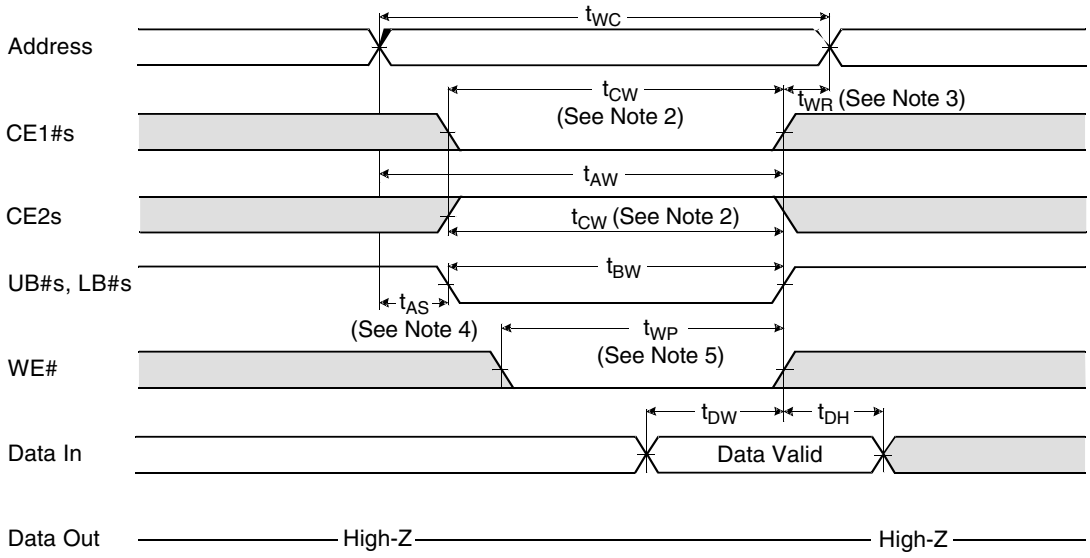


Notes:

1. *CE1#s controlled.*
2. *t_{CW} is measured from CE1#s going low to the end of write.*
3. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CE1#s or WE# going high.*
4. *t_{AS} is measured from the address valid to the beginning of write.*
5. *A write occurs during the overlap (t_{WP}) of low CE#1 and low WE#. A write begins when CE1#s goes low and WE# goes low when asserting UB#s or LB#s for a single byte operation or simultaneously asserting UB#s and LB#s for a double byte operation. A write ends at the earliest transition when CE1#s goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

Figure 50. SRAM Write Cycle—CE1#s Control

SRAM AC CHARACTERISTICS



Notes:

1. *UB#s and LB#s controlled.*
2. *t_{CW} is measured from CE1#s going low to the end of write.*
3. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CE1#s or WE# going high.*
4. *t_{AS} is measured from the address valid to the beginning of write.*
5. *A write occurs during the overlap (t_{WP}) of low CE#1 and low WE#. A write begins when CE1#s goes low and WE# goes low when asserting UB#s or LB#s for a single byte operation or simultaneously asserting UB#s and LB#s for a double byte operation. A write ends at the earliest transition when CE1#s goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

Figure 51. SRAM Write Cycle—UB#s and LB#s Control

ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	32 Kword	0.4	5	s	Excludes 00h programming prior to erasure (Note 4)
	4 Kword	0.2	5		
Chip Erase Time		54		s	
Word Programming Time		9	210	µs	Excludes system level overhead (Note 5)
Accelerated Word Programming Time		4	120	µs	
Chip Programming Time (Note 3)		38	114	s	Excludes system level overhead (Note 5)
Accelerated Chip Programming Time		17	50	s	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 1.8 V V_{CC}, 1 million cycles. Additionally, programming typicals assumes a checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 1.65 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 16, "Command Definitions," on page 40 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 1 million cycles.*

BGA BALL CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	3.9	4.7	pF

Notes:

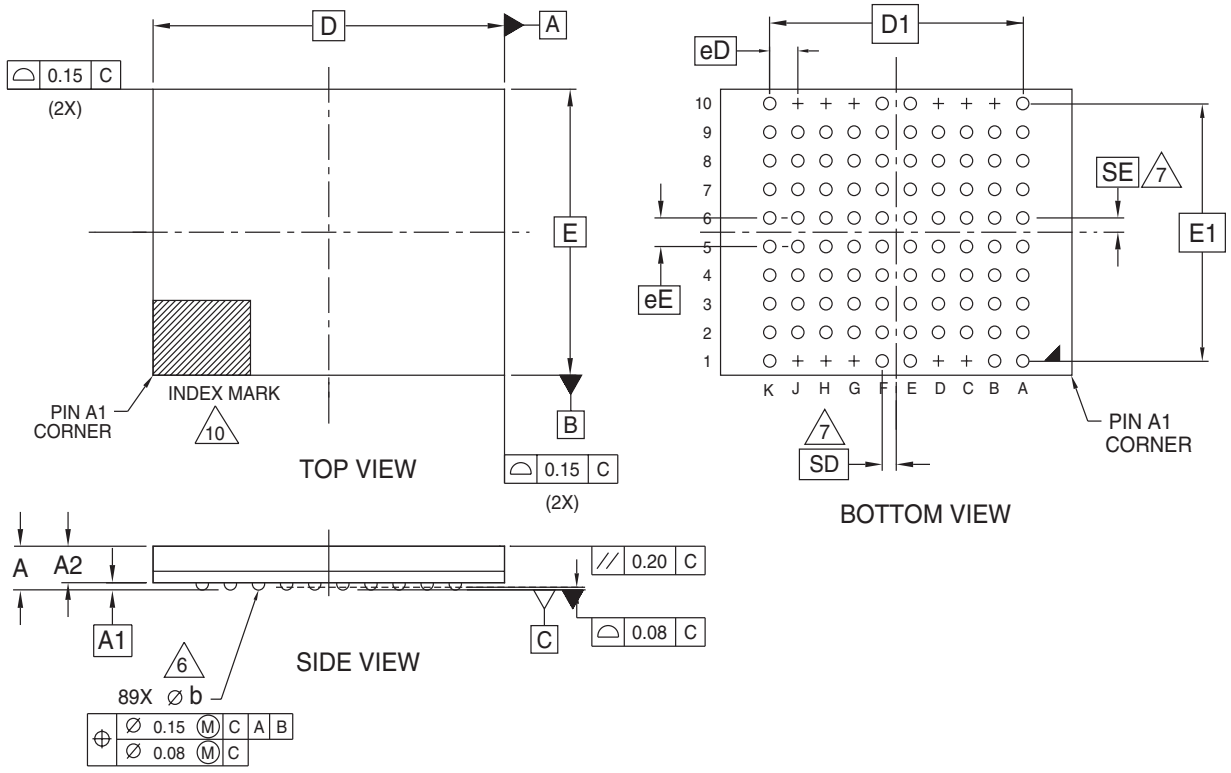
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PHYSICAL DIMENSIONS

TLB 089—89-ball Fine-Pitch Ball Grid Array (FBGA) 10 x 8 mm Package



PACKAGE	TLB089			
JEDEC	N/A			
	10.00 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		10.00 BSC.		BODY SIZE
E		8.00 BSC.		BODY SIZE
D1		7.20 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		10		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		89		BALL COUNT
ϕb	0.33	---	0.43	BALL DIAMETER
eE		0.80 BSC		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC		SOLDER BALL PLACEMENT
		B10,C1,C10,D1,D10,G1,G10 H1,H10,J1,J10		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3294\ 16-038.22a

Note: *BSC is an ANSI standard for Basic Space Centering*

REVISION SUMMARY

Revision A (July 14, 2003)

Initial release.

Revision A+1 (July 15, 2003)

Corrected Ordering Information OPNs.

Revision A+2 (July 21, 2003)

Corrected typos in datasheet regarding package name.

Revision A+3 (October 23, 2003)

Corrected globally all pSRAM to SRAM. Remove 80 MHz option throughout.

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