2.0-6.5 GHz 0.5W Power Amplifier

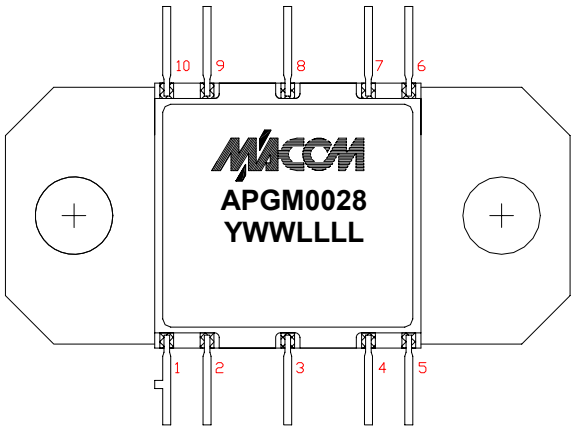
MAAPGM0028
RO-P-DS-3096
Preliminary Information

Features

- **0.5 Watt Saturated Output Power Level**
- **Variable Drain Voltage (4-10V) Operation**
- **MSAG™ Process**

Primary Applications

- **MMDS, WLL**
- **5.1- 5.9 GHz HyperLAN**
- **UNII**



Pin Number	RF Designator
1	No Connection
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3	RF IN
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5	V_{GG}
6	No Connection
7	No Connection
8	RF OUT
9	No Connection
10	V_{DD}

Description

The MAAPGM0028 is a packaged, 2-stage, 0.5W power amplifier with on-chip bias networks in a bolt down ceramic package, allowing easy assembly. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate MESFET Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes.

Maximum Operating Conditions [1]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	23.0	dBm
Drain Supply Voltage	V_{DD}	+12.0	V
Gate Supply Voltage	V_{GG}	-3.0	V
Quiescent Drain Current (No RF, 40% IDSS)	I_{DQ}	470	mA
Quiescent DC Power Dissipated (No RF)	P_{DISS}	3.2	W
Junction Temperature	T_J	180	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Processing Temperature		230	°C

1. Operation outside of these ranges may reduce product reliability.

- **North America** Tel: 800.366.2266 / Fax: 978.366.2266
- **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
- **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

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Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	V_{DD}	4.0	8.0	10.0	V
Gate Supply Voltage	V_{GG}	-2.4	-2.0	-1.5	V
Input Power	P_{IN}		18.0	21	dBm
Junction Temperature	T_J			150	°C
Thermal Resistance	Θ_{JC}		28.4		°C/W
Package Base Temperature	T_B			Note 2	°C

2. Maximum Package Base Temperature = 150°C — Θ_{JC}* V_{DD} * I_{DQ}

Electrical Characteristics: T_B = 40°C, Z_0 = 50 Ω, V_{DD} = 8V, I_{DQ} ≈ 300 mA[3], P_{in} = 18 dBm, R_G ≈ 250 Ω

Parameter	Symbol	Typical	Units
Bandwidth	f	2.0-6.5	GHz
Output Power	POUT	29	dBm
Power Added Efficiency	PAE	25	%
1-dB Compression Point	P1dB	26	dBm
Small Signal Gain	G	14	dB
Input VSWR	VSWR	2:1	
Output VSWR	VSWR	2.2:1	
Gate Supply Current	I_{GG}	< 2	mA
Drain Supply Current	I_{DD}	< 450	mA
Noise Figure	NF	8	dB
2nd Harmonic	2f	-10	dBc
3rd Harmonic	3f	-20	dBc
3rd Order Intermodulation Distortion, Single Carrier Level = 17 dBm	IM3	-20	dBm
5th Order Intermodulation Distortion, Single Carrier Level = 17 dBm	IM5	-46	dBm

3. Adjust V_{GG} between –2.4 to –1.5V to achieve indicated I_{DQ}.

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{GG} ≈ -1.8V, V_{DD}= 0 V.
2. Ramp V_{DD} to desired voltage, typically 8 V.
3. Adjust V_{GG} to set I_{DQ}, (See Note 3 above).
4. Set RF input.
5. Power down sequence in reverse. Turn V_{GG} off last.

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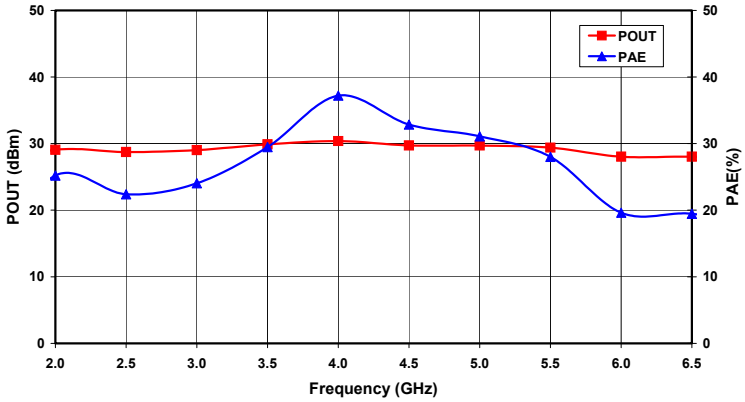

Figure 1. Output Power and Power Added Efficiency vs. Frequency at V_{DD} = 8V and P_{in} = 18 dBm

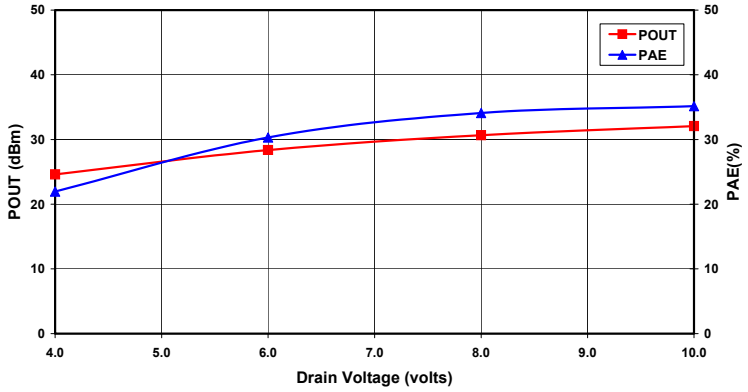

Figure 2. Saturated Output Power and Power Added Efficiency vs. Drain Voltage at f_o = 4 GHz

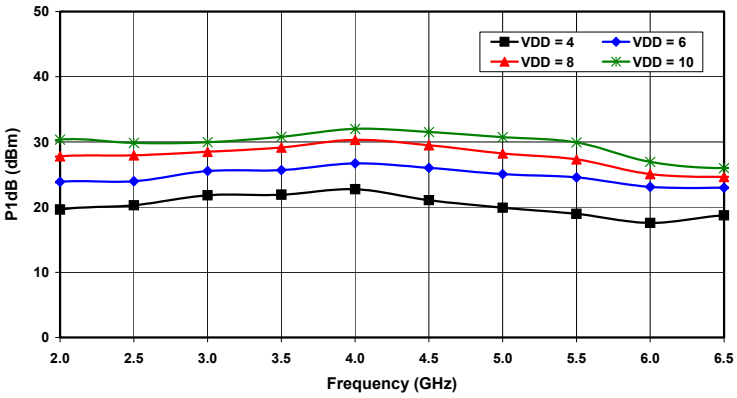

Figure 3. 1dB Compression Point vs. Drain Voltage

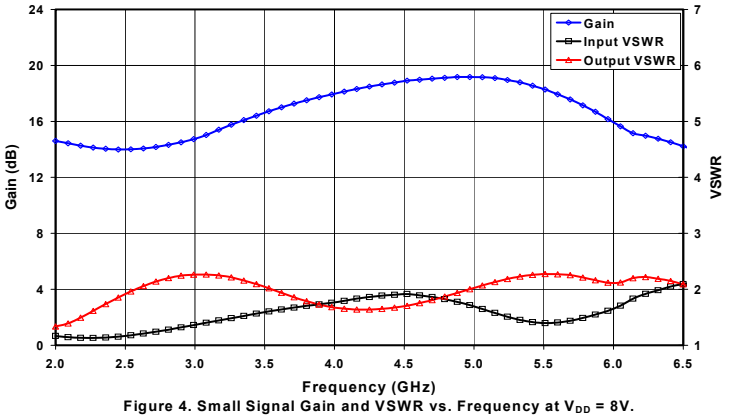

Figure 4. Small Signal Gain and VSWR vs. Frequency at V_{DD} = 8V.

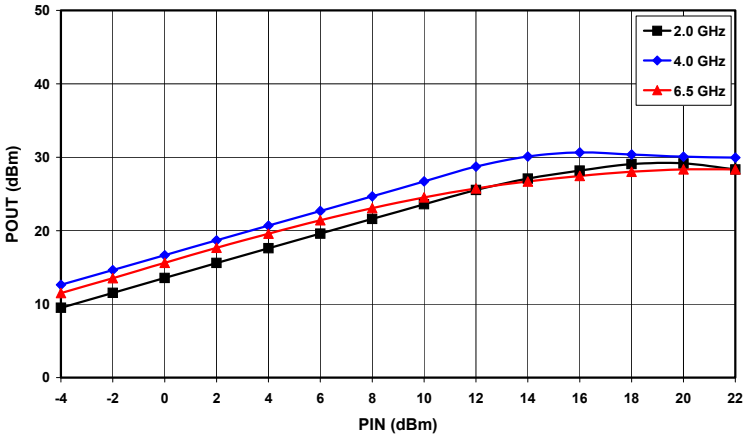

Figure 5. Output Power vs. Input Power at V_{DD} = 8V

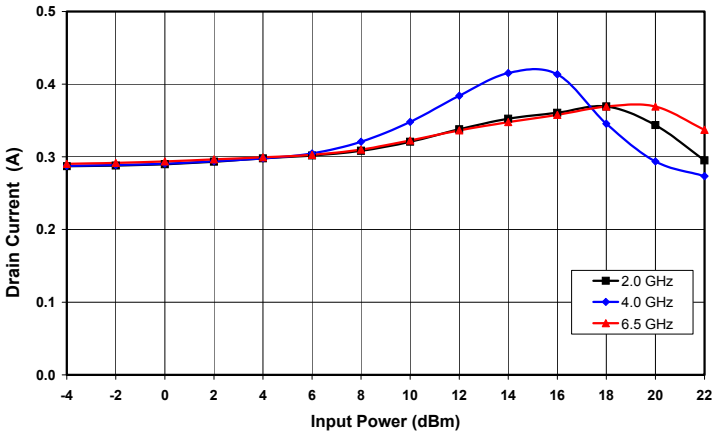

Figure 6. Drain Current vs. Input Power at V_{DD} = 8V.

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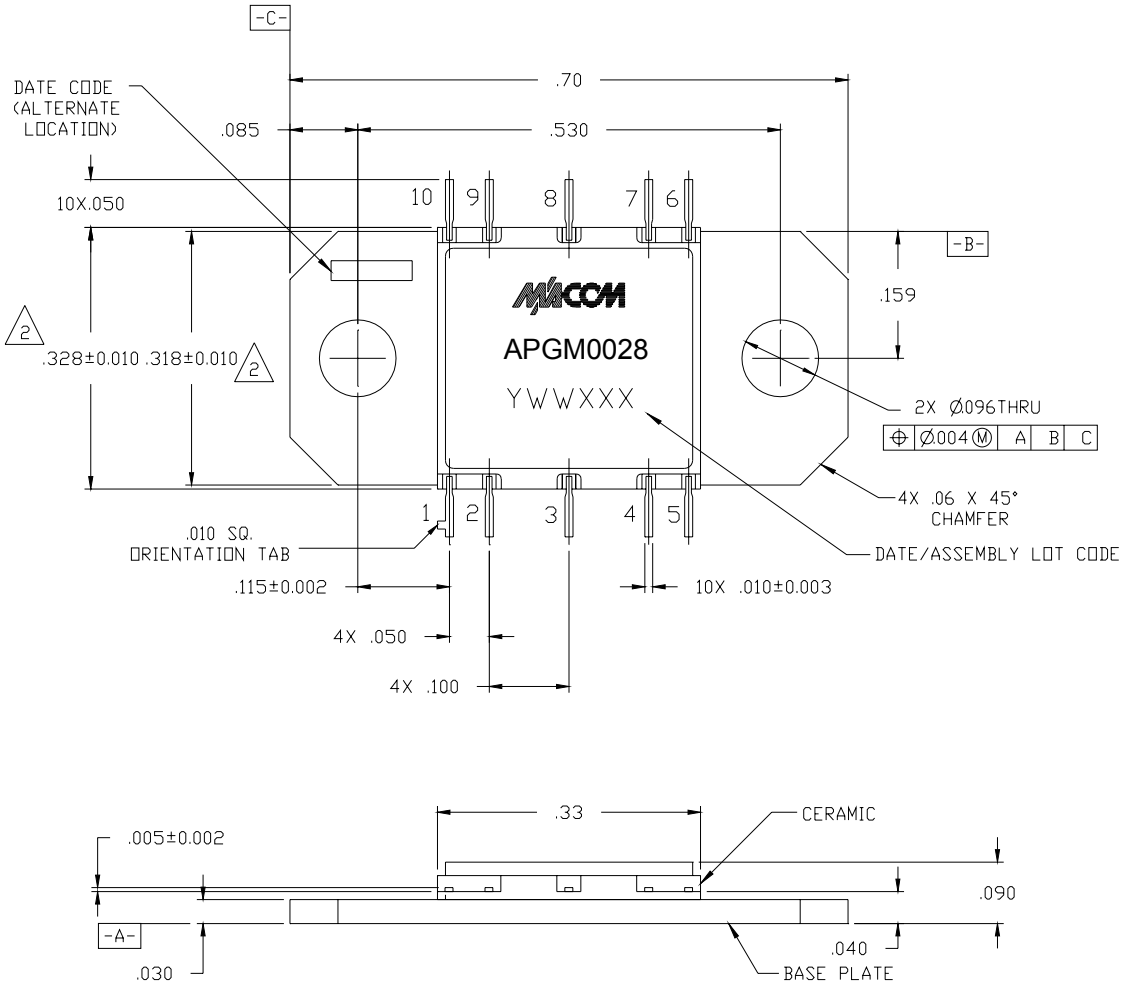

Figure 7. CR-15 Package Dimensions

The CR-15 is a high frequency, low thermal resistance package. The package consists of a cofired ceramic construction with a copper-tungsten base and iron-nickel-cobalt leads. The finish consists of electrolytic gold over nickel plate.

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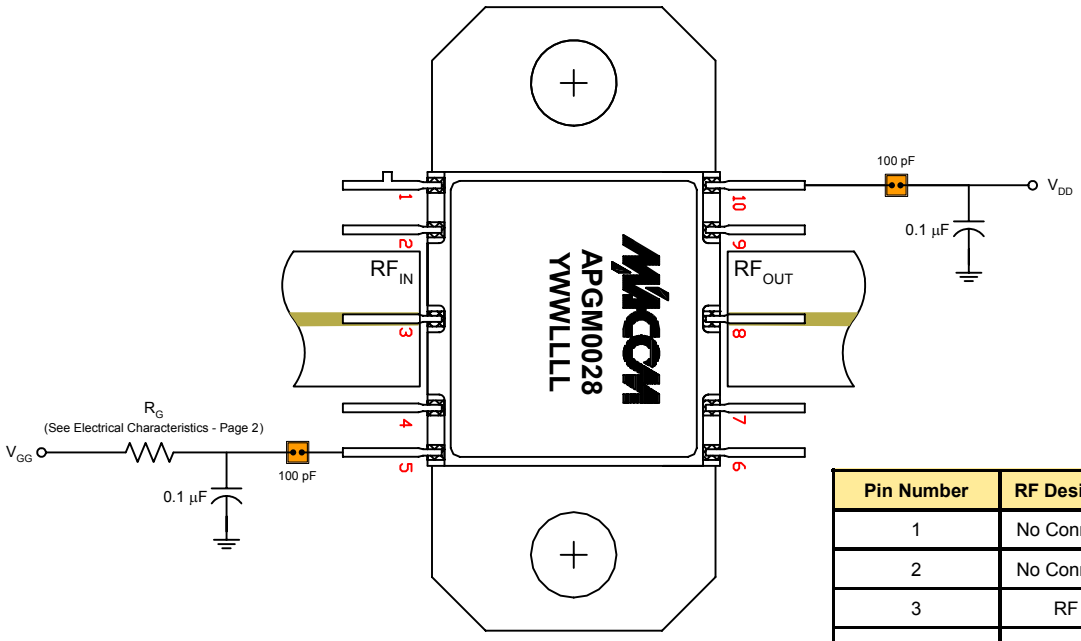
Figure 8. Recommended Bias Configuration



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Assembly Instructions:

This flange mount style package provides a robust interface between a highly integrated GaAs MMIC device and a circuit board which may be assembled using conventional surface mount techniques. A thin shim made of a thermally and electrically conductive, ductile material should be used prior to installation of the CR-15 to improve the thermal and electrical performance of the package to housing interface. Refer to **M/A-COM Application Note #M567*** for more information .

For applications where surface mount components are to be installed after the CR-15 installation, this package will not be damaged when subjected to typical convection or IR oven reflow profiles. Refer to **M/A-COM Application Note #M538*** for maximum allowable reflow time and temperature. Alternatively, the package leads may be individually soldered. Whether an iron or hot gas soldering equipment is used, care should be taken to insure that the temperature is well controlled and electric static discharge (ESD) safe.

* Application Notes can be found by going to the Site Search Page on M/A-COM's web page (http://www.macom.com/search/search.jsp) and searching for the required Application Note.

Biasing Notes:

- The 100pF bypass capacitors must be placed as close to the V_{GG} and V_{DD} pins as possible (recommended < 100 mils).
- A negative bias must be applied to V_{GG} before applying a positive bias to V_{DD} to prevent damage to the amplifier.

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