

Amplifier, Power, 1.2W  
9.0-12.0 GHz

MAAP-000038-PKG003

Rev —  
Advance Information

## Features

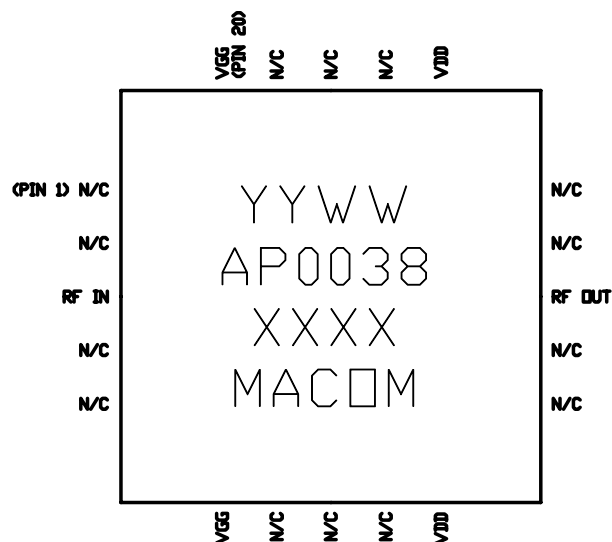
- ◆ 2 Watt Saturated Output Power Level
- ◆ Variable Drain Voltage (4-10V) Operation
- ◆ MSAG Process
- ◆ 5x5 mm 20 Lead MLP Package

## Description

The MAAP-000038-PKG003 is a packaged, 3-stage, 1.2 W power amplifier with on-chip bias networks in a 20 lead MLP package, allowing easy assembly. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate MESFET Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.



## Primary Applications

- ◆ Point-to-Point Radio
- ◆ Weather Radar
- ◆ Airborne Radar

## Maximum Operating Conditions<sup>1</sup>

Parameter	Symbol	Absolute Maximum	Units
Input Power	P <sub>IN</sub>	21.0	dBm
Drain Supply Voltage	V <sub>DD</sub>	+12.0	V
Gate Supply Voltage	V <sub>GG</sub>	-3.0	V
Quiescent Drain Current (No RF, 40% IDSS)	I <sub>DQ</sub>	1.15	A
Quiescent DC Power Dissipated (No RF)	P <sub>DISS</sub>	7.5	W
Junction Temperature	T <sub>J</sub>	180	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C
Processing Temperature		230	°C

1. Operation beyond these limits may result in permanent damage to the part.

## Recommended Operating Conditions<sup>2</sup>

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	V <sub>DD</sub>	4.0	8.0	10.0	V
Gate Supply Voltage	V <sub>GG</sub>	-2.4	-2.0	-1.3	V
Input Power	P <sub>IN</sub>		16.0	19.0	dBm
Junction Temperature	T <sub>J</sub>			150	°C
Thermal Resistance	Θ <sub>JC</sub>		12.3		°C/W
Package Base Temperature	T <sub>B</sub>			Note 3	°C

2. Operation outside of these ranges may reduce product reliability.

3. Maximum Package Base Temperature = 150°C — Θ<sub>JC</sub> \* V<sub>DD</sub> \* I<sub>DQ</sub>

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Visit [www.macom.com](http://www.macom.com) for additional data sheets and product information.

**Electrical Characteristics:**  $T_B = 40^\circ\text{C}^4$ ,  $Z_0 = 50 \text{ W}$ ,  $V_{DD} = 8\text{V}$ ,  $I_{DQ} \approx 710 \text{ mA}^3$ ,  $P_{in} = 16 \text{ dBm}$ ,  $R_G \approx 100 \Omega$

Parameter	Symbol	Typical*	Units
Bandwidth	f	9-12	GHz
Output Power	POUT	31.5	dBm
Power Added Efficiency	PAE	17	%
1-dB Compression Point	P1dB	30	dBm
Small Signal Gain	G	21	dB
Input VSWR	VSWR	3	—
Output VSWR	VSWR	2.5:1	—
Gate Supply Current	$I_{GG}$	<10	mA
Drain Supply Current	$I_{DD}$	0.9	A
Noise Figure	NF	9	dB
2 <sup>nd</sup> Harmonic	2f	-20	dBc
3 <sup>rd</sup> Harmonic	3f	-36	dBc
Output Third Order Intercept	OTOI	40	dBm
3 <sup>rd</sup> Order Intermodulation Distortion, Single Carrier Level = 21 dBm	IM3	-13	dBm
5 <sup>th</sup> Order Intermodulation Distortion, Single Carrier Level = 21 dBm	IM5	-30	dBm

4. Adjust  $V_{GG}$  between  $-2.4$  to  $-1.3\text{V}$  to achieve indicated  $I_{DQ}$ .

## Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply  $V_{GG} \approx -1.7\text{V}$ ,  $V_{DD} = 0 \text{ V}$ .
2. Ramp  $V_{DD}$  to desired voltage, typically 8 V.
3. Adjust  $V_{GG}$  to set  $I_{DQ}$ . (See Note 3 above).
4. Set RF input.
5. Power down sequence in reverse. Turn  $V_{GG}$  off last.



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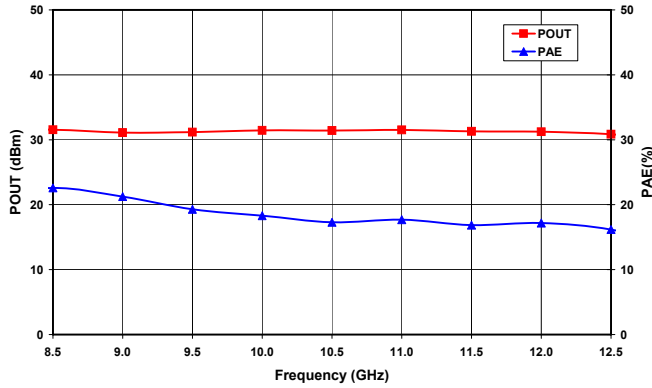


Figure 1. Output Power and Power Added Efficiency vs. Frequency at  $V_{DD} = 8V$  and  $P_{in} = 16\text{ dBm}$

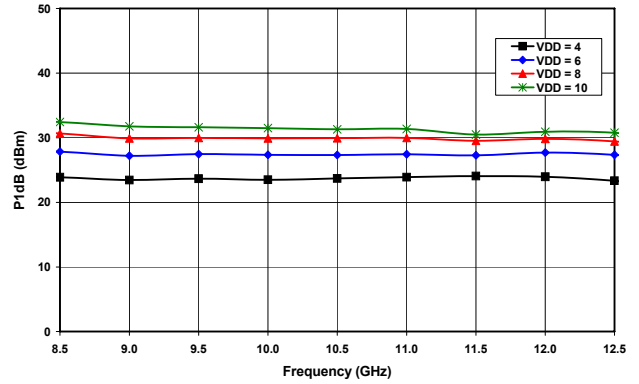


Figure 2. 1dB Compression Point vs. Drain Voltage

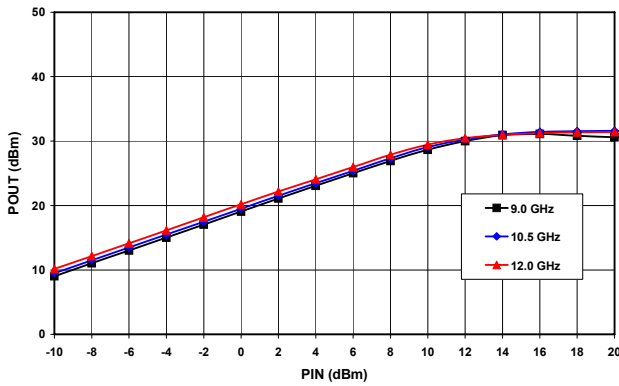


Figure 3. Output Power vs. Input Power at  $V_{DD} = 8V$

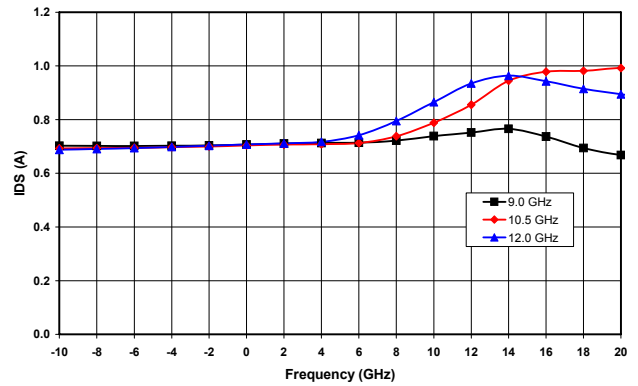


Figure 4. Drain Current vs. Input Power at  $V_{DD} = 8V$

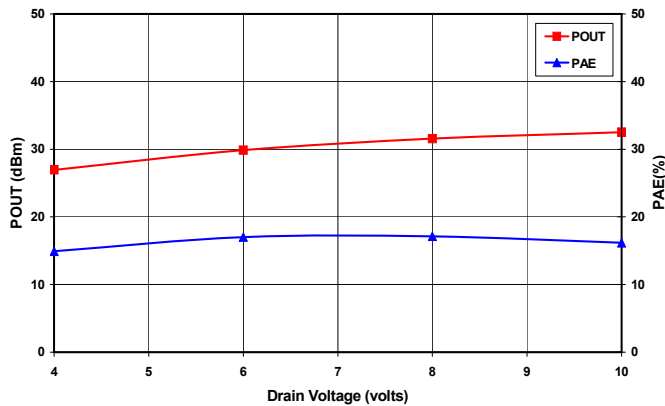


Figure 5. Saturated Output Power and Power Added Efficiency vs. Drain Voltage at  $f_0 = 10.5\text{ GHz}$

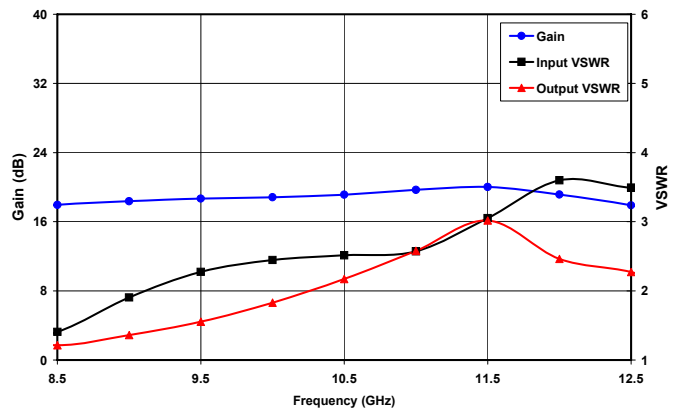


Figure 6. Small Signal Gain and VSWR vs. Frequency at  $V_{DD} = 8V$ .

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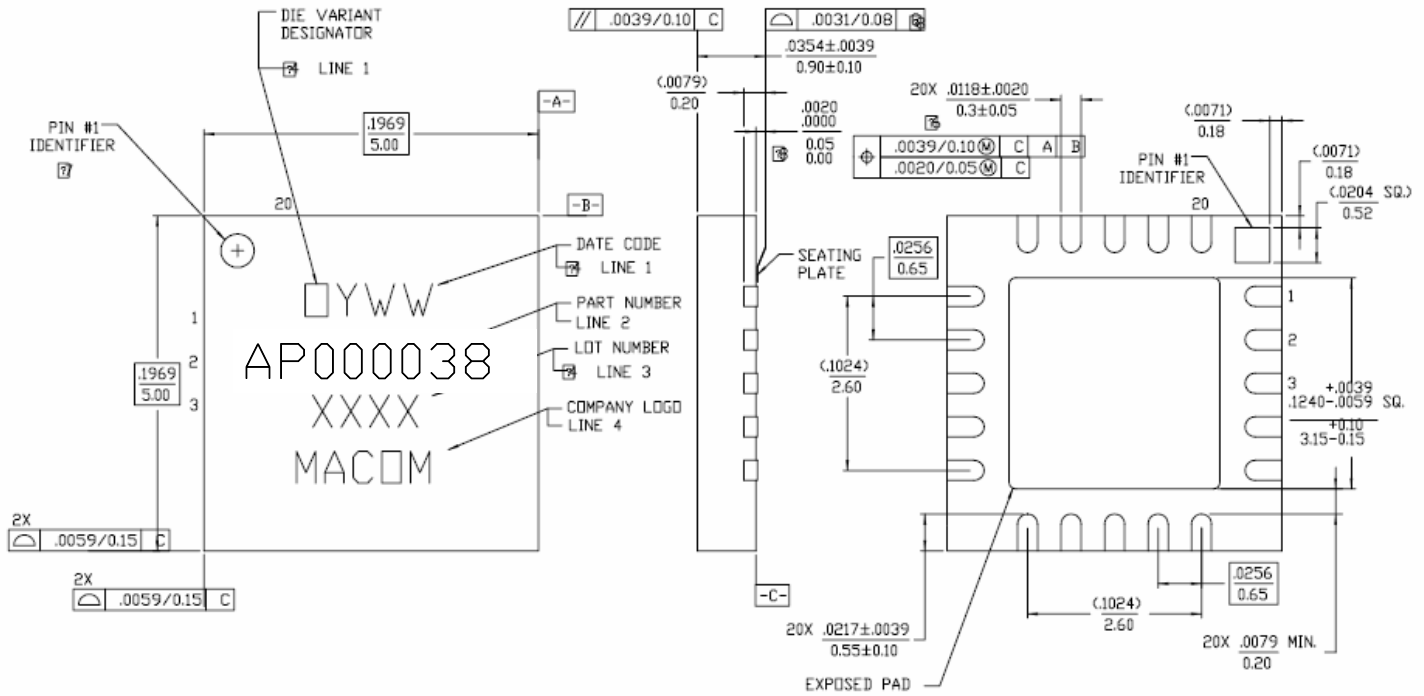


Figure 7. 5x5 mm 20-Lead MLP.

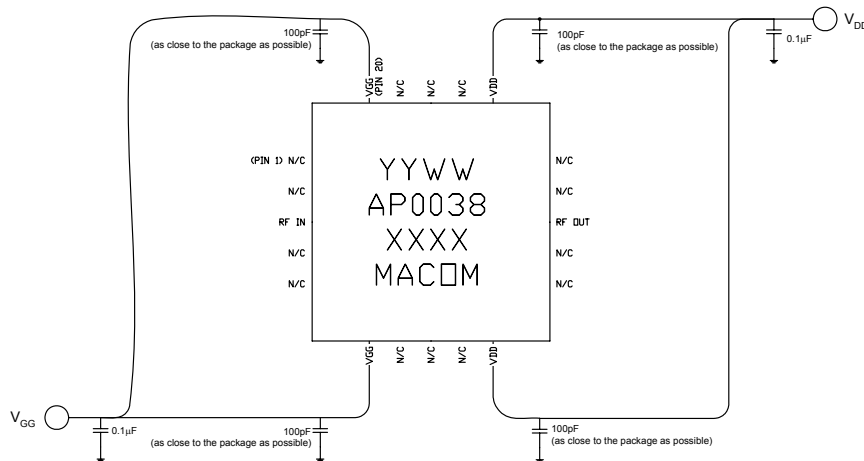


Figure 8. Recommended Bias Configuration.

Note: The exposed pad centered on the package bottom must be connected to RF and dc ground for proper electrical and thermal operation.

Refer to M/A-COM Application Note **Surface Mounting Instructions for PQFN Packages #S2083\*** for assembly guidelines.

**Additional Precaution: All parts must receive a bake-out of 125°C for 24 hours prior to any solder reflow operation.**

\*Application Notes can be found by going to the Site Search Page of M/A-COM's web page (<http://www.macom.com/search/search.jsp>) and searching for the required Application Note.

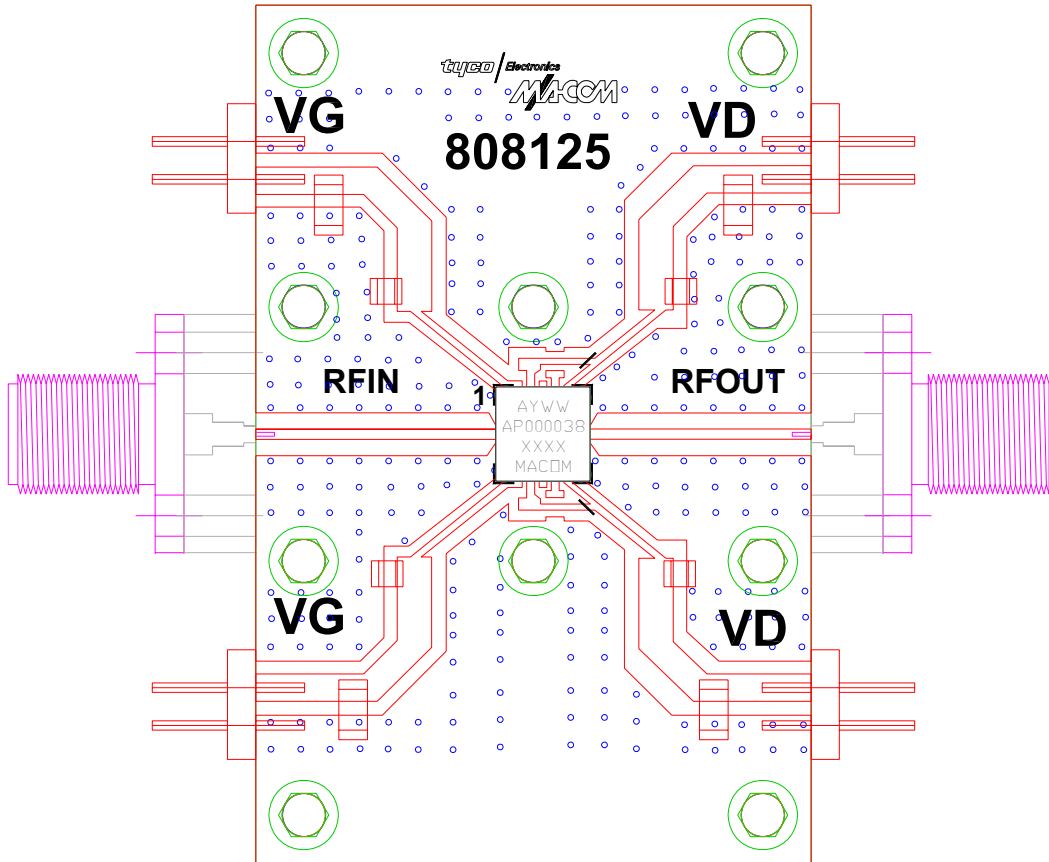


Figure 9. Demonstration Board PN MAAP-000038-PKG-SMB (available upon request).