

**Amplifier, Power, 2W  
5.7-8.5 GHz**

**MAAP-000067-PKG003**

Rev A  
Preliminary Datasheet

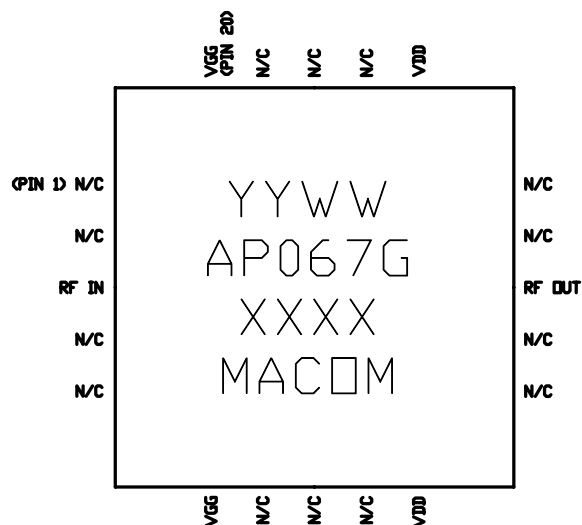
## Features

- ◆ **2 Watt Saturated Output Power Level**
- ◆ **Variable Drain Voltage (6-10V) Operation**
- ◆ **MSAG™ Process**
- ◆ **5x5 mm 20 Lead PQFN Package**

## Description

The MAAP-000067-PKG003 is a 3-stage 2 W power amplifier with on-chip bias networks in a 20 lead MLP package, allowing easy assembly. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using M/A-COM's GaAs Multifunction Self-Aligned Gate (MSAG™) Process.



## Primary Applications:

- ◆ **Point-to-Point Radio**
- ◆ **SatCom**

## Also Available in:

Also Available in:		SAMPLES		
Description	Die	Sample Board (Die)	Sample Board (Package)	Mechanical Sample (Die)
Part Number	MAAPGM0067-DIE	MAAP-000067-SMB004	MAAP-000067-SMB003	MAAP-000067-MCH000

**Electrical Characteristics:  $T_C = 35^\circ\text{C}^1$ ,  $Z_0 = 50\Omega$ ,  $V_{DD} = 8\text{V}$ ,  $I_{DQ} = 640\text{mA}^2$ ,  $P_{in} = 12\text{dBm}$ ,  $R_G=150\Omega$**

Parameter	Symbol	Typical	Units
Bandwidth	f	5.7-8.5	GHz
Output Power	$P_{OUT}$	33	dBm
1-dB Compression Point	$P_{1dB}$	33	dBm
Small Signal Gain	G	26	dB
Power Added Efficiency	PAE	30	%
Input VSWR	VSWR	1.7:1	
Output VSWR	VSWR	2.5:1	
Gate Supply Current	$I_{GG}$	7	mA
Drain Supply Current, under RF Drive	$I_{DD}$	900	mA
Output Third Order Intercept	TOI	41	dBm
Output Third Order Intermod, Single Carrier Level = 23 dBm	IM3	35	dBc

1.  $T_C$  = Case Temperature
2. Adjust  $V_{GG}$  between  $-2.6$  and  $-1.2\text{V}$  to achieve specified  $I_{DQ}$ .

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### Maximum Ratings<sup>3</sup>

Parameter	Symbol	Absolute Maximum	Units
Input Power	$P_{IN}$	17	dBm
Drain Supply Voltage	$V_{DD}$	+12.0	V
Gate Supply Voltage	$V_{GG}$	-3.0	V
Quiescent Drain Current (No RF)	$I_{DQ}$	1.02	A
Quiescent DC Power Dissipated (No RF)	$P_{DISS}$	10.2	W
Junction Temperature	$T_J$	170	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C

3. Operation beyond these limits may result in permanent damage to the part.

### Recommended Operating Conditions<sup>4</sup>

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	$V_{DD}$	6.0	8.0	10.0	V
Gate Supply Voltage	$V_{GG}$	-2.6	-2.0	-1.2	V
Input Power	$P_{IN}$		12.0	15.0	dBm
Thermal Resistance	$\Theta_{JC}$		15.6		°C/W
Case Temperature	$T_C$			Note 5	°C

4. Operation outside of these ranges may reduce product reliability.

5. Case Temperature =  $170^{\circ}\text{C} - \Theta_{JC} * V_{DD} * I_{DQ}$

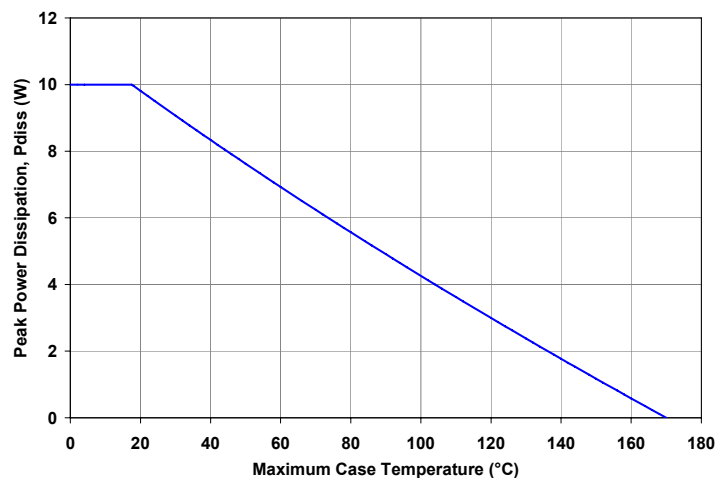


### Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply  $V_{GG} = -2.7\text{V}$ ,  $V_{DD} = 0\text{V}$ .
2. Ramp  $V_{DD}$  to desired voltage, typically 8.0 V.
3. Adjust  $V_{GG}$  to set  $I_{DQ}$ , (approximately @  $-2.0\text{V}$ ).
4. Set RF input.
5. Power down sequence in reverse. Turn  $V_{GG}$  off last.

Power Derating Curve, Quiescent (No RF)



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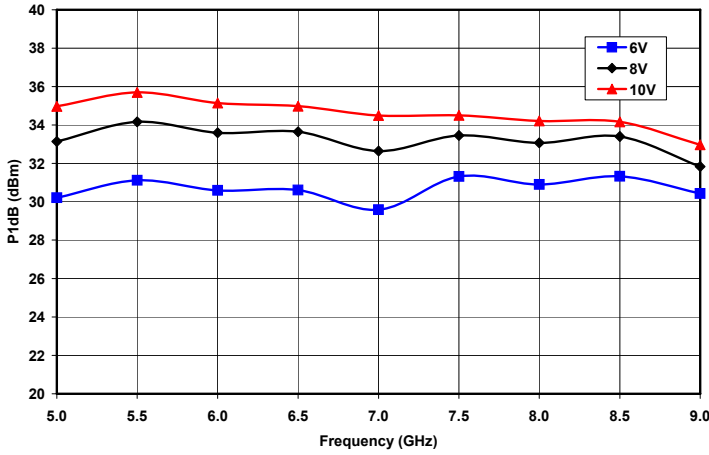


Figure 1. 1dB Compression Point vs. Frequency and Drain Voltage at IDQ = 640mA

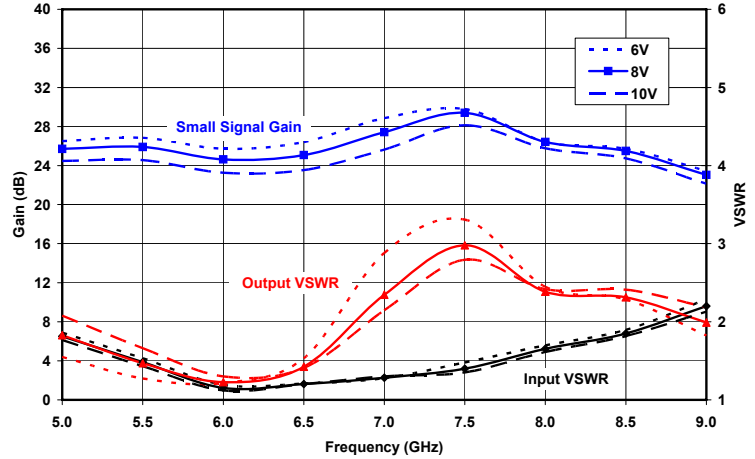


Figure 2. Small Signal Gain and Input & Output VSWR vs. Frequency and Drain Voltage at IDQ = 640 mA

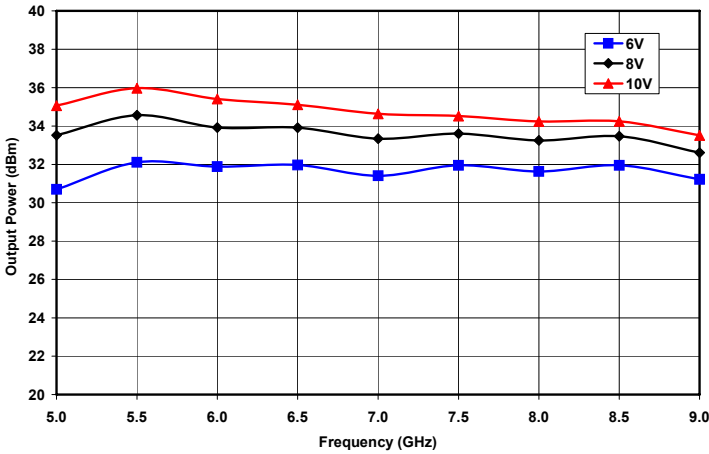


Figure 3. Saturated Output Power vs. Frequency and Drain Voltage at IDQ = 640mA

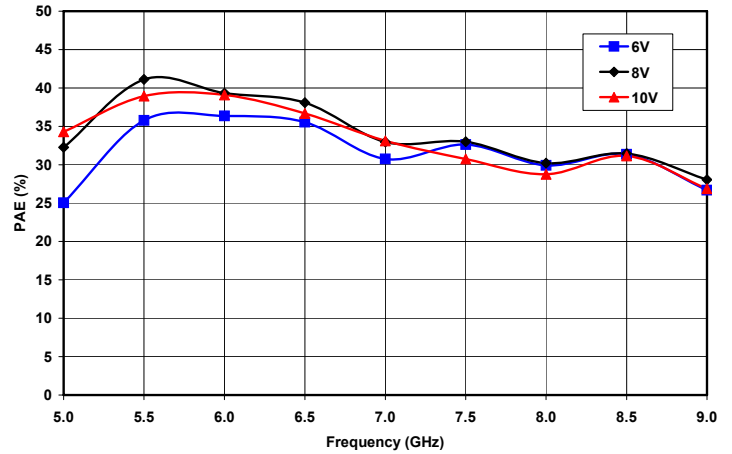


Figure 4. Saturated Power Added Efficiency vs. Frequency and Drain Voltage at IDQ = 640mA

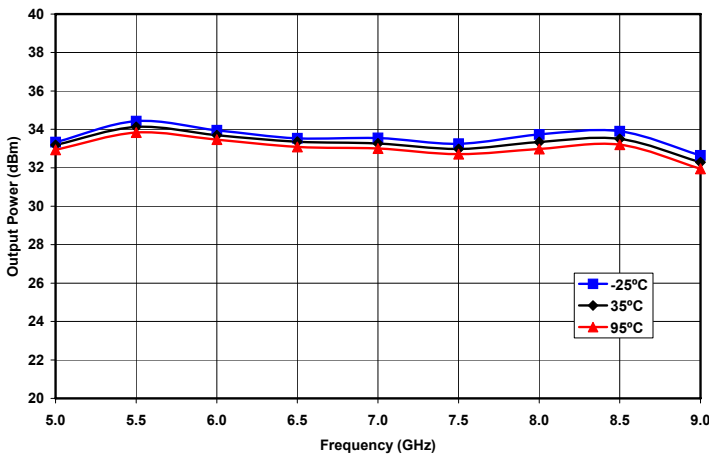


Figure 5. Saturated Output Power vs Frequency and Case Temperature at Vd = 8V and IDQ = 640mA

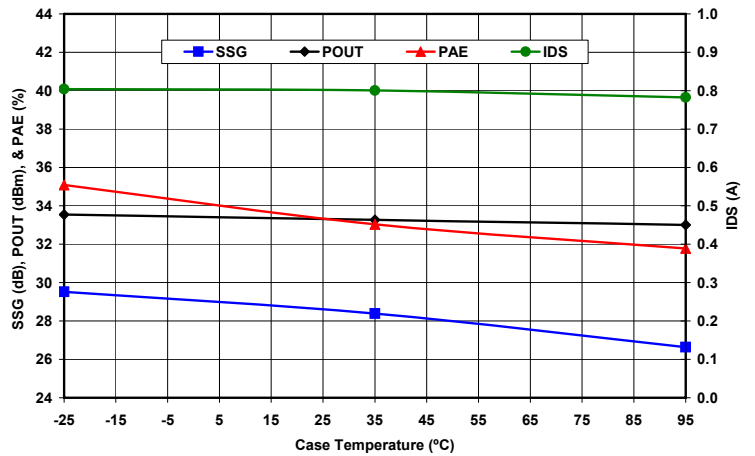


Figure 6. Small Signal Gain & Saturated Output Power, Power Added Efficiency, and Drain Current vs Case Temperature at 7GHz, Vd = 8V and IDQ = 640mA

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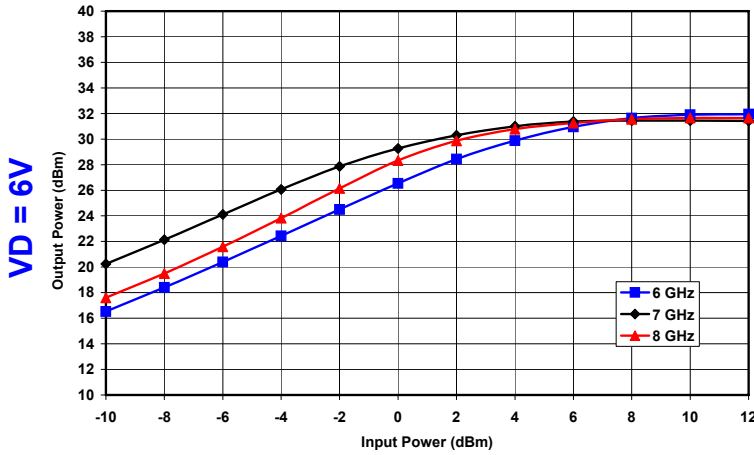


Figure 7. Output Power vs. Input Power and Frequency at VD = 6V and IDQ = 640mA

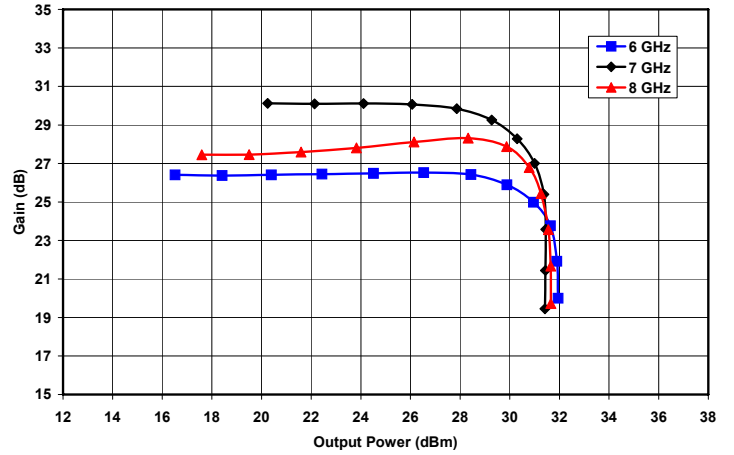


Figure 8. Gain vs. Output Power and Frequency at VD = 6V and IDQ = 640mA

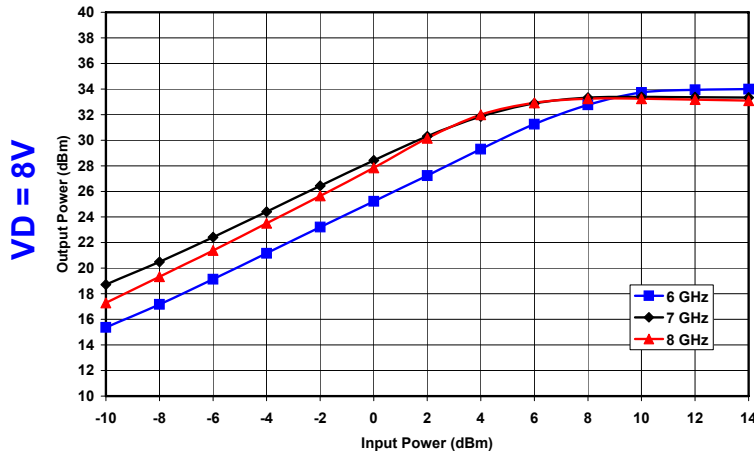


Figure 9. Output Power vs. Input Power and Frequency at VD = 8V and IDQ = 640mA

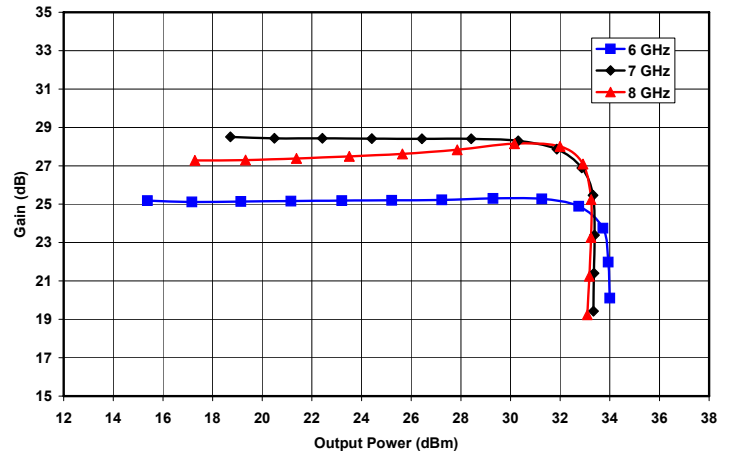


Figure 10. Gain vs. Output Power and Frequency at VD = 8V and IDQ = 640mA

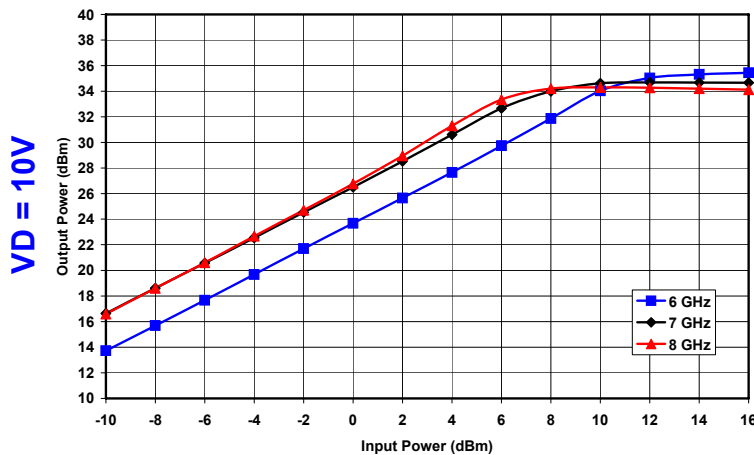


Figure 11. Output Power vs. Input Power and Frequency at VD = 10V and IDQ = 640mA

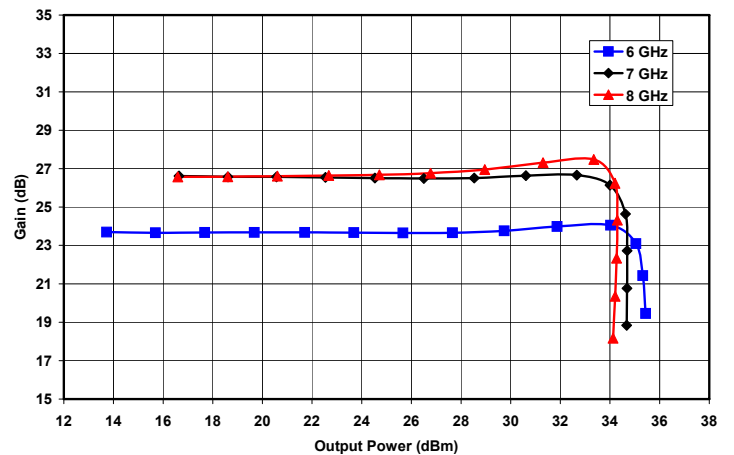


Figure 12. Gain vs. Output Power and Frequency at VD = 10V and IDQ = 640mA

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**VD = 6V**

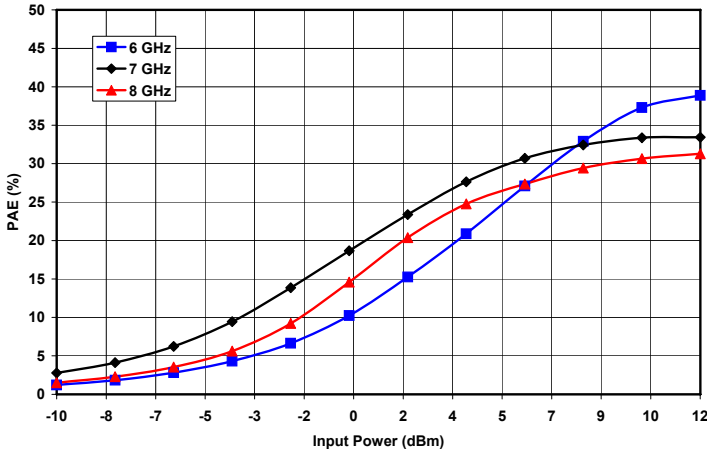


Figure 13. Power Added Efficiency vs. Input Power and Frequency at VD = 6V and IDQ = 640mA

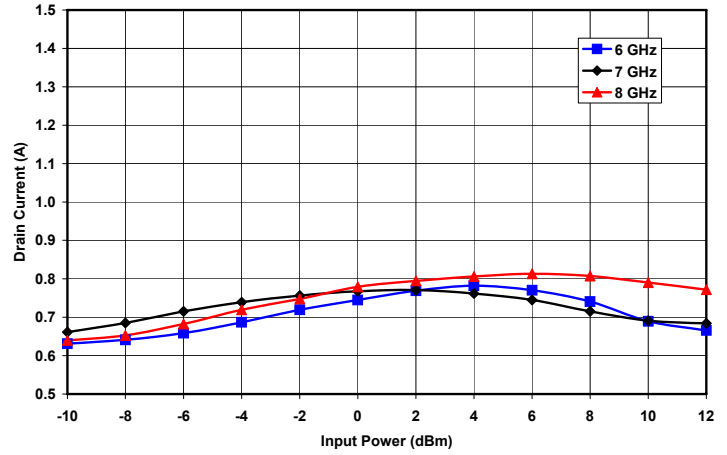


Figure 14. Drain Current vs. Input Power and Frequency at VD = 6V and IDQ = 640mA

**VD = 8V**

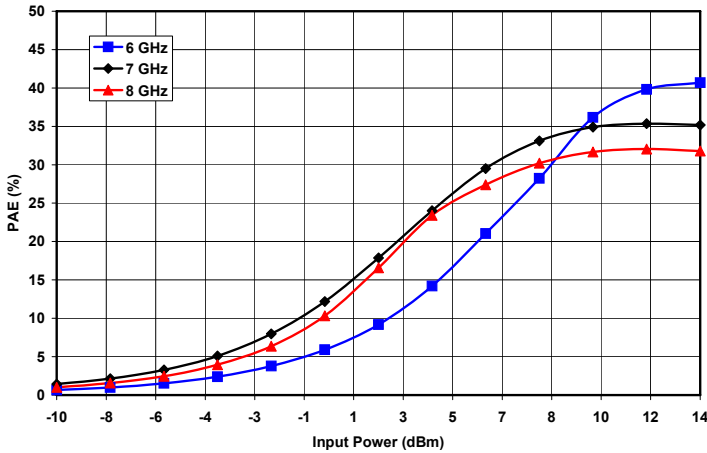


Figure 15. Power Added Efficiency vs. Input Power and Frequency at VD = 8V and IDQ = 640mA

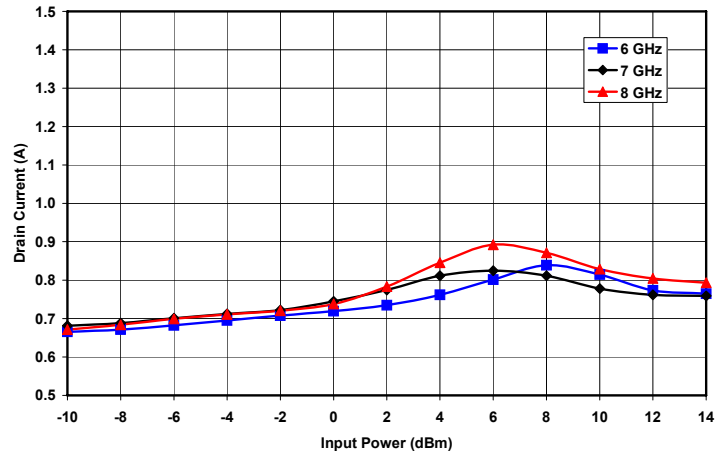


Figure 16. Drain Current vs. Input Power and Frequency at VD = 8V and IDQ = 640mA

**VD = 10V**

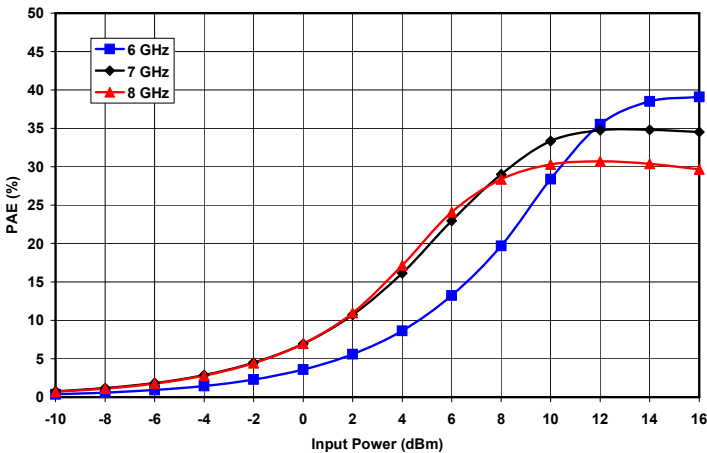


Figure 17. Power Added Efficiency vs. Input Power and Frequency at VD = 10V and IDQ = 640mA

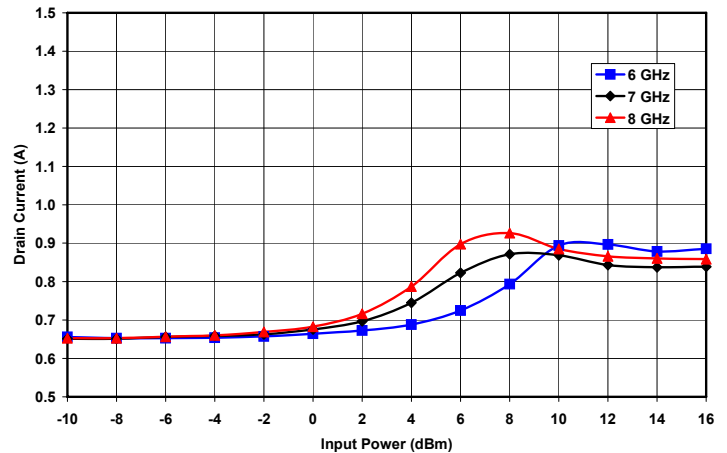


Figure 18. Drain Current vs. Input Power and Frequency at VD = 10V and IDQ = 640mA

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VD = 6V

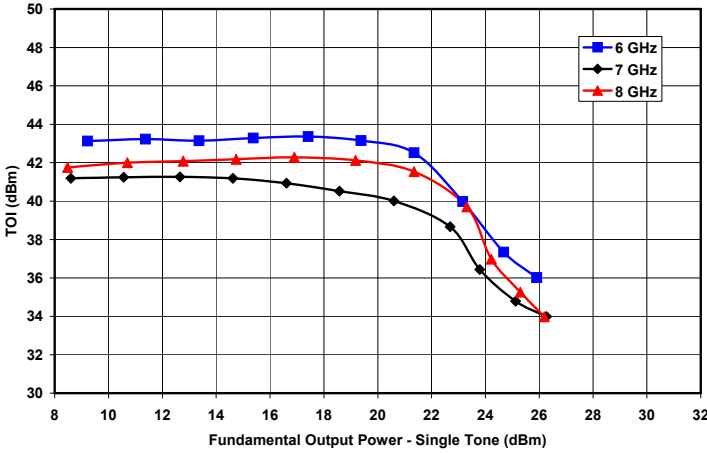


Figure 19. Third Order Intercept vs. Output Power and Frequency at VD = 6V and IDQ = 640mA

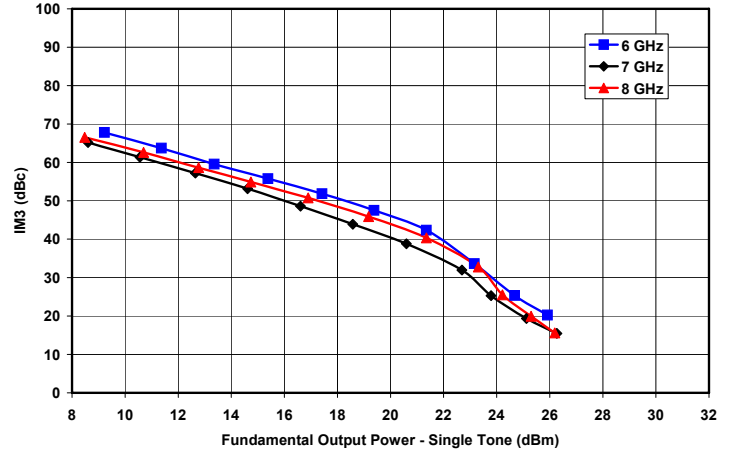


Figure 20. Third Order Intermod vs. Output Power and Frequency at VD = 6V and IDQ = 640mA

VD = 8V

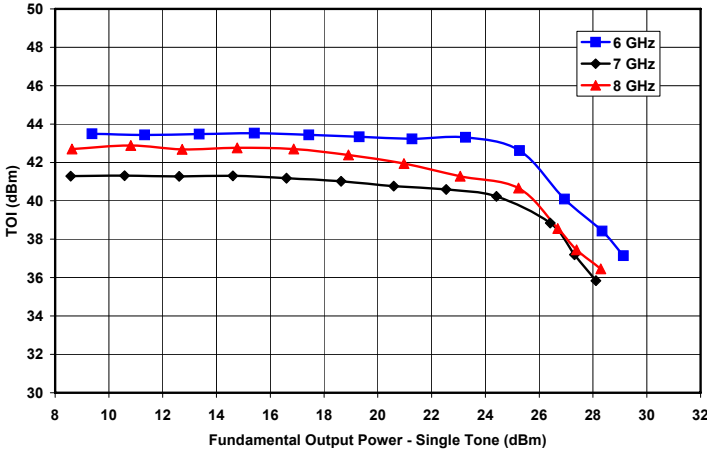


Figure 21. Third Order Intercept vs. Output Power and Frequency at VD = 8V and IDQ = 640mA

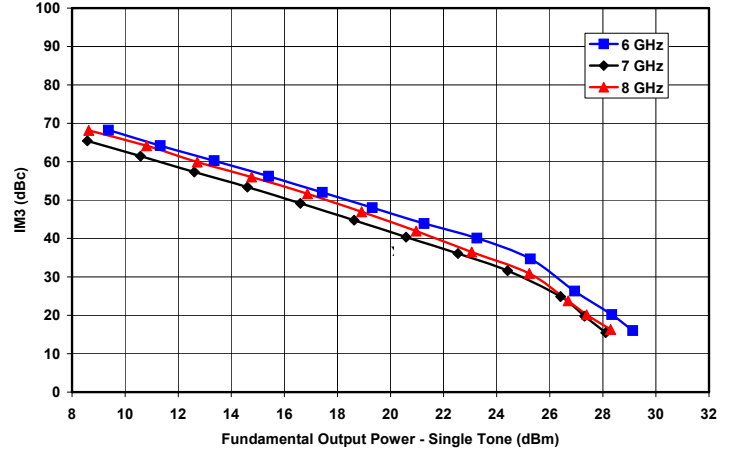


Figure 22. Third Order Intermod vs. Output Power and Frequency at VD = 8V and IDQ = 640mA

VD = 10V

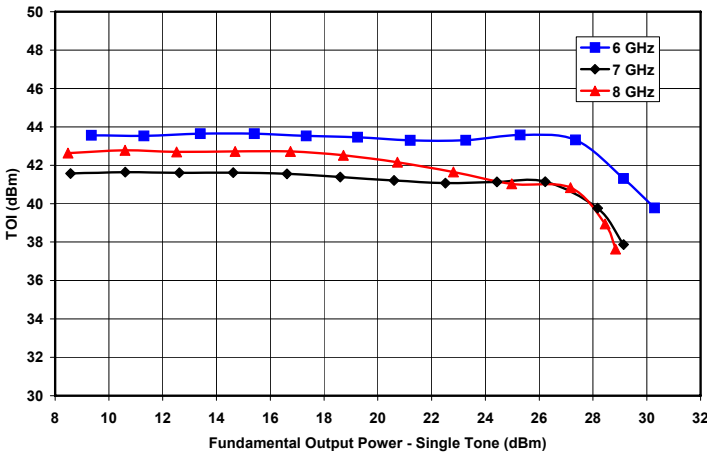


Figure 23. Third Order Intercept vs. Output Power and Frequency at VD = 10V and IDQ = 640mA

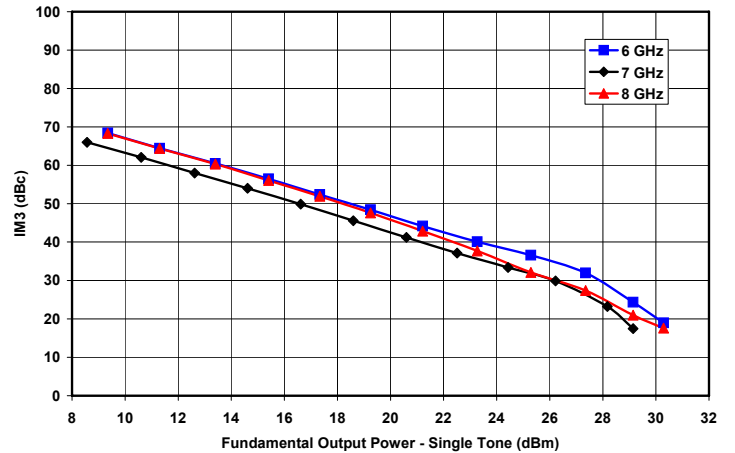


Figure 24. Third Order Intermod vs. Output Power and Frequency at VD = 10V and IDQ = 640mA

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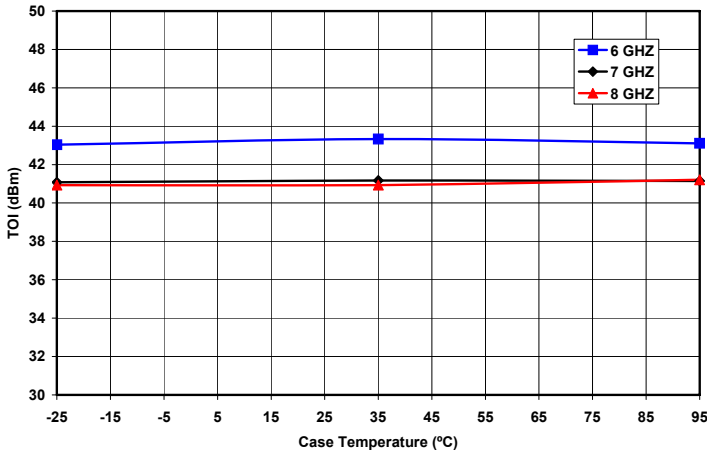


Figure 25. Third Order Intercept vs. Temperature and Frequency at Single Carrier Output Power Level = 23 dBm, VD = 8V and IDQ = 640mA

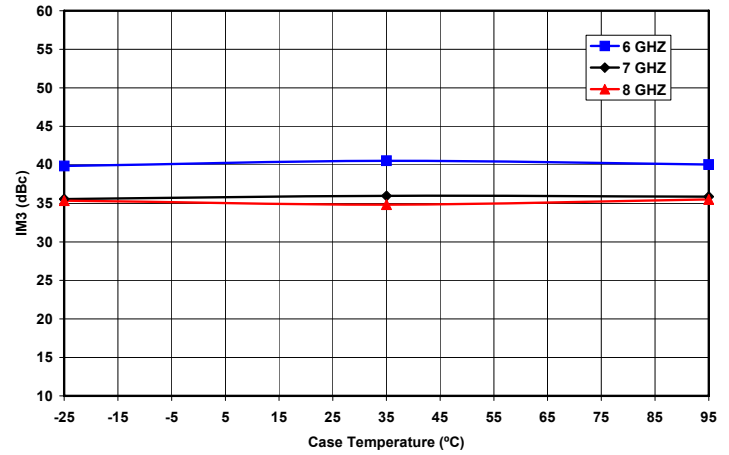
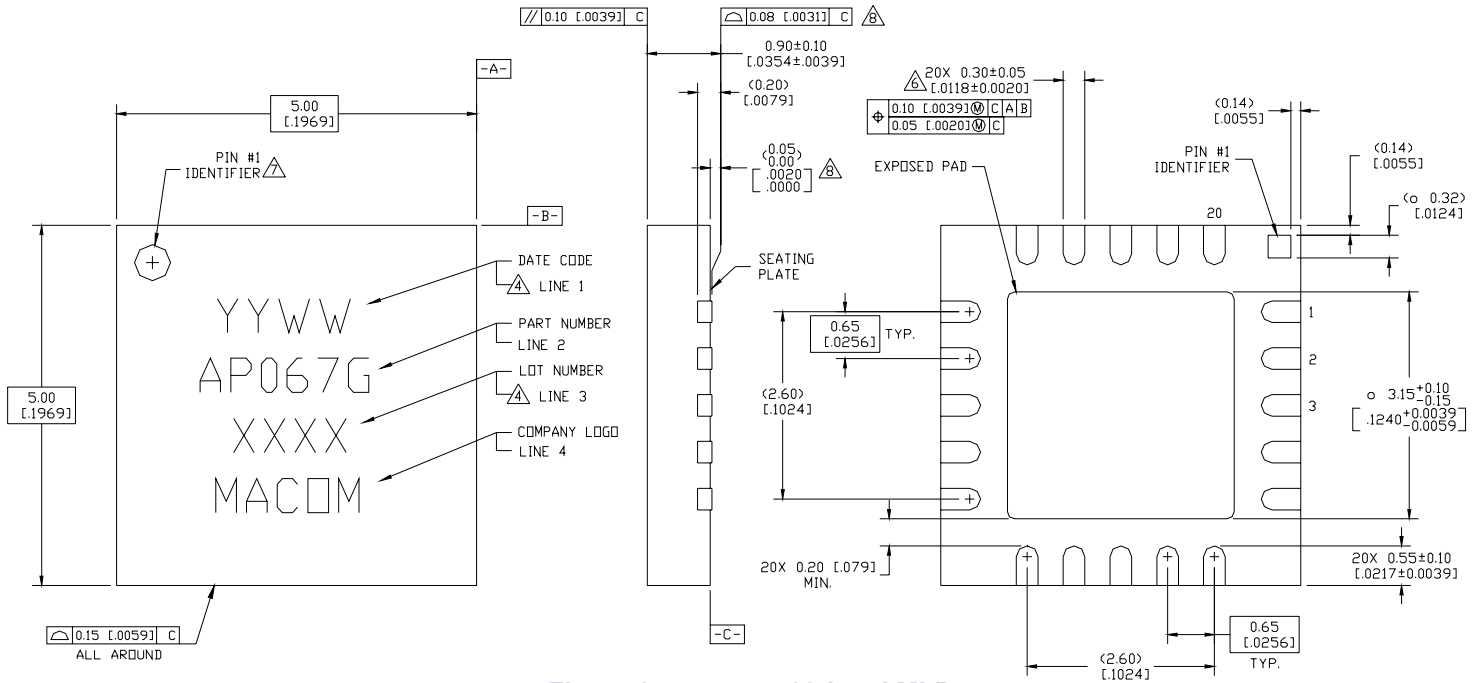
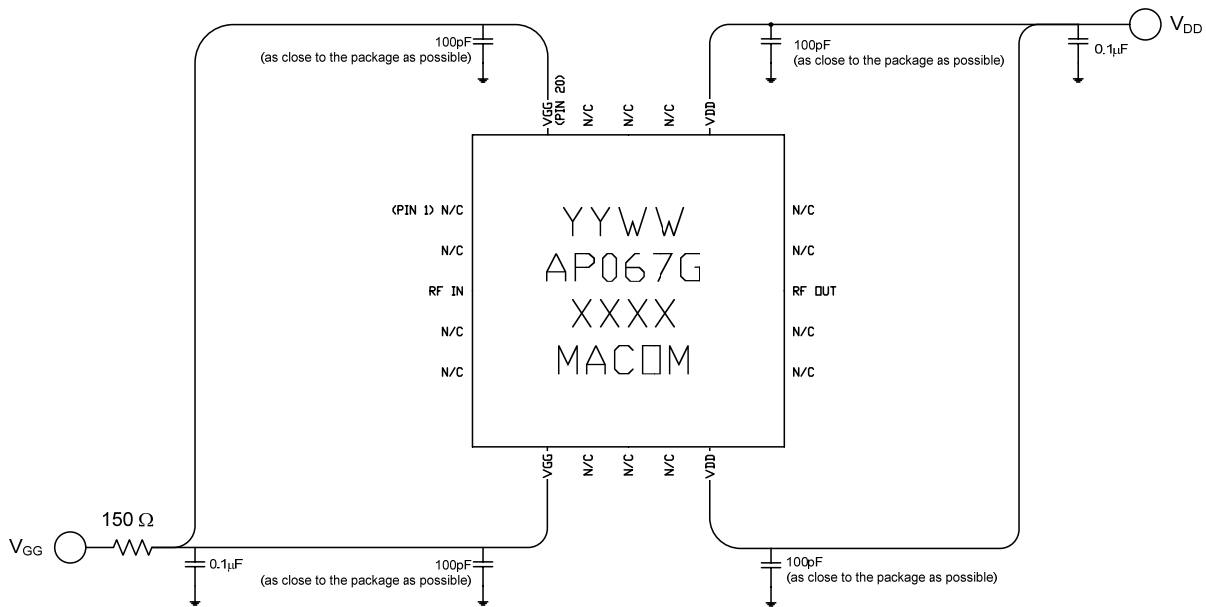


Figure 26. Third Order Intermod vs. Temperature and Frequency at Single Carrier Output Power Level = 23 dBm, VD = 8V and IDQ = 640mA



**Figure 27. 5x5 mm 20-Lead MLP.**



**Figure 28. Recommended Bias Configuration.**

Note: The exposed pad centered on the package bottom must be connected to RF and dc ground for proper electrical and thermal operation.

Refer to M/A-COM Application Note **Surface Mounting Instructions for PQFN Packages #S2083\*** for assembly guidelines.

**Additional Precaution: All parts must receive a bake-out of 125°C for 24 hours prior to any solder reflow operation.**

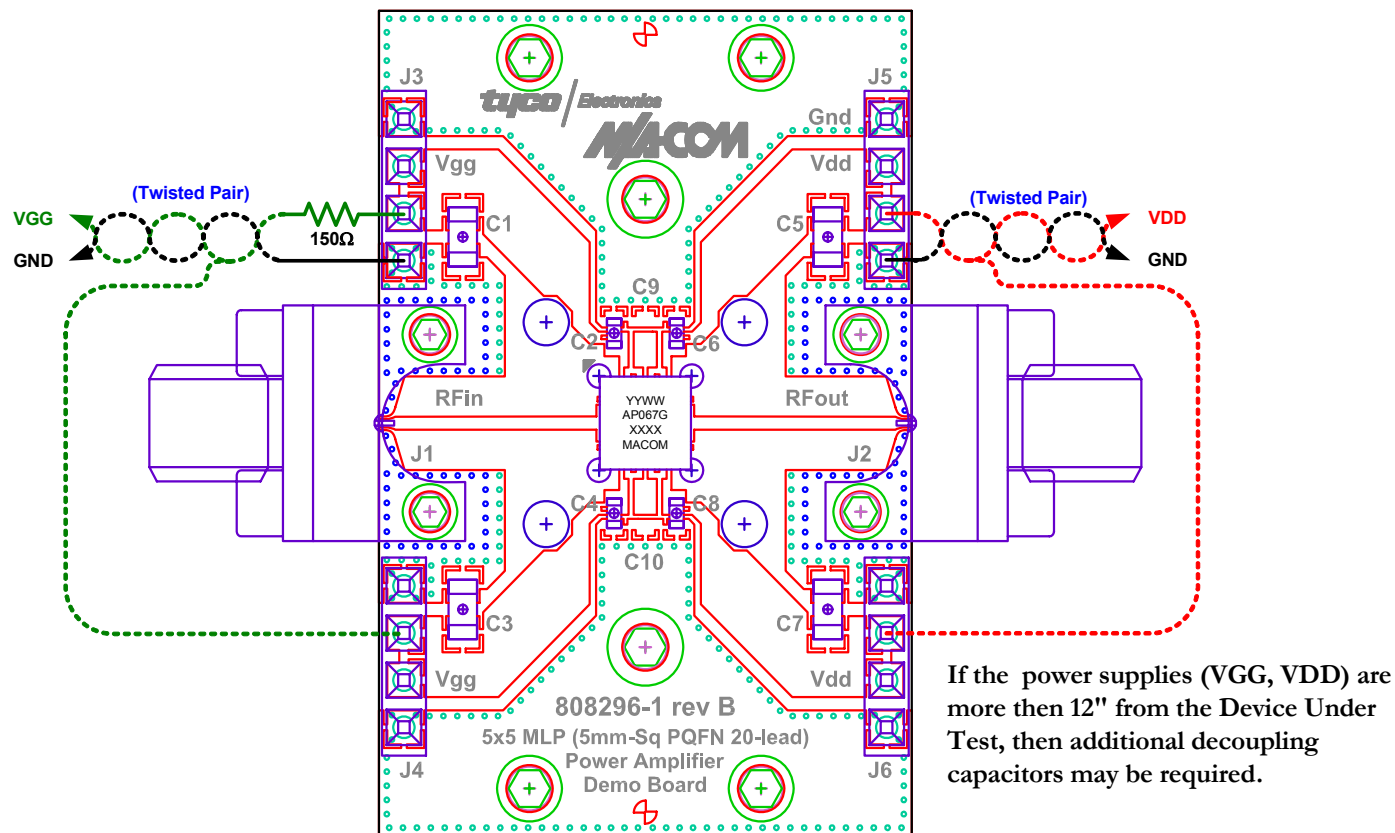
\*Application Notes can be found by going to the Site Search Page of M/A-COM's web page (<http://www.macom.com/Application%20Notes/index.htm>) and searching for the required Application Note.



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**Figure 29. Demonstration Board PN MAAP-000067-SMB003 (available upon request).**