DATA SHEET

OQ2541BHP; OQ2541BU
SDH/SONET data and clock recovery unit STM1/4/16 OC3/12/48 GE

Product specification
File under Integrated Circuits, IC19

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Philips Semiconductors

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SDH/SONET data and clock recovery unit STM1/4/16 OC3/12/48 GE

OQ2541BHP; OQ2541BU

FEATURES

- Data and clock recovery up to 2.5 Gbits/s
- Multirate configurable (155, 622, 1250 or 2500 Mbits/s)
- Full ITU-T jitter compliance (G.958 and G.813)
- Full Bellcore jitter compliance
- Differential data input with 2.5 mV (p-p) typical sensitivity
- Differential Current-Mode Logic (CML) data and clock outputs with 50 Ω driving capability
- Adjustable CML output level
- Bypass mode for non SDH/SONET or Gigabit Ethernet (GE) bit rates
- Loop mode for system testing
- Bit Error Rate (BER) related Loss Of Signal (LOS) detection
- Few external components needed
- Single supply voltage
- Power dissipation 400 mW (typical value)
- LQFP48 plastic package.

APPLICATIONS

- Data and clock recovery in STM1/OC3, STM4/OC12 and STM16/OC48 transmission systems
- Data and clock recovery in GE transmission systems
- Regenerator and repeater applications
- Wavelength conversion regenerator in Dense Wavelength Division Multiplexing (D)WDM applications.

DESCRIPTION

The OQ2541B is a data and clock recovery IC intended for use in Synchronous Digital Hierarchy (SDH) and Synchronous Optical Network (SONET) systems. The circuit recovers data and extracts the clock signal from an incoming bitstream up to 2.5 Gbits/s.

The OQ2541B can be configured for use in STM1/OC3, STM4/OC12, STM16/OC48 and GE systems, with full ITU-T G.958 and G.813 jitter compliance, or Bellcore jitter compliance, whichever is applicable. The OQ2541B also features a bypass mode, for non SDH/SONET or GE bit rates, in which the clock recovery function is bypassed.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OQ2541BHP	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
OQ2541BU	–	bare die; 2360 × 2360 × 380 μm	–

BLOCK DIAGRAM

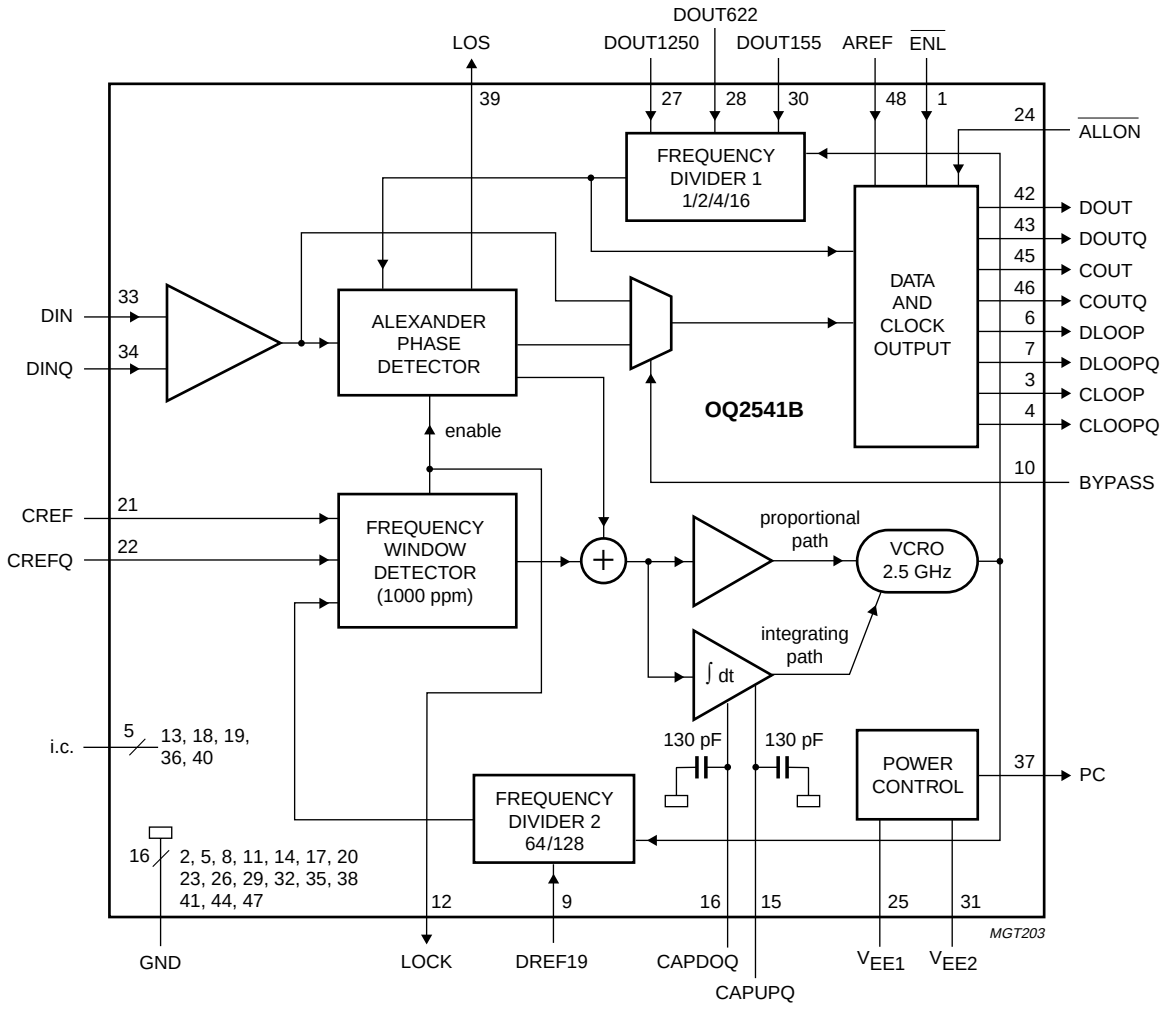


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{ENL}$	1	loop mode enable input (active LOW)
GND	2	ground; note 1
CLOOP	3	clock output in loop mode (differential)
CLOOPQ	4	inverted clock output in loop mode (differential)
GND	5	ground; note 1
DLOOP	6	data output in loop mode (differential)
DLOOPQ	7	inverted data output in loop mode (differential)
GND	8	ground; note 1
DREF19	9	reference frequency select input 1 (see Table 2)
BYPASS	10	data recovery and clock extraction bypass mode input
GND	11	ground; note 1
LOCK	12	phase lock detection output
i.c.	13	internally connected; note 2
GND	14	ground; note 1
CAPUPQ	15	external loop filter capacitor connection
CAPDOQ	16	external loop filter capacitor return connection
GND	17	ground; note 1
i.c.	18	internally connected; note 2
i.c.	19	internally connected; note 2
GND	20	ground; note 1
CREF	21	reference clock input (differential)
CREFQ	22	inverting reference clock input (differential)
GND	23	ground; note 1
$\overline{ALLON}$	24	enable all outputs (input active LOW)
V_{EE1}	25	negative supply voltage (–3.3 V); note 3
GND	26	ground; note 1
DOUT1250	27	STM mode select input 1 (see Table 3)
DOUT622	28	STM mode select input 2 (see Table 3)
GND	29	ground; note 1
DOUT155	30	STM mode select input 3 (see Table 3)
V_{EE2}	31	negative supply voltage (–3.3 V); note 3
GND	32	ground; note 1
DIN	33	data input (differential)
DINQ	34	inverting data input (differential)
GND	35	ground; note 1
i.c.	36	internally connected; note 2
PC	37	control output for negative power supply
GND	38	ground; note 1
LOS	39	loss of signal detection output
i.c.	40	internally connected; note 2

SYMBOL	PIN	DESCRIPTION
GND	41	ground; note 1
DOUT	42	data output in normal mode (differential)
DOUTQ	43	inverted data output in normal mode (differential)
GND	44	ground; note 1
COUT	45	clock output in normal mode (differential)
COUTQ	46	inverted clock output in normal mode (differential)
GND	47	ground; note 1
AREF	48	reference voltage input for controlling voltage swing on data and clock outputs

Notes

1. All GND pins or pads must be bonded; do not leave one single GND pin or pad unconnected.
2. All pins or pads denoted ‘i.c.’ should not be connected. Connections to these pins or pads degrade device performance.
3. All V_{EE} pins or pads must be bonded; do not leave one single V_{EE} pin or pad unconnected.

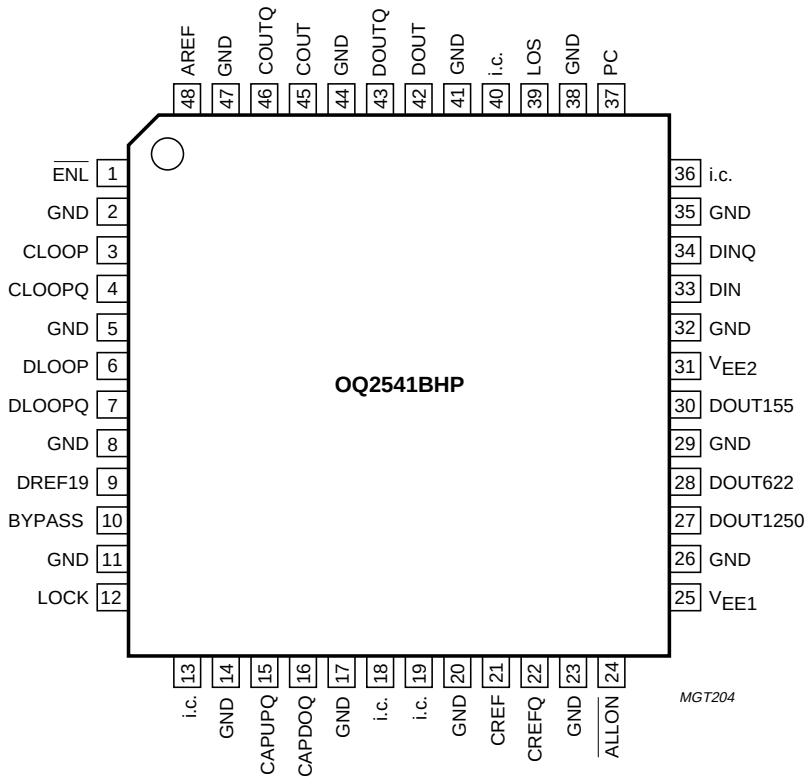


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The OQ2541B recovers data and clock signals from an incoming high speed bitstream. The input signal on pins DIN and DINQ is buffered and amplified by the input circuit (see Fig.1). The signal is then fed into the Alexander phase detector, where the phase of the incoming data signal is compared with that of the internal clock. If the signals are out of phase, the phase detector generates correction pulses (up or down) that shift the phase of the Voltage Controlled Ring Oscillator (VCRO) output in discrete amounts ($\Delta\varphi$) until the clock and data signals are in phase. The technique used is based on principles first proposed by J.D.H. Alexander, hence the name of the phase detector.

Data sampling

The eye pattern of the incoming data is sampled at three instants A, T and B (see Fig.3). When clock and data signals are synchronized (locked):

- A is the centre of the data bit
- T is in the vicinity of the next transition
- B is in the centre of the bit following the transition.

If the same level is recorded at both A and B, a transition has not occurred and no action is taken, regardless of level T. However, if levels A and B are different, a transition has occurred and the phase detector uses level T to determine whether the clock was too early or too late with respect to the data transition.

If levels A and T are the same but different from level B, the clock was too early and needs to be slowed down a little. The Alexander phase detector then generates a down pulse which stretches a single output pulse from the ring oscillator by approximately 0.25% which is 1 ps of the 400 ps bit period in the STM16/OC48 mode. This forces the VCRO to run at a slightly lower frequency for one bit period. The phase of the clock signal is thus shifted fractionally with respect to the data signal.

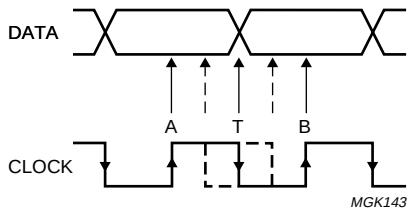


Fig.3 Data sampling.

If, on the other hand, levels B and T are the same but different from level A, the clock was too late and needs to be speeded up for synchronization. The phase detector generates an up pulse, forcing the VCRO to run at a slightly higher frequency (+0.25%) for one bit period. The phase of the clock signal is shifted with respect to the data signal (as above, but in the opposite direction). While making these phase adjustments, only the proportional path is active. Because the instantaneous frequency of the VCRO can be changed in one of two discrete steps only ($\pm$0.25%), this type of loop is also known as a Bang/Bang Phase-Locked Loop (PLL).

If not only the phase but also the frequency of the VCRO is incorrect, a long train of up or down pulses will be generated. This pulse train is integrated to generate a control voltage that is used to shift the centre frequency of the VCRO. Once the correct frequency has been established, only the phase needs to be adjusted for synchronization. The proportional path adjusts the phase of the clock signal, whereas the integrating path adjusts the centre frequency.

Frequency window detector

The frequency window detector checks the VCRO frequency, which has to be within a 1000 ppm (parts per million) window around the required frequency.

The detector compares the output of frequency divider 2 with the reference frequency on pins CREF and CREFQ (19.44 or 38.88 MHz; see Table 2). If the VCRO frequency is found to be outside this window, the frequency window detector disables the Alexander phase detector and forces the VCRO output to a frequency within the window. Then, the phase detector starts acquiring lock again. Due to the loose coupling of 1000 ppm, the reference frequency does not need to be highly accurate or stable. Any crystal-based oscillator that generates a reasonably accurate frequency (e.g. 100 ppm) will do.

Since sampling point A is always in the centre of the eye pattern when the data and clock signals are in phase (locked), the values recorded at this point are taken as the retrieved data. The data and clock signals are available at the CML output buffers that are capable of driving a 50 Ω load.

RF data and clock input circuit

The schematic of the input circuit is shown in Fig.4.

RF data and clock output circuit

The schematic of the output circuit is shown in Fig.5.

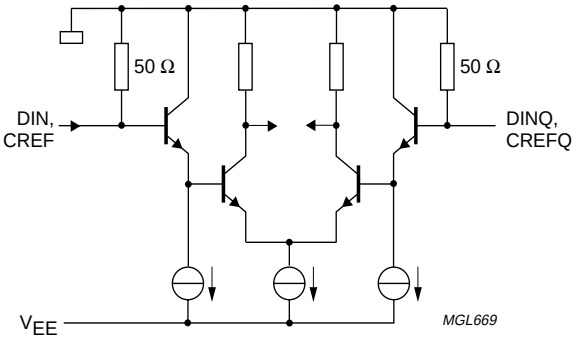


Fig.4 RF data and clock input circuit.

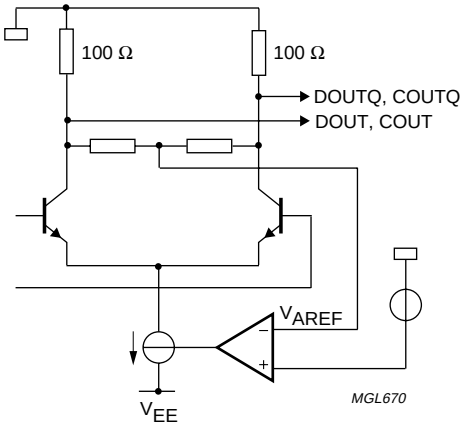


Fig.5 RF data and clock output circuit.

Power supply and power control loop

The OQ2541B contains an on-board voltage regulator. An external power transistor is needed to deliver the supply to this circuit. The required external circuit is straightforward, and can be built using a few components. A suitable circuit with a power supply of –4.5 V is illustrated in Fig.6. Do not omit the 2 Ω resistor in series with the 100 nF decoupling capacitor.

A different configuration could be used, as long as the power supply rejection ratio is greater than 60 dB for all frequencies. The inductor is an RF choke with an impedance greater than 50 Ω at frequencies higher than 2 MHz. Any transistor with a β of approximately 100 and sufficient current sink capability can be used.

The OQ2541B can also be used with a power supply of –5.0 or –5.2 V. The only adaptation to be made to the power control circuit is to change the emitter resistor R1 (see Table 1).

Table 1 Value of resistor R1

POWER SUPPLY	RESISTOR R1
–4.5 V	6.8 Ω
–5.0 V	8.2 Ω
–5.2 V	10.0 Ω

Output amplitude reference

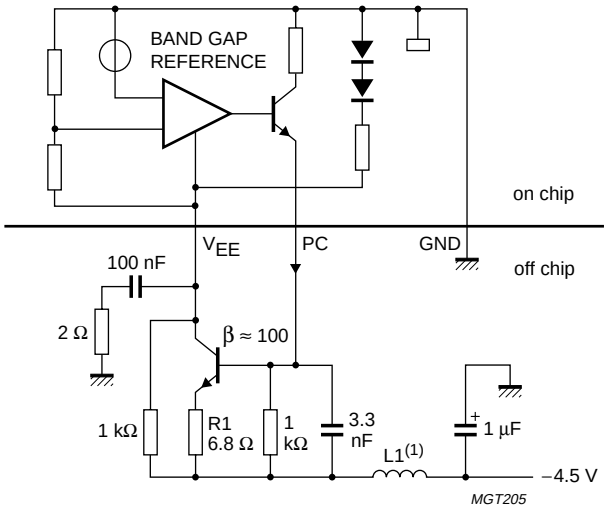
The voltage swing at the CML compatible output stages (pins DOUT, DOUTQ, COUT, COUTQ, DLOOP, DLOOPQ, CLOOP and CLOOPQ) can be controlled by adjusting the voltage on pin AREF (see Fig.7). An internal voltage divider of 500 Ω and 16 kΩ connected between ground and V_{EE} initially fixes this level.

In most applications, the outputs will be DC coupled to a 50 Ω load. The output level regulation circuit will maintain a 200 mV (p-p) single-ended swing across this load. The voltage on pin AREF is half the single-ended peak-to-peak value of the output signal (–100 mV). No adjustments are necessary with DC coupling.

If the outputs are AC coupled, the voltage on pin AREF is half the single-ended peak-to-peak value of the output signal multiplied by a factor $\frac{R_L + R_0}{R_L}$

where R_L is the external load and R_0 is the output impedance of the OQ2541B (100 Ω).

The resulting output amplitude with the same voltage on pin AREF is thus different for DC and AC coupled loads.



(1) L1 = RF choke type Murata BLM21 or equivalent.

Fig.6 Schematic diagram of OQ2541B power control loop.

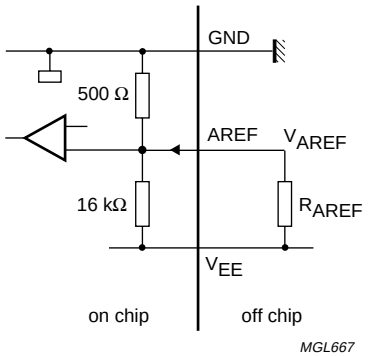


Fig.7 Functionality of pin AREF.

If the outputs are AC coupled, the formulae for calculating the required voltage on pin AREF and the value of the resistor connected between pins AREF and V_{EE} are as follows:

$$V_{AREF} = -\frac{R_L + R_O}{R_L} \times 0.5 V_{swing}$$

and:

$$R_{AREF} = \frac{R1 \times \left(\frac{V_{EE}}{V_{AREF}} - 1\right)}{1 - \left(\frac{R1}{R2} \times \left(\frac{V_{EE}}{V_{AREF}} - 1\right)\right)}$$

where R1 = 500 Ω, R2 = 16 kΩ and V_{EE} = –3.3 V.

To maintain a single-ended swing of 200 mV (p-p) across a 50 Ω AC-coupled load, the voltage on pin AREF must be

$$-100\ mV \times \frac{(50 + 100)\Omega}{50\ \Omega} = -300\ mV$$

This can be achieved by connecting a 7.3 kΩ resistor between pins AREF and V_{EE}.

External capacitor for loop filter

The loop filter is an integrator with a built-in capacitance of 2×130 pF. To ensure loop stability while the frequency window detector is active, an external capacitance of 360 nF (2 times 180 nF parallel) must be connected between pins CAPUPQ and CAPDOQ.

Loop mode enable

The loop mode is provided for system testing (see Fig.8).

The loop mode is enabled by applying a voltage between –0.8 and +0.8 V (LOW-level TTL) to pin $\overline{\text{ENL}}$. This selects the loop mode: the outputs on pins DLOOP, DLOOPQ, CLOOP and CLOOPQ are switched on.

If a voltage higher than 2.0 V (HIGH-level TTL) or lower than –2.0 V is applied to pin $\overline{\text{ENL}}$, then pins DOUT, DOUTQ, COUT and COUTQ are switched on while pins DLOOP, DLOOPQ, CLOOP and CLOOPQ are disabled to minimize power consumption.

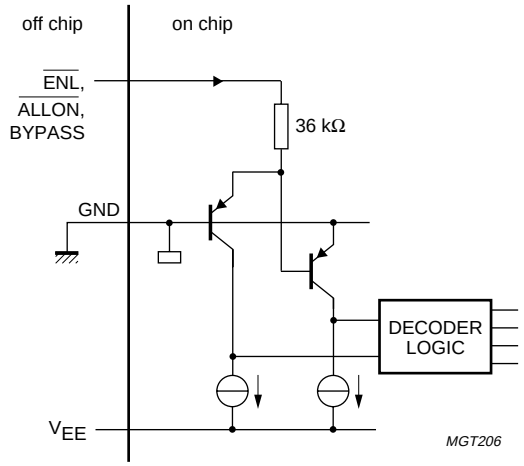


Fig.8 Input circuit of pins $\overline{\text{ENL}}$, $\overline{\text{ALLON}}$ and BYPASS.

All outputs active

All outputs (normal outputs DOUT, DOUTQ, COUT, COUTQ and loop mode outputs DLOOP, DLOOPQ, CLOOP and CLOOPQ) can be activated by applying a voltage lower than –2.0 V or higher than +2.0 V to pin $\overline{\text{ALLON}}$. If the voltage on this pin is between –0.8 and +0.8 V, the active outputs can be selected by pin $\overline{\text{ENL}}$. The input has the same structure as the $\overline{\text{ENL}}$ input (see Fig.8).

Bypass mode

The bypass mode is provided to use the OQ2541B at non standard SDH/SONET or GE bit rates. The data recovery and clock extraction function can be bypassed if no clock extraction is needed, or when the bit rate is different from 155, 622, 1250 or 2488 Mbit/s. Here, the incoming data from DIN and DINQ is directly fed to the RF outputs. Clock outputs COUT, COUTQ, CLOOP, CLOOPQ and the LOS detection have no meaning in this mode.

In the bypass mode, the data and clock recovery circuit is disabled to reduce crosstalk. The bypass mode can be activated by applying a voltage lower than –2.0 V or higher than +2.0 V to pin BYPASS. If the voltage on this pin is between –0.8 and +0.8 V, extracted data and recovered clock are present on the RF outputs (normal DCR operation). The input has the same structure as the $\overline{\text{ENL}}$ input (see Fig.8).

Lock detection

Pin LOCK should be interpreted as an indication of the presence of the reference clock on pin CREF and of the proper functioning of the acquisition aid (frequency window detector).

Pin LOCK is an open-collector TTL output and is to be pulled up with a 10 kΩ resistor to a positive supply voltage. If the VCO frequency is within a 1000 ppm window around the desired frequency, pin LOCK will stay at a HIGH level. If no reference clock is present, or the VCO is outside the 1000 ppm window, pin LOCK will be at a LOW level. The logic level on pin LOCK does not indicate locking of the PLL to the incoming data; this is indicated by the signal on pin LOS.

Loss of signal detection

The LOS function is closely related to the functionality of the Alexander phase detector; see Fig.3 for the meaning of A, B and T in this section.

The functional description states that the phase detector does not take any action if the value at sample points A and B are the same, as there has not been any transition. However, if levels A and B are the same but different from level T, this still means there has not been any transition, but level T has got the wrong level somehow. This is probably due to noise or bad signal integrity, which will lead to a bit error. Hence, the occurrence of this particular situation is an indication of bit errors. If too many of these bit errors occur per time and the PLL is gradually losing lock, the LOS alarm is asserted. The LOS alarm assert level is around BER = 5×10^{-2} and the de-assert level is around BER = 1×10^{-3}.

The LOS function will only work properly if the input signal is larger than the input offset of the OQ2541B. Otherwise, the signal will be masked by the input offset and interpreted as consecutive bits of the same sign, thus obstructing a proper LOS detection. In practice, an optical front-end device with a noise level (RMS value) larger than the specified offset of the OQ2541B will ensure a proper LOS indication.

The LOS detection is BER related, but neither dependent on the data stream content nor protocol. Therefore, an SDH/SONET data stream is not a prerequisite for a proper LOS function. Since the LOS function of the OQ2541B is derived from digital signals, it is a good supplement to an analog, amplitude based, LOS indication.

Pin LOS is an open-collector TTL compatible output. A pull-up resistor is to be connected to a positive supply voltage.

The LOS pin will be at a HIGH level (TTL) if the data signal is absent on pins DIN and DINQ or if BER $> 5 \times 10^{-2}$. Otherwise, pin LOS will be at a LOW level if BER $< 1 \times 10^{-3}$.

Reference frequency select

A reference clock signal of 19.44 or 38.88 MHz must be connected to pins CREF and CREFQ. It should be noted that the reference frequency should be either 39.0625 or 19.53125 MHz in a GE system. Pin DREF19 is used to select the appropriate output frequency at frequency divider 2 (see Table 2).

To minimize the adverse influence of reference clock crosstalk, a differential signal with an amplitude from 75 to 150 mV (p-p) is advised.

Since the reference clock is only used as an acquisition aid for the PLL of the frequency window detector, the quality of the reference clock (i.e. phase noise) is not important. There is no phase noise specification imposed on the reference clock generator and even frequency stability may be in the order of 100 ppm. In general, most inexpensive crystal-based oscillators are suitable.

When the OQ2541B is used in an application with a fixed reference clock frequency, it is best to connect pin DREF19 through a short track or a via to the ground plane or pin V_{EE}. If a selectable reference clock frequency is required in the application, the pin can be controlled through a low ohmic switching FET, e.g. BSH103 or equivalent (low R_{DSon}).

Table 2 Reference frequency selection

FREQUENCY (MHz)	DIVISION FACTOR	LEVEL ON PIN DREF19
38.88	64	ground
19.44	128	V_{EE}

STM mode selection

The VCRO has a large tuning range. However, the performance of the OQ2541B is optimized for SDH/SONET, including GE bit rates.

Due to the nature of the PLL, the wide tuning range is a necessity for proper lock behaviour over the guaranteed temperature range, aging and batch to batch spread.

Though it might seem that the OQ2541B is capable of recovering other bit rates than SDH/SONET and GE bit rates (STM1/OC3, STM4/OC12, STM16/OC48 and 1250 Mbits/s), the behaviour cannot be guaranteed.

The required SDH/SONET bit rate is selected by connecting pins DOUT155, DOUT622 and DOUT1250 to ground or to the supply voltage V_{EE} (see Table 3):

- For STM16/OC48 (2488.32 Mbits/s) operation, all three pins have to be connected to ground
- For GE (1250 Mbits/s) operation, pin DOUT1250 has to be connected to V_{EE}
- For STM4/OC12 (622.08 Mbits/s) operation, pins DOUT1250 and DOUT622 have to be connected to V_{EE} (the dividers are daisy chained)
- For STM1/OC3 (155,52 Mbits/s) operation, all three pins have to be connected to V_{EE}.

The connections to V_{EE} and ground carry a current of a few mA and should have low resistance and inductance. Therefore, short printed-circuit board tracks are recommended. In some cases, a small decoupling capacitor (approximately 100 pF) near the selection pins might be necessary to provide a clean return path for RF currents.

When the OQ2541B is used in an application with a fixed data rate, it is best to connect pins DOUT155, DOUT622 and DOUT1250 through a short track or a via to the ground plane or pin V_{EE}. If a selectable bit rate is required in the application, the pins can be controlled through low-ohmic switching FETs, e.g. BSH103 or equivalent (low R_{DSon}).

Table 3 STM mode select

MODE	BIT RATE (Mbits/s)	DIVISION FACTOR	LEVEL ON PIN		
			DOUT155	DOUT622	DOUT1250
STM1/OC3	155.52	16	V_{EE}	V_{EE}	V_{EE}
STM4/OC12	622.08	4	ground	V_{EE}	V_{EE}
Gigabit Ethernet	1250.00	2	ground	ground	V_{EE}
STM16/OC48	2488.32	1	ground	ground	ground

Application with positive supply voltage

The versatile design of the OQ2541B also allows it to operate in a positive supply voltage application, although some pins have a different mode of operation. This section deals with these differences and supports the user with achieving a successful application of the OQ2541B in a 5 V environment.

APPLICATION DIAGRAM

Fig.32 shows a sample application diagram. It should be noted that all pins GND are now connected to V_{CC} and all pins V_{EE} are connected to the regulated voltage from the power controller.

OUTPUT SELECTION

In a positive supply voltage application, the functions of pins $\overline{ENL}$, $\overline{ALLON}$ and BYPASS are different than in a negative supply application, see also Table 4.
The functions can be activated by a voltage more than 2.0 V lower than 5.0 V (V_{CC}). Preferably, they should be connected to V_{EE} (pin 25), which is approximately 3.3 V below V_{CC}. If the pins do not differ by more than 0.8 V of V_{CC} (5.0 V), the functions are deactivated.

If the pin is connected to GND (0 V) in the negative supply application, it should now be connected to 5.0 V (the voltage on pins GND). If the pin is connected to a positive voltage >0.8 V in the negative supply application, then it should be connected to V_{EE} (pin 25, approximately 3.3 V below V_{CC}). Beware not to connect pins $\overline{ENL}$, $\overline{ALLON}$ or BYPASS to a voltage lower than that on pin 25, because this causes serious damage to the OQ2541B.

CAUTION
Do not connect pins $\overline{ENL}$, $\overline{ALLON}$ or BYPASS to ground, because this will destroy the IC.

LOSS OF SIGNAL AND LOCK DETECTION

In the negative supply application, pins LOS and LOCK are open-collector outputs that require pull-up resistors to a positive supply voltage.

In the positive supply application, the pull-up voltage needs to be higher than the positive supply voltage and the signals on pins LOS and LOCK would no longer be TTL compatible. However, the internal circuit on pins LOS and LOCK can be used in a current mirror configuration (see Fig.9). This requires only an external PNP transistor (e.g. BC857 or equivalent) to mirror the current. A 10 kΩ pull-down resistor from the collector of the external transistor to ground yields a TTL compatible signal again, albeit inverted. Table 5 shows the meaning of the LOS and LOCK flags, when used in the positive supply application.

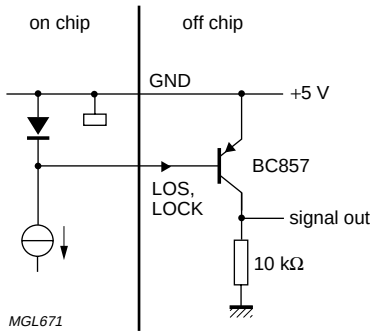


Fig.9 Signal out for LOS and LOCK indications in a positive supply voltage application.

Table 4 Output selection in a positive supply voltage application

MODE	LEVEL ON PIN			OUTPUT	
	$\overline{ENL}$	$\overline{ALLON}$	BYPASS	DLOOP, DLOOPQ, CLOOP AND CLOOPQ	DOUT, DOUTQ, COUT AND COUTQ
DCR loop	V_{CC} (5 V)	V_{CC} (5 V)	V_{CC} (5 V)	active	–
DCR all outputs	–	V_{EE} (V_{CC} – 3.3 V)	V_{CC} (5 V)	active	active
DCR normal	V_{EE} (V_{CC} – 3.3 V)	V_{CC} (5 V)	V_{CC} (5 V)	–	active
Bypass loop	V_{CC} (5 V)	V_{CC} (5 V)	V_{EE} (V_{CC} – 3.3 V)	active	–
Bypass all outputs	–	V_{EE} (V_{CC} – 3.3 V)	V_{EE} (V_{CC} – 3.3 V)	active	active
Bypass normal	V_{EE} (V_{CC} – 3.3 V)	V_{CC} (5 V)	V_{EE} (V_{CC} – 3.3 V)	–	active

Table 5 LOS and LOCK indication in a positive supply voltage application

SIGNAL	DESCRIPTION	LEVEL	TTL
LOS active	loss of signal: BER > 5×10^{-2}	0 V (ground)	LOW
LOS inactive	no loss of signal: BER < 1×10^{-3}	5 V (V_{CC})	HIGH
LOCK active	reference clock present and VCRO inside 1000 ppm window	0 V (ground)	LOW
LOCK inactive	no reference clock present or VCRO outside 1000 ppm window	5 V (V_{CC})	HIGH

DIVIDER SETTINGS

The reference frequency dividers and the STM mode selectors still operate the same in a positive supply voltage application. The only difference is that pins formerly connected to ground should now be connected to V_{CC} (5 V). Pins connected to V_{EE} should still be connected to V_{EE} because connecting these pins to ground (0 V) will damage the IC.

RF INPUT AND OUTPUTS

All RF inputs, outputs and internal signals of the OQ2541B are referenced to pins GND. In the positive supply voltage application, this means that all RF signals are referenced to V_{CC}. Therefore, a clean V_{CC} rail is of utmost importance for proper RF performance. The best performance is obtained when the transmission line reference plane is also decoupled to V_{CC}. Careful design of V_{CC} and good decoupling schemes should be taken into account. While designing the printed-circuit board, bear in mind that the V_{CC} has become what was formerly ground.

While laying out the application, the return path is the most important issue to be considered. It is always advised to carefully examine the current carrying loops in the design. Care should be taken that low ohmic and low inductance return paths are available for all frequencies (both of interest and not of interest). These return paths should preferably have an enclosed area as small as possible, both horizontally and vertically (by means of through-holes or vias). The position of a decoupling capacitor is very important. A decoupling capacitor at an unfavourable position could do more damage than completely omitting the capacitor, while at the right location it might mean the difference between mediocre results and the ultimate achievement.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{EE}	negative supply voltage	−6	+0.5	V
V_n	DC voltage on pins			
	CLOOP, CLOOPQ, DLOOP, DLOOPQ, CREF, CREFQ, DIN, DINQ, DOUT, DOUTQ, COUT and COUTQ	−1	+0.5	V
	$\overline{ENL}$, $\overline{ALLON}$, BYPASS, LOCK and LOS	V_{EE} − 0.5	+5.5	V
	DREF19, DOUT1250, DOUT622, DOUT155, PC and AREF	V_{EE} − 0.5	+0.5	V
	CAPUPQ and CAPDOQ	V_{EE} + 0.5	−0.5	V
I_n	input current on pins			
	$\overline{ENL}$, $\overline{ALLON}$ and BYPASS	−	1	mA
	CREF, CREFQ, DIN and DINQ	−20	+10	mA
P_{tot}	total power dissipation	−	700	mW
T_{amb}	ambient temperature	−10	+85	°C
T_j	junction temperature	−10	+110	°C
T_{stg}	storage temperature	−65	+150	°C

HANDLING INSTRUCTIONS

Precautions should be taken to avoid damage through electrostatic discharge. This is particularly important during assembly and handling of the bare die. Additional safety can be obtained by bonding the V_{EE} and GND pads first, the remaining pads may then be bonded to their external connections in any order.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-s)}$	thermal resistance from junction to solder point		46	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; note 1	67	K/W

Note

1. Thermal resistance from junction to ambient is determined with the IC soldered on a standard single sided $57 \times 57 \times 1.6$ mm FR4 epoxy PCB with 35 μm thick copper tracks. The measurements are performed in still air.

CHARACTERISTICS

V_{EE} = –3.35 V; T_{amb} = –10 to +85 °C; typical values measured at T_{amb} = 25 °C; all voltages are measured with respect to GND.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EE}	negative supply voltage	see Fig.12; note 1	–3.50	–3.35	–3.10	V
I_{EE}	negative supply current	50 Ω loaded; see Fig.13	–	125	160	mA
P_{tot}	total power dissipation		–	400	560	mW
Data and clock inputs: pins DIN, DINQ, CREF and CREFQ						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	50 Ω measurement system; see Fig.10; notes 2 and 3	7	200	450	mV
$V_{i(sens)(p-p)}$	input sensitivity (peak-to-peak value)	50 Ω measurement system; notes 2 and 4	–	2.5	7	mV
V_{IO}	DC input offset voltage	50 Ω measurement system	–3	0	+3	mV
V_I	input voltage	50 Ω measurement system	–600	–200	+250	mV
Z_i	input impedance	single-ended; see Fig.4; note 5	–	50	–	Ω
Data and clock outputs: pins DOUT, DOUTQ, DLOOP, DLOOPQ, COUT, COUTQ, CLOOP and CLOOPQ						
$V_{o(p-p)}$	output voltage swing (peak-to-peak value)	50 Ω measurement system; single-ended; see Fig.10				
		default adjustment; note 6	170	200	210	mV
		special adjustment; note 7	50	–	400	mV
V_O	output voltage		–600	–	0	mV
Z_o	output impedance	single-ended	–	100	–	Ω
$t_{r(C)}$	clock output rise time	differential; 20% to 80%	–	50	–	ps
$t_{f(C)}$	clock output fall time	differential; 20% to 80%	–	50	–	ps
$t_{r(D)}$	data output rise time	differential; 20% to 80%	–	120	–	ps
$t_{f(D)}$	data output fall time	differential; 20% to 80%	–	120	–	ps
$t_{d(D-C)}$	data-to-clock delay	see Figs. 11 and 14; note 8	220	260	300	ps
Output amplitude adjustment: pin AREF						
V_{AREF}	output amplitude reference voltage	floating pin	–110	–100	–90	mV
Power control output: pin PC						
g_m	transconductance		–84	–60	–42	mA/V
I_O	output current		1	–	3.5	mA
Loop mode enable input: pins $\overline{\text{ENL}}$, $\overline{\text{ALLON}}$ and BYPASS						
V_{IL}	LOW-level input voltage		–0.8	–	0.8	V
V_{IH}	HIGH-level input voltage	see descriptions of $\overline{\text{ENL}}$, $\overline{\text{ALLON}}$ and BYPASS	–3.3	–	–2.0	V
			2.0	–	5.0	V
Phase lock indicator: pin LOCK						
V_{OL}	LOW-level output voltage	note 9	–0.6	–	–	V
V_{OH}	HIGH-level output voltage	note 9	–	–	3.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Loss of signal indicator: pin LOS						
V_{OL}	LOW-level output voltage	note 9	–0.6	–	–	V
V_{OH}	HIGH-level output voltage	note 9	–	–	3.3	V
t_{as}	assert time	note 10	–	0.1	–	µs
t_{das}	de-assert time	note 10	–	10	–	µs
BER_{as}	assert bit error rate	note 10	–	5×10^{-2}	–	BER
BER_{das}	de-assert bit error rate	note 10	–	1×10^{-3}	–	BER
PLL characteristics						
t_{acq}	acquisition time	CREF = 19.44 MHz	–	100	200	µs
		CREF = 38.88 MHz	–	50	200	µs
$J_{tol(p-p)}$	jitter tolerance (peak-to-peak value)	STM1/OC3 mode; note 11				
		f = 6.5 kHz	1.5	>2.5	–	UI
		f = 65 kHz	0.15	0.8	–	UI
		f = 1 MHz	0.15	0.8	–	UI
		STM4/OC12 mode; note 11				
		f = 25 kHz	1.5	>2.5	–	UI
		f = 250 kHz	0.15	0.7	–	UI
		f = 5 MHz	0.15	0.7	–	UI
		STM16/OC48 mode; note 11				
		f = 100 kHz	1.5	>2.5	–	UI
		f = 1 MHz	0.15	0.4	–	UI
		f = 10 MHz	0.15	0.3	–	UI
$J_{transfer}$	3 dB corner frequency for jitter transfer	STM1/OC3 mode; note 11; see Fig.17	–	125	180	kHz
		STM4/OC12 mode; note 11; see Fig.19	–	500	700	kHz
		STM16/OC48 mode; note 11; see Fig.21	–	1.8	2.8	MHz
$J_{gen(p-p)}$	jitter generation (peak-to-peak value)	STM1/OC3 mode; note 12				
		f = 500 Hz to 1.3 MHz	–	0.04	0.50	UI
		f = 12 kHz to 1.3 MHz	–	0.025	0.10	UI
		f = 65 kHz to 1.3 MHz	–	0.02	0.10	UI
		STM4/OC12 mode; note 12				
		f = 1 kHz to 5 MHz	–	0.050	0.50	UI
		f = 12 kHz to 5 MHz	–	0.035	0.10	UI
		f = 250 kHz to 5 MHz	–	0.030	0.10	UI
		STM16/OC48 mode; note 12				
		f = 5 kHz to 20 MHz	–	0.06	0.50	UI
		f = 12 kHz to 20 MHz	–	0.05	0.10	UI
		f = 1 to 20 MHz	–	0.045	0.10	UI

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$J_{gen(rms)}$	jitter generation (RMS value)	STM1/OC3 mode; note 12				
		f = 500 Hz to 1.3 MHz	–	0.005	–	UI
		f = 12 kHz to 1.3 MHz	–	0.0025	–	UI
		f = 65 kHz to 1.3 MHz	–	0.002	–	UI
		STM4/OC12 mode; note 12				
		f = 1 kHz to 5 MHz	–	0.006	–	UI
		f = 12 kHz to 5 MHz	–	0.004	–	UI
		f = 250 kHz to 5 MHz	–	0.004	–	UI
		STM16/OC48 mode; note 12				
		f = 5 kHz to 20 MHz	–	0.008	–	UI
		f = 12 kHz to 20 MHz	–	0.007	–	UI
		f = 1 to 20 MHz	–	0.0065	–	UI
TDR	transitionless data run	note 13	–	2000	–	bits

Notes

1. Typical power supply voltage for the voltage regulator is –4.5 V (see Fig.6).
2. It is assumed that both CML inputs carry a complementary signal with the specified peak-to-peak value (true differential excitation).
3. The specified input voltage range is the guaranteed and tested range for proper operation; BER < 1×10^{-10}.
4. In DCR mode, an input sensitivity of 7 mV (p-p) for BER < 1×10^{-10} is guaranteed. The typical input sensitivity for BER < 1×10^{-10} is 2.5 mV (p-p). In bypass mode, full clipping of the output signal occurs at about 25 mV (p-p), see Fig.15.
5. CML inputs are terminated internally using on-chip resistors of 50 Ω connected to ground.
6. Output voltage range with default reference voltage on pin AREF (floating).
7. Output voltage range with adjustment of voltage on pin AREF (see Section “Output amplitude reference”).
8. Measured with ‘1010’ data pattern, single-ended output signals and rising edges of the signals on pins COUT to DOUT or pins CLOOP to DLOOP. It should be noted that small deviations of the specified value are possible if measured differentially.
9. External pull-up resistor of 10 kΩ connected to supply voltage of 3.3 V.
10. LOS assert or de-assert timing and BER level are for indication only. The values are neither production tested nor guaranteed.
11. Measured in accordance with ITU specification G.958. Measured with demoboard OM5801 for STM16/OC48, STM4/OC12 and STM1/OC3. See for more information *“Application note AN96051”*.
12. Measured in accordance with ITU specification G.813 and 10 dB above the system input sensitivity power level. Measured with demoboard OM5801 for STM16/OC48, STM4/OC12 and STM1/OC3.
13. TDR is bit rate independent.

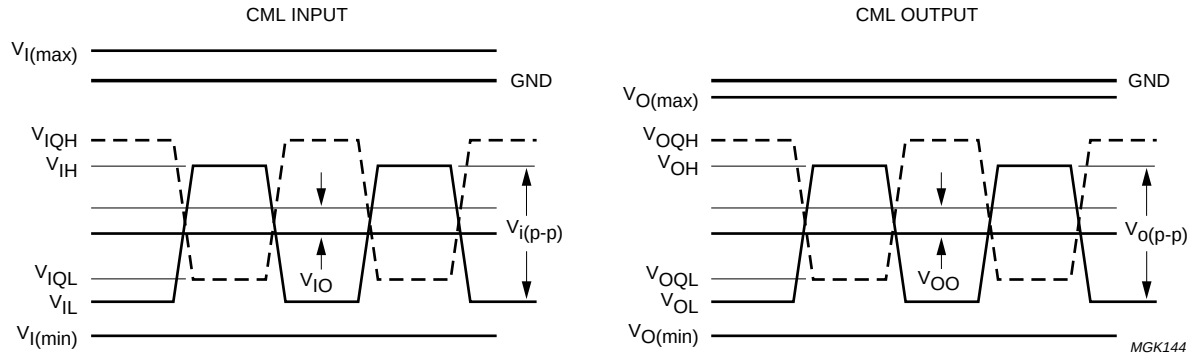


Fig.10 Logic level symbol definitions for CML.

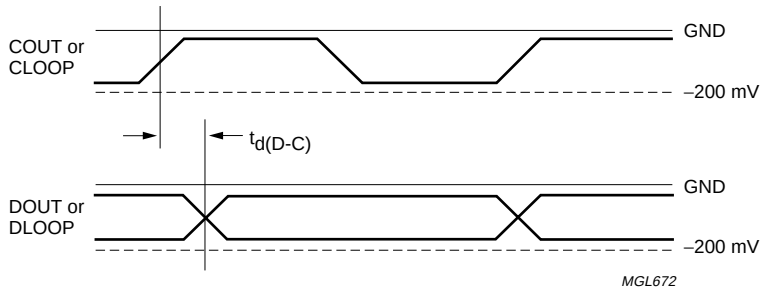
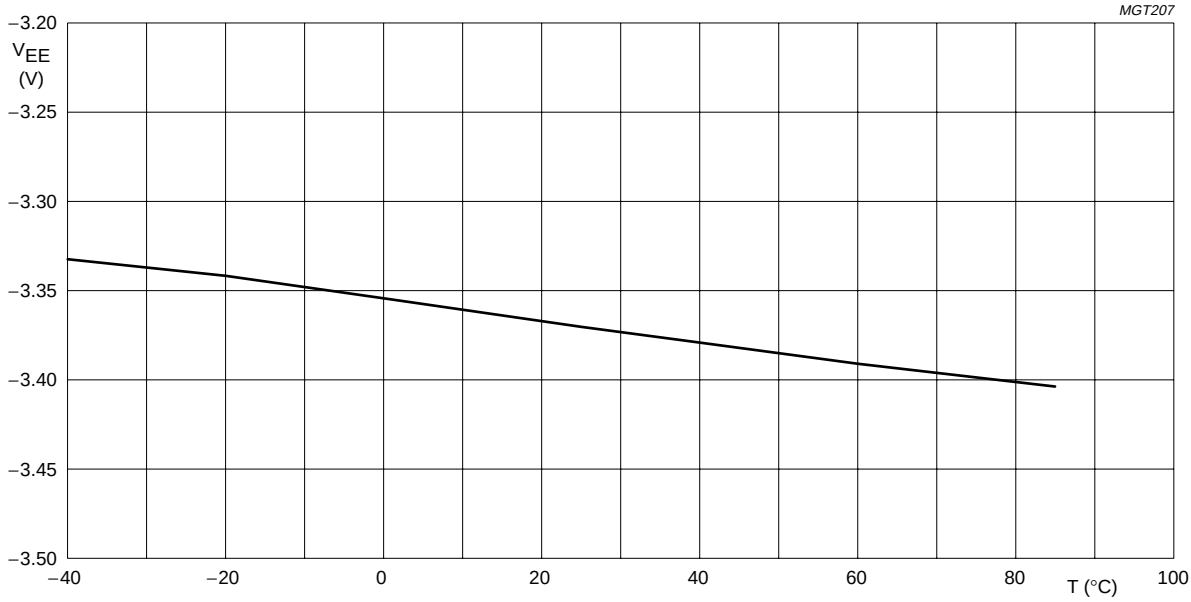


Fig.11 Data-to-clock delay for CML outputs: COUT to DOUT or CLOOP to DLOOP.

TYPICAL PERFORMANCE CHARACTERISTICS



The supply voltage is regulated by the power controller.

Fig.12 Supply voltage as a function of the temperature.

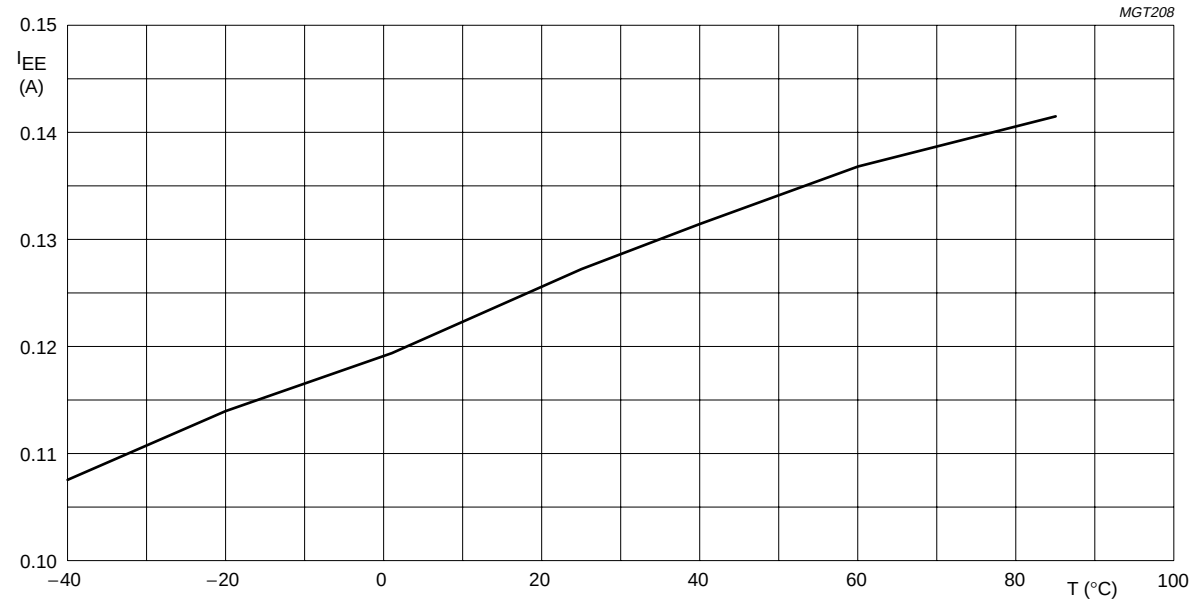
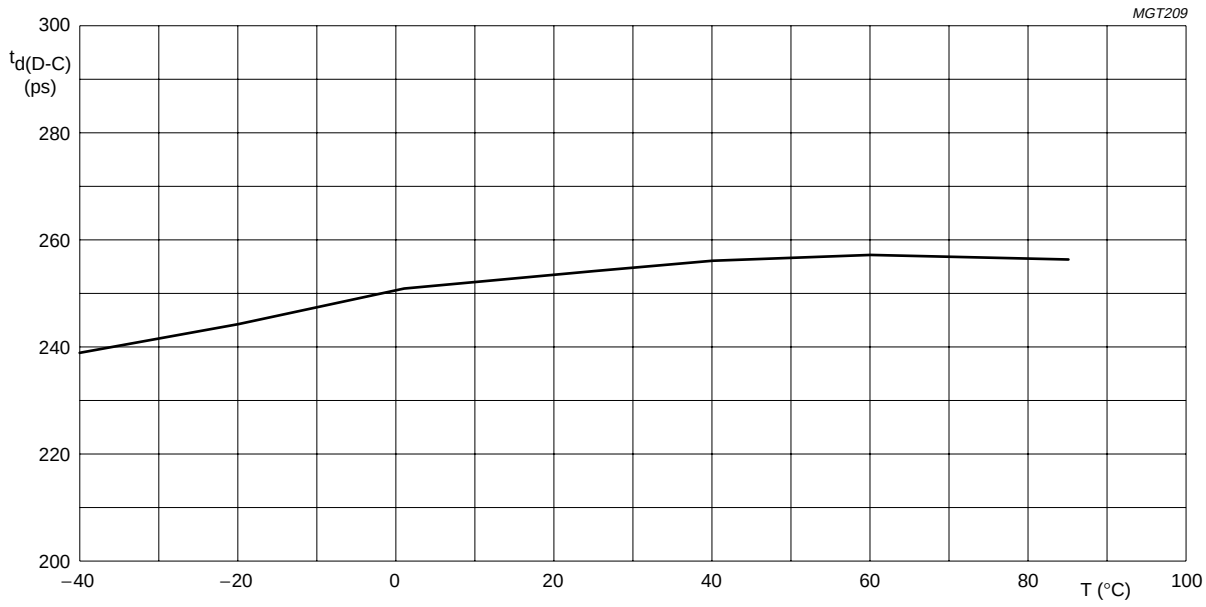


Fig.13 Supply current as a function of the temperature.



See Fig.11 for the definition of $t_{d(D-C)}$.

Fig.14 Data-to-clock delay time as a function of the temperature.

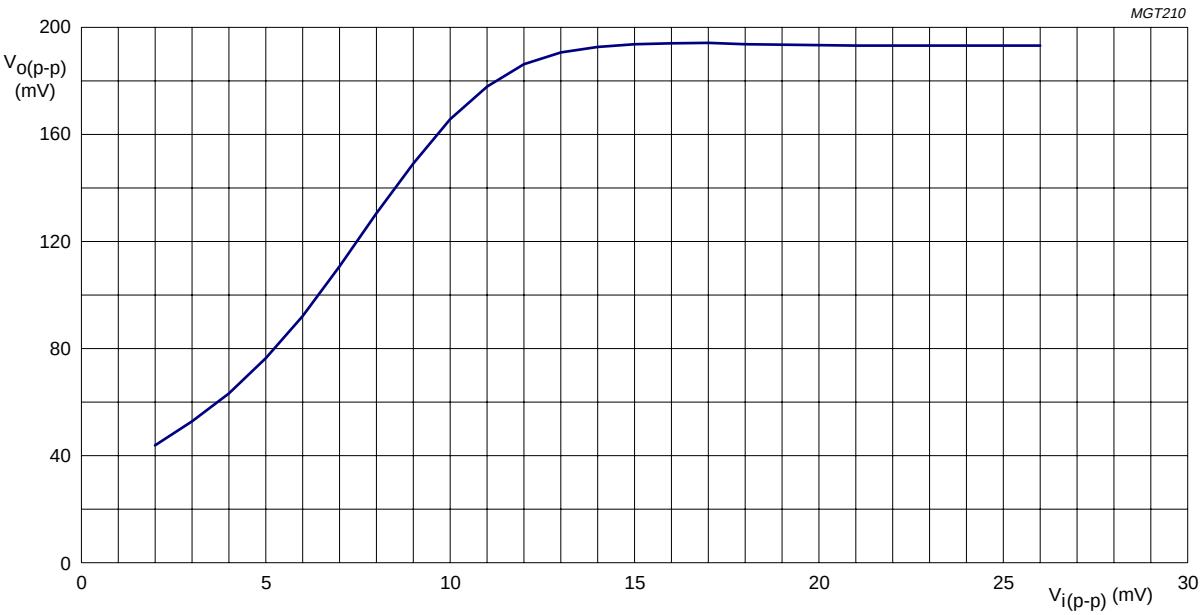
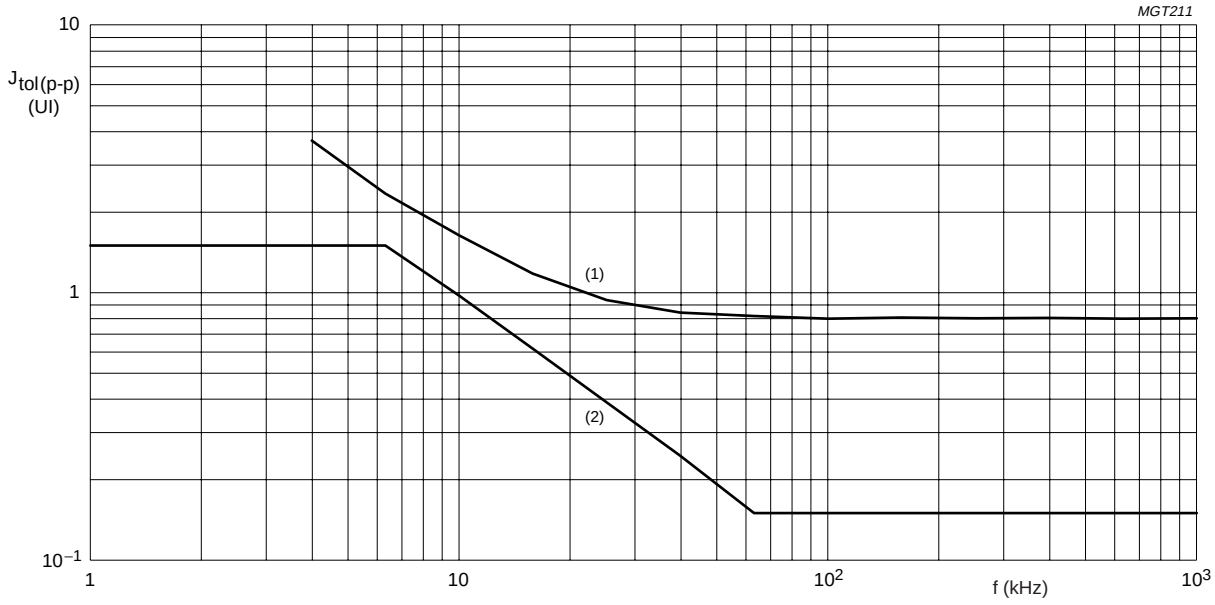
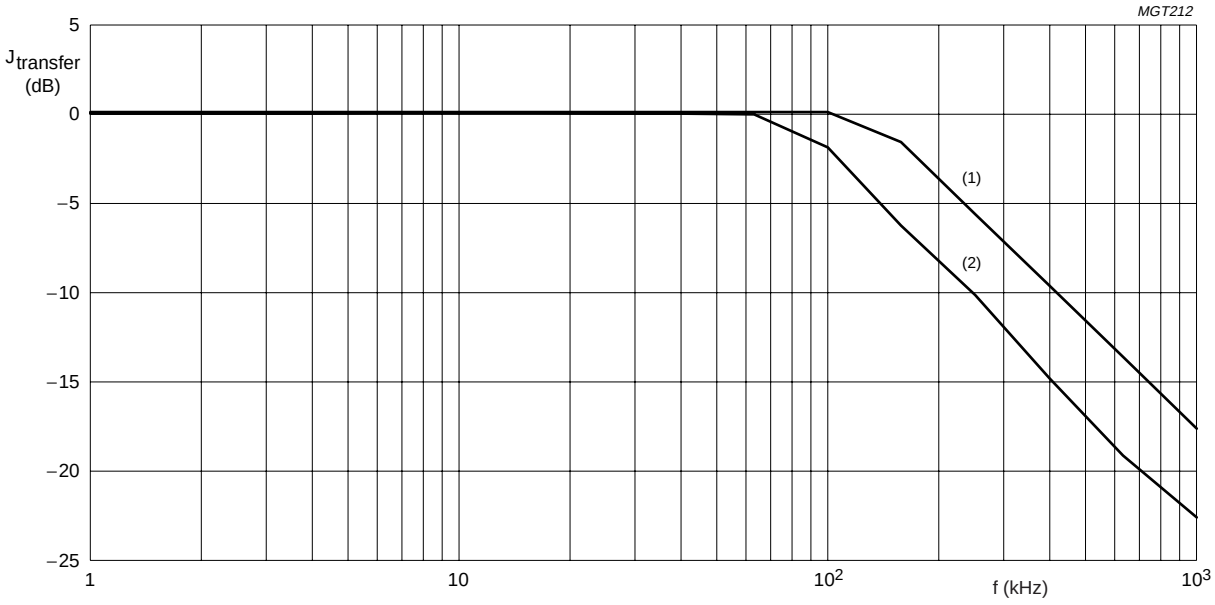


Fig.15 Output voltage as a function of input voltage in bypass mode.



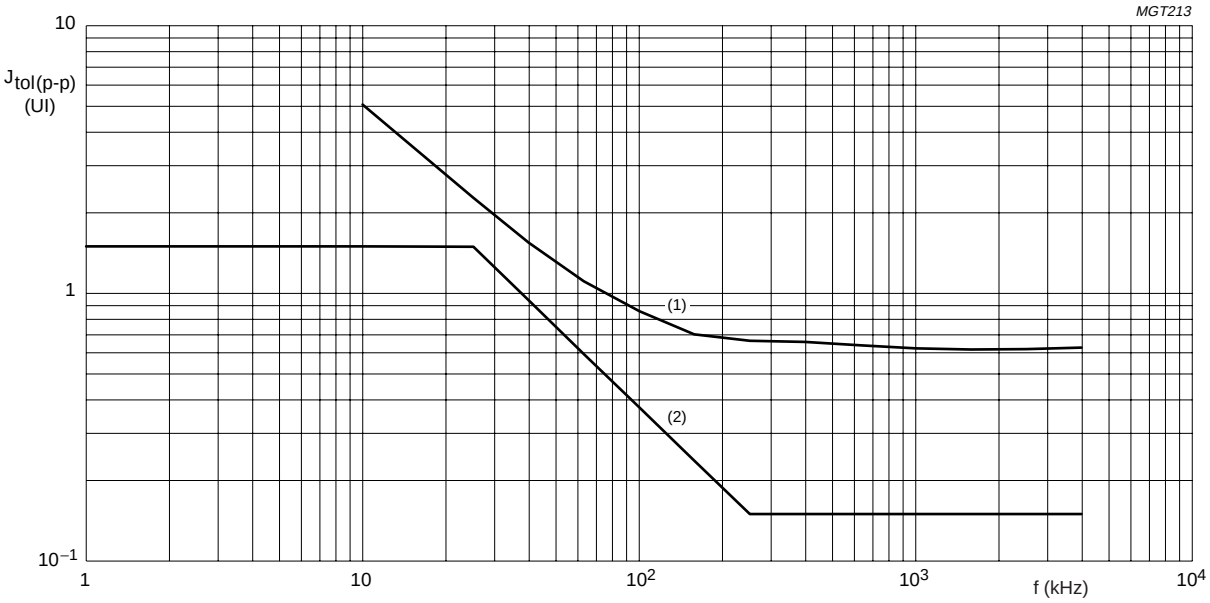
(1) OQ2541B; (2) ITU STM1.

Fig.16 Jitter tolerance as a function of the jitter frequency in the STM1/OC3 mode (155.52 Mbits/s).



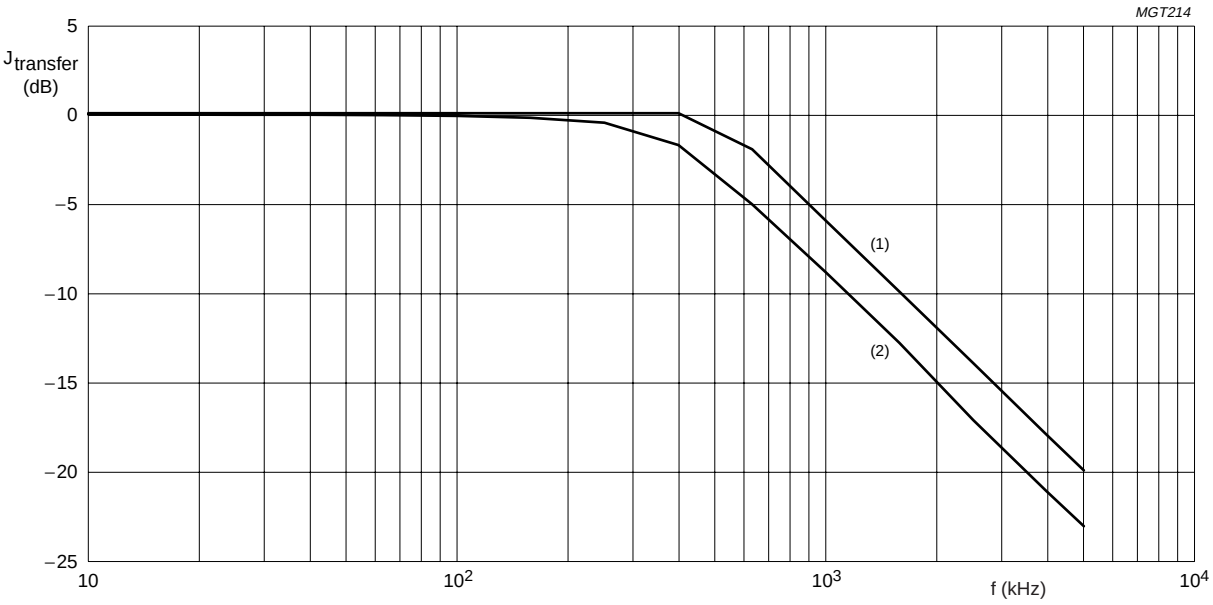
(1) ITU STM1; (2) OQ2541B.

Fig.17 Jitter transfer as a function of the jitter frequency in the STM1/OC3 mode (155.52 Mbits/s).



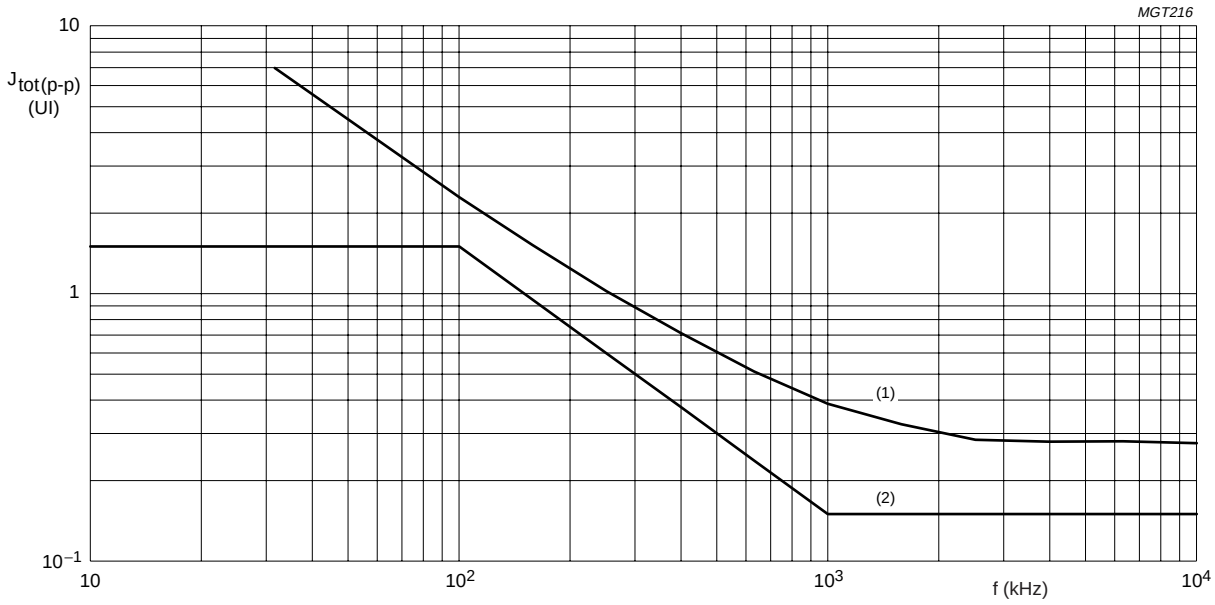
(1) OQ2541B; (2) ITU STM4.

Fig.18 Jitter tolerance as a function of the jitter frequency in the STM4/OC12 mode (622.08 Mbits/s).



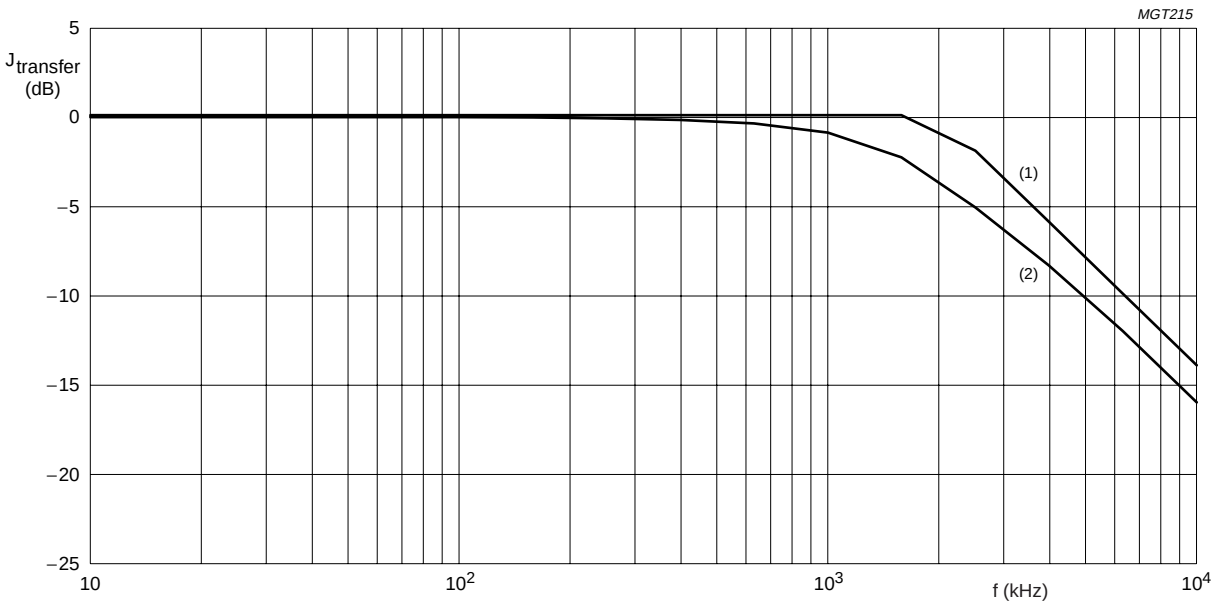
(1) ITU STM4; (2) OQ2541B.

Fig.19 Jitter transfer as a function of the jitter frequency in the STM4/OC12 mode (622.08 Mbits/s).



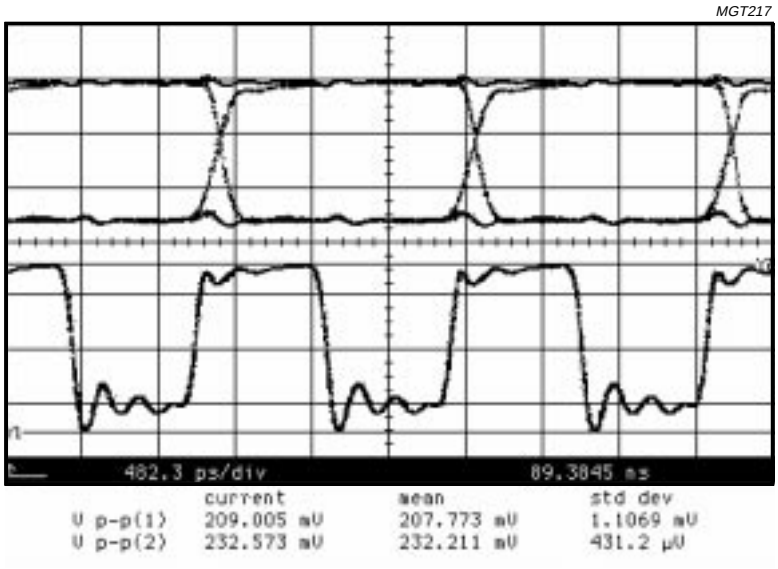
(1) OQ2541B; (2) ITU STM16.

Fig.20 Jitter tolerance as a function of the jitter frequency in the STM16/OC48 mode (2488.32 Mbits/s).



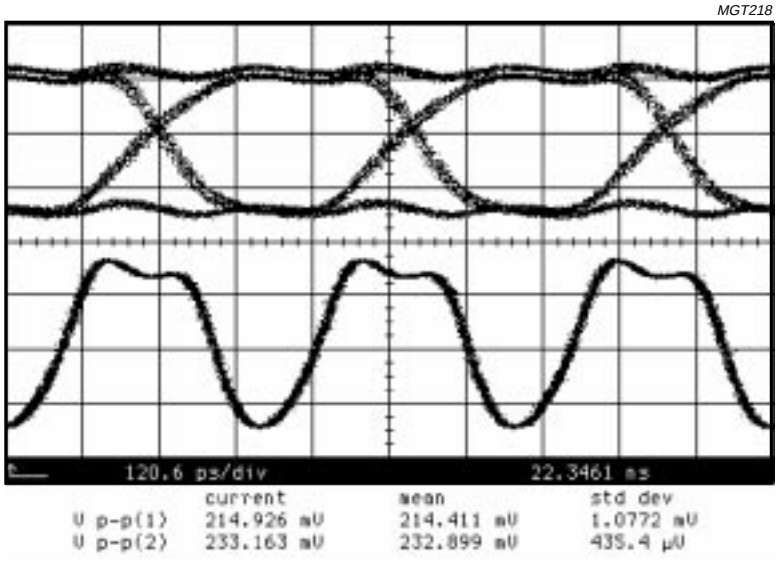
(1) ITU STM16; (2) OQ2541B.

Fig.21 Jitter transfer as a function of the jitter frequency in the STM16/OC48 mode (2488.32 Mbits/s).



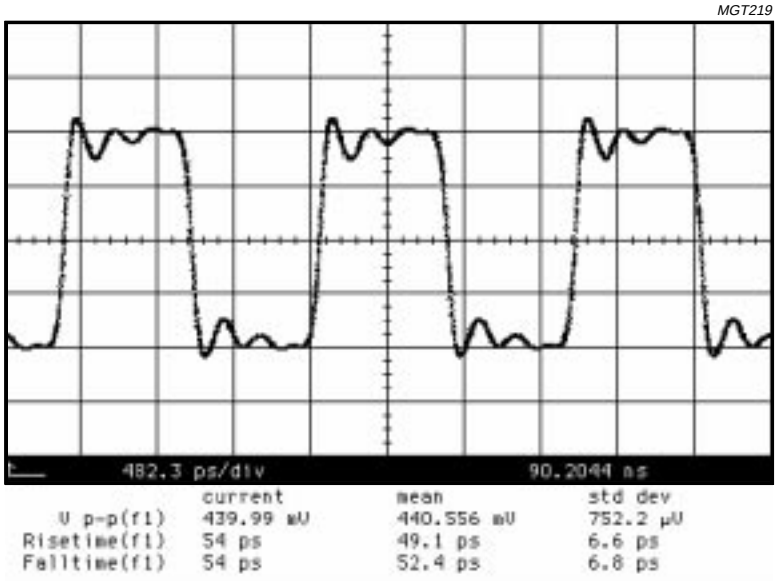
Measured single ended.

Fig.22 Data and clock output waveforms in the STM4/OC12 mode (622.08 Mbits/s).



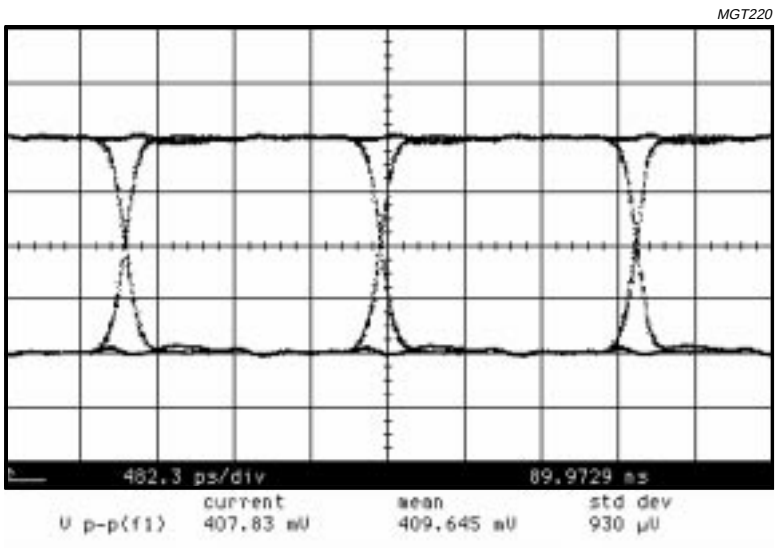
Measured single ended.

Fig.23 Data and clock output waveforms in the STM16/OC48 mode (2488.32 Mbits/s).



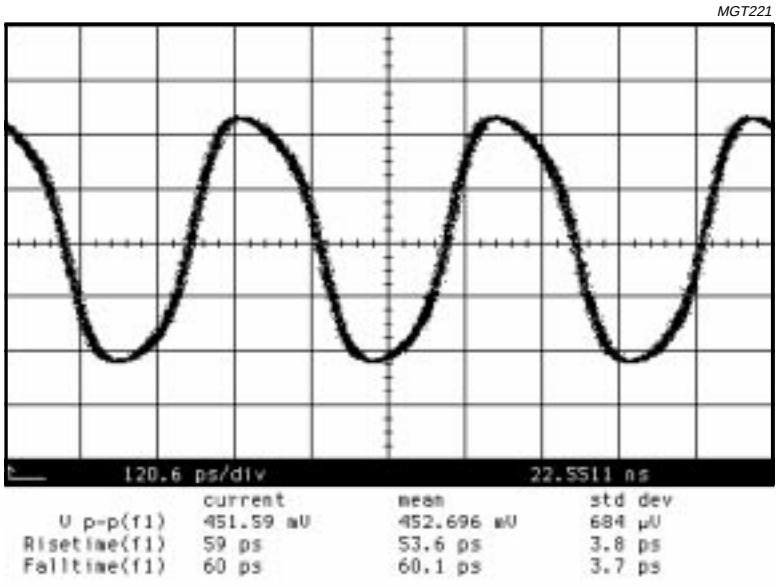
Measured differentially.

Fig.24 Clock output waveform in the STM4/OC12 mode (622.08 Mbits/s).



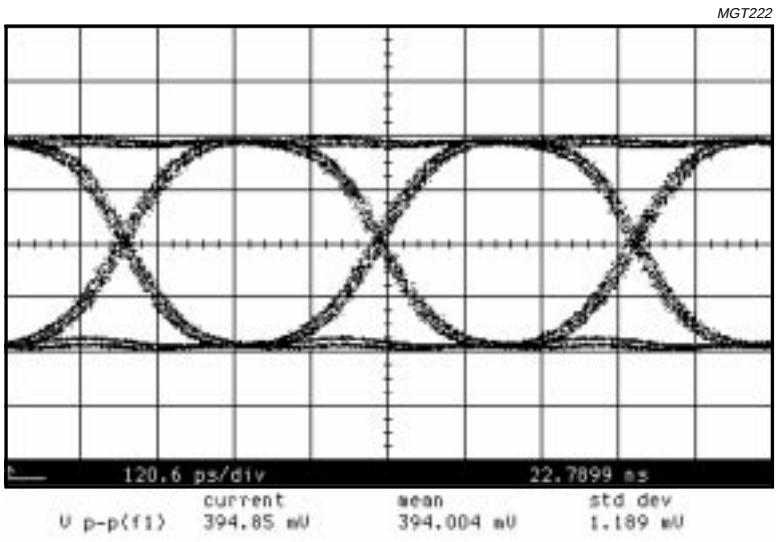
Measured differentially; PRBS $2^{23} - 1$ pattern.

Fig.25 Data output waveform in the STM4/OC12 mode (622.08 Mbits/s).



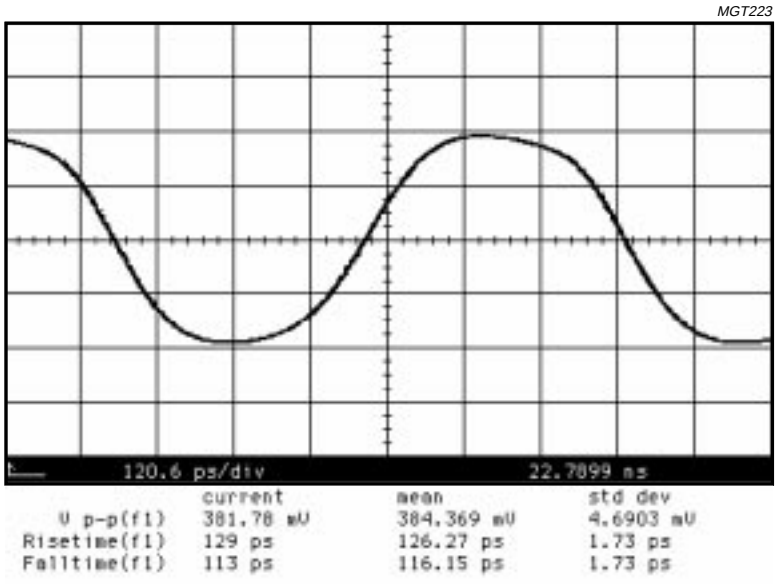
Measured differentially.

Fig.26 Clock output waveform in the STM16/OC48 mode (2488.32 Mbits/s).



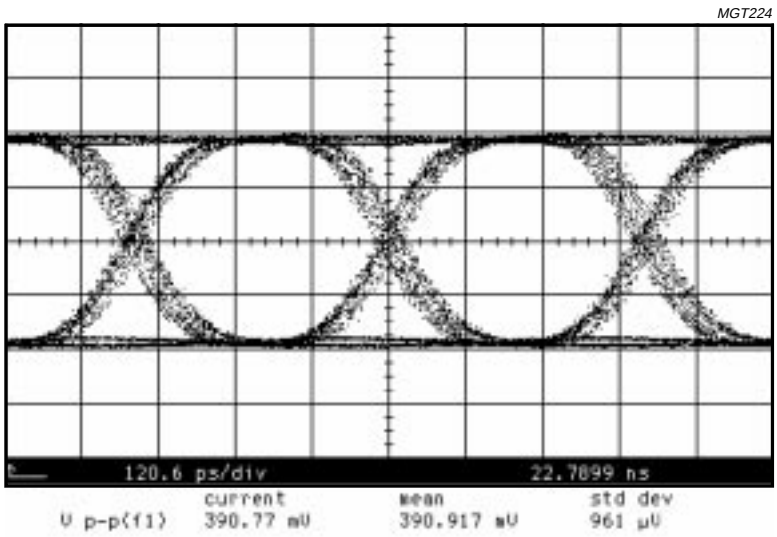
Measured differentially; PRBS $2^{23} - 1$

Fig.27 Data output waveform in the STM16/OC48 mode (2488.32 Mbits/s).



Measured differentially; 10101010 pattern.

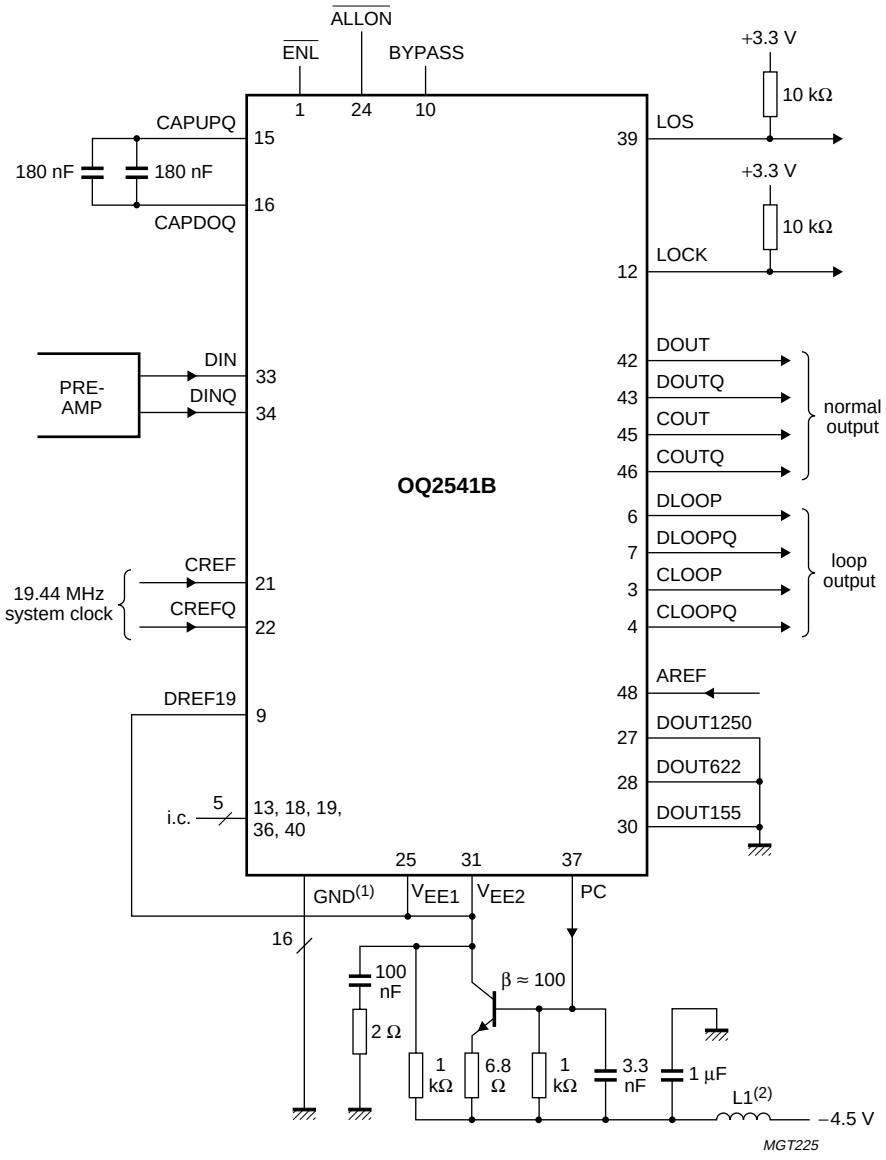
Fig.28 Data output waveform in the STM16/OC48 mode (2488.32 Mbits/s).



Measured differentially; bypass mode.

Fig.29 Data output waveform in the STM16/OC48 mode (2488.32 Mbits/s).

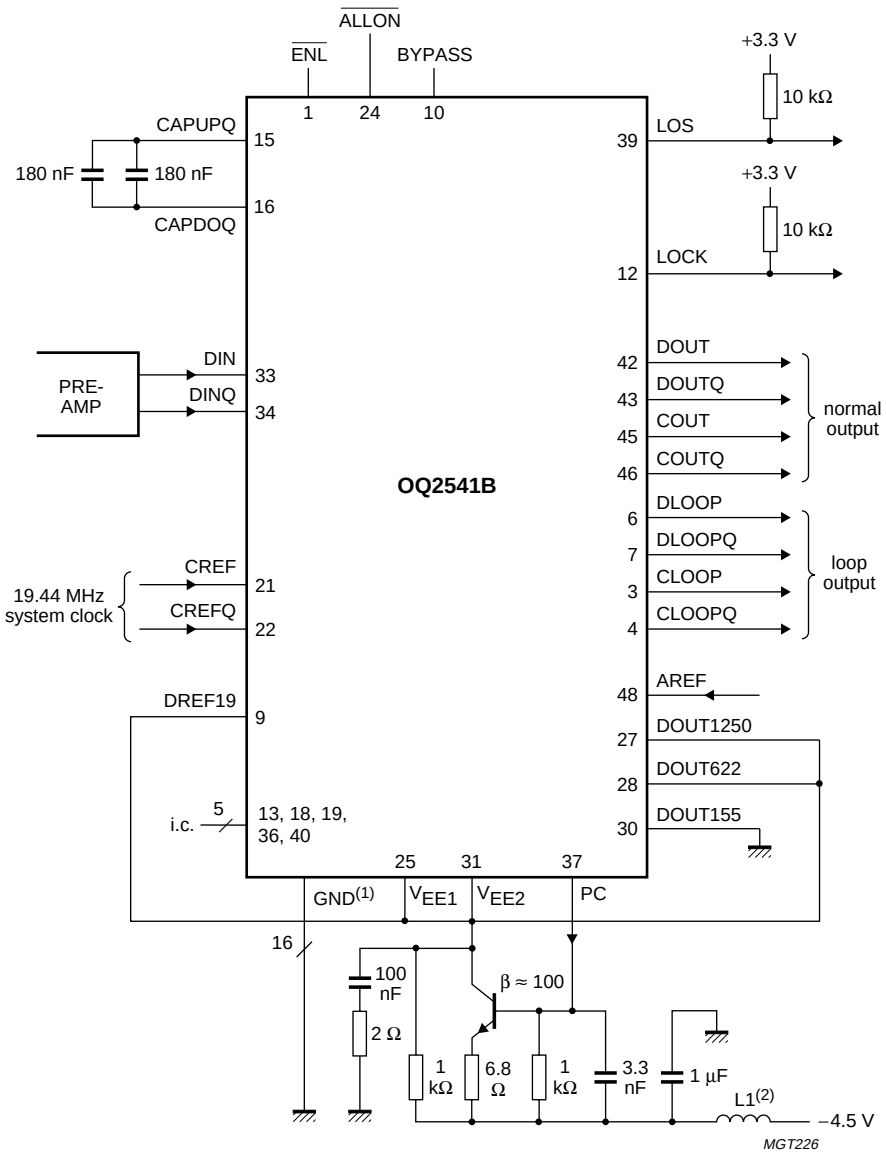
APPLICATION INFORMATION



(1) All pins GND must be connected directly to the PCB ground plane (pins 2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44 and 47).

(2) L1 = RF choke type Murata BLM21.

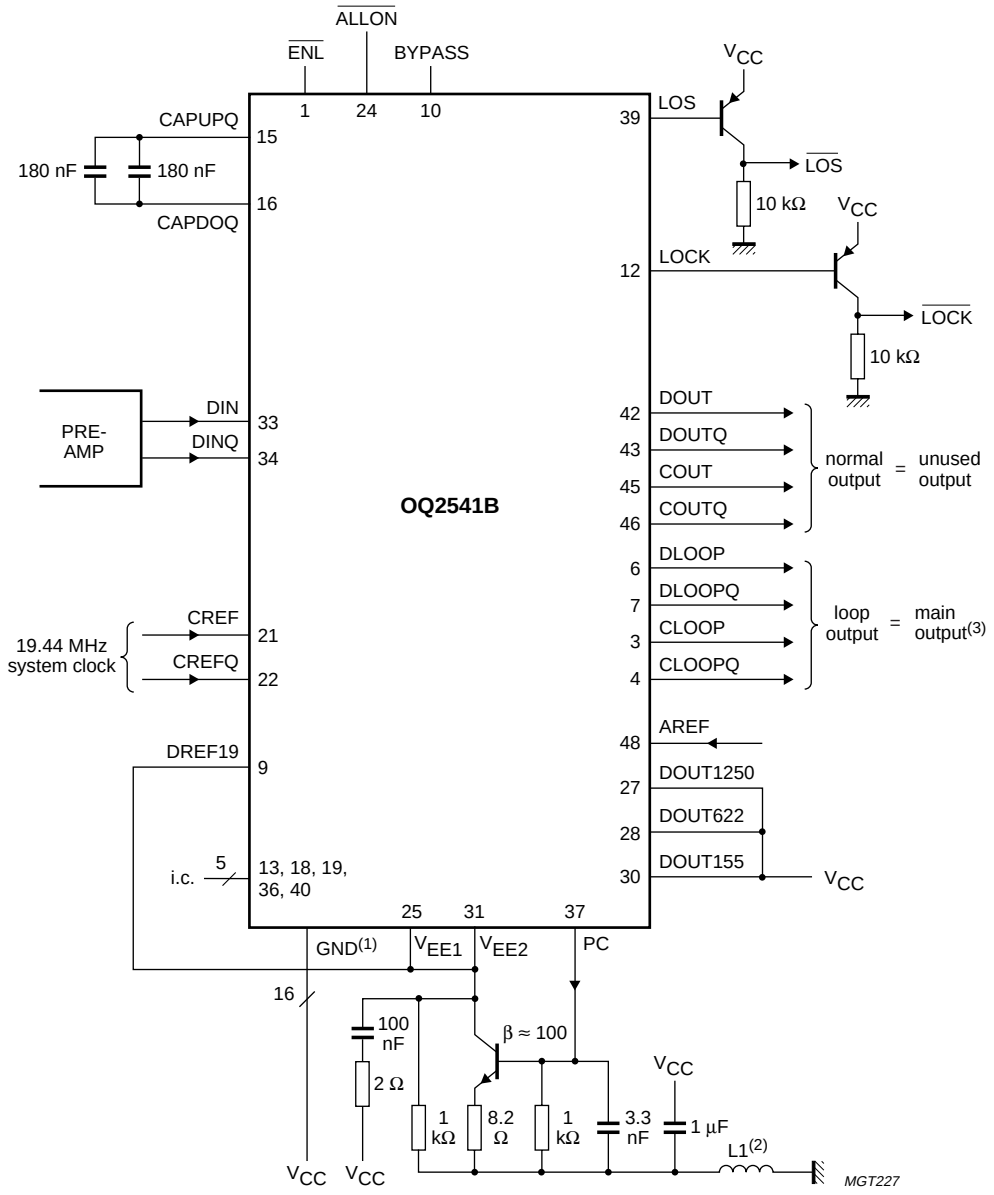
Fig.30 Application diagram showing the OQ2541B configured for the STM16/OC48 mode (2488.32 Mbits/s).



(1) All pins GND must be connected directly to the PCB ground plane (pins 2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44 and 47).

(2) L1 = RF choke type Murata BLM21.

Fig.31 Application diagram showing the OQ2541B configured for the STM4/OC12 mode (622.08 Mbits/s).



(1) All GND pins must be connected directly to V_{CC} on the PCB plane of 5 V (pins 2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44 and 47).

(2) L1 = RF choke type Murata BLM21.

(3) The loop mode outputs are used as main outputs.

Fig.32 Application diagram showing the OQ2541B configured for the STM16/OC48 mode (2488.32 Mbits/s) with a positive supply voltage application (V_{CC} = +5 V).

BONDING PAD LOCATIONS

Table 6 Bonding pad locations.

SYMBOL	PAD	COORDINATES(1)	
		x	y
$\overline{ENL}$	1	–1017.5	+852.5
GND	2	–1017.5	+697.5
CLOOP	3	–1017.5	+542.5
CLOOPQ	4	–1017.5	+387.5
GND	5	–1017.5	+232.5
DLOOP	6	–1017.5	+77.5
DLOOPQ	7	–1017.5	–77.5
GND	8	–1017.5	–232.5
DREF19	9	–1017.5	–387.5
BYPASS	10	–1017.5	–542.5
GND	11	–1017.5	–697.5
LOCK	12	–1017.5	–852.5
i.c.	13	–852.5	–1017.5
GND	14	–697.5	–1017.5
CAPUPQ	15	–542.5	–1017.5
CAPDOQ	16	–387.5	–1017.5
GND	17	–232.5	–1017.5
i.c.	18	–77.5	–1017.5
i.c.	19	+77.5	–1017.5
GND	20	+232.5	–1017.5
CREF	21	+387.5	–1017.5
CREFQ	22	+542.5	–1017.5
GND	23	+697.5	–1017.5
$\overline{ALLON}$	24	+852.5	–1017.5
V_{EE1}	25	+1017.5	–852.5
GND	26	+1017.5	–697.5
DOUT1250	27	+1017.5	–542.5
DOUT622	28	+1017.5	–387.5
GND	29	+1017.5	–232.5
DOUT155	30	+1017.5	–77.5
V_{EE2}	31	+1017.5	+77.5
GND	32	+1017.5	+232.5
DIN	33	+1017.5	+387.5
DINQ	34	+1017.5	+542.5
GND	35	+1017.5	+697.5
i.c.	36	+1017.5	+852.5
PC	37	+852.5	+1017.5
GND	38	+697.5	+1017.5
LOS	39	+542.5	+1017.5
i.c.	40	+387.5	+1017.5
GND	41	+232.5	+1017.5
DOUT	42	+77.5	+1017.5
DOUTQ	43	–77.5	+1017.5
GND	44	–232.5	+1017.5
COUT	45	–387.5	+1017.5
COUTQ	46	–542.5	+1017.5
GND	47	–697.5	+1017.5
AREF	48	–852.5	+1017.5

Note

1. All x and y coordinates represent the position of the centre of the pad in μm with respect to the centre of the die (see Fig.33).

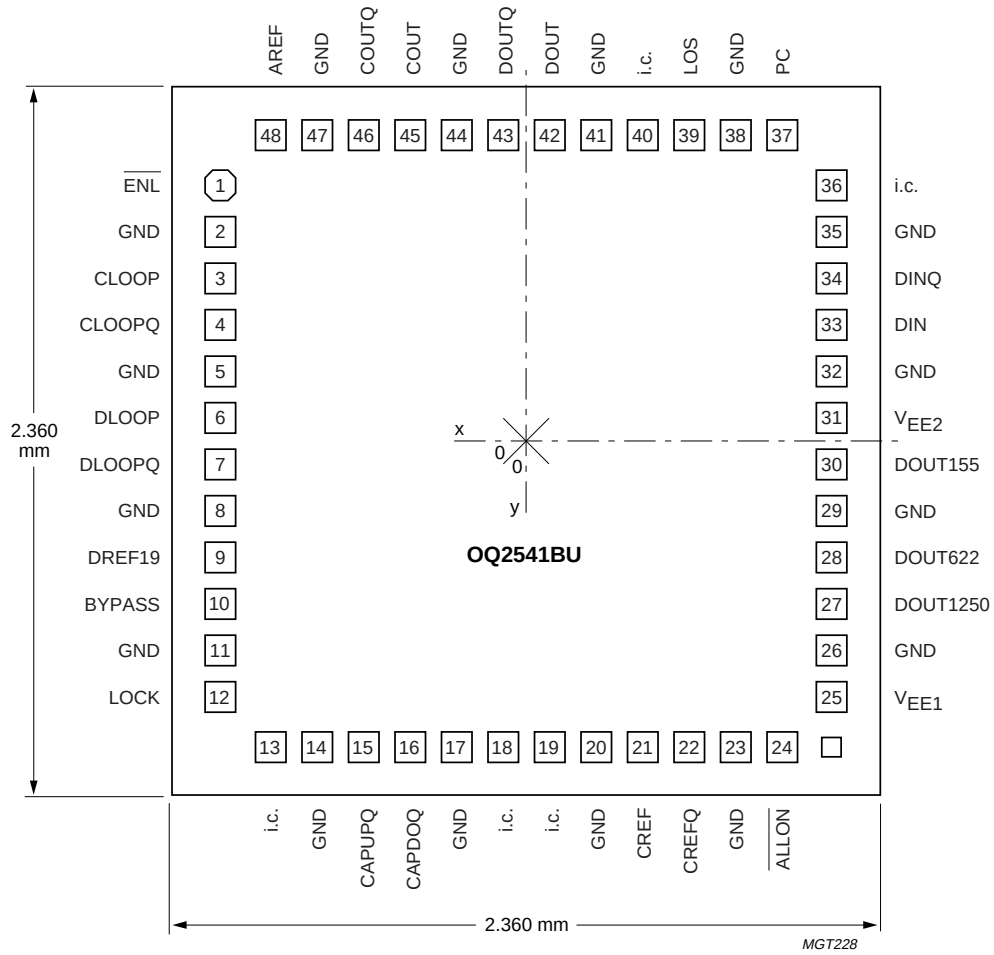


Fig.33 Bonding pad locations of OQ2541BU.

Table 7 Physical characteristics of bare die

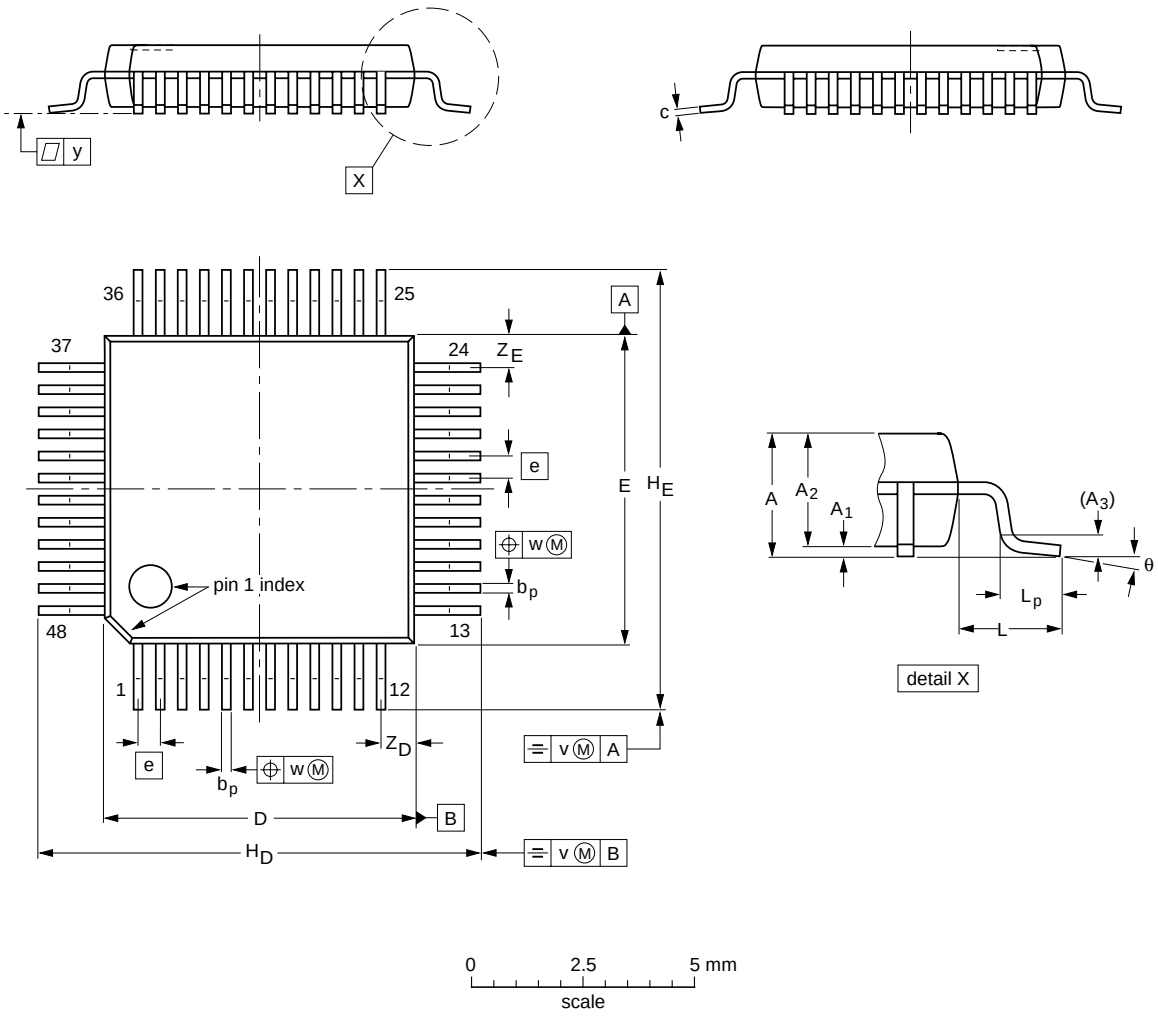
NAME	DESCRIPTION
Glass passivation	0.8 μm silicon nitride on top of 0.9 μm PSG (PhosphoSilicate Glass)
Bonding pad dimension	minimum dimension of exposed metallization is 90 × 90 μm (pad size = 100 × 100 μm)
Metallization	1.8 μm AlCu (1% Cu)
Thickness	380 μm nominal
Size	2.360 × 2.360 mm (5.5696 mm^2)
Backing	silicon; electrically connected to V_{EE} potential through substrate contacts
Attach temperature	<440 °C; recommended die attach is glue
Attach time	<15 s

Thermal considerations

To improve heat transfer away from the product, a large area fill is recommended as a die pad. The die should be mounted on this with a heat conductive glue. All supply and ground pads must be bonded to ensure good electrical performance; this also improves heat transfer to the die pad or other copper area fills. The more copper leading away from the die, the better the heat transport. In turn, this copper should be able to lose its heat to the environment through radiation, natural convection (unforced airflow over the printed-circuit board) or forced cooling.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				~~99-12-27~~ 00-01-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
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Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

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