Demo Kit Available

# 32-Channel High Voltage Amplifier Array

## Features

- ❑ 32 independent high voltage amplifiers
- ❑ 300V operating voltage
- ❑ 295V output voltage
- ❑ 2.2V/µs typical output slew rate
- ❑ Adjustable output current limit
- ❑ Internal closed loop gain of 72V/V
- ❑ 12MΩ feedback impedance
- ❑ Layout ideal for die applications

## Application

- ❑ MEMS (microelectromechanical systems) driver
- ❑ Piezoelectric transducer driver
- ❑ Optical crosspoint switches (using MEMS technology)

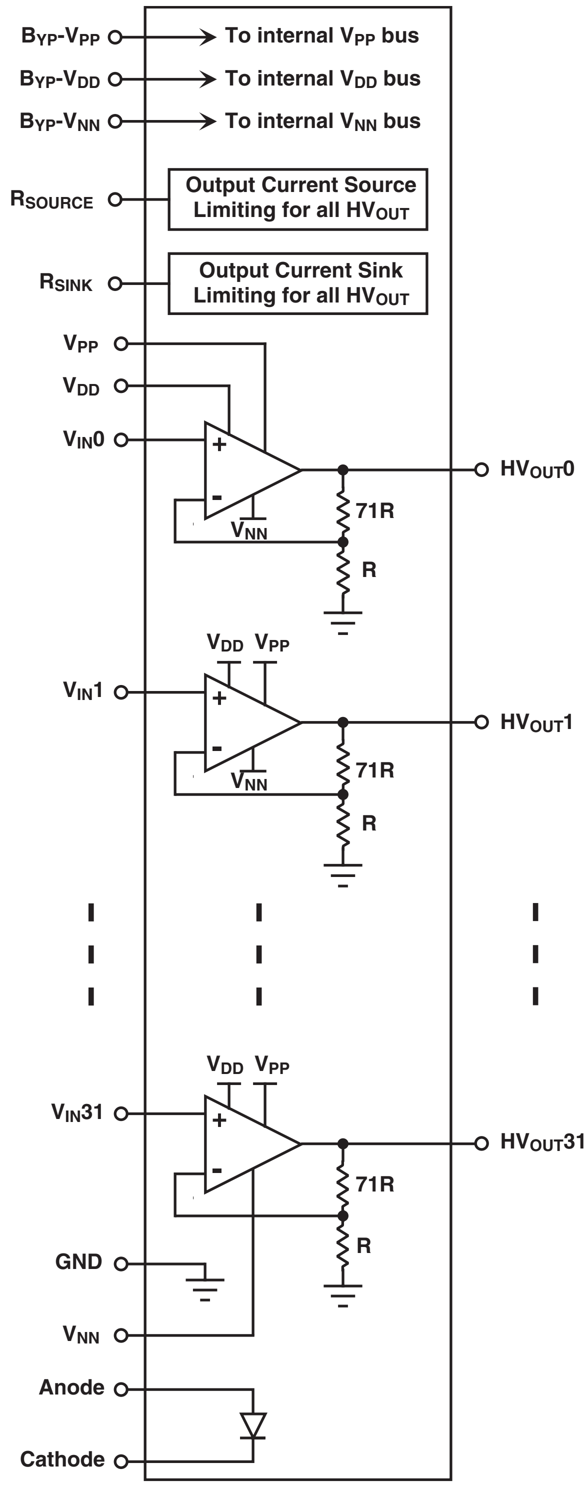
## General Description

The Supertex HV256 is a 32-channel high voltage amplifier array integrated circuit. It operates on a single high voltage supply, up to 300V and two low voltage supplies, $V_{DD}$ and $V_{NN}$.

The input voltage range is from 0V to 4.096V. The internal closed loop gain is 72V/V giving an output voltage of 295V when 4.096V is applied. Input voltages of up to 5V can be applied but will cause the output to saturate. The maximum output voltage swing is 5V below the $V_{PP}$ high voltage supply. The outputs can drive capacitive loads of up to 3000pF.

The maximum output source and sink current can be adjusted by using two external resistors. An external $R_{SOURCE}$ resistor controls the maximum sourcing current and an external $R_{SINK}$ resistor controls the maximum sinking current. The current limit is approximately 12.5V divided by the external resistor value. The setting is common for all 32 outputs. A low voltage silicon junction diode is made available to help monitor the die temperature.

## Block Diagram




A112304

## Ordering Information

| Device | Maximum Output Voltage | Nominal Closed Loop Gain | Package Options | |
|---|---|---|---|---|
| | | | 100 Lead MQFP | Die |
| HV256 | 295V | 72V/V | HV256FG | HV256X |

## Absolute Maximum Ratings*

| | |
|---|---|
| $V_{PP}$, High voltage supply | 310V |
| $V_{DD}$, Low voltage positive supply | 8.0V |
| $V_{NN}$, Low voltage negative supply | -7.0V |
| $V_{IN}$, Analog input signal | 0V to $V_{DD}$ |
| Storage temperature range | -65°C to 150°C |
| Maximum junction temperature | 150°C |

**Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

## Electrical Characteristics *(Over operating conditions unless otherwise noted.)*

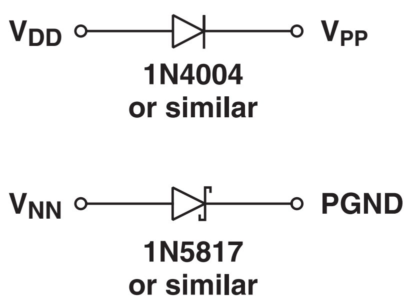
| Symbol | Parameter | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|---|
| **Operating Conditions** | | | | | | |
| $V_{PP}$ | High voltage positive supply | 125 | | 300 | V | |
| $V_{DD}$ | Low voltage positive supply | 6.0 | | 7.5 | V | |
| $V_{NN}$ | Low voltage negative supply | -4.5 | | -6.5 | V | |
| $I_{PP}$ | $V_{PP}$ supply current | | | 0.8 | mA | $V_{PP}$=300V, All $HV_{OUT}$=0V, No Load |
| $I_{DD}$ | $V_{DD}$ supply current | | | 4.3 | mA | $V_{DD}$ = 6.0V to 7.5V |
| $I_{NN}$ | $V_{NN}$ supply current | -5.2 | | | mA | $V_{NN}$ = -4.5V to -6.5V |
| $T_J$ | Junction temperature range | -10 | | 125 | ˚C | |
| **High Voltage Amplifier** | | | | | | |
| $HV_{OUT}$ | $HV_{OUT}$ voltage swing | 0 | | $V_{PP}$-5 | V | |
| $V_{IN}$ | Input voltage range | 0 | | 5.00 | V | |
| $V_{INOS}$ | Input voltage offset | | | ±50 | mV | Input referred. |
| SR | $HV_{OUT}$ slew rate rise | | 2.2 | | V/µs | No Load |
| | $HV_{OUT}$ slew rate fall | | 2.0 | | V/µs | No Load |
| BW | $HV_{OUT}$ -3dB channel bandwidth | | 4.0 | | KHz | $V_{PP}$=300V |
| $A_O$ | Open loop gain | 70 | 100 | | dB | |
| $A_V$ | Closed loop gain | 68.4 | 72.0 | 75.6 | V/V | |
| $R_{FB}$ | Feedback resistance from $HV_{OUT}$ to ground | 9.6 | 12 | | KΩ | |
| $C_{LOAD}$ | $HV_{OUT}$ capacitive load | 0 | | 3000 | pF | |
| $I_{SOURCE}$ | $HV_{OUT}$ sourcing current limiting range | 385 | 550 | 715 | µA | $R_{SOURCE}$=25KΩ |
| $I_{SINK}$ | $HV_{OUT}$ sinking current limiting range | 385 | 550 | 715 | µA | $R_{SINK}$=25KΩ |
| $R_{SOURCE}$ | External resistance range for setting current source limit | 25 | | 250 | KΩ | |
| $R_{SINK}$ | External resistance range for setting current sink limit | 25 | | 250 | KΩ | |
| $CT_{DC}$ | DC channel to channel crosstalk | -80 | | | dB | |
| PSRR | Power supply rejection ratio for $V_{PP}$, $V_{DD}$, and $V_{NN}$ | -40 | | | dB | |

## Diode

| Symbol | Parameter | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|---|
| PIV | Peak inverse voltage | | | 5.0 | V | cathode to anode |
| $V_F$ | Forward diode drop | | 0.60 | | V | If=100µA, anode to cathode |
| $I_F$ | Forward diode current | | | 100 | µA | anode to cathode |
| $T_C$ | $V_F$ temperature coefficient | | -2.20 | | mV/°C | anode to cathode |

## Power Up/Down Sequence

The device can be damaged due to improper power up / down sequence. To prevent damage, please follow the acceptable power up /down sequences and add two external diodes as shown in the diagram below. The first diode is a high voltage diode across $V_{PP}$ and $V_{DD}$ where the anode of the diode is connected to $V_{DD}$ and the cathode of the diode is connected to Vpp. Any low current high voltage diode such as a 1N4004 will be adequate. The second diode is a schottky diode across $V_{NN}$ and DGnd where the anode of the schottky diode is connected to $V_{NN}$ and the cathode is connected to DGnd. Any low current schottky diode such as a 1N5817 will be adequate.




**Acceptable Power Up Sequences**

1) $V_{PP}$ 2) $V_{NN}$ 3) $V_{DD}$ 4) Inputs & Anode
or
1) $V_{NN}$ 2) $V_{DD}$ 3) $V_{PP}$ 4) Inputs & Anode

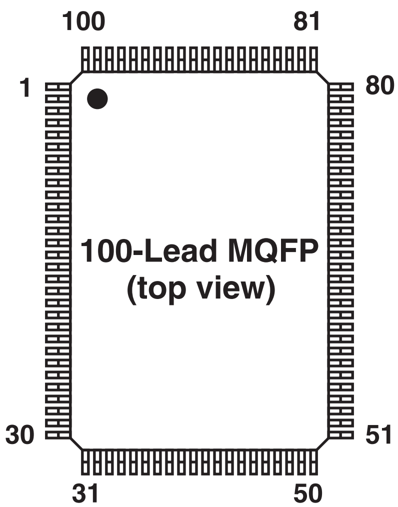
**Acceptable Power Down Sequences**

1) Inputs & Anode 2) $V_{DD}$ 3) $V_{NN}$ 4) $V_{PP}$
or
1) Inputs & Anode 2) $V_{PP}$ 3) $V_{DD}$ 4) $V_{NN}$

## Pin Description

| | |
|---|---|
| $V_{PP}$ | High voltage positive supply. There are two pads. |
| $B_{YP}$-$V_{PP}$ | A low voltage 1.0 to 10nF decoupling capacitor across $V_{PP}$ and $B_{YP}$-$V_{PP}$ is required. |
| $V_{DD}$ | Analog low voltage positive supply. There are four pads. |
| $B_{YP}$-$V_{DD}$ | A low voltage 1.0 to 10nF decoupling capacitor across $V_{DD}$ and $B_{YP}$-$V_{DD}$ is required. |
| $V_{NN}$ | Analog low voltage negative suply. There are four pads. |
| $B_{YP}$-$V_{NN}$ | A low voltage 1.0 to 10nF decoupling capacitor across $V_{NN}$ and $B_{YP}$-$V_{NN}$ is required. |
| GND | Device ground. There are four pads. |
| $R_{SOURCE}$ | External resistor from $R_{SOURCE}$ to $V_{NN}$ sets output current sourcing limit. Current limit is approximately 12.5V divided by Rsource resistor value. |
| $R_{SINK}$ | External resistor from $R_{SINK}$ to $V_{NN}$ sets output current sinking limit. Current limit is approximately 12.5V divided by $R_{SINK}$ resistor value. |
| Anode | Anode side of a low voltage silicon diode that can be used to monitor die temperature. |
| Cathode | Cathode side of a low voltage silicon diode that can be used to monitor die temperature. |
| $V_{IN}0$ to $V_{IN}31$ | Amplifier inputs |
| $HV_{OUT}0$ to $HV_{OUT}31$ | Amplifier outputs |

## Pin Configuration

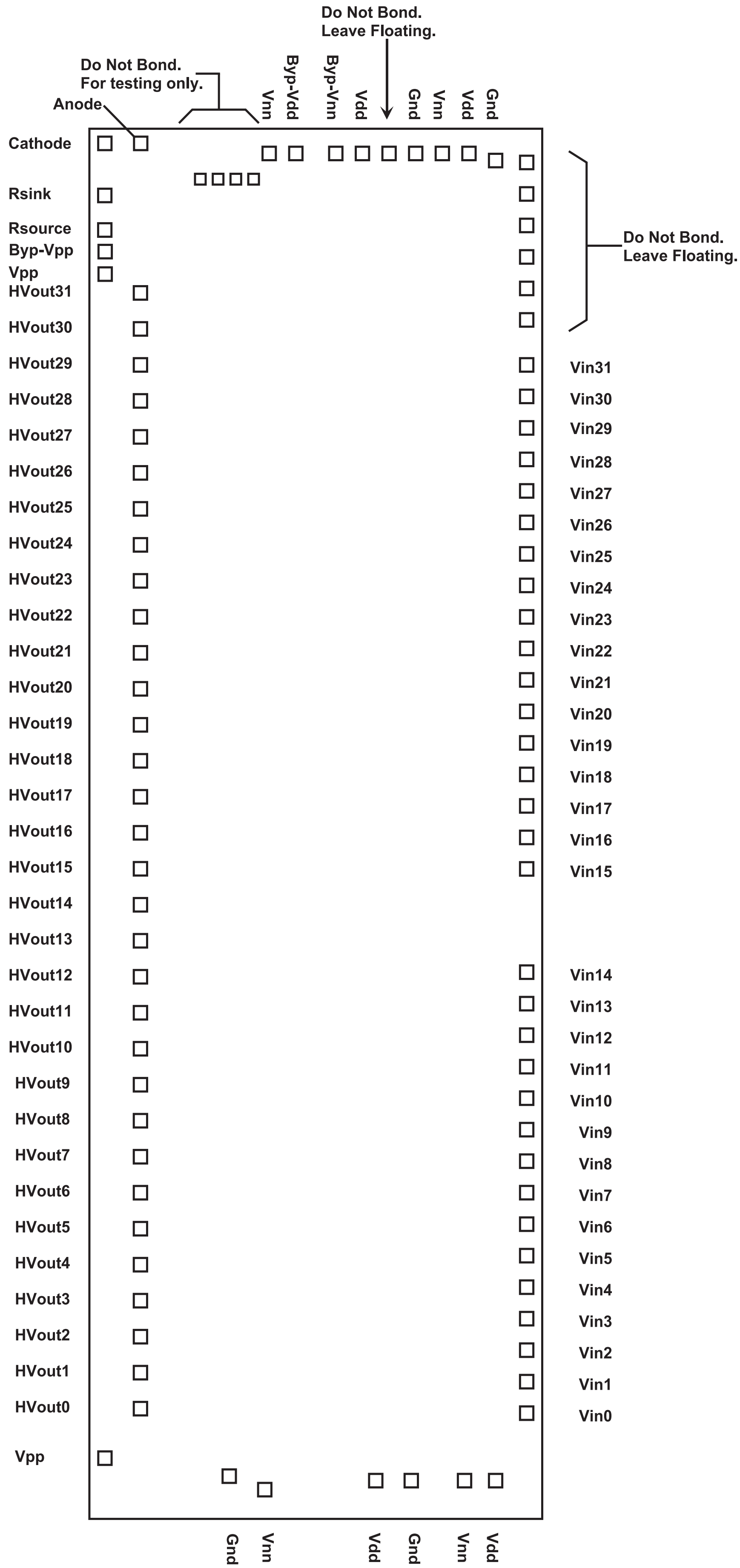



## Pin Configuration

| Pin # | Function | Pin # | Function | Pin # | Function | Pin # | Function |
|---|---|---|---|---|---|---|---|
| 1 | $HV_{OUT}31$ | 26 | $HV_{OUT}6$ | 51 | $V_{IN}3$ | 76 | $V_{IN}28$ |
| 2 | $HV_{OUT}30$ | 27 | $HV_{OUT}5$ | 52 | $V_{IN}4$ | 77 | $V_{IN}29$ |
| 3 | $HV_{OUT}29$ | 28 | $HV_{OUT}4$ | 53 | $VI_{IN}5$ | 78 | $V_{IN}30$ |
| 4 | $HV_{OUT}28$ | 29 | $HV_{OUT}3$ | 54 | $V_{IN}6$ | 79 | $V_{IN}31$ |
| 5 | $HV_{OUT}27$ | 30 | $HV_{OUT}2$ | 55 | $V_{IN}7$ | 80 | NC |
| 6 | $HV_{OUT}26$ | 31 | $HV_{OUT}1$ | 56 | $V_{IN}8$ | 81 | NC |
| 7 | $HV_{OUT}25$ | 32 | $HV_{OUT}0$ | 57 | $V_{IN}9$ | 82 | NC |
| 8 | $HV_{OUT}24$ | 33 | $V_{PP}$ | 58 | $V_{IN}10$ | 83 | NC |
| 9 | $HV_{OUT}23$ | 34 | NC | 59 | $V_{IN}11$ | 84 | NC |
| 10 | $HV_{OUT}22$ | 35 | NC | 60 | $V_{IN}12$ | 85 | NC |
| 11 | $HV_{OUT}21$ | 36 | NC | 61 | $V_{IN}13$ | 86 | Gnd |
| 12 | $HV_{OUT}20$ | 37 | NC | 62 | $V_{IN}14$ | 87 | $V_{DD}$ |
| 13 | $HV_{OUT}19$ | 38 | NC | 63 | $V_{IN}15$ | 88 | $V_{NN}$ |
| 14 | $HV_{OUT}18$ | 39 | Gnd | 64 | $VI_{IN}16$ | 89 | Gnd |
| 15 | $HV_{OUT}17$ | 40 | $V_{NN}$ | 65 | $V_{IN}17$ | 90 | NC |
| 16 | $HV_{OUT}16$ | 41 | NC | 66 | $V_{IN}18$ | 91 | $V_{DD}$ |
| 17 | $HV_{OUT}15$ | 42 | $V_{DD}$ | 67 | $V_{IN}19$ | 92 | Byp-$V_{NN}$ |
| 18 | $HV_{OUT}14$ | 43 | Gnd | 68 | $V_{IN}20$ | 93 | Byp-$V_{DD}$ |
| 19 | $HV_{OUT}13$ | 44 | $V_{NN}$ | 69 | $V_{IN}21$ | 94 | $V_{NN}$ |
| 20 | $HV_{OUT}12$ | 45 | $V_{DD}$ | 70 | $V_{IN}22$ | 95 | Anode |
| 21 | $HV_{OUT}11$ | 46 | NC | 71 | $V_{IN}23$ | 96 | Cathode |
| 22 | $HV_{OUT}10$ | 47 | NC | 72 | $V_{IN}24$ | 97 | $R_{SINK}$ |
| 23 | $HV_{OUT}9$ | 48 | $V_{IN}0$ | 73 | $V_{IN}25$ | 98 | $R_{SOURCE}$ |
| 24 | $HV_{OUT}8$ | 49 | $V_{IN}1$ | 74 | $V_{IN}26$ | 99 | Byp-$V_{PP}$ |
| 25 | $HV_{OUT}7$ | 50 | $V_{IN}2$ | 75 | $V_{IN}27$ | 100 | $V_{PP}$ |

NC=No Connect.

## Pad Configuration *(Not Drawn to Scale)*



# Pad Coordinates

Chip Size: 17004µm x 5480µm
Center of die is (0,0)

| Pad Name | X (µm) | X(µm) |
|---|---|---|
| $V_{PP}$ | -8338.5 | 2708.5 |
| $HV_{OUT}0$ | -7895.0 | 2305.5 |
| $HV_{OUT}1$ | -7448.5 | 2305.5 |
| $HV_{OUT}2$ | -7001.5 | 2305.5 |
| $HV_{OUT}3$ | -6554.5 | 2305.5 |
| $HV_{OUT}4$ | -6107.5 | 2305.5 |
| $HV_{OUT}5$ | -5660.5 | 2305.5 |
| $HV_{OUT}6$ | -5213.5 | 2305.5 |
| $HV_{OUT}7$ | -4766.5 | 2305.5 |
| $HV_{OUT}8$ | -4319.5 | 2305.5 |
| $HV_{OUT}9$ | -3872.5 | 2305.5 |
| $HV_{OUT}10$ | -3425.5 | 2305.5 |
| $HV_{OUT}11$ | -2978.5 | 2305.5 |
| $HV_{OUT}12$ | -2531.5 | 2305.5 |
| $HV_{OUT}13$ | -2084.5 | 2305.5 |
| $HV_{OUT}14$ | -1637.5 | 2305.5 |
| $HV_{OUT}15$ | -1190.5 | 2305.5 |
| $HV_{OUT}16$ | -743.5 | 2305.5 |
| $HV_{OUT}17$ | -296.5 | 2305.5 |
| $HV_{OUT}18$ | 150.0 | 2305.5 |
| $HV_{OUT}19$ | 597.5 | 2305.5 |
| $HV_{OUT}20$ | 1044.5 | 2305.5 |
| $HV_{OUT}21$ | 1491.5 | 2305.5 |
| $HV_{OUT}22$ | 1938.5 | 2305.5 |
| $HV_{OUT}23$ | 2385.5 | 2305.5 |
| $HV_{OUT}24$ | 2832.5 | 2305.5 |
| $HV_{OUT}25$ | 3279.5 | 2305.5 |
| $HV_{OUT}26$ | 3726.5 | 2305.5 |
| $HV_{OUT}27$ | 4173.5 | 2305.5 |

| Pad Name | X(µm) | Y(µm) |
|---|---|---|
| $HV_{OUT}28$ | 4620.5 | 2305.5 |
| $HV_{OUT}29$ | 5067.5 | 2305.5 |
| $HV_{OUT}30$ | 5514.5 | 2305.5 |
| $HV_{OUT}31$ | 5961.5 | 2305.5 |
| $V_{PP}$ | 6659 | 2709 |
| Byp-$V_{PP}$ | 7045 | 2709 |
| $R_{SOURCE}$ | 7489 | 2709 |
| $R_{SINK}$ | 7969 | 2709 |
| Cathode | 8366 | 2709 |
| Anode | 8366 | 2199 |
| $V_{NN}$ | 8047 | 425.0 |
| Byp-$V_{DD}$ | 8047 | 125.5 |
| Byp-$V_{NN}$ | 8047 | -345.5 |
| $V_{DD}$ | 8047 | -704.5 |
| GND | 8047 | -1424.0 |
| $V_{NN}$ | 8066.5 | -1590.0 |
| $V_{DD}$ | 8066.5 | -1958.5 |
| GND | 7867.0 | -2192.0 |
| $V_{IN}31$ | 5043.5 | -2686.0 |
| $V_{IN}30$ | 4638.5 | -2686.0 |
| $V_{IN}29$ | 4233.5 | -2686.0 |
| $V_{IN}28$ | 3828.5 | -2686.0 |
| $V_{IN}27$ | 3423.5 | -2686.0 |
| $V_{IN}26$ | 3018.5 | -2686.0 |
| $V_{IN}25$ | 2613.5 | -2686.0 |
| $V_{IN}24$ | 2208.5 | -2686.0 |
| $V_{IN}23$ | 1803.5 | -2686.0 |
| $V_{IN}22$ | 1398.5 | -2686.0 |
| $V_{IN}21$ | 993.5 | -2686.0 |

| Pad Name | X(µm) | Y(µm) |
|---|---|---|
| $V_{IN}20$ | 588.5 | -2686.0 |
| $V_{IN}19$ | 183.5 | -2686.0 |
| $V_{IN}18$ | -221.5 | -2686.0 |
| $V_{IN}17$ | -626.5 | -2686.0 |
| $V_{IN}16$ | -1031.5 | -2686.0 |
| $V_{IN}15$ | -1436.5 | -2686.0 |
| $V_{IN}14$ | -2412.0 | -2686.0 |
| $V_{IN}13$ | -2817 | -2686.0 |
| $V_{IN}12$ | -3222 | -2686.0 |
| $V_{IN}11$ | -3627 | -2686.0 |
| $V_{IN}10$ | -4032 | -2686.0 |
| $V_{IN}9$ | -4437 | -2686.0 |
| $V_{IN}8$ | -4842 | -2686.0 |
| $V_{IN}7$ | -5247 | -2686.0 |
| $V_{IN}6$ | -5652 | -2686.0 |
| $V_{IN}5$ | -6052 | -2686.0 |
| $V_{IN}4$ | -6462 | -2686.0 |
| $V_{IN}3$ | -6867 | -2686.0 |
| $V_{IN}2$ | -7272 | -2686.0 |
| $V_{IN}1$ | -7677 | -2686.0 |
| $V_{IN}0$ | -8082 | -2686.0 |
| $V_{DD}$ | -8373 | -2250.5 |
| $V_{NN}$ | -8373 | -1949.0 |
| GND | -8367 | -1561. |
| $V_{DD}$ | -8387 | -1143.0 |
| $V_{NN}$ | -8338.5 | 577.5 |
| GND | -8341.0 | 916.5 |



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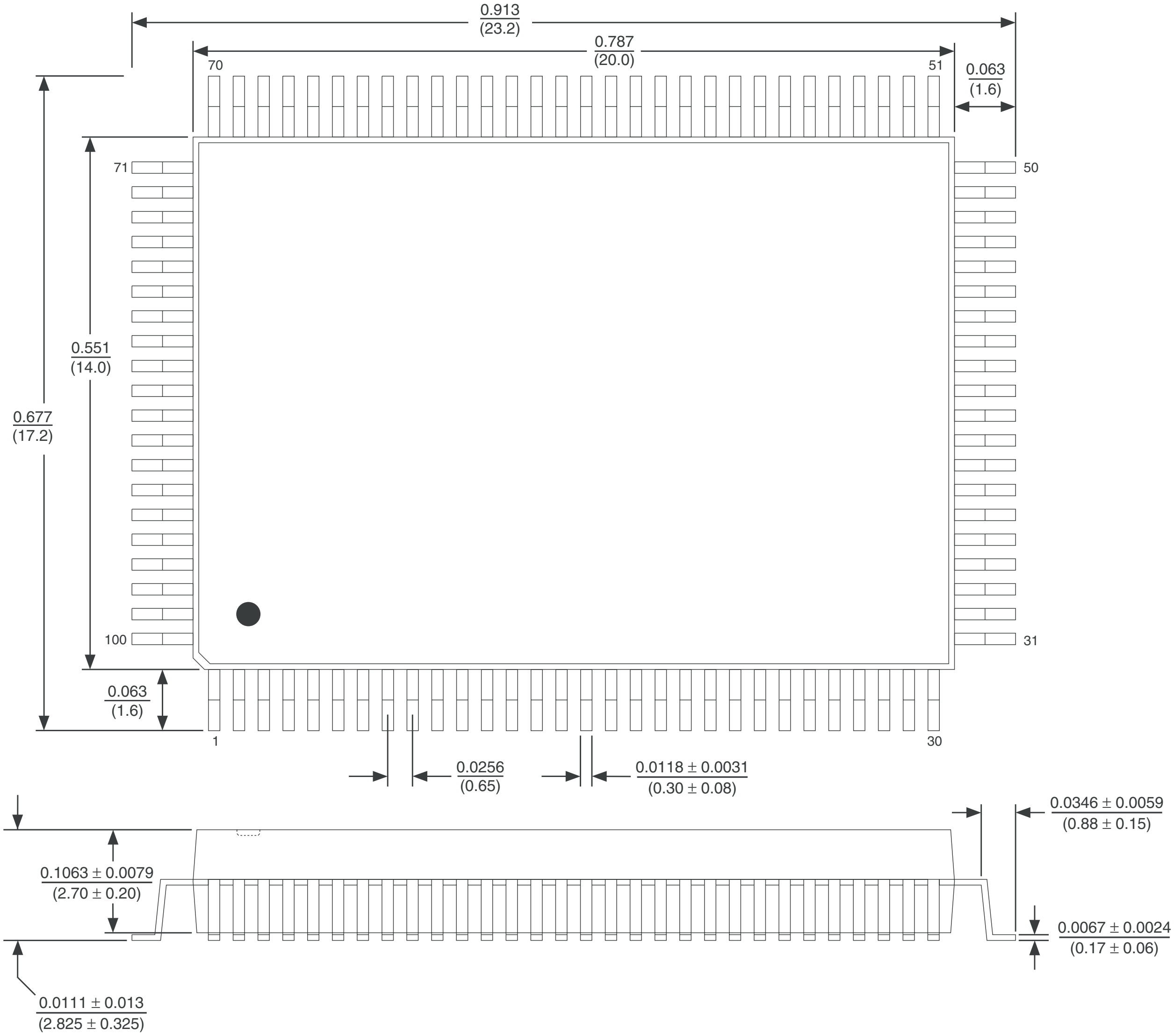
*DOC #: DSFP-HV256* *A112304*

# 100-LEAD MQFP PACKAGE OUTLINE (FG)




**Note:** Circle (e.g. (B)) indicates JEDEC Reference.

Measurement Legend = Dimensions in Inches / (Dimensions in Millimeters)



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