HOLT INTEGRATED CIRCUITS INC.

HI-3189

ARINC 429 Differential Line Driver

August 2008

GENERAL DESCRIPTION

The HI-3189 bus interface product is a silicon gate CMOS device designed as a line driver in accordance with the ARINC 429 bus specifications. It is a drop-in alternate source for the RM3182A (Fairchild /Raytheon) and DEI3182A.

Inputs are provided for clocking and synchronization. These signals are AND'd with the DATA inputs to enhance system performance and allow the HI-3189 to be used in a variety of applications. Both logic and synchronization inputs feature built-in 2,000V minimum ESD input protection as well as TTL and CMOS compatibility.

The HI-3189 has a digitally controlled data-rate input, allowing ARINC 429 line driver rise and fall times to be generated without changing the value of external timing components.

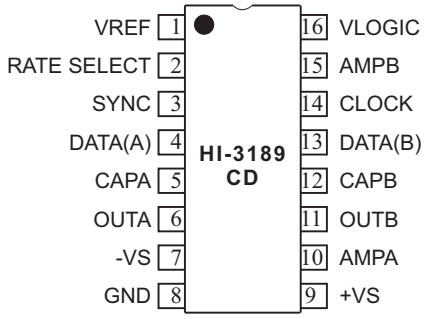
The output voltage swing is adjustable by the application of an external voltage to the VREF input. The OUTA and OUTB outputs have internal 37.5 Ohm series resistors to meet ARINC 429 line driver impedance requirements, voltage clamp diodes to improve robustness to over-voltage conditions and are short-circuit tolerant. Alternately, the AMPA and AMPB outputs have no internal resistors for applications that require additional clamping circuits to protect the HI-3189 from voltages that exceed the Maximum Ratings.

The HI-3189 line driver is intended for use where logic signals must be converted to ARINC 429 levels such as when using an ASIC, for example the HI-3584 429 Serial Transmitter/Dual Receiver, the HI-6010 ARINC 429 Transmitter/Receiver or similar ARINC Interface Device. Holt products are readily available for both industrial and military applications. Please contact the Holt Sales Department for additional information.

FEATURES

- Direct replacement for Fairchild/Raytheon RM3182A and DEI3182A
- TTL and CMOS compatible inputs
- Programmable output voltage swing
- Programmable ARINC rise and fall times
- Plastic 16-pin ceramic DIP and 28-lead ceramic LCC package options
- Operates at data rates up to 100 Kbits/s
- Overvoltage and short-circuit tolerance
- Industrial and Military temperature ranges

PIN CONFIGURATION (Top View)



16 - Pin Ceramic Side Brazed DIP

(See ordering information for additional pin configurations)

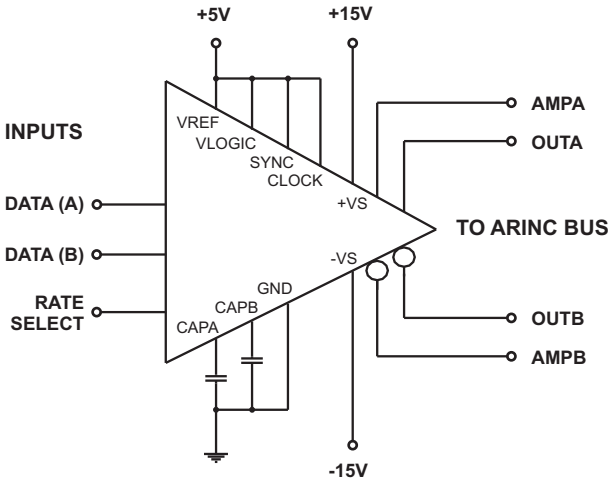


Figure 1. ARINC 429 Bus Application

TRUTH TABLE

SYNC	CLOCK	DATA(A)	DATA(B)	AOUT	BOUT	COMMENTS
X	L	X	X	0V	0V	NULL
L	X	X	X	0V	0V	NULL
H	H	L	L	0V	0V	NULL
H	H	L	H	-VREF	+VREF	LOW
H	H	H	L	+VREF	-VREF	HIGH
H	H	H	H	0V	0V	NULL

Table 1. Truth Table

PIN DESCRIPTIONS

SYMBOL	FUNCTION	DESCRIPTION
VREF	ANALOG	Ref. voltage used to determine output voltage swing. Pin sources current to allow use of a zener reference.
RATE SELECT	INPUT	Selects ARINC 429 data rate. See Table 2 for operation.
SYNC	INPUT	Synchronizes data inputs
DATA (A)	INPUT	Data input terminal A
CAPA	INPUT	Connection for DATA (A) slew-rate capacitor
OUTA	OUTPUT	ARINC output terminal A with 37.5 Ohms internal series resistance
-VS	POWER	-15V ± 10%
GND	POWER	0.0V
+VS	POWER	+15V ± 10%
AMPA	OUTPUT	ARINC output terminal A with 0 Ohms internal series resistance
OUTB	OUTPUT	ARINC output terminal B with 37.5 Ohms internal series resistance
CAPB	INPUT	Connection for DATA (B) slew-rate capacitor
DATA (B)	INPUT	Data input terminal B
CLOCK	INPUT	Synchronizes data inputs
AMPB	OUTPUT	ARINC output terminal B with 0 Ohms internal series resistance
VLOGIC	POWER	+5V ±10%

Rate Select	CAPA, CAPB Value (pF)	Rise / Fall Time 10% - 90% (us)	Data Rate (Kbits/sec)	Comments
Logic “0”	68	1.0 - 2.0	100	ARINC 429 High-Speed
Logic “1”	68	5.0 - 15.0	12.0 - 14.5	ARINC 429 Low-Speed
Logic “0”	470	5.0 - 15.0	12.0 - 14.5	ARINC 429 Low-Speed
Logic “1”	470	N/A	N/A	Not Used

Table 2. Rate Select Pin Truth Table

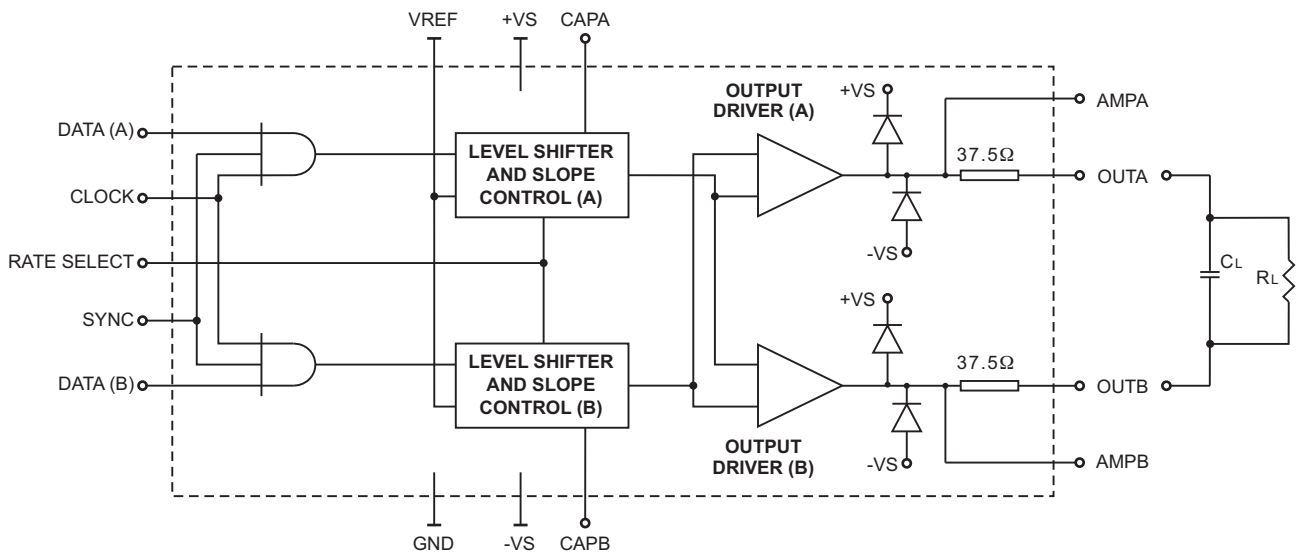


Figure 2. Functional Block Diagram

FUNCTIONAL DESCRIPTION

The HI-3189 is a complete differential line driver IC. When DATA (A) = DATA (B) or SYNC or CLOCK signal is low, the driver forces the output to a voltage Null level (0V +/- 250 mV). Designed to address the ARINC 429 standard, the HI-3189 has output rise and fall times that can be adjusted by the selection of an external capacitor (CAPA or CAPB) and an output voltage range adjustable through an externally applied VREF signal. All logic inputs and sync control inputs are TTL/CMOS compatible. The HI-3189 is available in 16-lead ceramic side-brazed DIP, 16-pin Cerdip and 28-pin ceramic LCC packages. See ordering information for available screening options.

The device contains three main functional blocks. The first block is a digital section used to decode the ARINC Clock, Synchronization, and Data inputs as shown in the Functional Block Diagram (Figure 2). This block takes these inputs and channels the data to the Level Shifter and Slope control Circuit. The logical relationship for these pins is presented in Table 1.

The second functional block is a charge pump circuit used to control the output waveform and its timing characteristics. This is achieved through charging and discharging a capacitor with a known current. The capacitor is user-selectable, and is connected between the CAPA or CAPB pins and ground. A Rate Select pin (digital input) is used to set the rise and fall time. If this pin is tied to ground, the device functions in the high-speed data rate. This mode is recommended if the user does not have an application requiring data rate switching. Table 2 gives recommended capacitor values for each possible data combination.

The last functional block of the device consists of a voltage follower and high power output differential amplifier. The voltage follower buffers the signals presented at the charge capacitors and presents the mirrored signal to the difference amplifier to drive the ARINC line. Two different outputs are available from the differential amplifiers: AMPA, AMPB, and OUTA, OUTB. The outputs AMPA and AMPB are the direct outputs of the power amplifier. The outputs OUTA and OUTB include 37.5 Ohm series resistors added to minimize bus reflections by matching the power amplifier's output impedance to the cable's impedance of 75 Ohms. AMPA and AMPB may be used to customize the output impedance of the device. These outputs can also be used to enhance the device's drive capability, for example, when driving the standard 10 nF // 400 Ohm load defined in the ARINC 429 specification (see output drive capability and capacitive loads for more details). All outputs are protected from voltage spikes with diodes connected between the output pins and the supply lines.

APPLICATIONS

Heat Sinking / Air Flow and Short Circuit Protection

The user application will determine if and how much heat sinking / air flow will be required for the HI-3189. Consideration must be given to ambient temperature, load conditions and output voltage swing. In addition, power increases with increased operating frequency. Use the thermal conductivity numbers given in the Ordering Information section to determine that the maximum allowable junction temperature of 175°C is not exceeded.

Outputs OUTA and OUTB will survive a short circuit to ground or to each other. During a short circuit of the output to either power supply or ground, the device must be able to dissipate the generated heat. For example, if the output is shorted to ground and +VS = +15V, the device must dissipate 15V x 0.165A = 2.5W. An appropriate heat sink is required in this situation.

Note that AMPA and AMPB outputs have no internal series resistance. Shorting these pins to either power supply or ground may cause failure of the device. An added external resistor will protect the circuit by limiting the current.

Power Supply Considerations

Three power supplies are required to operate the HI-3189 in a typical ARINC 429 bus application: +15V for +VS, -15V for -VS and +5V for both VREF and VLOGIC. The differential output swing of the HI-3189 is equal to 2 x VREF. Using +5V gives a differential output swing of 10V. If a different output voltage swing is required, an additional power supply is needed to set VREF.

Each power supply pin should be decoupled to ground using a high quality 10 uF tantalum capacitor. This is especially true when driving a large capacitive or resistive load. The decoupling capacitors should be located as close to the device pins as possible to eliminate the wiring inductance.

ABSOLUTE MAXIMUM RATINGS

All Voltages referenced to GND, TA = Operating Temperature Range (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	OPERATING RANGE	MAXIMUM	UNIT
Differential Voltage	V_{DIF}	Voltage between +VS and -VS terminals		40	V
Supply Voltage	+VS -VS VLOGIC		+13.5 to +16.5 -13.5 to -16.5 +5 ±10%	20 -20 +7	V V V
Voltage Reference	V_{REF}	For ARINC 429	+5 ±10%	6	V
Input Voltage Range	V_{IN}			≥ GND -0.5 ≤ V_{LOGIC} +0.5	V V
Operating Temperature Range	T_A	High-temp & Military Industrial	-55 to +125 -40 to +85		°C °C
AMPA/B Transient pulse	V_{PULSE}	150 us pulse applied through an external 37.5 Ohm resistor		±70	V
Storage Temperature Range	T_{STG}			-65 to +150	°C
Lead Temperature		Soldering, 60 seconds		+300	°C
Junction Temperature	T_J			-55 +175	°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TIMING DIAGRAMS

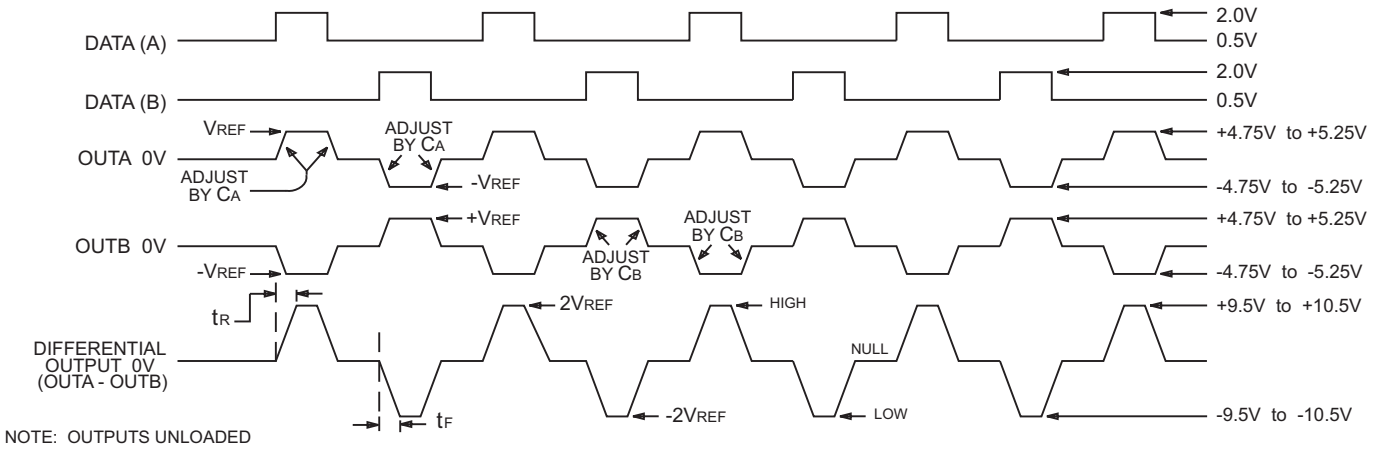


Figure 3. **SWITCHING WAVEFORMS**

AC ELECTRICAL CHARACTERISTICS

+V = +15V, -V = -15V, V_{LOGIC} = V_{REF} = +5.0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Rise Time (A_{OUT}, B_{OUT}) - High Speed	t_R	Rate Select = VIL, C_A = C_B = 68pF	1.0		2.0	µs
Fall Time (A_{OUT}, B_{OUT}) - High Speed	t_F	Rate Select = VIL, C_A = C_B = 68pF	1.0		2.0	µs
Rise Time (A_{OUT}, B_{OUT}) - Low Speed	t_R	Rate Select = VIH, C_A = C_B = 68pF	5.0		15.0	µs
Fall Time (A_{OUT}, B_{OUT}) - Low Speed	t_F	Rate Select = VIH, C_A = C_B = 68pF	5.0		15.0	µs

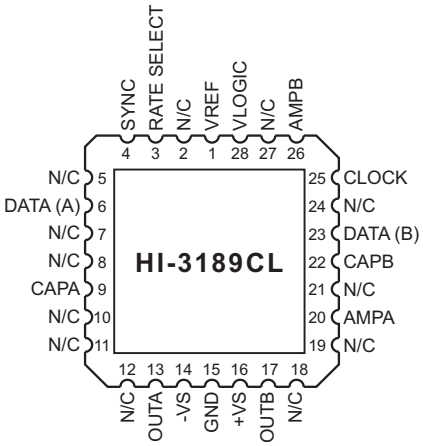
DC ELECTRICAL CHARACTERISTICS

+V = +15V, -V = -15V, V_{LOGIC} = V_{REF} = +5.0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Supply Current +VS	I_{CC}	+VS = 16.5V, -VS=-16.5V VLOGIC = VREF = 5.5V DATA(A) = CLOCK = SYNC = "1" DATA(B) = RATE SELECT = "0" Data Rate = 0 to 100 KHz, no load			18	mA
Supply Current -VS	I_{EE}	+VS = 16.5V, -VS=-16.5V VLOGIC = VREF = 5.5V DATA(A) = CLOCK = SYNC = "1" DATA(B) = RATE SELECT = "0" Data Rate = 0 to 100 KHz, no load			18	mA
Supply Current +VLOGIC	I_{LOGIC}	+VS = 16.5V, -VS=-16.5V VLOGIC = VREF = 5.5V DATA(A) = CLOCK = SYNC = "1" DATA(B) = RATE SELECT = "0" Data Rate = 0 to 100 KHz, no load			300	µA
Supply Current +VREF	I_{REF}	+VS = 16.5V, -VS=-16.5V VLOGIC = VREF = 5.5V DATA(A) = CLOCK = SYNC = "1" Data Rate = 0 to 100 KHz, no load	-800		-100	µA
Input Voltage High	V_{IH}		2.0			V
Input Voltage Low	V_{IL}				0.5	V
Input Current (Input High)	I_{IH}	VIN = 2.0V VLOGIC = VREF = 4.5V			1.0	µA
Input Current (Input Low)	I_{IL}	VIN = 0.5V VLOGIC = VREF = 5.5V	-645			nA
Input Capacitance	C_{IN}	See Note 1			15	pF
Output Voltage High (Output to Ground)	V_{OH}	No Load (0 -100KBPS) VREF = 5.0V Supplies min to max	+VREF -.25		+VREF +.25	V
Output Voltage Low (Output to Ground)	V_{OL}	No Load (0 -100KBPS) VREF = 5.0V Supplies min to max	-VREF -.25		-VREF +.25	V
Output Voltage Null	V_{NULL}	No Load (0-100KBPS)	-250		+250	mV
Output Impedance	Zo	Combined output impedance of OUTA and OUTB (See Note: 2)	67.5		82.5	Ω
Output Short Circuit Current	I_{SC}	OUTA and/or OUTB shorted line-to-line or to GND. Outputs High or Low	100		156	mA
+VS Short Circuit Current	I_{SC+VS}	OUTA and/or OUTB shorted line-to-line or to GND. Outputs High or Low			165	mA
-VS Short Circuit Current	I_{SC-VS}	OUTA and/or OUTB shorted line-to-line or to GND. Outputs High or Low	-165			mA

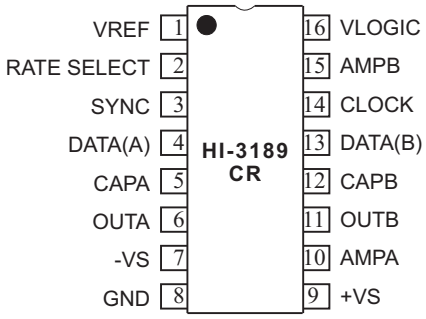
Note 1. Guaranteed by design, but not tested.
Note 2. Tested at DC only.

ADDITIONAL PIN CONFIGURATIONS (See page 1 for 16-Pin Ceramic Side-Brazed DIP))



28 - Pin Ceramic LCC

(See page 1 for additional pin configurations)



16 - Pin Cerdip package

(See page 1 for additional pin configurations)

ORDERING INFORMATION

HI - 3189 xx x

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No
M	-55°C TO +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION	LEAD FINISH	Theta JA	Theta JC
CD	16 PIN CERAMIC SIDE BRAZED DIP (16C)	Gold ('M' Flow: Solder)	70°C/W	28°C/W
CL	28 PIN CERAMIC LEADLESS CHIP CARRIER (LCC) (28S)	Gold ('M' Flow: Solder)	60°C/W	25°C/W
CR	16 PIN CERDIP (16D) not available with 'M' flow	Solder	70°C/W	28°C/W

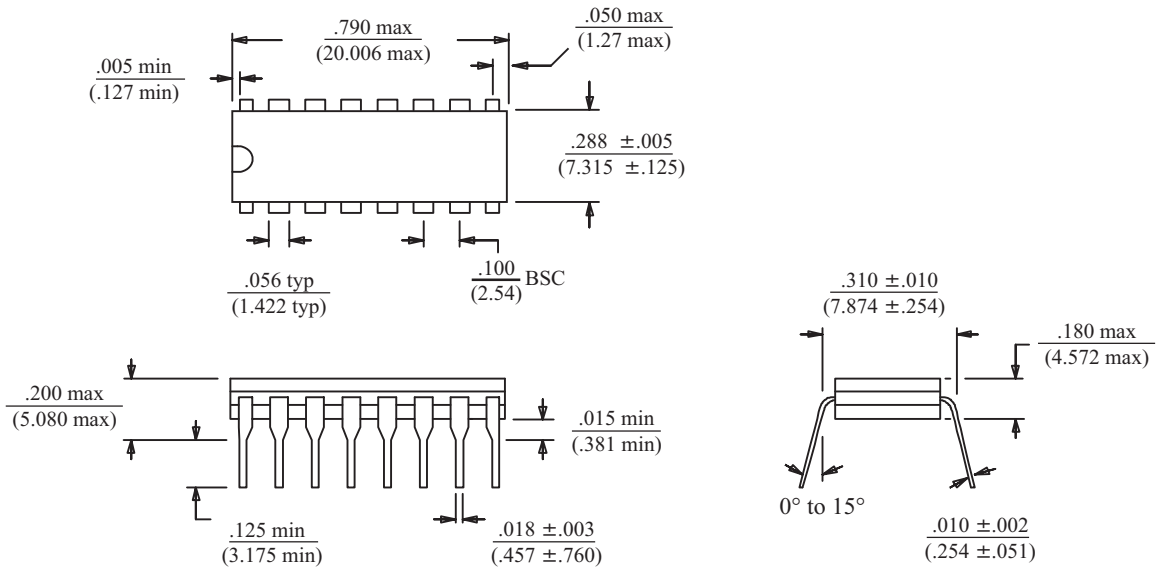
REVISION HISTORY

Revision	Date	Description of Change
DS-3189, Rev. New	08/22/08	Initial Release

16-PIN CERDIP

inches (millimeters)

Package Type: 16D

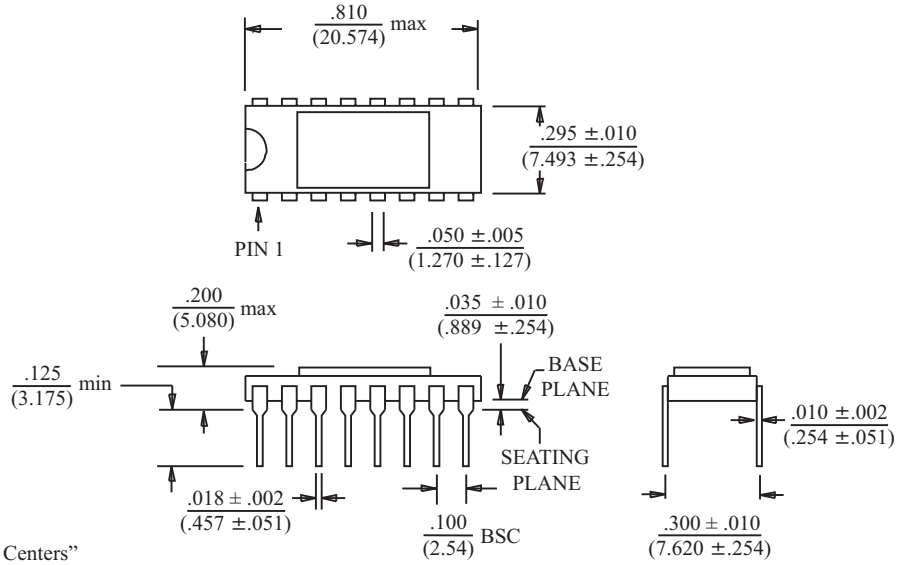


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

16-PIN CERAMIC SIDE-BRAZED DIP

inches (millimeters)

Package Type: 16C

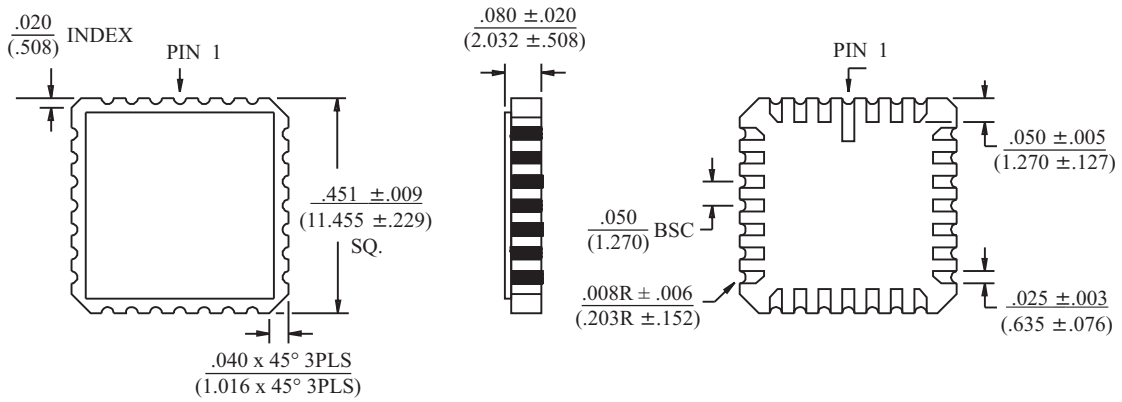


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

28-PIN CERAMIC LEADLESS CHIP CARRIER

inches (millimeters)

Package Type: 28S



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)