HOLT INTEGRATED CIRCUITS INC.

HI-3598, HI-3599

Octal ARINC 429 Receivers with Label Recognition and SPI Interface

June 2008

GENERAL DESCRIPTION

The HI-3598 and HI-3599 from Holt Integrated Circuits are silicon gate CMOS ICs for interfacing eight ARINC 429 receive buses to a high-speed Serial Peripheral Interface (SPI) enabled microcontroller. Each receiver has user-programmable label recognition for up to 16 labels, a four-word data buffer (FIFO), and an on-chip analog line receiver. Receive FIFO status can be monitored using the programmable external interrupt pins, or by polling the status register. Other features include the ability to switch the bit-significance of the ARINC 429 label, and to recognize the 32nd received ARINC bit as data or a parity flag. Versions are available with different input resistance values to provide flexibility when using external lightning protection circuitry.

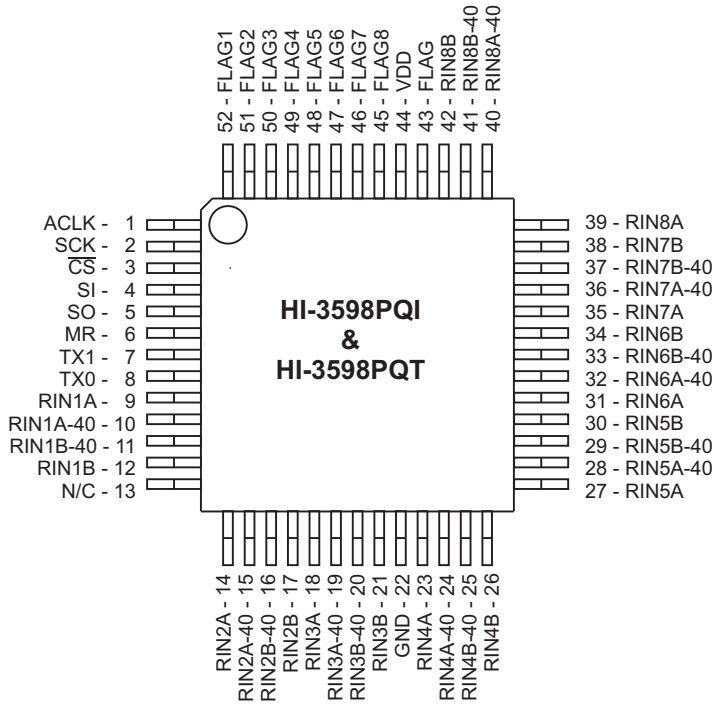
The Serial Peripheral Interface minimizes the number of host interface signals, providing a small footprint device which can be interfaced to a wide variety of industry-standard microcontrollers supporting SPI. Alternatively, the SPI interface may be controlled using four general purpose I/O port pins from a microcontroller or custom FPGA. The SPI and all control signals are CMOS and TTL compatible and support 3.3V or 5V operation.

The HI-3599 is identical to the HI-3598 except not all pins are available. This allows a minimum package footprint to be achieved with only slightly less hardware flexibility.

FEATURES

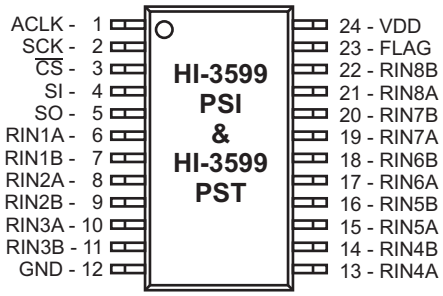
- ARINC 429 compliant
- 8 independent receive channels
- 3.3V or 5.0V logic supply operation
- On-chip analog line receivers connect directly to ARINC 429 bus
- Programmable label recognition for 16 labels per channel
- Independent data rate selection for each receiver
- Four-wire SPI interface
- Label bit-order control
- 32nd bit can be data or parity
- Reduced pin-count version (HI-3599) for minimum footprint
- Low power
- Industrial & extended temperature ranges

PIN CONFIGURATIONS (Top View)



HI-3598 Full function, full pin-out version
52 - Pin Plastic Quad Flat Pack (PQFP)

(See ordering information for additional pin configurations)

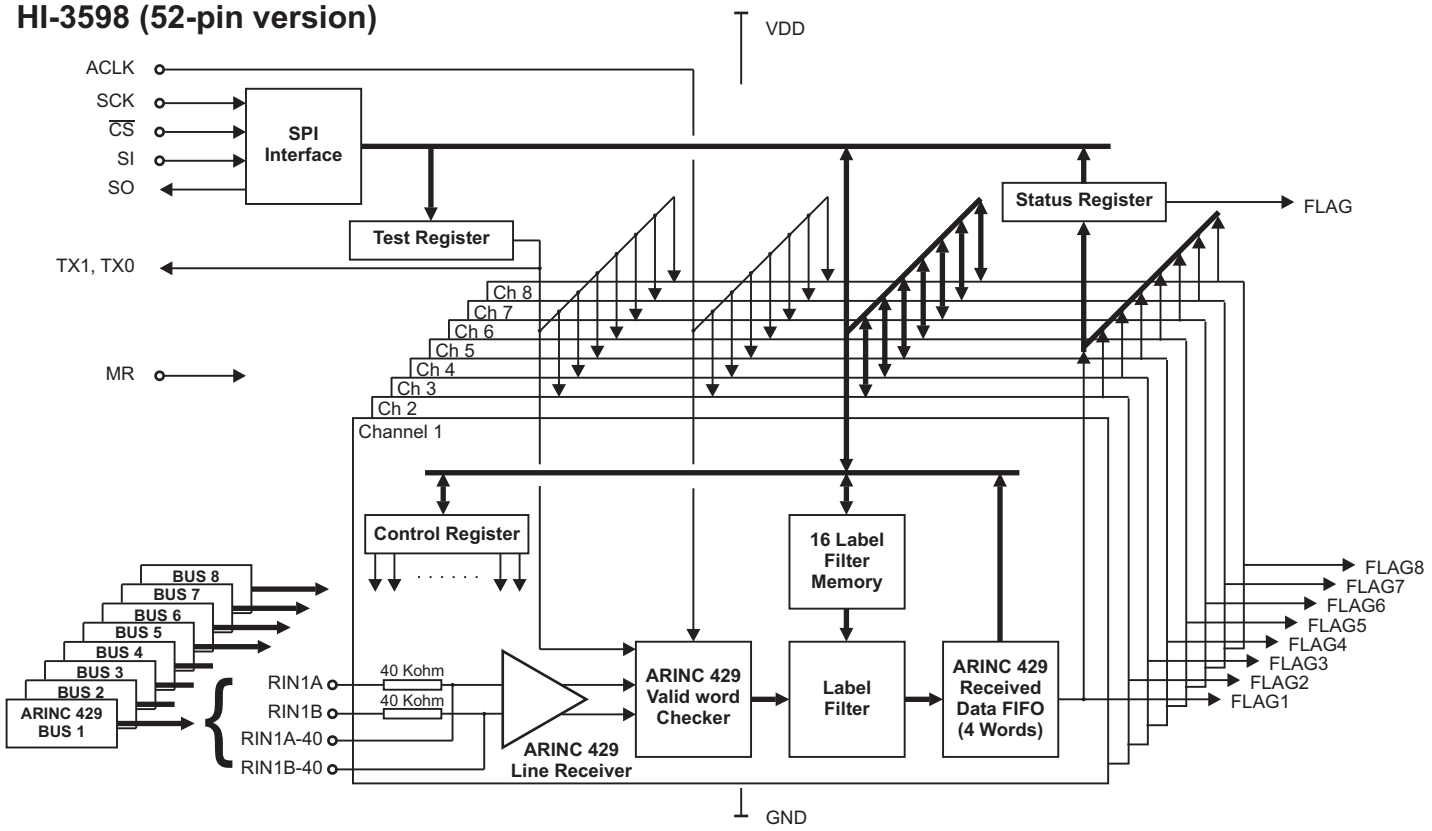


HI-3599 minimum footprint, reduced pin-out version
24 - Pin Plastic Small Outline package (SOIC)

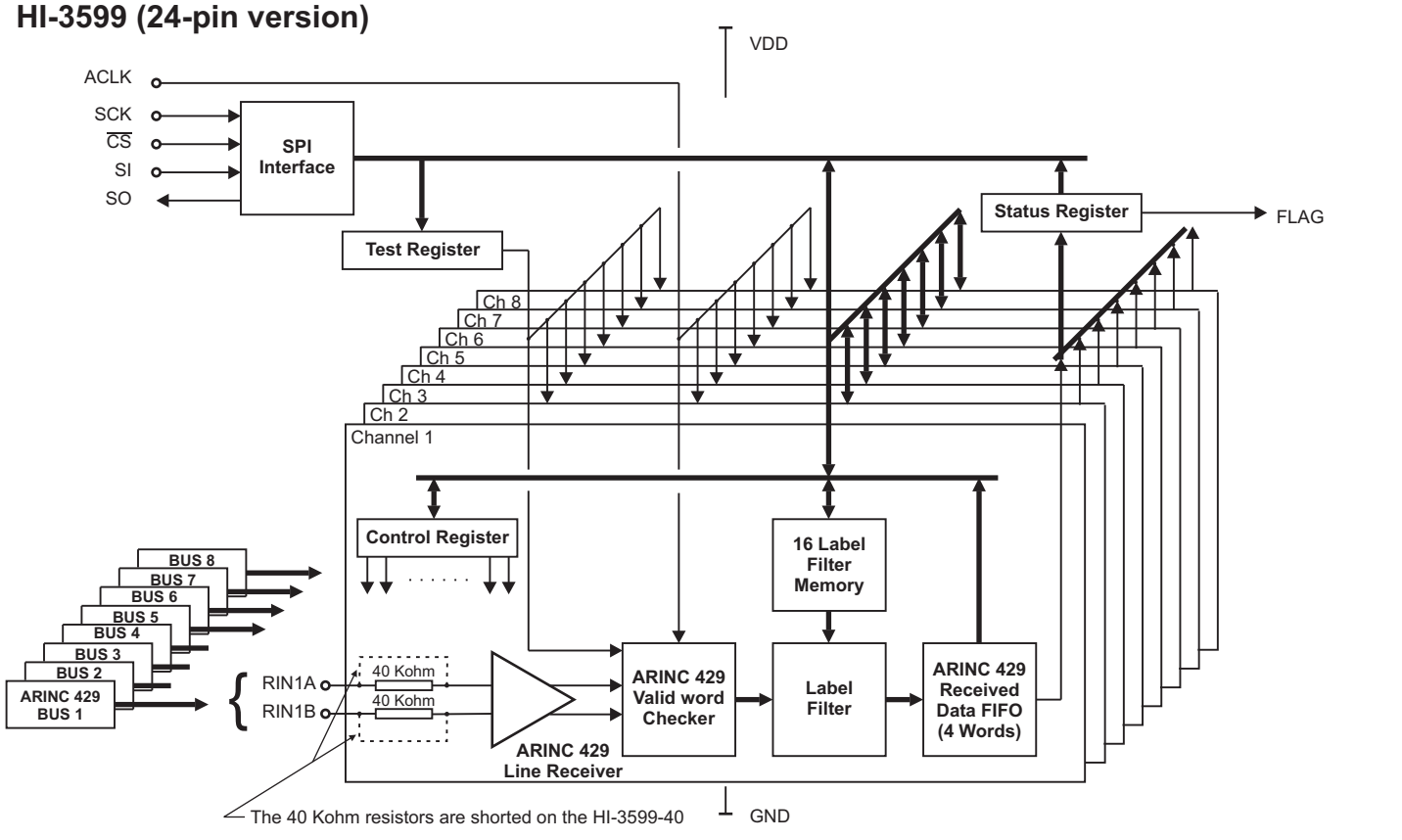
(See ordering information for additional pin configurations)

BLOCK DIAGRAMS

HI-3598 (52-pin version)



HI-3599 (24-pin version)



PIN DESCRIPTIONS

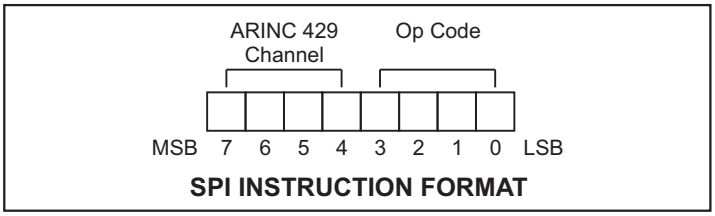
SIGNAL	FUNCTION	DESCRIPTION	3598	3599
VDD	POWER	3.3V or 5.0V power supply	X	X
GND	POWER	Chip 0V supply	X	X
$\overline{CS}$	INPUT	Chip select. Data is shifted into SI and out of SO when $\overline{CS}$ is low	X	X
SCK	INPUT	SPI Clock. Data is shifted into or out of the SPI interface using SCK	X	X
SI	INPUT	SPI interface serial data input	X	X
SO	OUTPUT	SPI interface serial data output	X	X
ACLK	INPUT	Master 1 MHz timing reference for the ARINC 429 receiver and transmitter	X	X
RINA1 - RINA8	ARINC INPUT	ARINC receiver positive input. Direct connection to ARINC 429 bus	X	Std
RINB1 - RINB8	ARINC INPUT	ARINC receiver negative input. Direct connection to ARINC 429 bus	X	Std
RINA1-40 - RINA8-40	ARINC INPUT	Alternate ARINC receiver positive input. Requires external 40K ohm resistor	X	-40
RINB1-40 - RINB8-40	ARINC INPUT	Alternate ARINC receiver negative input. Requires external 40K ohm resistor	X	-40
FLAG1 - FLAG8	OUTPUT	Goes high when ARINC 429 receiver FIFO is not empty (CR1=0), or full (CR1=1)	X	
FLAG	OUTPUT	Logical OR of FLAG1 through FLAG8	X	X
TX1	OUTPUT	ARINC 429 test word ONE state serial output pin	X	
TX0	OUTPUT	ARINC 429 test word ZERO state serial output pin	X	
MR	INPUT	Hardware active high Master Reset. Clears all receivers and FIFOs. Does not affect Control Register contents.	X	

INSTRUCTIONS

Instruction op codes are used to read, write and configure the HI-3598 & HI-3599. When $\overline{CS}$ goes low, the next 8 clocks at the SCK pin shift an instruction op code into the decoder, starting with the first rising edge. The op code is fed into the SI pin, most significant bit first.

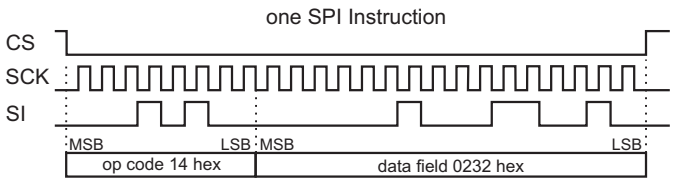
For write instructions, the most significant bit of the data word must immediately follow the instruction op code and is clocked into its register on the next rising SCK edge. Data word length varies depending on word type written: 16-bit Control Register writes, 32-bit self-test register writes or 128-bit writes to a channel's label-matching enable/disable memory.

For read instructions, the most significant bit of the requested data word appears at the SO pin after the last op code bit is clocked into the decoder, at the next falling SCK edge. As in write instructions, the data field bit-length varies with read instruction type.
Channel-specific instructions use the upper four bits to specify an ARINC 429 receiver channel, 1-8 hex. The lower four bits specify the op code, described in Table 1. The four channel assignment bits are "don't care" for instructions that are not channel-specific, such as Master Reset.



SPI INSTRUCTION FORMAT

Example:



ie: Load channel 1 control register with 0232 hex

TABLE 1. DEFINED INSTRUCTIONS

ARINC Channel	OP CODE Hex	DATA FIELD	DESCRIPTION
X	0h	None	Instruction not implemented. No operation.
1h - 8h	1h	128 bits	Load label values to label memory. The data field consists of 16, 8-bit labels. If fewer than 16 labels are needed for the application, the memory must be padded with redundant (duplicate) label values.
1h - 8h	2h	128 bits	Read the contents of the label memory for this channel
1h - 8h	3h	32 bits	Read an ARINC word from the receive FIFO for this channel. If the FIFO is empty all zeros will be read
1h - 8h	4h	16 bits	Load the specified channel's Control Register and clear that channel's FIFO
1h - 8h	5h	16 bits	Read the specified channel's Control Register
X	6h	16 bits	Read the Status Register.
X	7h	None	Master Reset (All channels)
X	8h	32 bits	Load the Self Test Register and send the test word to all receivers (High-speed data rate)
X	9h	32 bits	Load the Self Test Register and send the test word to all receivers (Low-speed data rate)
X	Ah - Fh	None	Instruction not implemented. No operation.

FUNCTIONAL DESCRIPTION

CONTROL WORD REGISTER

Each HI-3598 and HI-3599 receive channel is assigned a 16-bit Control Register which configures that receiver. Control Register bits CR15 - CR0 are loaded from a 16-bit data value appended to SPI instruction n4 hex, where “n” is the channel number 1-8 hex. Writing to the Control Register also clears the data FIFO for that channel. The Control Register contents may be read using SPI instruction n5 hex. The Control Register bits have the following functions:

CR Bit	FUNCTION	STATE	DESCRIPTION
Cr0 (LSB)	Receiver Data Rate Select	0	Data rate = ACLK/10 (ARINC 429 High-Speed)
		1	Data rate = ACLK/80 (ARINC 429 Low-Speed)
CR1	RFLAG Definition	0	FLAG goes high when receive FIFO is not empty (Contains at least one word)
		1	FLAG goes high when receive FIFO is full
CR2	Enable Label Recognition	0	Label recognition disabled
		1	Label recognition enabled
CR3	Reset Receiver	0	Normal operation
		1	Reset this receiver (Clear receiver logic and FIFO) The receive channel is disabled if CR3 is left high
CR4	Receiver Parity Check Enable	0	Receiver parity check disabled
		1	Receiver odd parity check enabled
CR5	Self Test	0	Receiver’s inputs are connected to the Self Test Register serial data output
		1	Normal operation
CR6	Receiver Decoder	0	Receiver decoder disabled
		1	ARINC bits 10 and 9 must match CR7 and CR8
CR7	-	-	If receiver decoder is enabled, the ARINC bit 10 must match this bit
CR8	-	-	If receiver decoder is enabled, the ARINC bit 9 must match this bit
CR9	ARINC Label Bit Order	0	Label bit order reversed (See Table 2)
		1	Label bit order same as received (See Table 2)
CR10	Not used	X	Control register read returns “0” for this bit
CR11	Not used	X	Control register read returns “0” for this bit
CR12	Not used	X	Control register read returns “0” for this bit
CR13	Not used	X	Control register read returns “0” for this bit
CR14	Not used	X	Control register read returns “0” for this bit
CR15 (MSB)	Not used	X	Control register read returns “0” for this bit

STATUS REGISTER

The HI-3598 and HI-3599 have a single 16-bit Status Register which is read to determine status for the eight received data FIFOs. The Status Register is read using SPI instruction n6 hex. The following table defines the Status Register bits:

SR Bit	FUNCTION	STATE	DESCRIPTION
SR0 (LSB)	Receiver 1 FIFO Empty	0	Receiver 1 FIFO contains valid data. Resets to Zero when all data has been read. FLAG pin reflects the state of this bit when CR1=”0”
		1	Receiver 1 FIFO is empty
SR1	Receiver 2 FIFO Empty	0	Receiver 2 FIFO contains valid data
		1	Receiver 2 FIFO is empty
SR2	Receiver 3 FIFO Empty	0	Receiver 3 FIFO contains valid data
		1	Receiver 3 FIFO is empty
SR3	Receiver 4 FIFO Empty	0	Receiver 4 FIFO contains valid data
		1	Receiver 4 FIFO is empty
SR4	Receiver 5 FIFO Empty	0	Receiver 5 FIFO contains valid data
		1	Receiver 5 FIFO is empty
SR5	Receiver 6 FIFO Empty	0	Receiver 6 FIFO contains valid data
		1	Receiver 6 FIFO is empty
SR6	Receiver 7 FIFO Empty	0	Receiver 7 FIFO contains valid data
		1	Receiver 7 FIFO is empty
SR7	Receiver 8 FIFO Empty	0	Receiver 8 FIFO contains valid data
		1	Receiver 8 FIFO is empty
SR8	Receiver 1 FIFO Full	0	Receiver 1 FIFO not full. FLAG pin reflects the state of this bit when CR1=”1”
		1	Receiver 1 FIFO full. To avoid data loss, the FIFO must be read within one ARINC word period
SR9	Receiver 2 FIFO Full	0	Receiver 2 FIFO not full.
		1	Receiver 2 FIFO full.
SR10	Receiver 3 FIFO Full	0	Receiver 3 FIFO not full.
		1	Receiver 3 FIFO full.
SR11	Receiver 4 FIFO Full	0	Receiver 4 FIFO not full.
		1	Receiver 4 FIFO full.
SR12	Receiver 5 FIFO Full	0	Receiver 5 FIFO not full.
		1	Receiver 5 FIFO full.
SR13	Receiver 6 FIFO Full	0	Receiver 6 FIFO not full.
		1	Receiver 6 FIFO full.
SR14	Receiver 7 FIFO Full	0	Receiver 7 FIFO not full.
		1	Receiver 7 FIFO full.
SR15 (MSB)	Receiver 8 FIFO Full	0	Receiver 8 FIFO not full.
		1	Receiver 8 FIFO full.

FUNCTIONAL DESCRIPTION (cont.)

ARINC 429 DATA FORMAT

Control Register bit CR9 controls how individual bits in the received ARINC word are mapped to the HI-3598 and HI-3599 SPI data word during data read operations. The following table describes this mapping:

Table 2. SPI / ARINC bit-mapping

SPI bit	1	2	3	4	5	6	7	8	9	10	11 - 31	32
ARINC bit CR9=0	8 Label (LSB)	7 Label	6 Label	5 Label	4 Label	3 Label	2 Label	1 Label (MSB)	9 SDI	10 SDI	11 - 31 Data	32 Parity
ARINC bit CR9=1	1 Label (MSB)	2 Label	3 Label	4 Label	5 Label	6 Label	7 Label	8 Label (LSB)	9 SDI	10 SDI	11 - 31 Data	32 Parity

ARINC 429 RECEIVER

ARINC BUS INTERFACE

Figure 1 shows the input circuit for each on-chip ARINC 429 line receiver. The ARINC 429 specification requires the following detection levels:

STATE	DIFFERENTIAL VOLTAGE
ONE	+6.5 Volts to +13 Volts
NULL	+2.5 Volts to -2.5 Volts
ZERO	-6.5 Volts to -13 Volts

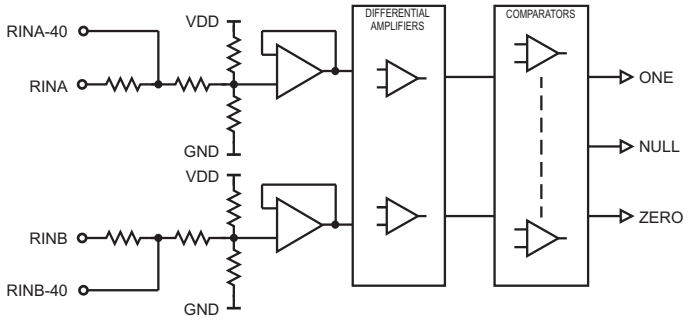


FIGURE 1. ARINC RECEIVER INPUT

The HI-3598 and HI-3599 guarantee recognition of these levels with a common mode Voltage with respect to GND less than ±30V for the worst case condition (3.15V supply and 13V signal level).

The tolerances in the design guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the ARINC signal is out of the actual acceptance ranges, including the nulls, the chip rejects the data.

RECEIVER LOGIC OPERATION

Figure 2 is a block diagram showing the logic for each receiver.

BIT TIMING

The ARINC 429 specification defines the following timing tolerances for received data:

	HIGH SPEED	LOW SPEED
BIT RATE	100K BPS ± 1%	12K -14.5K BPS
PULSE RISE TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSE FALL TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSE WIDTH	5 µsec ± 5%	34.5 to 41.7 µsec

The HI-3598 and HI-3599 accept signals within these tolerances and rejects signals outside these tolerances. Receiver logic achieves this as described below:

1. An accurate 1MHz clock source is required to validate the receive signal timing. Less than 0.1% error is recommended.

2. The receiver uses three separate 10-bit sampling shift registers for Ones detection, Zeros detection and Null detection. When the input signal is within the differential voltage range for any shift register's state (One Zero or Null) sampling clocks a high bit into that register. When the receive signal is outside the differential voltage range defined for any shift register, a low bit is clocked. Only one shift register can clock a high bit for any given sample. All three registers clock low bits if the differential input voltage is between defined state voltage bands.

Valid data bits require at least three consecutive One or Zero samples (three high bits) in the upper half of the Ones or Zeros sampling shift register, and at least three consecutive Null samples (three high bits) in the lower half of the Null sampling shift register within the data bit interval.

A word gap Null requires at least three consecutive Null samples (three high bits) in the upper half of the Null sampling shift register and at least three consecutive Null samples (three high bits) in the lower half of the Null sampling shift register. This guarantees the minimum pulse width.

3. To validate the receive data bit rate, each bit must follow its preceding bit by not less than 8 samples and not more than 12 samples. With exactly 1MHz input clock frequency, the acceptable data bit rates are:

	HIGH SPEED	LOW SPEED
DATA BIT RATE MIN	83K BPS	10.4K BPS
DATA BIT RATE MAX	125K BPS	15.6K BPS

4. Following the last data bit of a valid reception, the Word Gap timer samples the Null shift register every 10 input clocks (every 80 clocks for low speed). If a Null is present, the Word Gap counter is incremented. A Word Gap count of 3 enables the next reception.

FUNCTIONAL DESCRIPTION (cont.)

RECEIVER PARITY

If enabled by setting Control Register CR4 bit to ”1”, the receiver parity circuit counts Ones received, including the parity bit. If the result is odd, then a "0" appears in the 32nd bit.

Setting Control Register CR4 bit to ”0” disables parity checking and all 32 bits are treated as data.

RETRIEVING DATA

Once 32 valid bits are recognized, the receiver logic generates an End of Sequence (EOS). Depending on the state of Control Register bits CR2, CR6, CR7 and CR8, the received 32-bit ARINC word is then checked for correct decoding and label match before it is loaded into the 4 x 32 Receive FIFO. ARINC words that do not match required 9th and 10th ARINC bit and do not have a label match are ignored and are not loaded into the Receive FIFO. The adjacent table describes this operation.

TABLE 3. FIFO LOADING CONTROL

CR2	ARINC word matches Enabled label	CR6	ARINC word bits 10, 9 match CR7, 8	FIFO
0	X	0	X	Load FIFO
1	No	0	X	Ignore data
1	Yes	0	X	Load FIFO
0	X	1	No	Ignore data
0	X	1	Yes	Load FIFO
1	Yes	1	No	Ignore data
1	No	1	Yes	Ignore data
1	No	1	No	Ignore data
1	Yes	1	Yes	Load FIFO

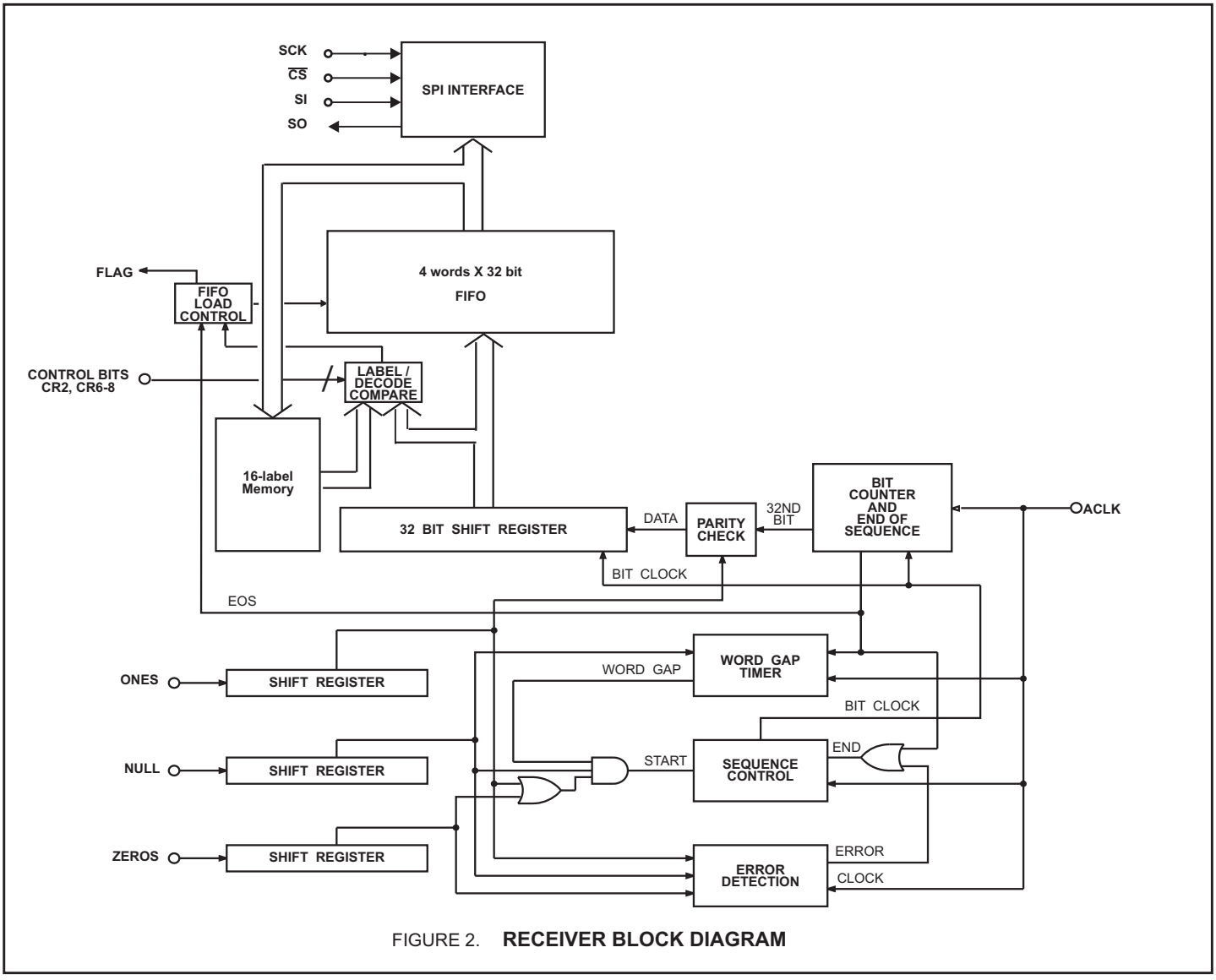


FIGURE 2. **RECEIVER BLOCK DIAGRAM**

FUNCTIONAL DESCRIPTION (cont.)

Once a valid ARINC word is loaded into the FIFO, the EOS signal clocks the Data Ready flip-flop to a "1", and the corresponding channel's Status Register FIFO Empty bit (SR0- SR7) goes to a "0". The channel's Empty bit remains low until the corresponding Receive FIFO is empty. Each received ARINC word is retrieved via the SPI interface using SPI instruction n3 hex where "n" is the channel number 1-8 hex.

Up to 4 ARINC words may be held in each channel's Receive FIFO. The Status Register FIFO Full bit (SR8 - SR15) goes high when the corresponding channel's Receive FIFO is full. Failure to offload a full Receive FIFO causes additional received valid ARINC words to overwrite the last received word.

LABEL RECOGNITION

The user loads the 16 byte label look-up table to specify which 8-bit incoming ARINC labels are captured by the receiver, and which are discarded. If fewer than 16 labels are required, spare label memory locations must be filled with duplicate copies of any valid label. After the look-up table is initialized, set channel Control Register bit CR2 to enable label recognition for that channel.

If label recognition is enabled, the receiver compares the label in each new ARINC word against the channel's stored label look-up table. If a label match is found, the received word is processed. If no match occurs, the new ARINC word is discarded and no indicators of received ARINC data are presented. Note that 00 hex is treated in the same way as any other label value. Label memory bit significance is not changed by the status of Control Register bit CR9. The most significant label bit is always compared to the first (MSB) bit of each SPI 8-bit data field from SPI instruction n1 hex, where "n" is the channel number 1-8 hex.

If a channel Control Register CR2 bit equals "0," the corresponding receiver recognizes all label values as valid, as shown in Table 3.

READING THE LABEL MEMORY

The contents of each channel's Label Memory may be read via the SPI interface using instruction n2 hex where "n" equals the channel number 1-8 hex, as described in Table 1.

SELF TEST

The HI-3598 and HI-3599 contain an on-chip ARINC 429 format self-test register which may be used to execute user-defined self-test sequences for each receiver. A 32-bit test word is loaded to the Test Register using SPI instructions n8 hex (for ARINC 429 high-speed data rate) or n9 hex (for ARINC 429 low speed). Upon completion of the instruction, the word is shifted out of the register and routed to all receivers. The serial test word may be observed at the HI-3598's TX1 and TX0 pins, as shown in Table 4. Each channel will respond to the test word if self-test mode is enabled for that channel (Control Register CR5 bit equals "0") and the receive channel is set to the correct speed. If a channel's CR5 bit equals "1" the channel ignores the self-test word and continues to respond to the external ARINC 429 bus.

The first bit shifted into the Self Test register will be the first bit sent to the receivers and the TX1 and TX0 pins. In ARINC 429 protocol, this bit is the LSB. Therefore the Self Test word is unique in that it is loaded LSB first with respect to the ARINC word.

Table 4. Test Outputs

TX1	TX0	ARINC 429 State
0	0	NULL
1	0	ONE
0	1	ZERO

TRANSMIT FUNCTION

The self test register can be used as a transmitter by connecting the TX1 and TX0 pins to an external ARINC 429 line driver (such as the HI-8570 or HI-8571).

LINE RECEIVER INPUT PINS

The HI-3598 has two sets of Line Receiver input pins, RINA/B and RINA/B-40. Only one pair may be used to connect to the ARINC 429 bus. THE RINA/B pins may be connected directly to the ARINC 429 bus. The RINA/B-40 pins require an external 40KOhm resistor to be added in series with each ARINC input without affecting the ARINC input thresholds. This option is especially useful in applications where lightning protection circuitry is also required.

When using the RINA/B-40 pins, each side of the ARINC bus must be connected through a 40K ohm series resistor in order for the chip to detect the correct ARINC levels. The typical 10 volt differential signal is translated and input to a window comparator and latch. The comparator levels are set so that with the external 40K ohm resistors, they are just below the standard 6.5 volt minimum ARINC data threshold and just above the standard 2.5 volt maximum ARINC null threshold.

When using the reduced pin-count HI-3599 option of this product, only one set of ARINC 429 receive inputs are provided for each channel. The standard HI-3599 device uses the direct-connection RINA / RINB pins. The HI-3599-40 device uses the RINA-40 / RINB-40 pins and requires external 40K ohm series resistors. See the ordering information table for complete part number options.

Please refer to the Holt AN-300 Application Note for additional information and recommendations on lightning protection of Holt line drivers and line receivers.

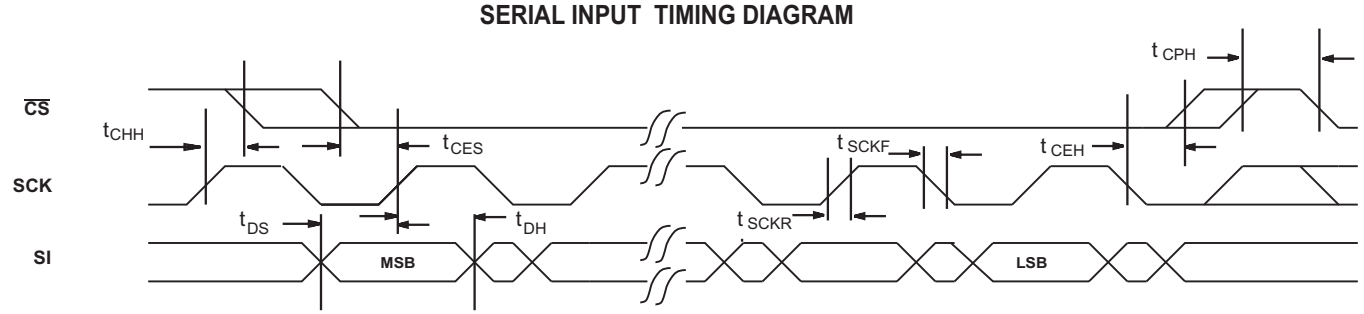
MASTER RESET (MR)

Assertion of Master Reset (MR) causes immediate termination of data reception. The eight Receive FIFOs are cleared. Status Register FIFO flags and FIFO status output signals are also cleared. Master Reset does not affect the eight channel Control Registers. Master Reset may be asserted using the MR input pin (HI-3598 only) or by executing SPI instruction n7 hex.

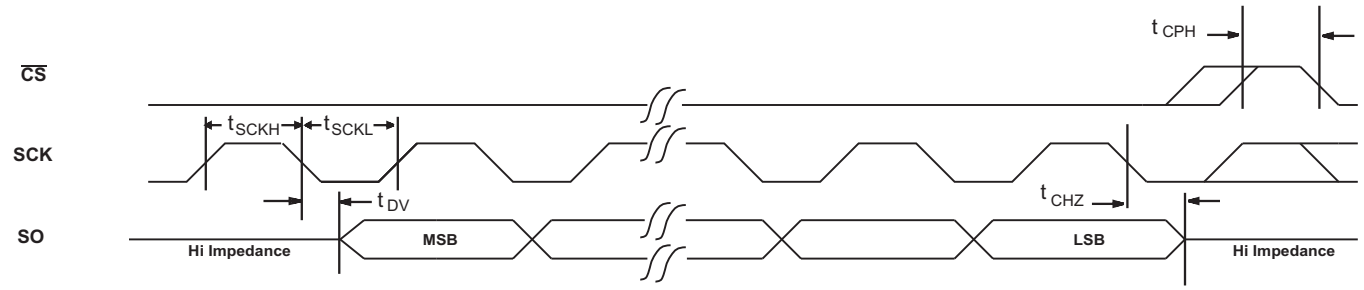
An individual receive channel can be reset by setting its corresponding Control Register CR3 bit to "1". This clears the channel's receiver logic and Receive FIFO and disables the receiver until CR3 is reset to "0". For applications requiring less than eight channels, unused receivers should be held in reset by setting the corresponding Control Register CR3 bits.

TIMING DIAGRAMS

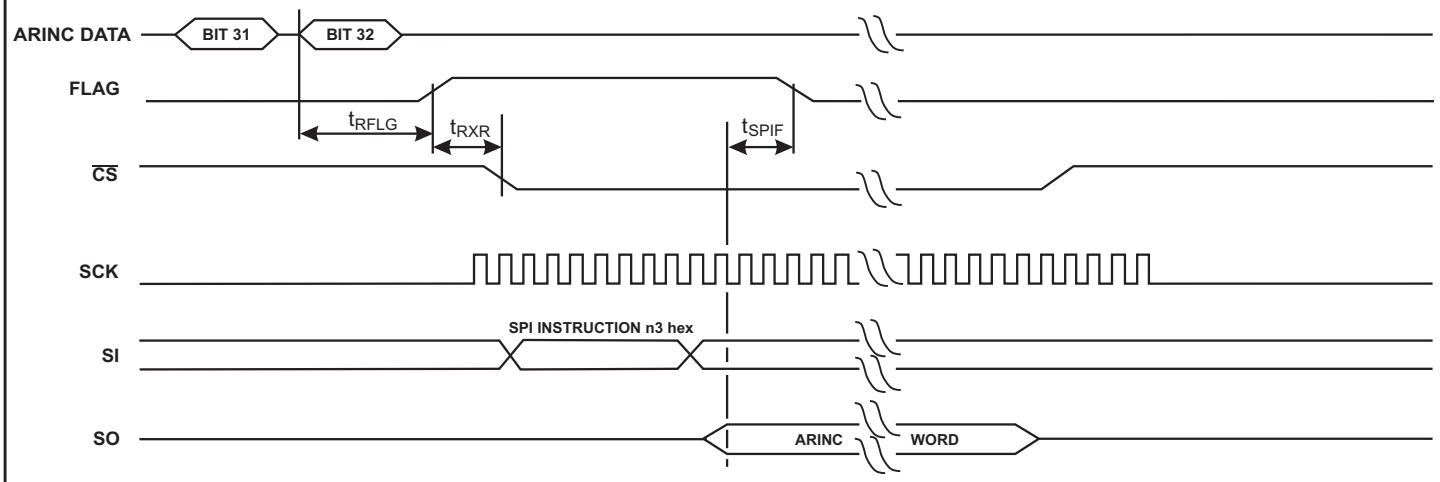
SERIAL INPUT TIMING DIAGRAM



SERIAL OUTPUT TIMING DIAGRAM



RECEIVER OPERATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltages V_{DD} ..... -0.3V to +7.0V	Power Dissipation at 25°C Plastic Quad Flat Pack .....1.5 W, derate 10mW/°C
Voltage at pins RIN1A, RIN1B, RIN2A, RIN2B ..... -29V to +29V	DC Current Drain per pin ..... ±10mA
Voltage at any other pin ..... -0.3V to V_{DD} +0.3V	Storage Temperature Range ..... -65°C to +150°C
Solder temperature (Leads) ..... 280°C for 10 seconds (Package) ..... 220°C	Operating Temperature Range (Industrial): .... -40°C to +85°C (Extended Temp.): .....-55°C to +125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3V or 5.0V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER		SYMBOL	CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
ARINC INPUTS - Pins RINA, RINB, RINA-40 (with external 40KOhms), RINB-40 (with external 40KOhms)							
Differential Input Voltage: (RIN1A to RIN1B, RIN2A to RIN2B, etc.)	ONE ZERO NULL	V_{IH} V_{IL} V_{NUL}	Common mode voltages less than ±30V with respect to GND	6.5 -13.0 -2.5	10.0 -10.0 0	13.0 -6.5 2.5	V V V
Input Resistance:	Differential To GND To V_{DD}	R_I R_G R_H		- - -	140 140 100	- - -	KΩ KΩ KΩ
Input Current:	Input Sink Input Source	I_{IH} I_{IL}		 -450		200	µA µA
Input Capacitance: (Guaranteed but not tested)	Differential To GND To V_{DD}	C_I C_G C_H	(RINA to RINB)			20 20 20	pF pF pF
LOGIC INPUTS							
Input Voltage:	Input Voltage HI Input Voltage LO	V_{IH} V_{IL}		70% VDD		 30% VDD	V V
Input Current:	Input Sink Input Source Pull-Down Current (MR, SI, SCK, ACLK pins) Pull-Up Current ($\overline{CS}$ pin)	I_{IH} I_{IL} I_{PD} I_{PU}		 -1.5 250 -600		1.5 600 -250	µA µA µA µA
LOGIC OUTPUTS							
Output Voltage:	Logic "1" Output Voltage Logic "0" Output Voltage	V_{OH} V_{OL}	I_{OH} = -100µA I_{OL} = 1.0mA	90%VDD		 10% VDD	V V
Output Current: (All Outputs & Bi-directional Pins)	Output Sink Output Source	I_{OL} I_{OH}	V_{OUT} = 0.4V V_{OUT} = V_{DD} - 0.4V	1.6		 -1.0	mA mA
Output Capacitance:		C_O			15		pF
Operating Voltage Range							
		V_{DD}		3.15		5.25	V
Operating Supply Current							
VDD		I_{DD}			2.5	7	mA

AC ELECTRICAL CHARACTERISTICS

VDD = 3.3V or 5.0V, GND = 0V, TA = Operating Temperature Range and fclk=1MHz ±0.1% with 60/40 duty cycle

PARAMETER	SYMBOL	LIMITS			UNITS
		MIN	TYP	MAX	
SPI INTERFACE TIMING					
SCK clock Period	t_{CYC}	130			ns
$\overline{CS}$ active after last SCK rising edge	t_{CHH}	25			ns
$\overline{CS}$ setup time to first SCK rising edge	t_{CES}	10			ns
$\overline{CS}$ hold time after last SCK falling edge	t_{CEH}	10			ns
$\overline{CS}$ inactive between SPI instructions	t_{CPH}	30			ns
SPI SI Data set-up time to SCK rising edge	t_{DS}	10			ns
SPI SI Data hold time after SCK rising edge	t_{DH}	30			ns
SCK rise time	t_{SCKR}			10	ns
SCK fall ime	t_{SCKF}			10	ns
SCK high time	t_{SCKH}	45			ns
SCK low time	t_{SCKL}	25			ns
SO valid after SCK falling edge	t_{DV}			65	ns
SO high-impedance after SCK falling edge	t_{CHZ}			65	ns
RECEIVER TIMING					
Delay - Last bit of received ARINC word to FLAG(Full or Empty) - Hi Speed	t_{RFLG}			16	µs
Delay - Last bit of received ARINC word to FLAG(Full or Empty) - Lo Speed	t_{RFLG}			126	µs
Received data available to SPI interface. FLAG to $\overline{CS}$ active	t_{RXR}	0			ns
SPI receiver read	t_{SPIF}			85	ns

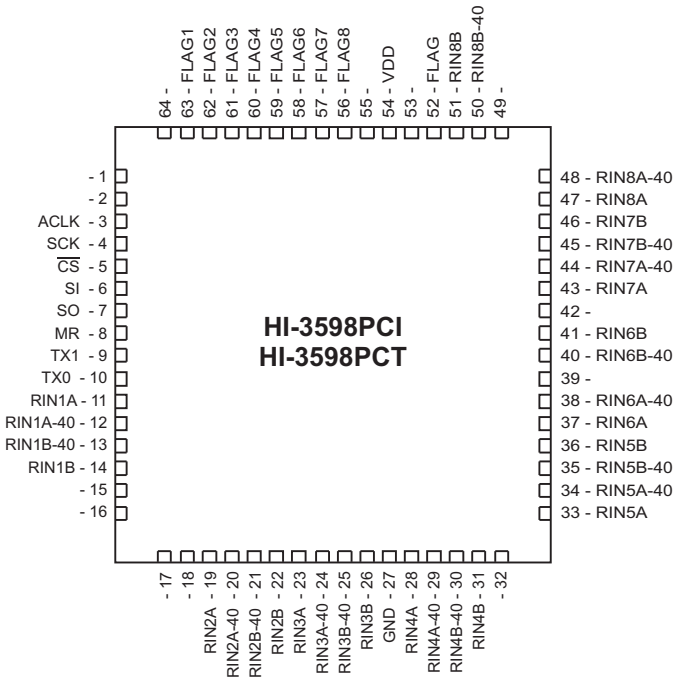
HEAT SINK - CHIP-SCALE PACKAGE ONLY

The HI-3598PCI, HI-3598PCT, HI-3599PCI and HI3599PCT use 44-pin or 64-pin plastic chip-scale packages. These packages have a metal heat sink pad on the bottom surface that is electrically connected to the die. For these receivers, small size is the primary advantage of this package style. Heat sinking provides little benefit because power dissipation is low. If connected, the bottom heat sink pad should be connected to VDD.

Do not connect heat sink pad to GND.

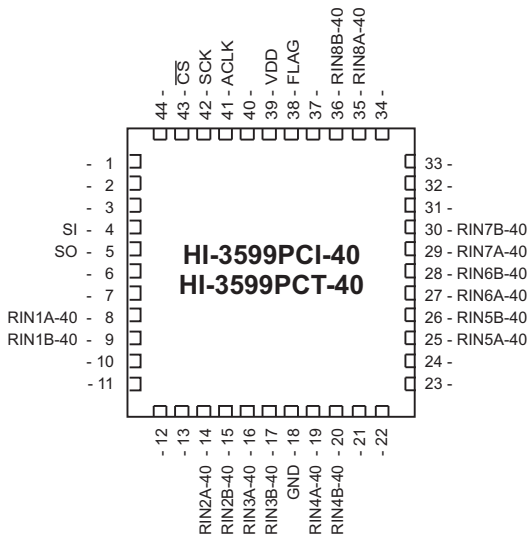
ADDITIONAL PIN / PACKAGE CONFIGURATIONS

HI-3598PCx



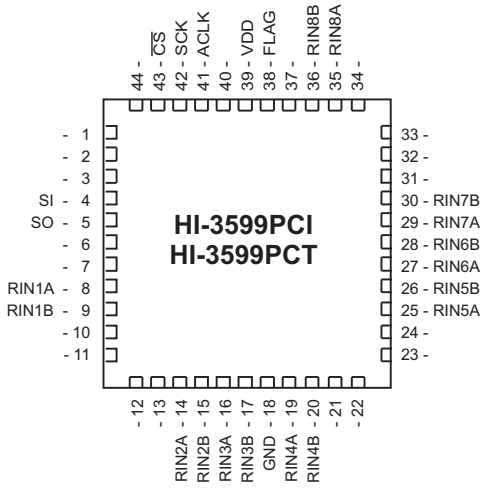
64 - Pin Plastic 9mm x 9mm Chip-Scale Package (QFN)

HI-3599PCx-40



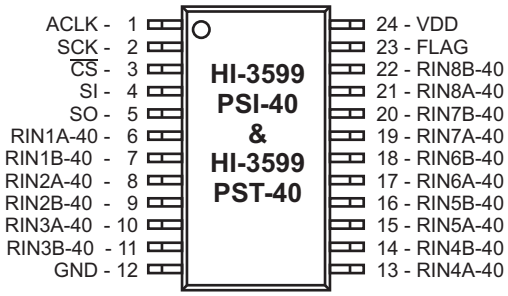
44 - Pin Plastic 7mm x 7mm Chip-Scale Package (QFN)

HI-3599PCx



44 - Pin Plastic 7mm x 7mm Chip-Scale Package (QFN)

HI-3599PSx-40



24 - Pin Plastic Small Outilne Package (SOIC)

ORDERING INFORMATION (HI-3598 all pins)

HI - 3598 xx x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION
PC	64 PIN PLASTIC CHIP-SCALE PKG, QFN (64PCS)
PQ	52 PIN PLASTIC QUAD FLAT PACK, PQFP (52PTQS)

ORDERING INFORMATION (HI-3599 Minimum pin-count version)

HI - 3599 xx x x - xx

PART NUMBER	INPUT RESISTANCE
Blank	140 KOhm. Direct connection to ARINC 429 bus
-40	100 KOhm.Requires external 40 KOhm resistors

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION
PC	44 PIN PLASTIC CHIP-SCALE PKG, QFN (44PCS)
PS	24 PIN PLASTIC WIDE SOIC (24HW)

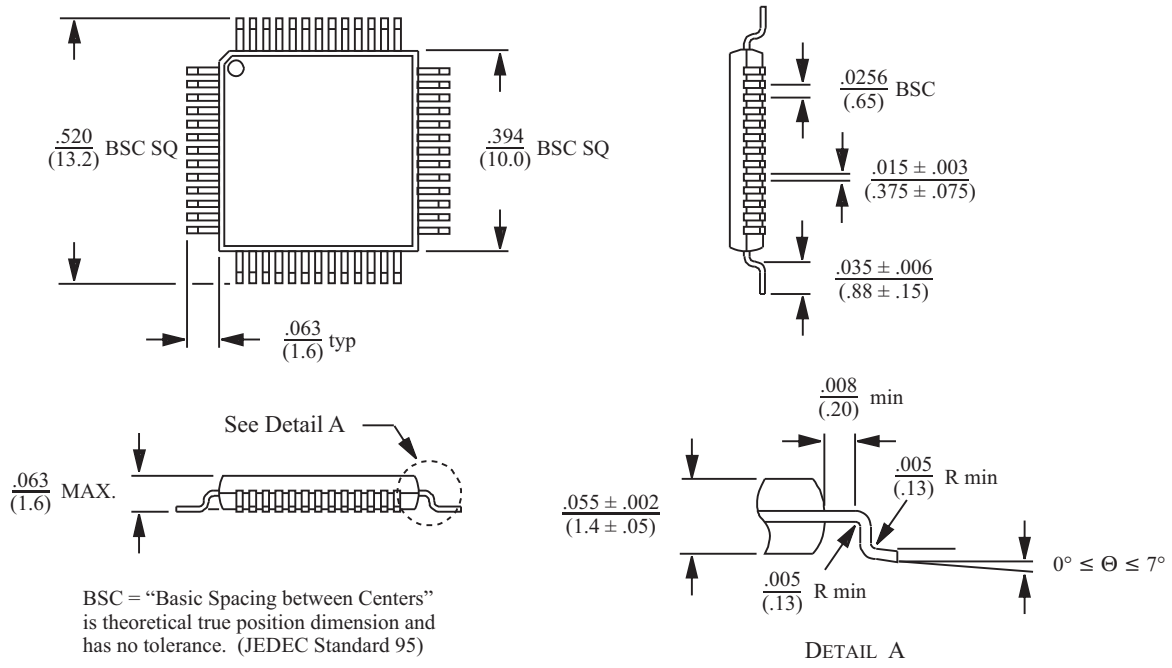
REVISION HISTORY

Revision	Date	Page	Description of Change
DS3598, Rev. NEW	06/12/08	All	Initial Release

52-PIN PLASTIC QUAD FLAT PACK (PQFP)

inches (millimeters)

Package Type: 52PTQS



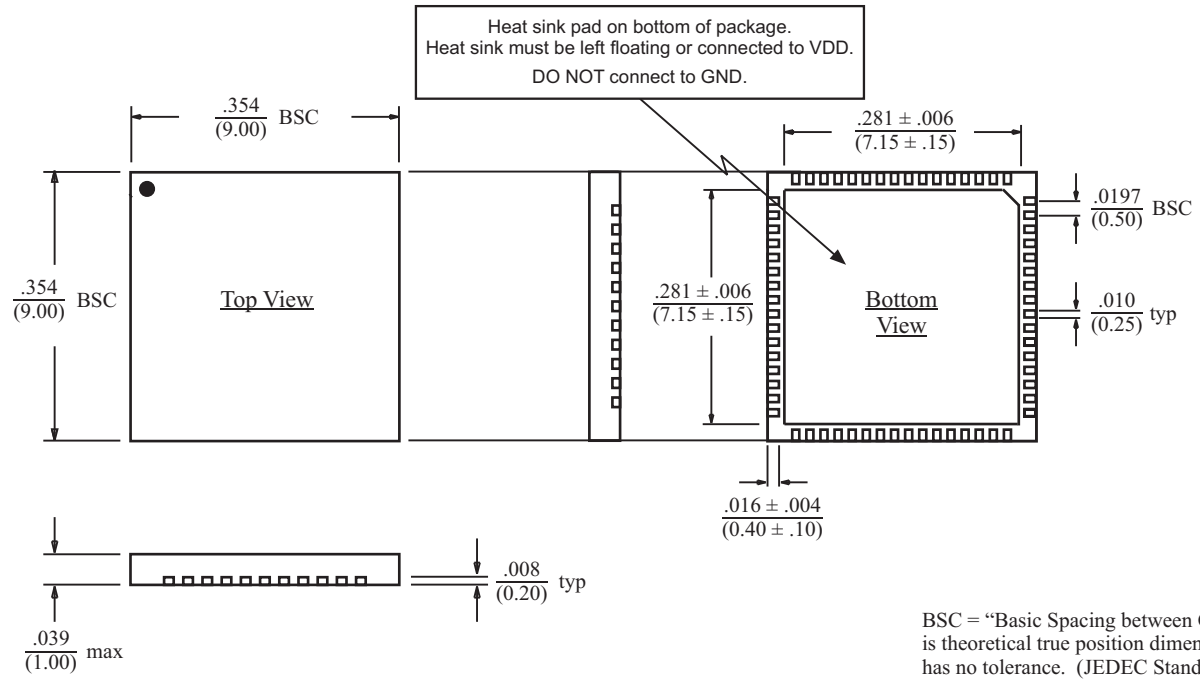
BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

DETAIL A

64-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

inches (millimeters)

Package Type: 64PCS

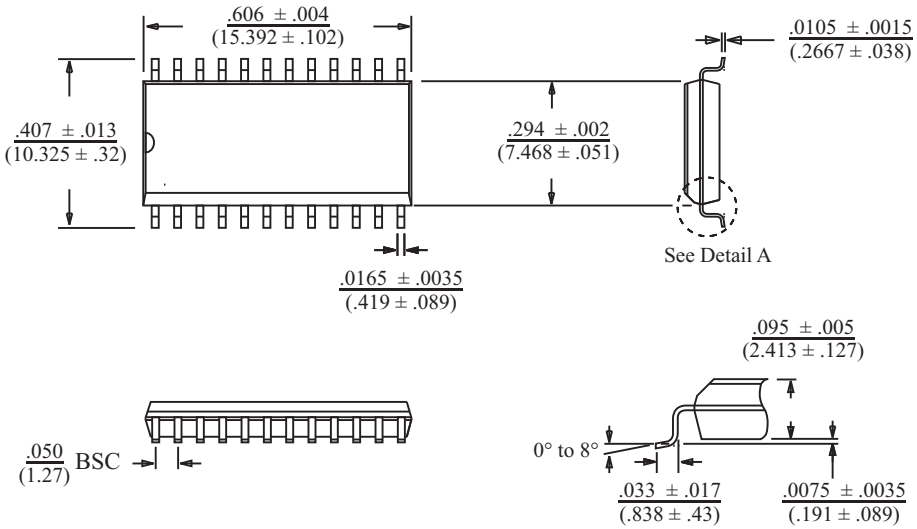


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

24-PIN PLASTIC SMALL OUTLINE (SOIC) - WB
(Wide Body)

inches (millimeters)

Package Type: 24HW



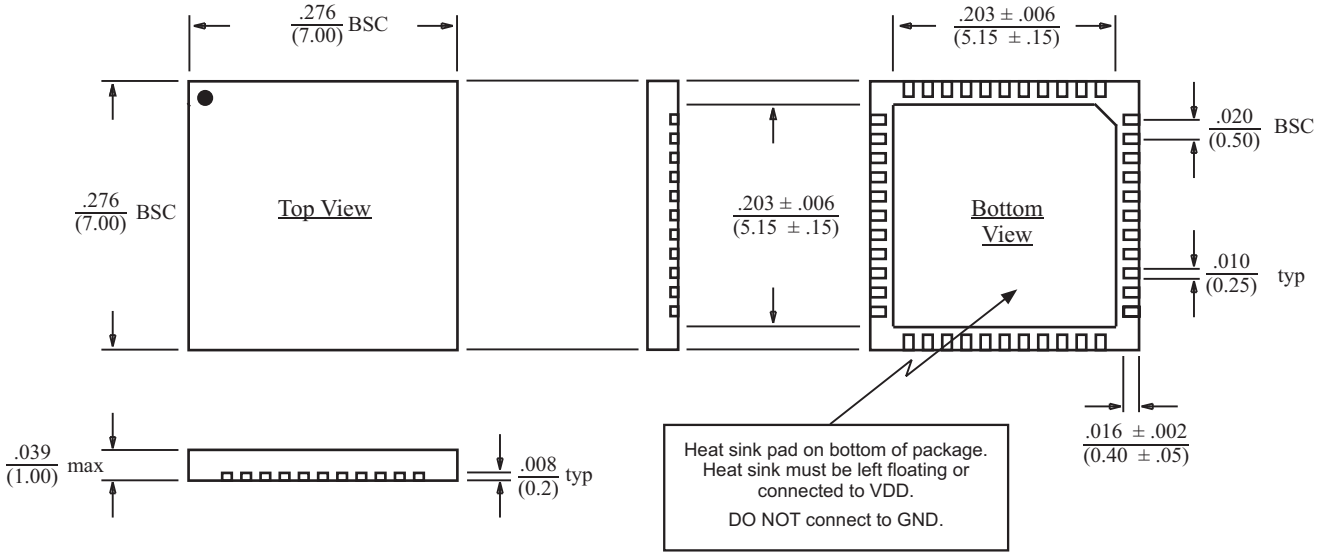
Detail A

BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

inches (millimeters)

Package Type: 44PCS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)