HOLT INTEGRATED CIRCUITS INC.

# HI-3587

## ARINC 429 Transmitter with SPI Interface

June 2008

## GENERAL DESCRIPTION

The HI-3587 from Holt Integrated Circuits is a silicon gate CMOS device for interfacing a Serial Peripheral Interface (SPI) enabled microcontroller to an ARINC 429 serial bus. The device provides one ARINC 429 transmitter with 32 X 32 Transmit FIFO and built-in line driver. Transmit FIFO status can be monitored using the programmable external interrupt pin, or by polling the HI-3587 Status Register. Other features include a programmable option of data or parity in the 32nd bit, and the ability to switch the bit-significance of ARINC 429 labels. Line driver output pins are available with different values of output resistance to provide flexibility when using external lightning protection circuitry.

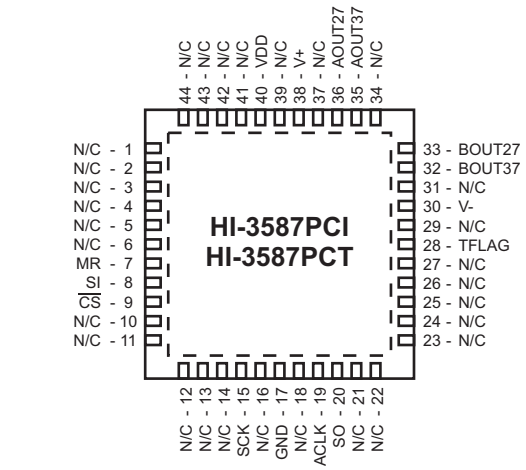
The Serial Peripheral Interface minimizes the number of host interface signals and provides a small footprint device that can be interfaced to a wide variety of industry-standard microcontrollers supporting SPI. Alternatively, the SPI signals may be controlled using four general purpose I/O port pins from a microcontroller or custom FPGA. The SPI and all control signals are CMOS and TTL compatible and support 3.3V or 5V operation.

The HI-3587 applies the ARINC 429 protocol to the transmitter. ARINC 429 databus timing comes from a 1 MHz clock input, or an internal counter can derive it from higher clock frequencies having certain fixed values, possibly the external host processor clock.

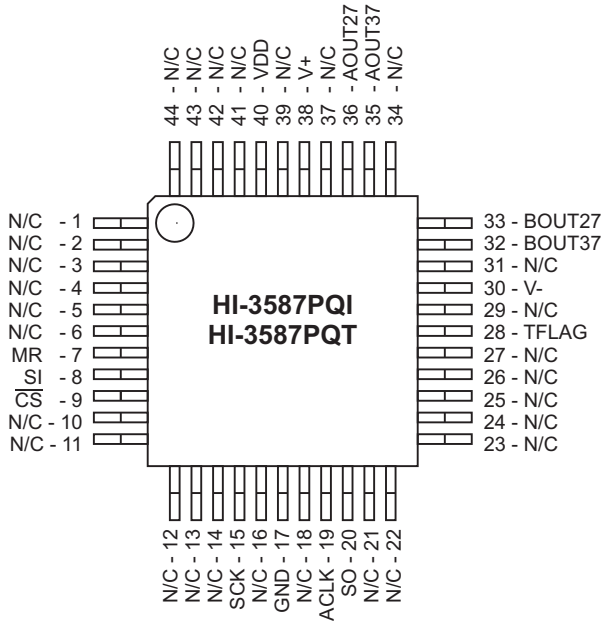
## FEATURES

- ARINC specification 429 compliant
- 3.3V or 5.0V logic supply operation
- On-chip analog line driver connects directly to ARINC 429 bus
- 32 x 32 Transmit Data FIFO
- Programmable data rate selection
- High-speed, four-wire Serial Peripheral Interface
- Label bit-order control
- 32nd transmit bit can be data or parity
- Low power
- Industrial & extended temperature ranges

## PIN CONFIGURATIONS (Top View)

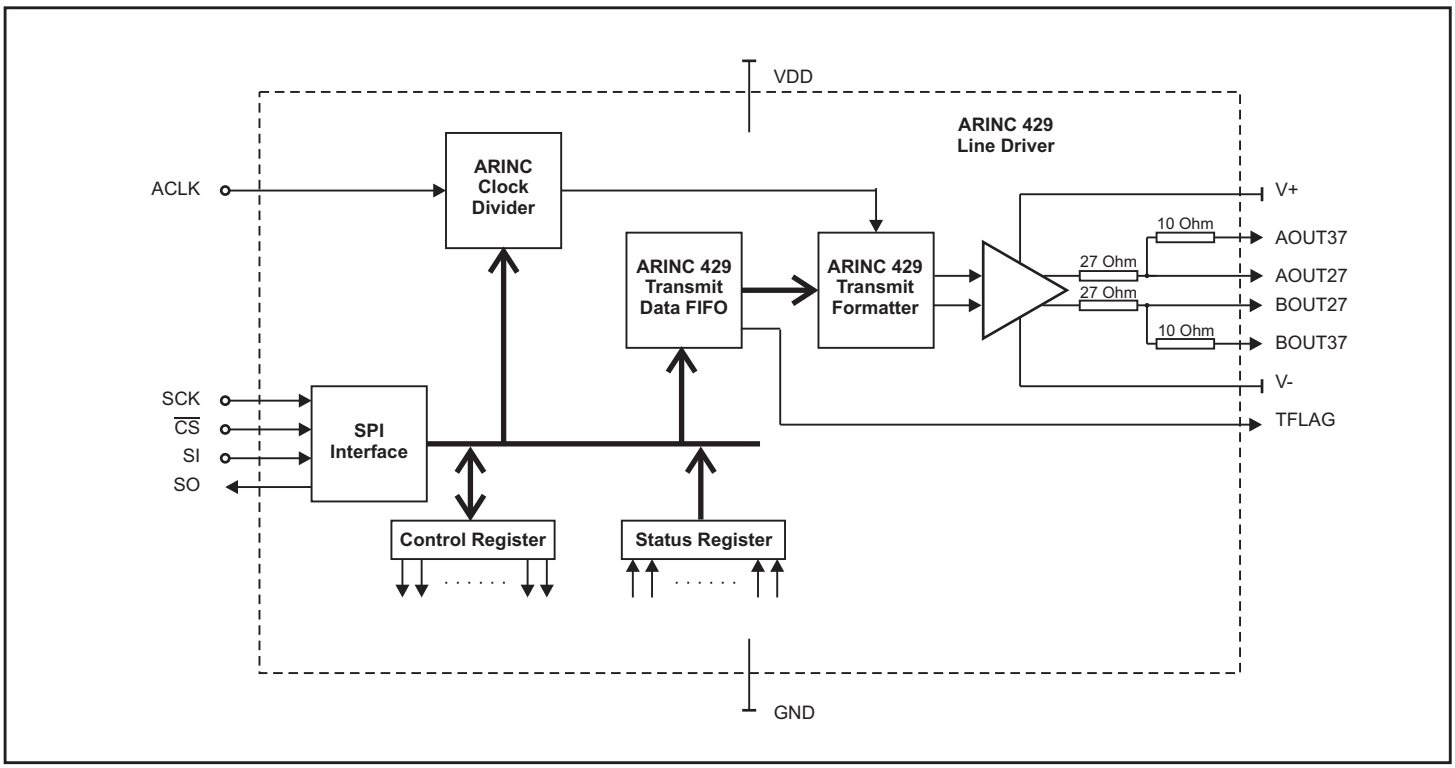



**44 - Pin Plastic 7mm x 7mm Chip-Scale Package (QFN)**




**44 - Pin Plastic Quad Flat Pack (PQFP)**

# BLOCK DIAGRAM




# PIN DESCRIPTIONS

| SIGNAL | FUNCTION | DESCRIPTION | PULL UP / DOWN |
|---|---|---|---|
| MR | INPUT | Master Reset. A positive pulse clears the Transmit data FIFO and flags | 10K ohm pull-down |
| SI | INPUT | SPI interface serial data input | 10K ohm pull-down |
| $\overline{CS}$ | INPUT | Chip select. Data is shifted into SI and out of SO when $\overline{CS}$ is low. | 10K ohm pull-up |
| SCK | INPUT | SPI Clock. Data is shifted into or out of the SPI interface using SCK | 10K ohm pull-down |
| GND | POWER | Chip 0V supply | |
| ACLK | INPUT | Master timing source for the ARINC 429 transmitter | 10K ohm pull-down |
| SO | OUTPUT | SPI interface serial data output | |
| TFLAG | OUTPUT | Goes high when ARINC 429 transmit FIFO is empty (CR14=0), or full (CR14=1) | |
| V- | POWER | Minus 5V power supply to ARINC 429 Line Driver | |
| BOUT37 | OUTPUT | ARINC line driver negative output. Direct connection to ARINC 429 bus | |
| BOUT27 | OUTPUT | Alternate ARINC line driver negative output. Requires external 10 ohm resistor | |
| AOUT27 | OUTPUT | Alternate ARINC line driver positive output. Requires external 10 ohm resistor | |
| AOUT37 | OUTPUT | ARINC line driver positive output. Direct connection to ARINC 429 bus | |
| V+ | POWER | Positive 5V power supply to ARINC 429 Line Driver | |
| VDD | POWER | 3.3V or 5.0V logic power | |

# INSTRUCTIONS

Instruction op codes are used to read, write and configure the HI-3587. When $\overline{CS}$ goes low, the next 8 clocks at the SCK pin shift an instruction op code into the decoder, starting with the first rising SCK edge. The op code is fed into the SI pin, most significant bit first.

For write instructions, the most significant bit of the data word must immediately follow the instruction op code and is clocked into its register on the next rising SCK edge. Data word length varies depending on word type written: 16-bit writes to Control Register or 32-bit ARINC word writes to transmit FIFO.

For read instructions, the most significant bit of the requested data word appears at the SO pin after the last op code bit is clocked into the decoder, at the next falling SCK edge. As in write instructions, read instruction data field bit-length varies with read instruction type.

Table 1 lists all instructions. Instructions that perform a reset or set, or enable transmission are executed after the last SI bit is received while $\overline{CS}$ is still low.

Example:

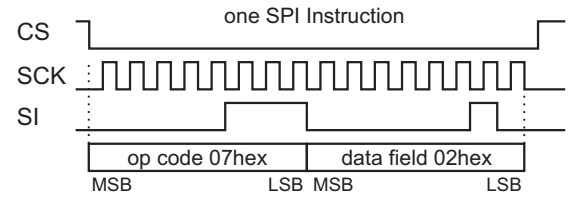



**TABLE 1. DEFINED INSTRUCTION OP CODES**

| OP CODE Hex | DATA FIELD | DESCRIPTION |
|---|---|---|
| 00 | None | No instruction implemented |
| 01 | None | After the 8th op-code bit is received, perform Master Reset (MR) |
| 02 | None | No instruction implemented |
| 03 | None | No instruction implemented |
| 04 | None | No instruction implemented |
| 05 | None | No instruction implemented |
| 06 | None | No instruction implemented |
| 07 | 8 bits | Programs a division of the ACLK input. If the divided ACLK frequency is 1 MHz and Control Register bit CR1 is set, the ARINC transmitter operates from the divided ACLK clock. Allowable values for division rate are X1, X2, X4, X8, or XA hex. Any other programmed value results in no clock. Note: ACLK input frequency and division ratio must result in 1 MHz clock." |
| 08 | [Note 1] | Reserved [Note 1] |
| 09 | [Note 1] | Reserved [Note 1] |
| 0A | 8 bits | Read the Status Register |
| 0B | 16 bits | Read the Control Register |
| 0C | 8 bits | Read the ACLK divide value programmed previously using op code 07 hex |
| 0D | [Note 1] | Reserved [Note 1] |
| 0E | N x 32 Bits | Write up to 32 words into the next empty position of the Transmitter FIFO |
| 0F | None | No instruction implemented |
| 10 | 16 bits | Write the Control Register |
| 11 | None | Reset the Transmitter FIFO. After the 8th op-code bit is received, the Xmit FIFO will be empty |
| 12 | None | Transmission enabled by this instruction only if Control Register bit 13 is zero |

Note 1: This instruction is reserved for factory test only. If executed, up to 1,024 data bits may be output from the SO pin.

# FUNCTIONAL DESCRIPTION

## CONTROL WORD REGISTER

The HI-3587 has a 16-bit Control Register which configures the device. Control Register bits CR15 - CR0 are loaded from a 16-bit data value appended to SPI instruction 10 hex. The Control Register contents may be read using SPI instruction 0B hex. Each bit of the Control Register has the following function:

| CR Bit | FUNCTION | STATE | DESCRIPTION |
|---|---|---|---|
| CR0 (LSB) | - | X | Not used |
| CR1 | ARINC Clock Source Select | 0 | ARINC CLK = ACLK input frequency |
| | | 1 | ARINC CLK = ACLK divided by the value programmed with SPI Instruction 07 hex |
| CR2 | - | X | Not used |
| CR3 | Transmitter Parity Bit Enable | 0 | Transmitter 32nd bit is data |
| | | 1 | Transmitter 32nd bit is parity |
| CR4 | - | X | Not used |
| CR5 | - | X | Not used |
| CR6 | - | X | Not used |
| CR7 | - | X | Not used |
| CR8 | - | X | Not used |
| CR9 | Transmitter Parity Select | 0 | Transmitter 32nd bit is Odd parity |
| | | 1 | Transmitter 32nd bit is Even parity |
| CR10 | Transmitter Data Rate | 0 | Data rate=CLK/10, O/P slope=1.5u |
| | | 1 | Data rate=CLK/80, O/P slope=10us |
| CR11 | ARINC Label Bit Order | 0 | Label bit order reversed (See Table 2) |
| | | 1 | Label bit order same as transmitted (See Table 2) |
| CR12 | Disable Line Driver | 0 | Line Driver enabled |
| | | 1 | Line Driver disabled (force outputs to Null state) |
| CR13 | Transmission Enable Mode | 0 | Start transmission by SPI instruction12h |
| | | 1 | Transmit whenever data is available in the Transmit FIFO |
| Cr14 | TFLAG Definition | 0 | TFLAG goes high when transmit FIFO is empty |
| | | 1 | TFLAG goes high when transmit FIFO is full |
| CR15 (MSB) | - | X | Not used |

## STATUS REGISTER

The HI-3587 contains an 8-bit Status Register which can be interrogated to determine status of the ARINC Transmit FIFO. The Status Register is read using SPI instruction 0A hex. Unused bits are undefined and may be read as either “1” or “0”. The following table defines the Status Register bits.

| SR Bit | FUNCTION | STATE | DESCRIPTION |
|---|---|---|---|
| SR0 (LSB) | Not used | X | Undefined |
| SR1 | Not used | X | Undefined |
| SR2 | Not used | X | Undefined |
| SR3 | Transmit FIFO Empty | 0 | Transmit FIFO not empty. Sets to One when all data has been sent. TFLAG pin reflects the state of this bit when CR14=0 |
| | | 1 | Transmit FIFO is empty. |
| SR4 | Transmit FIFO Half Full | 0 | Transmit FIFO contains less than 16 words |
| | | 1 | Transmit FIFO contains at least 16 words |
| SR5 | Transmit FIFO Full | 0 | Transmit FIFO not full. TFLAG pin reflects the state of this bit when CR14=1 |
| | | 1 | Transmit FIFO full. |
| SR6 | Not used | 0 | Always 0 |
| SR7 (MSB) | Not used | 0 | Always 0 |

# FUNCTIONAL DESCRIPTION (cont.)

## ARINC 429 DATA FORMAT

Control Register bit CR11 controls how individual bits in the transmitted ARINC word are mapped to the HI-3587 SPI data word bits during data read or write operations. The following table describes this mapping:

**Table 2. SPI / ARINC bit-mapping**

| SPI bit | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 - 31 | 32 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ARINC bit CR11=0 | 8 Label (LSB) | 7 Label | 6 Label | 5 Label | 4 Label | 3 Label | 2 Label | 1 Label (MSB) | 9 SDI | 10 SDI | 11 - 31 Data | 32 Parity |
| ARINC bit CR11=1 | 1 Label (MSB) | 2 Label | 3 Label | 4 Label | 5 Label | 6 Label | 7 Label | 8 Label (LSB) | 9 SDI | 10 SDI | 11 - 31 Data | 32 Parity |

## TRANSMITTER

### FIFO OPERATION

The Transmit FIFO is loaded with ARINC 429 words awaiting transmission. SPI op code 0E hex writes up to 32 ARINC words into the FIFO, starting at the next available FIFO location. If Status Register bit SR3 equals "1" (FIFO empty), then up to 32 words (32 bits each) may be loaded. If Status Register bit SR3 equals "0" then only the available positions may be loaded. If all 32 positions are full, Status Register bit SR5 is asserted. Further attempts to load the Transmit FIFO are ignored until at least one ARINC word is transmitted.

The Transmit FIFO half-full flag (Status Register bit SR4) equals "0" when the Transmit FIFO contains less than 16 words. When SR4 equals "0", the system microprocessor can safely initiate a 16-word ARINC block-write sequence.

In normal operation (Control Register bit CR3 = "1"), the 32nd bit transmitted is a word parity bit. Odd or even parity is selected by programming Control Register bit CR9 to a "0" or "1" respectively. If Control Register bit CR3 equals "0", all 32 bits loaded into the Transmit FIFO are treated as data and are transmitted.

SPI op code 11 hex asynchronously clears all data in the Transmit FIFO.

### DATA TRANSMISSION

If Control Register bit CR13 equals "1", ARINC 429 data is transmitted immediately following the $\overline{CS}$ rising edge of the SPI instruction that loaded data into the Transmit FIFO. Loading Control Register bit CR13 to "0" allows the software to control transmission timing; each time a 12 hex SPI op code is executed, all loaded Transmit FIFO words are transmitted. If new words are loaded into the Transmit FIFO before transmission stops, the new words will also be output. Once the Transmit FIFO is empty and transmission of the last word is complete, the FIFO can be loaded with new data which is held until the next SPI 12 hex instruction is executed. Once transmission is enabled, the FIFO positions are incremented with the top register loading into the data transmission shift register. Within 2.5 data clocks the first data bit appears at AOUT and BOUT. The 31 or 32 bits in the data transmission shift register are presented sequentially to the outputs in the ARINC 429 format with the following timing:

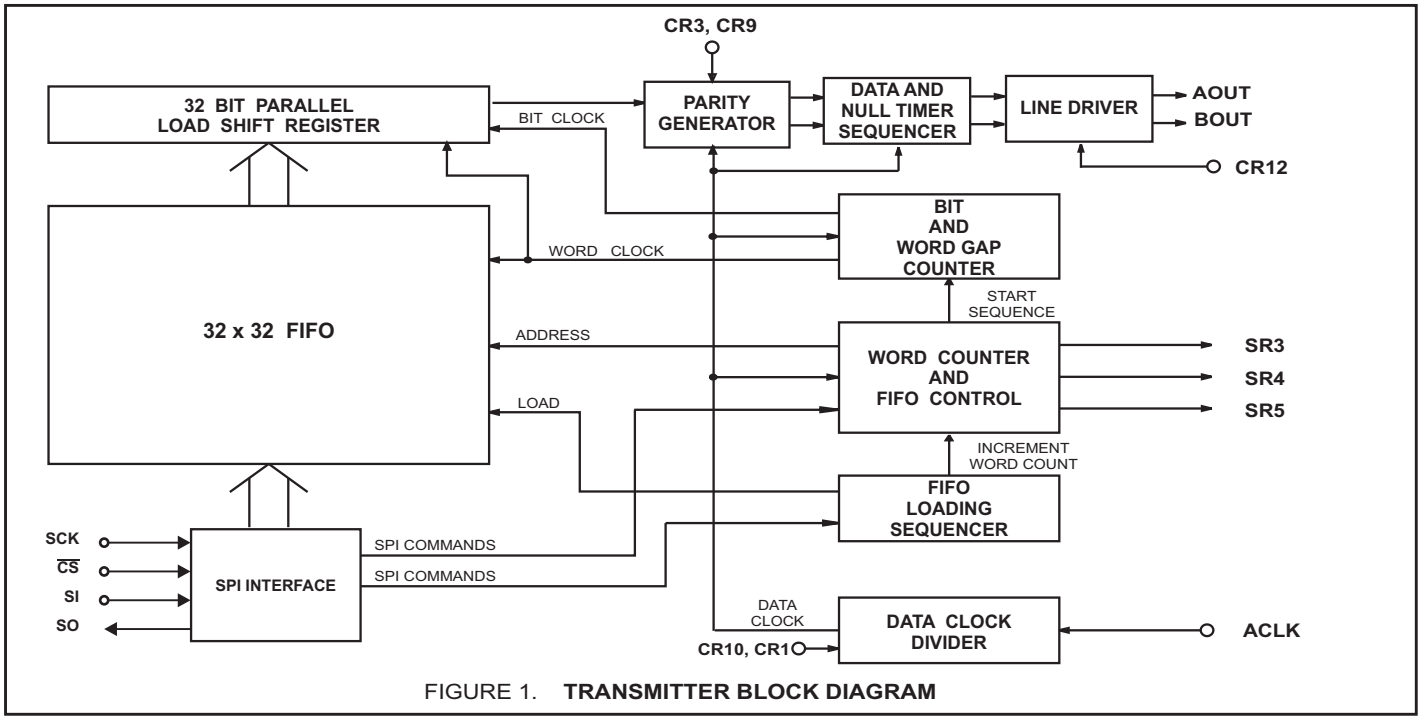



FIGURE 1. **TRANSMITTER BLOCK DIAGRAM**

# FUNCTIONAL DESCRIPTION (cont.)

| | HIGH SPEED | LOW SPEED |
|---|---|---|
| ARINC DATA BIT TIME | 10 Clocks | 80 Clocks |
| DATA BIT TIME | 5 Clocks | 40 Clocks |
| NULL BIT TIME | 5 Clocks | 40 Clocks |
| WORD GAP TIME | 40 Clocks | 320 Clocks |

The word counter detects when all loaded positions have been transmitted and sets the Status Register transmitter ready flag, SR3, high.

### TRANSMITTER PARITY

The parity generator counts the Ones in the 31-bit word. If control register bit CR9 is set to a "0", the 32nd bit transmitted will make parity odd. If the control bit is a "1", the parity is even. Setting CR3 to "0" bypasses the parity generator, and allows 32 bits of data to be transmitted.

### LINE DRIVER OPERATION

The line driver in the HI-3587 directly drives the ARINC 429 bus. The two ARINC outputs (AOUT37 and BOUT37) provide a differential voltage to produce a +10V One, a -10V Zero, and a 0 Volt Null. Control Register bit CR10 controls both the transmitter data rate and the slope of the differential output signal. No additional hardware is required to control the slope.

Transmit timing is derived from a 1MHz reference clock. Control register bit CR1 determines the reference clock source. If CR1 equals "0," a 50% duty cycle 1MHz clock should be applied to the ACLK input pin. If CR1 equals "1," the SPI clock SCK is used as the reference. SPI op code 07 hex is used to provide the HI-3587 with the correct division ratio to generate a 1 MHz reference from SCK.

Loading Control Register bit CR10 to "0" causes a 100 Kbit/s data rate and a slope of 1.5 µs on the ARINC outputs. Loading CR10 to "1" causes a 12.5 Kbit/s data rate and a slope of 10 µs. Timing is set by an on-chip resistor and capacitor and tested to be within ARINC 429 requirements.

### LINE DRIVER OUTPUT PINS

The HI-3587 AOUT37 and BOUT37 pins have 37.5 Ohms in series with each line driver output, and may be directly connected to an ARINC 429 bus. The alternate AOUT27 and BOUT27 pins have 27 ohms of internal series resistance and require external 10 ohm resistors at each pin. AOUT27 and BOUT27 are for applications where external series resistance is applied, usually for lightning protection.

### POWER SUPPLY SEQUENCING

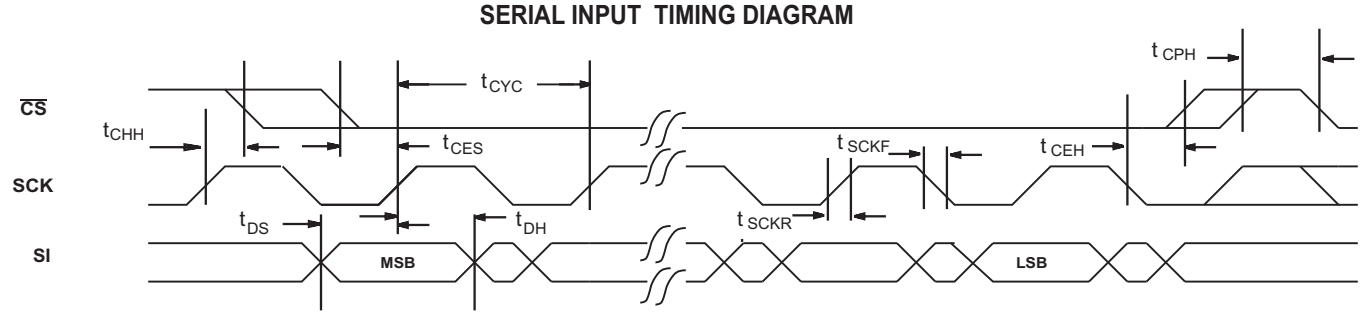
Power supply sequencing should be controlled to prevent large currents during supply turn-on and turn-off. The recommended sequence is V+ followed by $V_{DD}$, always ensuring that V+ is the most positive supply. The V- supply is not critical and can be applied at any time.

### MASTER RESET (MR)

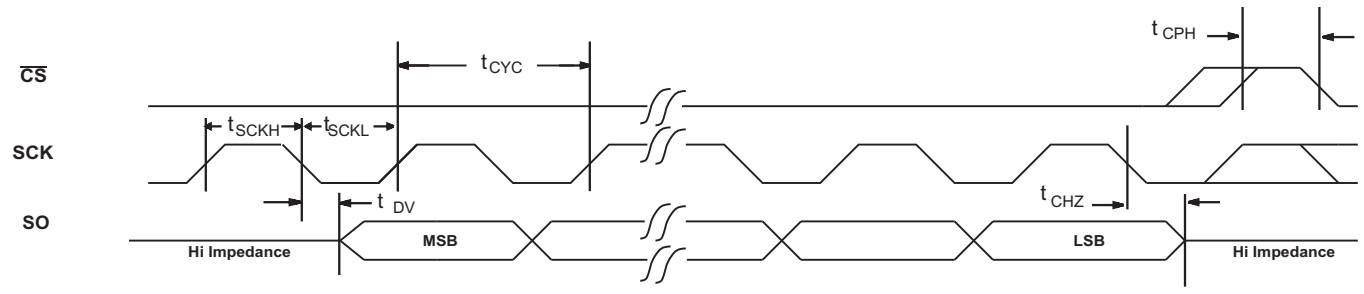
Application of a Master Reset causes immediate termination of data transmission. The transmit FIFO is cleared. Status Register FIFO flags and FIFO status output signal TFLAG is also cleared. The Control Register is not affected by a Master Reset.

# TIMING DIAGRAMS

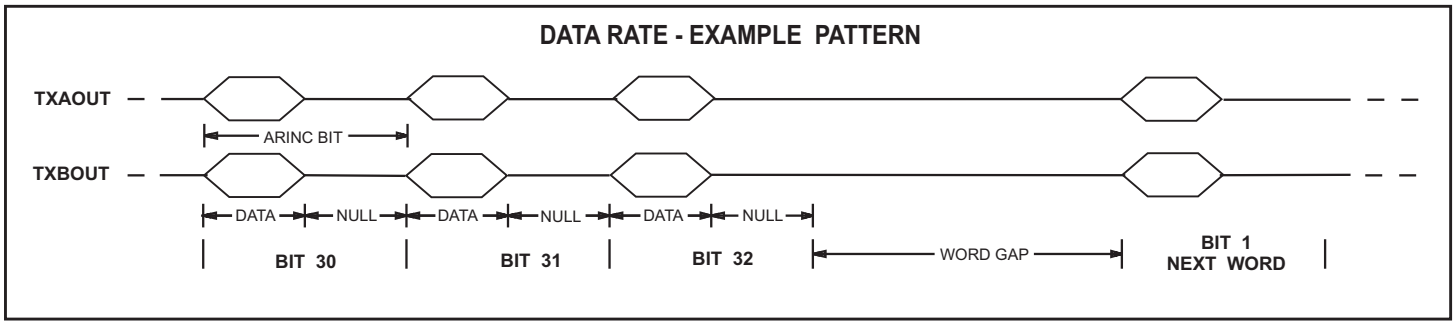
**SERIAL INPUT TIMING DIAGRAM**

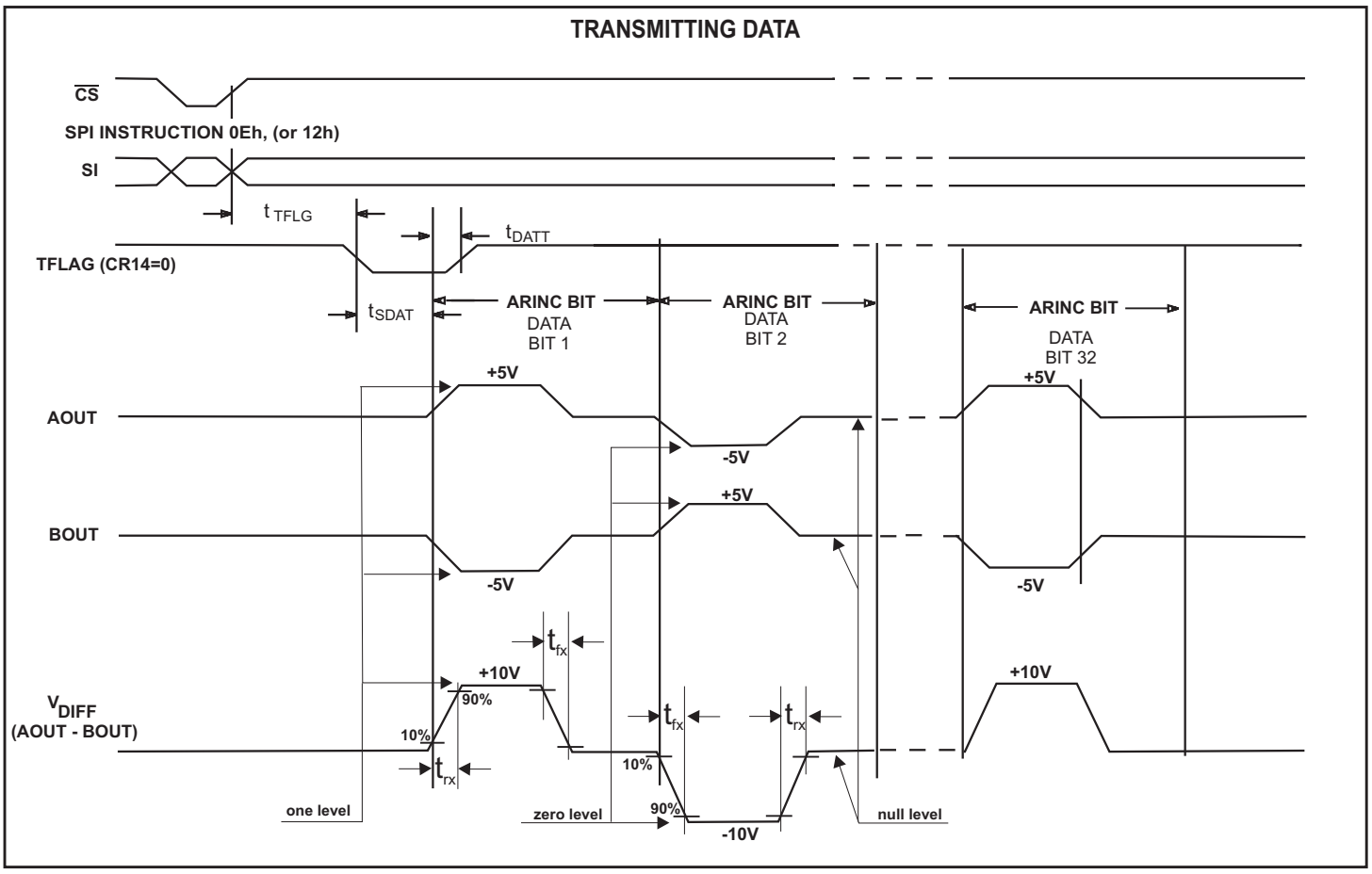



**SERIAL OUTPUT TIMING DIAGRAM**



# TIMING DIAGRAMS (Cont.)




## HEAT SINK - CHIP-SCALE PACKAGE ONLY

The HI-3587PCI and HI-3587PCT use a 44-pin plastic chip-scale package. This package has a metal heat sink pad on its bottom surface. This heat sink is electrically connected to the die. To enhance thermal dissipation, the heat sink can be soldered to matching circuit board pad. The heat sink may be connected to V+ or left floating.

Do not connect heat sink pad to VDD, GND or V-.

# ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltages $V_{DD}$ ..... -0.3V to +7.0V<br>V+ ..... +7.0V<br>V- ..... -7.0V | Power Dissipation at 25°C<br>Plastic Quad Flat Pack .....1.5 W, derate 10mW/°C |
| Voltage at any logic pin .....-0.3V to $V_{DD}$ +0.3V | Storage Temperature Range ..... -65°C to +150°C |
| DC Current Drain per pin ..... ±10mA | Operating Temperature Range (Industrial): .... -40°C to +85°C<br>(Hi-Temp): .....-55°C to +125°C |
| Solder temperature (Leads) ..... 280°C for 10 seconds<br>(Package) ..... 220°C | |

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# DC ELECTRICAL CHARACTERISTICS

$V_{DD}$ = 3.3V or 5.0V , V+ = +5V, V- = -5V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

| PARAMETER | SYMBOL | CONDITIONS | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNIT |
|---|---|---|---|---|---|---|
| **LOGIC INPUTS** | | | | | | |
| Input Voltage: Input Voltage HI | $V_{IH}$ | | 80% VDD | | | V |
| Input Voltage LO | $V_{IL}$ | | | | 20% VDD | V |
| Input Current: Input Sink | $I_{IH}$ | | | | 1.5 | µA |
| Input Source | $I_{IL}$ | | -1.5 | | | µA |
| Pull-down Current (MR, SI, SCK, ACLK pins) | $I_{PD}$ | | 250 | | 600 | µA |
| Pull-up Current ($\overline{CS}$ pin) | $I_{PU}$ | | -600 | | -300 | µA |
| **ARINC OUTPUTS - Pins AOUT37, BOUT37, (or AOUT27, BOUT27 with external 10 Ohms)** | | | | | | |
| ARINC output voltage (Ref. To GND) One or zero | $V_{DOUT}$ | No load and magnitude at pin, | 4.50 | 5.00 | 5.50 | V |
| Null | $V_{NOUT}$ | | -0.25 | | 0.25 | V |
| ARINC output voltage (Differential) One or zero | $V_{DDIF}$ | No load and magnitude at pin, | 9.0 | 10.0 | 11.0 | V |
| Null | $V_{NDIF}$ | | -0.5 | | 0.5 | V |
| ARINC output current | $I_{OUT}$ | Momentary current | 80 | | | mA |
| **LOGIC OUTPUTS** | | | | | | |
| Output Voltage: Logic "1" Output Voltage | $V_{OH}$ | $I_{OH}$ = -100µA | 90%VDD | | | V |
| Logic "0" Output Voltage | $V_{OL}$ | $I_{OL}$ = 1.0mA | | | 10% VDD | V |
| Output Current: Output Sink (All Outputs & Bi-directional Pins) | $I_{OL}$ | $V_{OUT}$ = 0.4V | 1.6 | | | mA |
| Output Source | $I_{OH}$ | $V_{OUT}$ = $V_{DD}$ - 0.4V | | | -1.0 | mA |
| Output Capacitance: | $C_O$ | | | 15 | | pF |
| **Operating Voltage Range** | | | | | | |
| | VDD | | 3.15 | | 5.25 | V |
| | V+ | | 4.75 | | 5.5 | V |
| | V- | | -4.75 | | -5.5 | V |
| **Operating Supply Current** | | | | | | |
| VDD | $I_{DD1}$ | | | 2.5 | 7 | mA |
| V+ | $I_{DD2}$ | | | 4 | 14 | mA |
| V- | $I_{EE1}$ | | | 4 | 12 | mA |

# AC ELECTRICAL CHARACTERISTICS

| PARAMETER | | SYMBOL | LIMITS | | | UNITS |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **SPI INTERFACE TIMING** | | | | | | |
| SCK clock period | | $t_{CYC}$ | 200 | | | ns |
| $\overline{CS}$ active after last SCK rising edge | | $t_{CHH}$ | 10 | | | ns |
| $\overline{CS}$ setup time to first SCK rising edge | | $t_{CES}$ | 10 | | | ns |
| $\overline{CS}$ hold time after last SCK falling edge | | $t_{CEH}$ | 40 | | | ns |
| $\overline{CS}$ inactive between SPI instructions | | $t_{CPH}$ | 35 | | | ns |
| SPI SI Data set-up time to SCK rising edge | | $t_{DS}$ | 20 | | | ns |
| SPI SI Data hold time after SCK rising edge | | $t_{DH}$ | 30 | | | ns |
| SCK rise time | | $t_{SCKR}$ | | | 10 | ns |
| SCK fall ime | | $t_{SCKF}$ | | | 10 | ns |
| SCK pulse width high | | $t_{SCKH}$ | 90 | | | ns |
| SCK pulse width low | | $t_{SCKL}$ | 80 | | | ns |
| SO valid after SCK falling edge | | $t_{DV}$ | | | 130 | ns |
| SO high-impedance after SCK falling edge | | $t_{CHZ}$ | | | 100 | ns |
| **TRANSMITTER TIMING** | | | | | | |
| SPI transmit data write or FIFO clear instruction to TFLAG (Empty or Full) | | $t_{TFLG}$ | | | 120 | ns |
| SPI instruction to ARINC 429 data output - Hi Speed | | $t_{SDAT}$ | | | 17 | µs |
| SPI instruction to ARINC 429 data output - Lo Speed | | $t_{SDAT}$ | | | 118 | µs |
| Delay TFLAG high after enable transmit - Hi Speed | | $t_{DATT}$ | | | 14 | µs |
| Delay TFLAG high after enable transmit - Lo Speed | | $t_{DATT}$ | | | 114 | µs |
| Line driver transition differential times: | | | | | | |
| (High Speed, control register CR10 = Logic 0) | high to low | $t_{fx}$ | 1.0 | 1.5 | 2.0 | µs |
| | low to high | $t_{rx}$ | 1.0 | 1.5 | 2.0 | µs |
| (Low Speed, control register CR10 = Logic 1) | high to low | $t_{fx}$ | 5.0 | 10 | 15 | µs |
| | low to high | $t_{rx}$ | 5.0 | 10 | 15 | µs |

# ORDERING INFORMATION

**HI - 3587 xx x x**

| PART NUMBER | LEAD FINISH |
|---|---|
| Blank | Tin / Lead (Sn / Pb) Solder |
| F | 100% Matte Tin (Pb-free, RoHS compliant) |

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN |
|---|---|---|---|
| I | -40°C TO +85°C | I | No |
| T | -55°C TO +125°C | T | No |

| PART NUMBER | PACKAGE DESCRIPTION |
|---|---|
| PC | 44 PIN PLASTIC CHIP-SCALE, QFN (44PCS) |
| PQ | 44 PIN PLASTIC QUAD FLAT PACK, PQFP (44PTQS) |

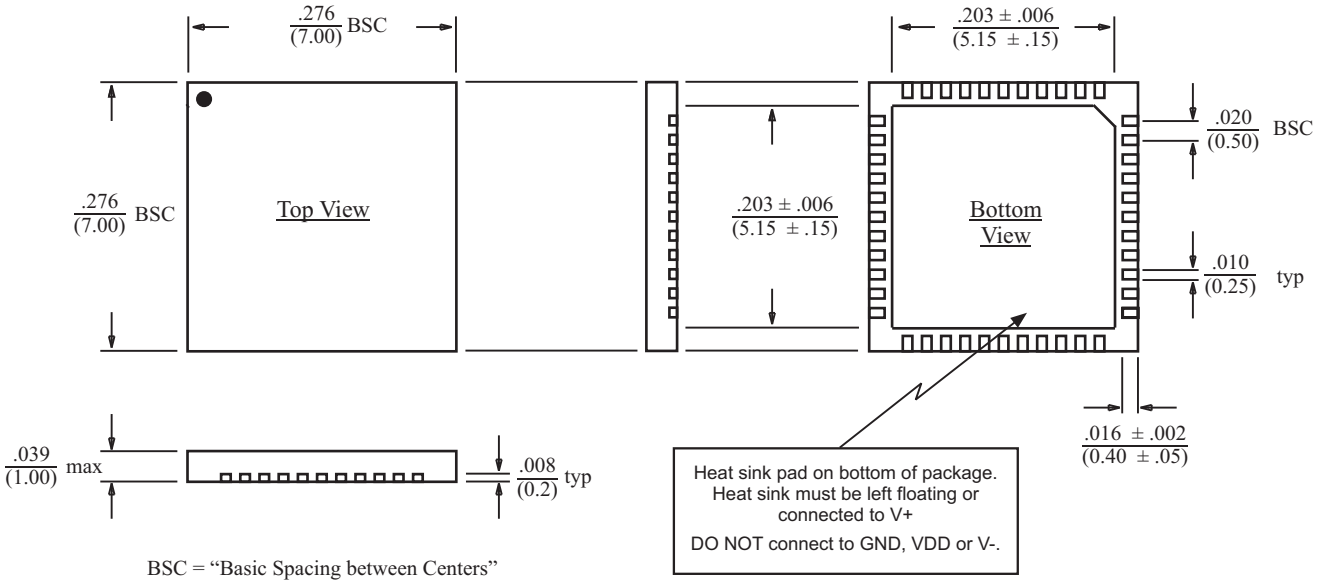
# REVISION HISTORY

| Revision | Date | Page | Description of Change |
|---|---|---|---|
| DS3587, Rev. NEW | 05/08/08 | All | Initial Release |
| Rev. A | 06/09/08 | 1 | Updated Date in header and Revision Letter/Date in footer. |
| | | 5 | Clarified the description of the FIFO operation for SPI op code 11. |

## 44-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

*inches (millimeters)*

Package Type: 44PCS

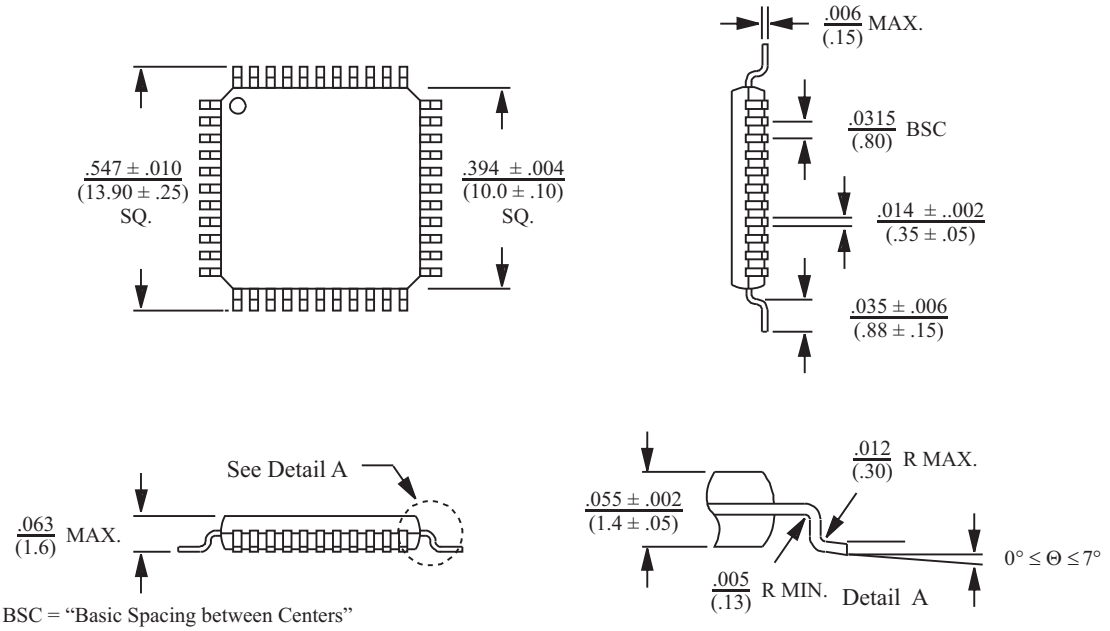



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

## 44-PIN PLASTIC QUAD FLAT PACK (PQFP)

*inches (millimeters)*

Package Type: 44PTQS

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