

GENERAL DESCRIPTION

The HI-3584A from Holt Integrated Circuits is a silicon gate CMOS device for interfacing a 16-bit parallel data bus to the ARINC 429 serial bus. The HI-3584A design offers a high-speed host CPU interface compared with the earlier HI-3584 product. The device provides two receivers each with label recognition, a 32 by 32 FIFO, and an analog line receiver. Up to 16 labels may be programmed for each receiver. The independent transmitter also has a 32 by 32 FIFO. The status of all three FIFOs can be monitored using the external status pins or by polling the HI-3584A's status register.

Other features include a programmable option of data or parity in the 32nd bit, and the ability to unscramble the 32 bit word. Also, versions are available with different values of input resistance to allow users to more easily add external lightning protection circuitry.

The 16-bit parallel data bus exchanges the 32-bit ARINC data word in two steps when either loading the transmitter or interrogating the receivers. The databus and all control signals are CMOS and TTL compatible.

The HI-3584A applies the ARINC protocol to the receivers and transmitter. Timing is based on a 1 Megahertz clock.

Additional interface circuitry such as the Holt HI-8570 or HI-8571 is required to translate the transmitter's 3.3 volt logic outputs to ARINC 429 drive levels.

FEATURES

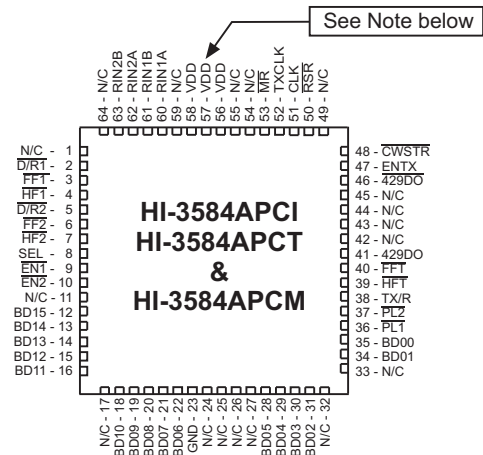
- ARINC specification 429 compatible
- 3.3V logic supply operation
- Dual receiver and transmitter interface
- Analog line receivers connect directly to ARINC bus
- Programmable label recognition
- On-chip 16 label memory for each receiver
- 32 x 32 FIFOs each receiver and transmitter
- Independent data rate selection for transmitter and each receiver
- Status register
- Data scramble control
- 32nd transmit bit can be data or parity
- Self test mode
- Low power
- Industrial & Extended temperature ranges

APPLICATIONS

- Avionics data communication
- Serial to parallel conversion
- Parallel to serial conversion

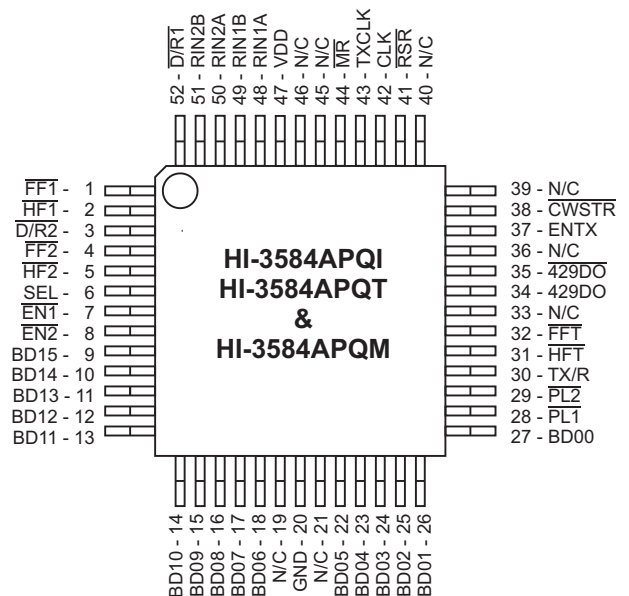
PIN CONFIGURATIONS (Top View)

(See page 13 for additional pin configuration)



(Note: All 3 VDD pins must be connected to the same 3.3V supply)

64 - Pin Plastic 9mm x 9mm Chip-Scale Package



52 - Pin Plastic Quad Flat Pack (PQFP)

PIN DESCRIPTIONS

| SIGNAL | FUNCTION | DESCRIPTION |
|--------------------|----------|---|
| VDD | POWER | +3.3V ±5% (All three VDD pins on the chip-scale package <u>must</u> be connect to the same supply) |
| RIN1A | INPUT | ARINC receiver 1 positive input |
| RIN1B | INPUT | ARINC receiver 1 negative input |
| RIN2A | INPUT | ARINC receiver 2 positive input |
| RIN2B | INPUT | ARINC receiver 2 negative input |
| $\overline{D/R1}$ | OUTPUT | Receiver 1 data ready flag |
| $\overline{FF1}$ | OUTPUT | FIFO full Receiver 1 |
| $\overline{HF1}$ | OUTPUT | FIFO Half full, Receiver 1 |
| $\overline{D/R2}$ | OUTPUT | Receiver 2 data ready flag |
| $\overline{FF2}$ | OUTPUT | FIFO full Receiver 2 |
| $\overline{HF2}$ | OUTPUT | FIFO Half full, Receiver 2 |
| SEL | INPUT | Receiver data byte selection (0 = BYTE 1) (1 = BYTE 2) |
| $\overline{EN1}$ | INPUT | Data Bus control, enables receiver 1 data to outputs |
| $\overline{EN2}$ | INPUT | Data Bus control, enables receiver 2 data to outputs if $\overline{EN1}$ is high |
| BD15 | I/O | Data Bus |
| BD14 | I/O | Data Bus |
| BD13 | I/O | Data Bus |
| BD12 | I/O | Data Bus |
| BD11 | I/O | Data Bus |
| BD10 | I/O | Data Bus |
| BD09 | I/O | Data Bus |
| BD08 | I/O | Data Bus |
| BD07 | I/O | Data Bus |
| BD06 | I/O | Data Bus |
| GND | POWER | 0 V |
| BD05 | I/O | Data Bus |
| BD04 | I/O | Data Bus |
| BD03 | I/O | Data Bus |
| BD02 | I/O | Data Bus |
| BD01 | I/O | Data Bus |
| BD00 | I/O | Data Bus |
| $\overline{PL1}$ | INPUT | Latch enable for byte 1 entered from data bus to transmitter FIFO. |
| $\overline{PL2}$ | INPUT | Latch enable for byte 2 entered from data bus to transmitter FIFO. Must follow $\overline{PL1}$. |
| TX/R | OUTPUT | Transmitter ready flag. Goes low when ARINC word loaded into FIFO. Goes high after transmission and FIFO empty. |
| \overline{HFT} | OUTPUT | Transmitter FIFO Half Full |
| \overline{FFT} | OUTPUT | Transmitter FIFO Full |
| 429DO | OUTPUT | "ONES" data output from transmitter |
| $\overline{429DO}$ | OUTPUT | "ZEROS" data output from transmitter |
| ENTX | INPUT | Enable Transmission |
| \overline{CWSTR} | INPUT | Clock for control word register |
| \overline{RSR} | INPUT | Read Status Register if SEL=0, read Control Register if SEL=1 |
| CLK | INPUT | Master Clock input |
| TX CLK | OUTPUT | Transmitter Clock equal to Master Clock (CLK), divided by either 10 or 80. |
| \overline{MR} | INPUT | Master Reset, active low |

FUNCTIONAL DESCRIPTION

CONTROL WORD REGISTER

The HI-3584A contains a 16-bit control register which is used to configure the device. The control register bits CR0 - CR15 are loaded from BD00 - BD15 when CWSTR is pulsed low. The control register contents are output on the databus when SEL = 1 and RSR is pulsed low. Each bit of the control register has the following function:

STATUS REGISTER

The HI-3584A contains a 9-bit status register which can be interrogated to determine the status of the ARINC receivers, data FIFOs and transmitter. The contents of the status register are output on BD00 - BD08 when the RSR pin is taken low and SEL = 0. Unused bits are output as zeros. The following table defines the status register bits.

| CR Bit | FUNCTION | STATE | DESCRIPTION |
|--------|---------------------------------------|-------|--|
| CR0 | Receiver 1 Data clock Select | 0 | Data rate = CLK/10 |
| | | 1 | Data rate = CLK/80 |
| CR1 | Label Memory Read / Write | 0 | Normal operation |
| | | 1 | Load 16 labels using <u>PL1</u> / <u>PL2</u> Read 16 labels using <u>EN1</u> / <u>EN2</u> |
| CR2 | Enable Label Recognition (Receiver 1) | 0 | Disable label recognition |
| | | 1 | Enable label recognition |
| CR3 | Enable Label Recognition (Receiver 2) | 0 | Disable Label Recognition |
| | | 1 | Enable Label recognition |
| CR4 | Enable 32nd bit as parity | 0 | Transmitter 32nd bit is data |
| | | 1 | Transmitter 32nd bit is parity |
| CR5 | Self Test | 0 | The 429DO and 429D0 digital outputs are internally connected to the receiver logic inputs |
| | | 1 | Normal operation |
| CR6 | Receiver 1 decoder | 0 | Receiver 1 decoder disabled |
| | | 1 | ARINC bits 9 and 10 must match CR7 and CR8 |
| CR7 | - | - | If receiver 1 decoder is enabled, the ARINC bit 9 must match this bit |
| CR8 | - | - | If receiver 1 decoder is enabled, the ARINC bit 10 must match this bit |
| CR9 | Receiver 2 Decoder | 0 | Receiver 2 decoder disabled |
| | | 1 | ARINC bits 9 and 10 must match CR10 and CR11 |
| CR10 | - | - | If receiver 2 decoder is enabled, the ARINC bit 9 must match this bit |
| CR11 | - | - | If receiver 2 decoder is enabled, the ARINC bit 10 must match this bit |
| CR12 | Invert Transmitter parity | 0 | Transmitter 32nd bit is Odd parity |
| | | 1 | Transmitter 32nd bit is Even parity |
| CR13 | Transmitter data clock select | 0 | Data rate=CLK/10, O/P slope=1.5us |
| | | 1 | Data rate=CLK/80, O/P slope=10us |
| CR14 | Receiver 2 data clock select | 0 | Data rate=CLK/10 |
| | | 1 | Data rate=CLK/80 |
| CR15 | Data format | 0 | Scramble ARINC data |
| | | 1 | Unscramble ARINC data |

| SR Bit | FUNCTION | STATE | DESCRIPTION |
|--------|-----------------------------|-------|---|
| SR0 | Data ready (Receiver 1) | 0 | Receiver 1 FIFO empty |
| | | 1 | Receiver 1 FIFO contains valid data Resets to zero when all data has been read. <u>D/R1</u> pin is the inverse of this bit |
| SR1 | FIFO half full (Receiver 1) | 0 | Receiver 1 FIFO holds less than 16 words |
| | | 1 | Receiver 1 FIFO holds at least 16 words. <u>HF1</u> pin is the inverse of this bit. |
| SR2 | FIFO full (Receiver 1) | 0 | Receiver 1 FIFO not full |
| | | 1 | Receiver 1 FIFO full. To avoid data loss, the FIFO must be read within one ARINC word period. <u>FF1</u> pin is the inverse of this bit |
| SR3 | Data ready (Receiver 2) | 0 | Receiver 2 FIFO empty |
| | | 1 | Receiver 2 FIFO contains valid data Resets to zero when all data has been read. <u>D/R2</u> pin is the inverse of this bit |
| SR4 | FIFO half full (Receiver 2) | 0 | Receiver 2 FIFO holds less than 16 words |
| | | 1 | Receiver 2 FIFO holds at least 16 words. <u>HF2</u> pin is the inverse of this bit. |
| SR5 | FIFO full (Receiver 2) | 0 | Receiver 2 FIFO not full |
| | | 1 | Receiver 2 FIFO full. To avoid data loss, the FIFO must be read within one ARINC word period. <u>FF2</u> pin is the inverse of this bit |
| SR6 | Transmitter FIFO empty | 0 | Transmitter FIFO not empty |
| | | 1 | Transmitter FIFO empty. |
| SR7 | Transmitter FIFO full | 0 | Transmitter FIFO not full |
| | | 1 | Transmitter FIFO full. <u>FFT</u> pin is the inverse of this bit. |
| SR8 | Transmitter FIFO half full | 0 | Transmitter FIFO contains less than 16 words |
| | | 1 | Transmitter FIFO contains at least 16 words. <u>HFT</u> pin is the inverse of this bit. |

FUNCTIONAL DESCRIPTION (cont.)

ARINC 429 DATA FORMAT

Control register bit CR15 is used to control how individual bits in the received or transmitted ARINC word are mapped to the HI-3584A data bus during data read or write operations. The following table describes this mapping:

| BYTE 1 | | | | | | | | | | | | | | | | |
|------------------|-------|-------|-------|-------|-------|-------|-------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| DATA BUS | BD 15 | BD 14 | BD 13 | BD 12 | BD 11 | BD 10 | BD 09 | BD 08 | BD 07 | BD 06 | BD 05 | BD 04 | BD 03 | BD 02 | BD 01 | BD 00 |
| ARINC BIT CR15=0 | 13 | 12 | 11 | 10 | 9 | 31 | 30 | 32 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| ARINC BIT CR15=1 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| | | | | SDI | SDI | | | Parity | Label | Label | Label | Label | Label | Label | Label | Label |

| BYTE 2 | | | | | | | | | | | | | | | | |
|------------------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| DATA BUS | BD 15 | BD 14 | BD 13 | BD 12 | BD 11 | BD 10 | BD 09 | BD 08 | BD 07 | BD 06 | BD 05 | BD 04 | BD 03 | BD 02 | BD 01 | BD 00 |
| ARINC BIT CR15=0 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 |
| ARINC BIT CR15=1 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 |
| | Parity | | | | | | | | | | | | | | | |

THE RECEIVERS

ARINC BUS INTERFACE

Figure 1 shows the input circuit for each receiver. The ARINC 429 specification requires the following detection levels:

| STATE | DIFFERENTIAL VOLTAGE |
|-------|--------------------------|
| ONE | +6.5 Volts to +13 Volts |
| NULL | +2.5 Volts to -2.5 Volts |
| ZERO | -6.5 Volts to -13 Volts |

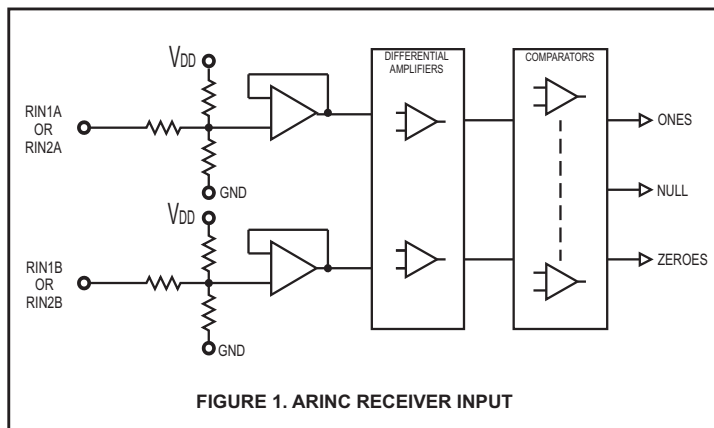


FIGURE 1. ARINC RECEIVER INPUT

The HI-3584A guarantees recognition of these levels with a common mode Voltage with respect to GND less than $\pm 4V$ for the worst case condition (3.0V supply and 13V signal level).

The tolerances in the design guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the ARINC signal is out of the actual acceptance ranges, including the nulls, the chip rejects the data.

RECEIVER LOGIC OPERATION

Figure 2 shows a block diagram of the logic section of each receiver.

BIT TIMING

The ARINC 429 specification contains the following timing specification for the received data:

| | HIGH SPEED | LOW SPEED |
|-----------------|-------------------------|------------------------|
| BIT RATE | 100K BPS $\pm 1\%$ | 12K -14.5K BPS |
| PULSE RISE TIME | 1.5 ± 0.5 μ sec | 10 ± 5 μ sec |
| PULSE FALL TIME | 1.5 ± 0.5 μ sec | 10 ± 5 μ sec |
| PULSE WIDTH | 5 μ sec $\pm 5\%$ | 34.5 to 41.7 μ sec |

The HI-3584A accepts signals that meet these specifications and rejects signals outside the tolerances. The way the logic operation achieves this is described below:

- Key to the performance of the timing checking logic is an accurate 1MHz clock source. Less than 0.1% error is recommended.
- The sampling shift registers are 10 bits long and must show three consecutive Ones, Zeros or Nulls to be considered valid data. Additionally, for data bits, the One or Zero in the upper bits of the sampling shift registers must be followed by a Null in the lower bits within the data bit time. For a Null in the word gap, three consecutive Nulls must be found in both the upper and lower bits of the sampling shift register. In this manner the minimum pulse width is guaranteed.
- Each data bit must follow its predecessor by not less than 8 samples and no more than 12 samples. In this manner the bit rate is checked. With exactly 1MHz input clock frequency, the acceptable data bit rates are as follows:

| | HIGH SPEED | LOW SPEED |
|-------------------|------------|-----------|
| DATA BIT RATE MIN | 83K BPS | 10.4K BPS |
| DATA BIT RATE MAX | 125K BPS | 15.6K BPS |

- The Word Gap timer samples the Null shift register every 10 input clocks (80 for low speed) after the last data bit of a valid reception. If the Null is present, the Word Gap counter is incremented. A count of 3 will enable the next reception.

FUNCTIONAL DESCRIPTION (cont.)

Once a valid ARINC word is loaded into the FIFO, then EOS clocks the data ready flag flip flop to a "1", $\overline{D/R1}$ or $\overline{D/R2}$ (or both) will go low. The data flag for a receiver will remain low until both ARINC bytes from that receiver are retrieved and the FIFO is empty. This is accomplished by first activating \overline{EN} with SEL, the byte selector, low to retrieve the first byte and then activating \overline{EN} with SEL high to retrieve the second byte. $\overline{EN1}$ retrieves data from receiver 1 and $\overline{EN2}$ retrieves data from receiver 2.

Up to 32 ARINC words may be loaded into each receiver's FIFO. The $\overline{FF1}$ ($\overline{FF2}$) pin will go low when the receiver 1 (2) FIFO is full. Failure to retrieve data from a full FIFO will cause the next valid ARINC word received to overwrite the existing data in FIFO location 32. A FIFO half full flag $\overline{HF1}$ ($\overline{HF2}$) goes low if the FIFO contains 16 or more received ARINC words. The $\overline{HF1}$ ($\overline{HF2}$) pin is intended to act as an interrupt flag to the system's external microprocessor, allowing a 16 word data retrieval routine to be performed, without the user needing to continually poll the HI-3584A's status register bits.

LABEL RECOGNITION

The chip compares the incoming label to the stored labels if label recognition is enabled. If a match is found, the data is processed. If a match is not found, no indicators of receiving ARINC data are presented. Note that 00(Hex) is treated in the same way as any other label value. Label bit significance is not changed by the status of control register bit CR15. Label bits BD00-BD07 are always compared to received ARINC bits 1-8 respectively.

LOADING LABELS

After a write that takes CR1 from 0 to 1, the next 16 writes of data (\overline{PL} pulsed low) load label data into each location of the label memory from the BD00 - BD07 pins. The $\overline{PL1}$ pin is used to write label data for receiver 1 and $\overline{PL2}$ for receiver 2. Note that ARINC word reception is suspended during the label memory write sequence.

READING LABELS

After the write that changes CR1 from 0 to 1, the next 16 data reads of the selected receiver (\overline{EN} taken low) are labels. $\overline{EN1}$ is used to read labels for receiver 1, and $\overline{EN2}$ to read labels for receiver 2. Label data is presented on BD00 - BD07.

When writing to, or reading from the label memory, SEL must be a one, all 16 locations should be accessed, and CR1 must be written to zero before returning to normal operation. Label recognition must be disabled ($CR2/3=0$) during the label read sequence.

TRANSMITTER

FIFO OPERATION

The FIFO is loaded sequentially by first pulsing $\overline{PL1}$ to load byte 1 and then $\overline{PL2}$ to load byte 2. The control logic automatically loads the 31 bit word (or 32 bit word if $CR4=0$) in the next available position of the FIFO. If TX/R, the transmitter ready flag is high (FIFO empty), then up to 32 words, each 31 or 32 bits long, may be loaded. If TX/R is low, then only the available positions may be loaded. If all 32 positions are full, the \overline{FFT} flag is asserted and the FIFO ignores further attempts to load data.

A transmitter FIFO half-full flag \overline{HFT} is provided. When the transmit FIFO contains less than 16 words, \overline{HFT} is high, indicating to the system microprocessor that a 16 ARINC word block write sequence can be initiated.

In normal operation ($CR4=1$), the 32nd bit transmitted is a parity bit. Odd or even parity is selected by programming control register bit CR12 to a zero or one. If CR4 is programmed to a 0, then all 32-bits of data loaded into the transmitter FIFO are treated as data and are transmitted.

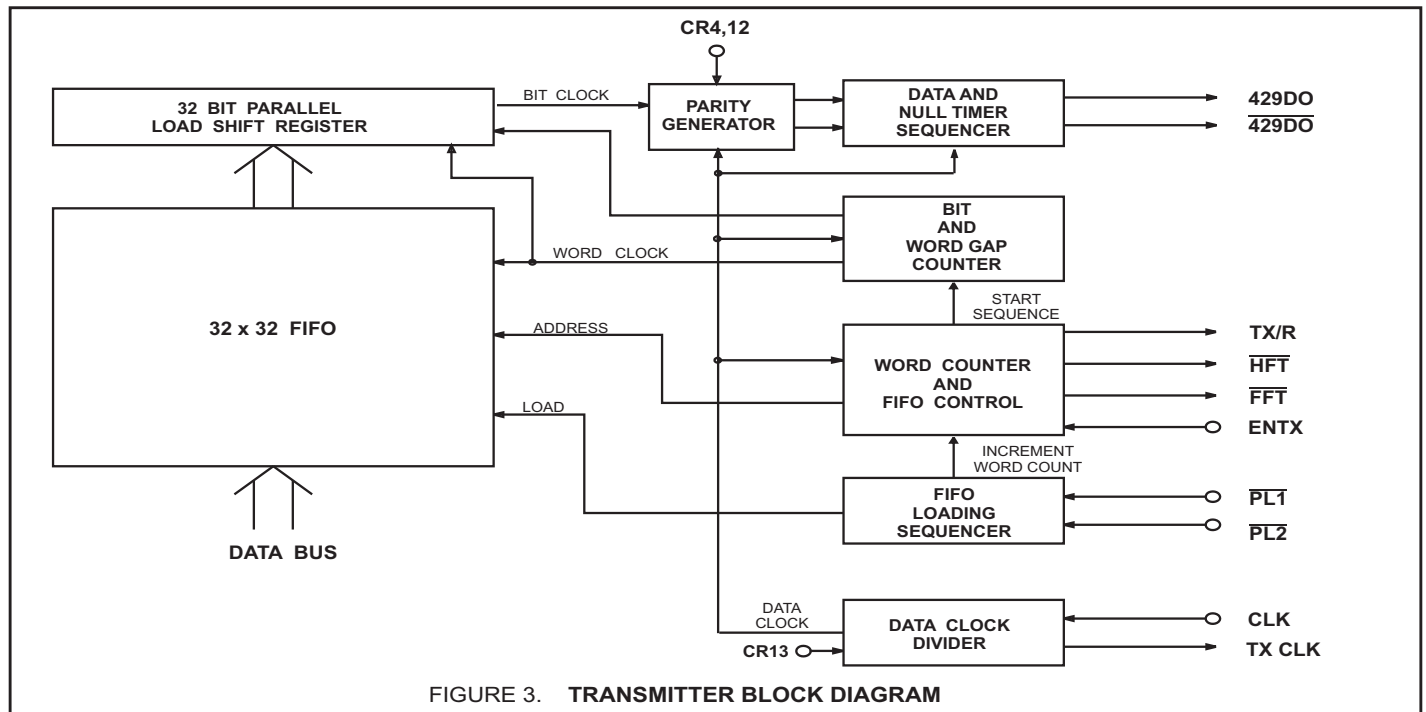


FIGURE 3. TRANSMITTER BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION (cont.)

DATA TRANSMISSION

When ENTX goes high, enabling transmission, the FIFO positions are incremented with the top register loading into the data transmission shift register. Within 2.5 data clocks the first data bit appears at $\overline{429DO}$ and $\overline{429DO}$. The 31 or 32 bits in the data transmission shift register are presented sequentially to the outputs in the ARINC 429 format with the following timing:

| | <u>HIGH SPEED</u> | <u>LOW SPEED</u> |
|---------------------|-------------------|------------------|
| ARINC DATA BIT TIME | 10 Clocks | 80 Clocks |
| DATA BIT TIME | 5 Clocks | 40 Clocks |
| NULL BIT TIME | 5 Clocks | 40 Clocks |
| WORD GAP TIME | 40 Clocks | 320 Clocks |

The word counter detects when all loaded positions have been transmitted and sets the transmitter ready flag, TX/R, high.

TRANSMITTER PARITY

The parity generator counts the Ones in the 31-bit word. If control register bit CR12 is set low, the 32nd bit transmitted will make parity odd. If the control bit is, high the parity is even. Setting CR4 to a Zero bypasses the parity generator, and allows 32 bits of data to be transmitted.

SELF TEST

If control register bit CR5 is set low, the transmitter serial output data are internally connected to each of the two receivers, bypassing the analog interface circuitry. Data is passed unmodified to receiver 1 and inverted to receiver 2. The serial data from the transmitter is always present on the $\overline{429DO}$ and $\overline{429DO}$ outputs regardless of the state of CR5.

SYSTEM OPERATION

The two receivers are independent of the transmitter. Therefore, control of data exchanges is strictly at the option of the user. The only restrictions are:

1. The received data will be overwritten if the receiver FIFO is full and at least one location is not retrieved before the next complete ARINC word is received.
2. The transmitter FIFO can store 32 words maximum and ignores attempts to load additional data if full.

REPEATER OPERATION

Repeater mode of operation allows a data word that has been received by the HI-3584A to be placed directly into the transmitter FIFO. Repeater operation is similar to normal receiver operation. In normal operation, either byte of a received data word may be read from the receiver latches first by use of SEL input. During repeater operation however, the lower byte of the data word must be read first. This is necessary because, as the data is being read, it is also being loaded into transmitter FIFO which is always loaded with the lower byte of the data word first. Signal flow for repeater operation is shown in the Timing Diagrams section.

HI-3584A-15

The HI-3584A-15 option is similar to the HI-3584A with the exception that it allows an external 15 Kohm resistor to be added in series with each ARINC input without affecting the ARINC input thresholds. This option is especially useful in applications where lightning protection circuitry is also required.

Each side of the ARINC bus must be connected through a 15 Kohm series resistor in order for the chip to detect the correct ARINC levels. The typical 10 volt differential signal is translated and input to a window comparator and latch. The comparator levels are set so that with the external 15 Kohm resistors, they are just below the standard 6.5 volt minimum ARINC data threshold and just above the standard 2.5 volt maximum ARINC null threshold.

Please refer to the Holt AN-300 Application Note for additional information and recommendations on lightning protection of Holt line drivers and line receivers.

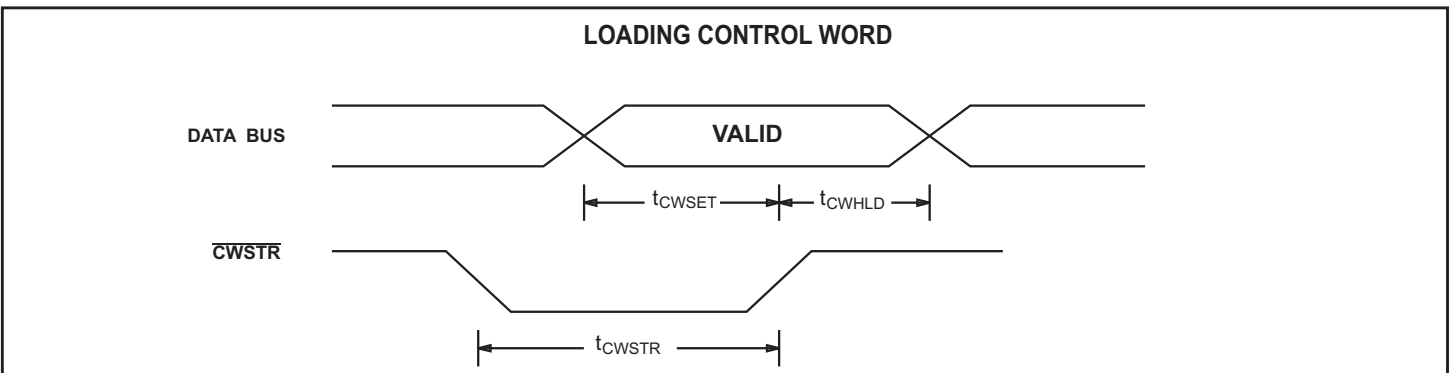
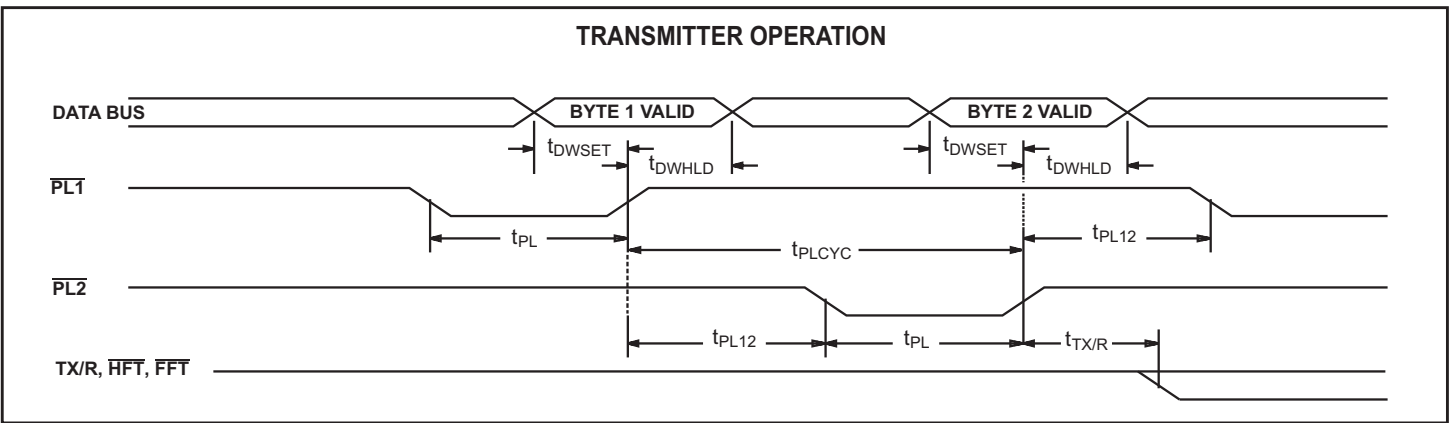
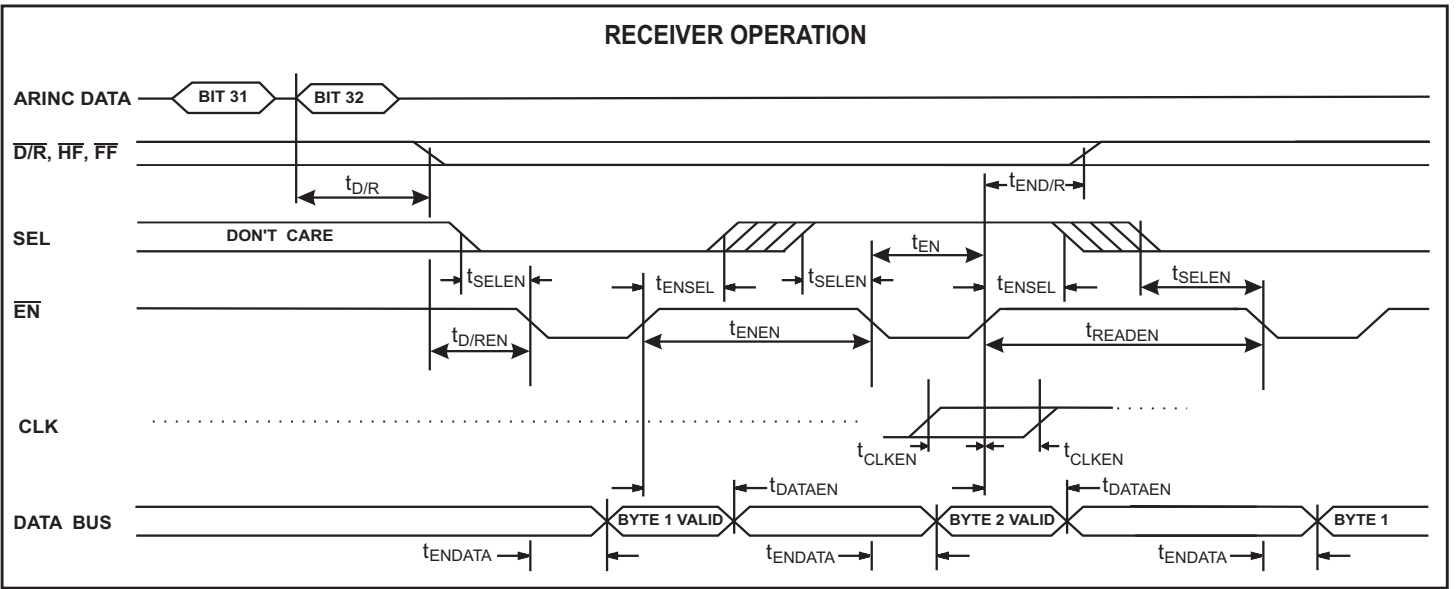
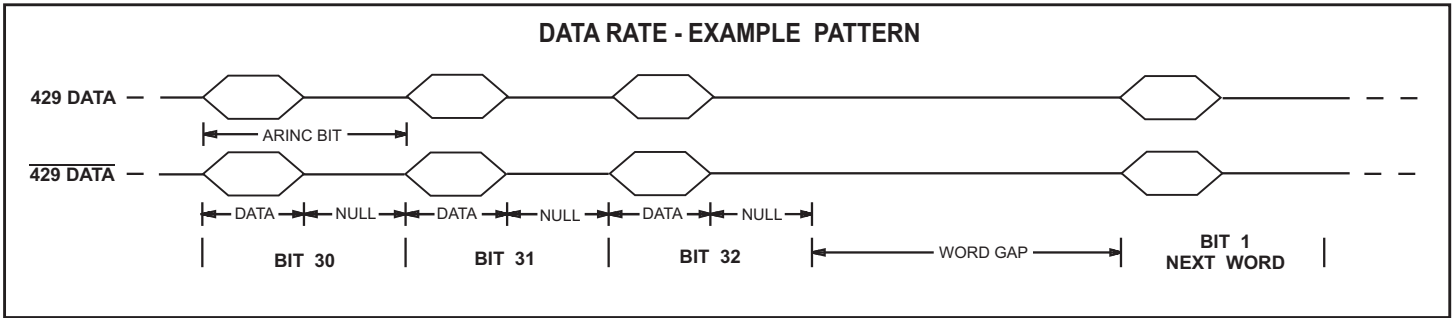
HIGH SPEED OPERATION

The HI-3584A may be operated at clock frequencies beyond that required for ARINC compliant operation. For operation at Master Clock (CLK) frequencies up to 5MHz, please contact Holt applications engineering.

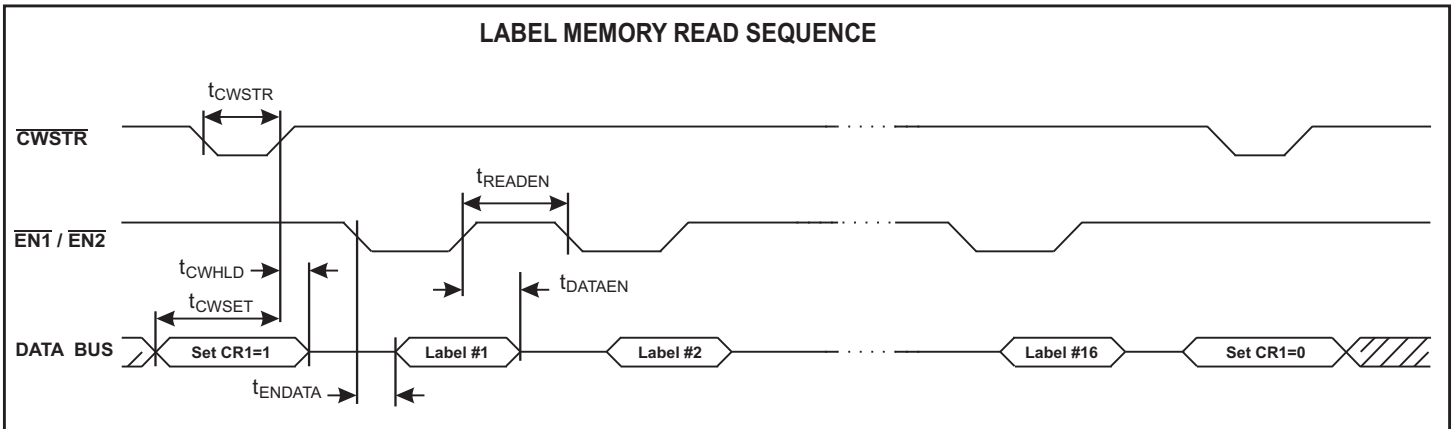
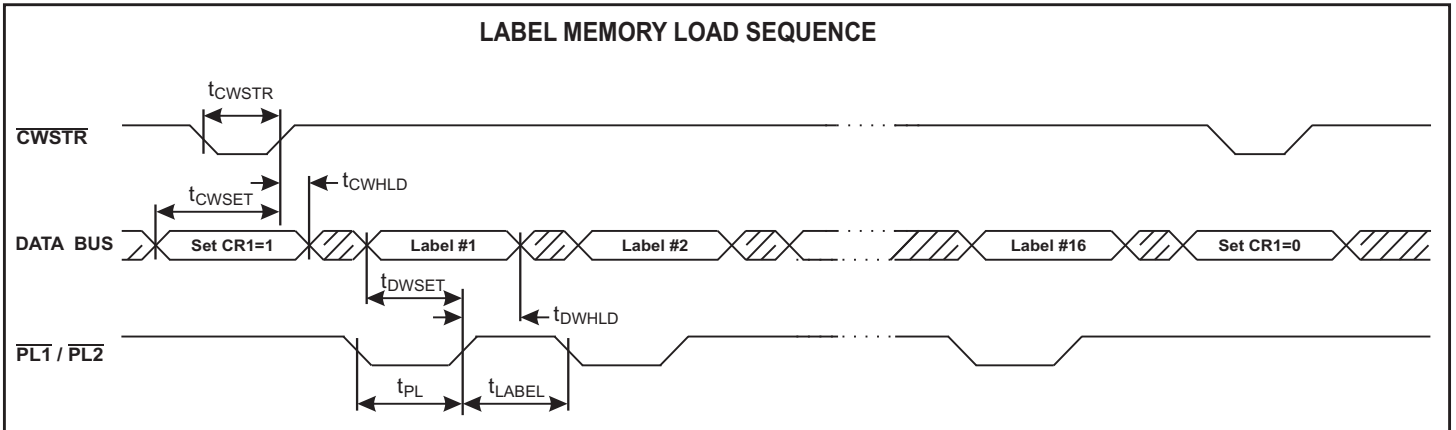
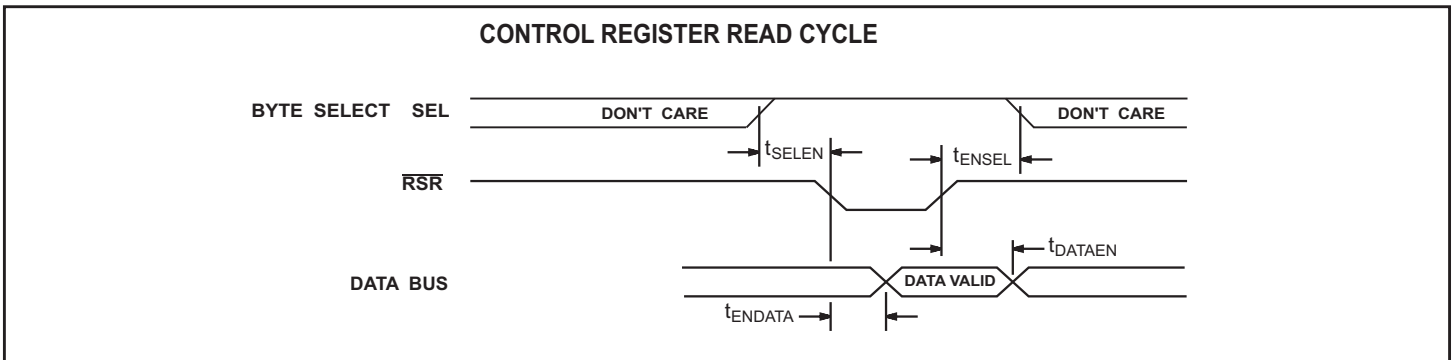
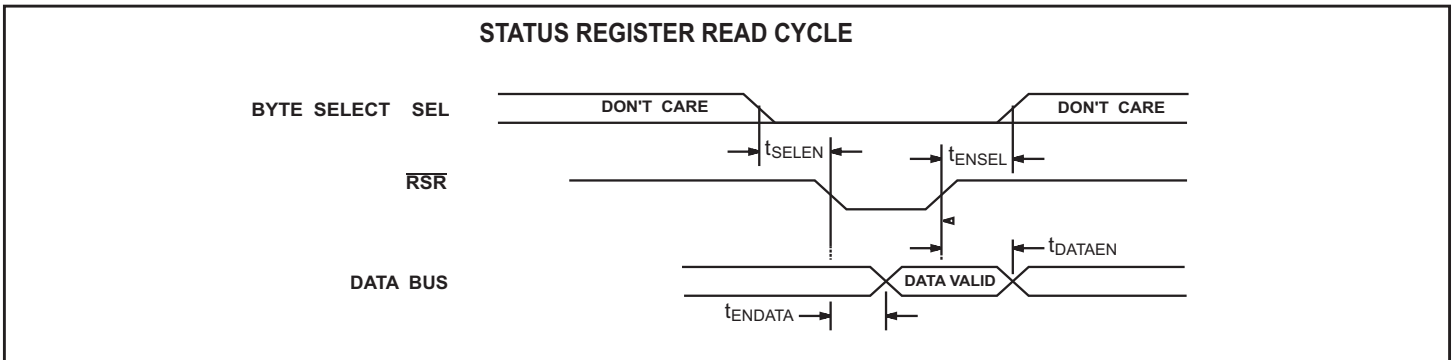
MASTER RESET (\overline{MR})

On a Master Reset data transmission and reception are immediately terminated, all three FIFOs are cleared as are the FIFO flags at the device pins and in the Status Register. The Control Register is not affected by a Master Reset.

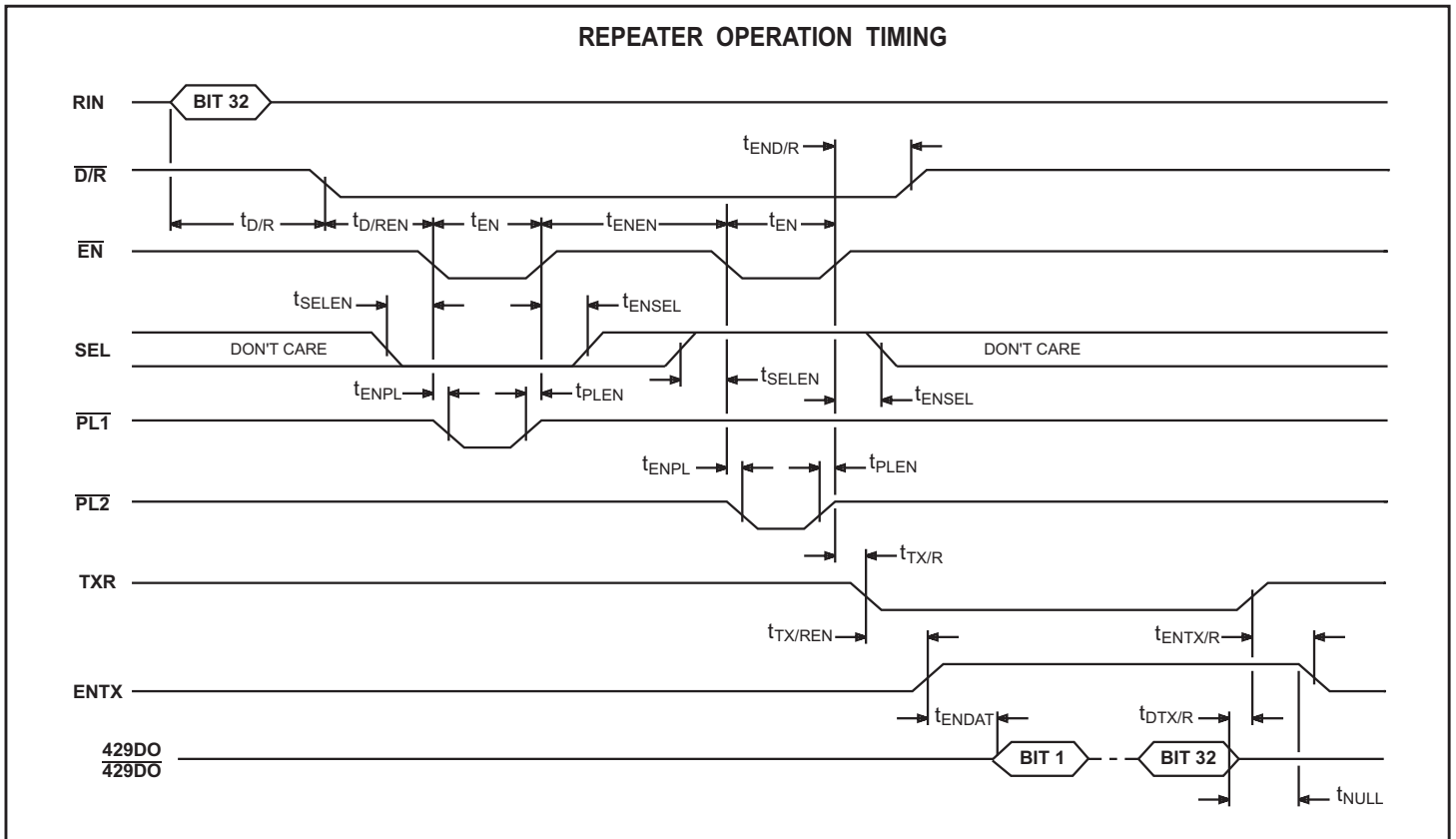
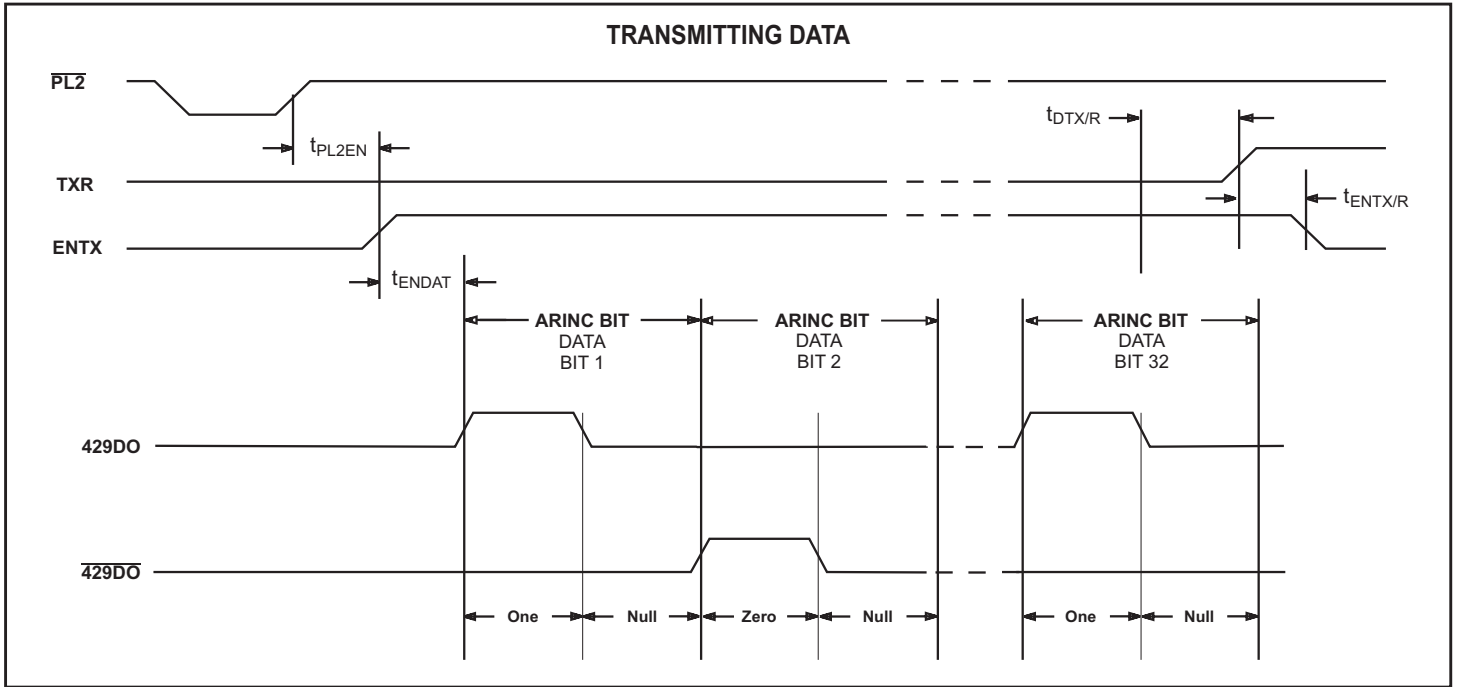
TIMING DIAGRAMS



TIMING DIAGRAMS (cont.)



TIMING DIAGRAMS (cont.)



ABSOLUTE MAXIMUM RATINGS

| | | | |
|--|--------------------------------|---|-----------------|
| Supply Voltages V _{DD} | -0.3V to +4V | Power Dissipation at 25°C | 500 mW |
| Voltage at pins RIN1A, RIN1B, RIN2A, RIN2B | -29V to +29V | DC Current Drain per pin | ±10mA |
| Voltage at any other pin | -0.3V to V _{DD} +0.3V | Storage Temperature Range | -65°C to +150°C |
| Solder temperature (Leads) | 280°C for 10 seconds | Operating Temperature Range (Industrial): | -40°C to +85°C |
| (Package) | 220°C | (Extended): | -55°C to +125°C |

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

| PARAMETER | SYMBOL | CONDITIONS | LIMITS | | | UNIT |
|---|---|------------------|---|------------------------|--------------------|-----------------|
| | | | MIN | TYP | MAX | |
| ARINC INPUTS - Pins RIN1A, RIN1B, RIN2A, RIN2B | | | | | | |
| Differential Input Voltage: (RIN1A to RIN1B, RIN2A to RIN2B) | ONE | V _{IH} | 6.5 | 10.0 | 13.0 | V |
| | ZERO | V _{IL} | -13.0 | -10.0 | -6.5 | V |
| | NULL | V _{NUL} | -2.5 | 0 | 2.5 | V |
| Input Resistance: | Differential To GND To V _{DD} | R _I | 12 | 80 | | KΩ |
| | | R _G | 12 | 45 | | KΩ |
| | | R _H | 12 | 45 | | KΩ |
| Input Current: | Input Sink Input Source | I _{IH} | | | 200 | μA |
| | | I _{IL} | -450 | | | μA |
| Input Capacitance: (Guaranteed but not tested) | Differential To GND To V _{DD} | C _I | | | 20 | pF |
| | | C _G | | | 20 | pF |
| | | C _H | | | 20 | pF |
| BI-DIRECTIONAL INPUTS - Pins BD00 - BD15 | | | | | | |
| Input Voltage: | Input Voltage HI Input Voltage LO | V _{IH} | 70% | | | V _{DD} |
| | | V _{IL} | | | 30% | V _{DD} |
| Input Current: | Input Sink Input Source | I _{IH} | | | 1.5 | μA |
| | | I _{IL} | -1.5 | | | μA |
| OTHER INPUTS | | | | | | |
| Input Voltage: | Input Voltage HI Input Voltage LO | V _{IH} | 70% | | | V |
| | | V _{IL} | | | 30% | V |
| Input Current: | Input Sink Input Source Pull-down Current (TEST pin) Pull-up Current (RSR pin) | I _{IH} | -1.5 | 330 | 1.5 | μA |
| | | I _{IL} | | | | |
| | | I _{PD} | | | | |
| | | I _{PU} | | | | |
| Input Capacitance: (Guaranteed but not tested) | C _I | | | | 15 | pF |
| | | | | | | |
| OUTPUTS | | | | | | |
| Output Voltage: | Logic "1" Output Voltage Logic "0" Output Voltage | V _{OH} | I _{OH} = -100μA | V _{DD} - 0.2V | | V |
| | | V _{OL} | I _{OL} = 1.0mA | | 10%V _{DD} | V |
| Output Current: (All Outputs & Bi-directional Pins) | Output Sink Output Source | I _{OL} | V _{OUT} = 0.4V | 1.6 | | mA |
| | | I _{OH} | V _{OUT} = V _{DD} - 0.4V | | -1.0 | mA |
| Output Capacitance: | C _O | | | | 15 | pF |
| Operating Supply Current | | | | | | |
| V _{DD} | I _{DD} | | | 3.5 | 7 | mA |

AC ELECTRICAL CHARACTERISTICS

VDD = 3.3V, GND = 0V, TA = Oper. Temp. Range and fclk=1MHz ±0.1% with 60/40 duty cycle

| PARAMETER | SYMBOL | LIMITS | | | UNITS |
|--|---------|--------|-----|---------|-------|
| | | MIN | TYP | MAX | |
| CONTROL WORD TIMING | | | | | |
| Pulse Width - \overline{CWSTR} | tCWSTR | 25 | | | ns |
| Setup - DATA BUS Valid to \overline{CWSTR} HIGH | tCWSET | 25 | | | ns |
| Hold - \overline{CWSTR} HIGH to DATA BUS Hi-Z | tCWHLDD | 5 | | | ns |
| RECEIVER FIFO AND LABEL READ TIMING | | | | | |
| Delay - Start ARINC 32nd Bit to $\overline{D/R}$ LOW: High Speed | tD/R | | | 16 | µs |
| Low Speed | tD/R | | | 128 | µs |
| Delay - $\overline{D/R}$ LOW to \overline{EN} LOW | tD/REN | 0 | | | ns |
| Delay - \overline{EN} HIGH to $\overline{D/R}$ HIGH | tEND/R | | | 25 | ns |
| Setup - SEL to \overline{EN} LOW | tSELEN | 10 | | | ns |
| Hold - SEL to \overline{EN} HIGH | tENSEL | 10 | | | ns |
| Delay - \overline{EN} LOW to DATA BUS Valid | tENDATA | | | 50 | ns |
| Delay - \overline{EN} HIGH to DATA BUS Hi-Z | tDATAEN | | | 20 | ns |
| Pulse Width - $\overline{EN1}$ or $\overline{EN2}$ | tEN | 50 | | | ns |
| Spacing - \overline{EN} HIGH to next \overline{EN} LOW (Same ARINC Word) | tENEN | 70 | | | ns |
| Spacing - \overline{EN} HIGH to next \overline{EN} LOW (Next ARINC Word) | tREADEN | 70 | | | ns |
| CLK HIGH separation from second \overline{EN} pulse HIGH (SEL is HIGH) | tCLKEN | 25 | | | ns |
| TRANSMITTER FIFO AND LABEL WRITE TIMING | | | | | |
| Pulse Width - $\overline{PL1}$ or $\overline{PL2}$ | tPL | 30 | | | ns |
| Setup - DATA BUS Valid to \overline{PL} HIGH | tDWSET | 30 | | | ns |
| Hold - \overline{PL} HIGH to DATA BUS Hi-Z | tDWHLD | 10 | | | ns |
| Spacing - $\overline{PL1}$ or $\overline{PL2}$ | tPL12 | 40 | | tCLK-10 | ns |
| Spacing - $\overline{PL1}$ rising to $\overline{PL2}$ rising | tPLCYC | | | | ns |
| Spacing between Label Write pulses | tLABEL | 40 | | | ns |
| Delay - $\overline{PL2}$ HIGH to TX/R LOW | tTX/R | | | 30 | ns |
| TRANSMISSION TIMING | | | | | |
| Spacing - $\overline{PL2}$ HIGH to ENTX HIGH | tPL2EN | 0 | | | µs |
| Delay - 32nd ARINC Bit to TX/R HIGH | tDTX/R | | | 50 | ns |
| Spacing - TX/R HIGH to ENTX LOW | tENTX/R | 0 | | | ns |
| Delay - ENTX HIGH to 429DO or 429D \overline{O} : High Speed | tENDAT | | | 25 | µs |
| Delay - ENTX HIGH to 429DO or 429D \overline{O} : Low Speed | tENDAT | | | 200 | µs |
| REPEATER OPERATION TIMING | | | | | |
| Delay - \overline{EN} LOW to \overline{PL} LOW | tENPL | 0 | | | ns |
| Hold - \overline{PL} HIGH to \overline{EN} HIGH | tPLEN | 0 | | | ns |
| Delay - TX/R LOW to ENTX HIGH | tTX/REN | 0 | | | ns |
| MASTER RESET PULSE WIDTH | | | | | |
| | tMR | 175 | | | ns |
| ARINC DATA RATE AND BIT TIMING | | | | | |
| | | | | ± 1% | |

HEAT SINK - CHIP-SCALE PACKAGE ONLY

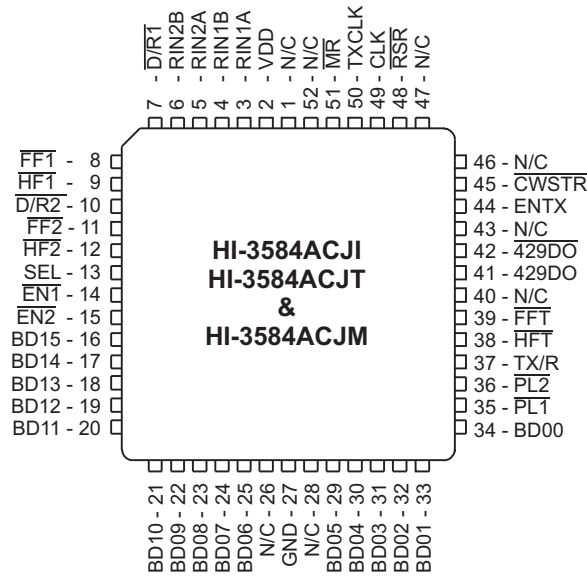
The HI-3584APCI and HI-3584APCT use a 64-pin plastic chip-scale package. This package has a metal heat sink pad on its bottom surface. This heat sink is electrically connected to the die. To enhance thermal dissipation, the

heat sink can be soldered to matching circuit board pad. The heat sink may be connected to GND or left floating.

Do not connect heat sink pad to VDD.

ADDITIONAL HI-3584A PIN CONFIGURATION

(See page 1 for additional pin configurations)



52 - Pin Cerquad J-lead

ORDERING INFORMATION

HI - 3584A xx x x - xx

| PART NUMBER | INPUT SERIES RESISTANCE | |
|----------------|-------------------------|---------------------|
| | BUILT-IN | REQUIRED EXTERNALLY |
| No dash number | 35K Ohm | 0 |
| -15 | 20K Ohm | 15K Ohm |

| PART NUMBER | PACKAGE DESCRIPTION |
|-------------|---|
| Blank | Tin / Lead (Sn / Pb) Solder |
| F | 100% Matte Tin (Pb-free RoHS compliant) |

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN |
|-------------|-------------------|------|---------|
| I | -40°C TO +85°C | I | No |
| T | -55°C TO +125°C | T | No |
| M | -55°C TO +125°C | M | Yes |

| PART NUMBER | PACKAGE DESCRIPTION |
|-------------|---|
| CJ | 52 PIN J-LEAD CERQUAD (52U) not available Pb-free |
| PC | 64 PIN PLASTIC CHIP-SCALE LPCC (64PCS) |
| PQ | 52 PIN PLASTIC QUAD FLAT PACK PQFP (52PTQS) |

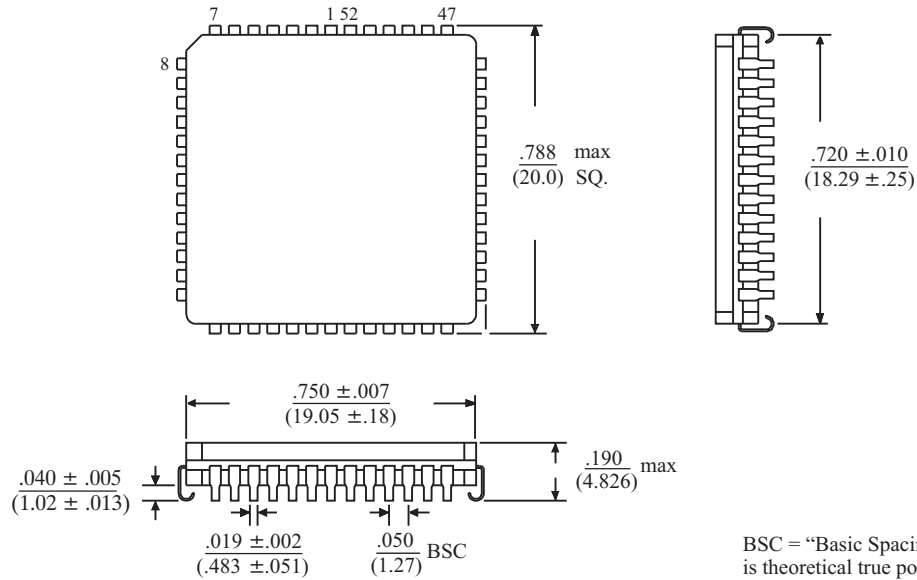
REVISION HISTORY

| P/N | Rev | Date | Description of Change |
|---------|-----|----------|-----------------------------------|
| DS3584A | NEW | 04/28/09 | Initial Release |
| | A | 04/27/10 | Added CLKEN to timing parameters. |
| | B | 06/29/10 | Added PLCYC to timing parameters. |

52-PIN J-LEAD CERQUAD

inches (millimeters)

Package Type: 52U

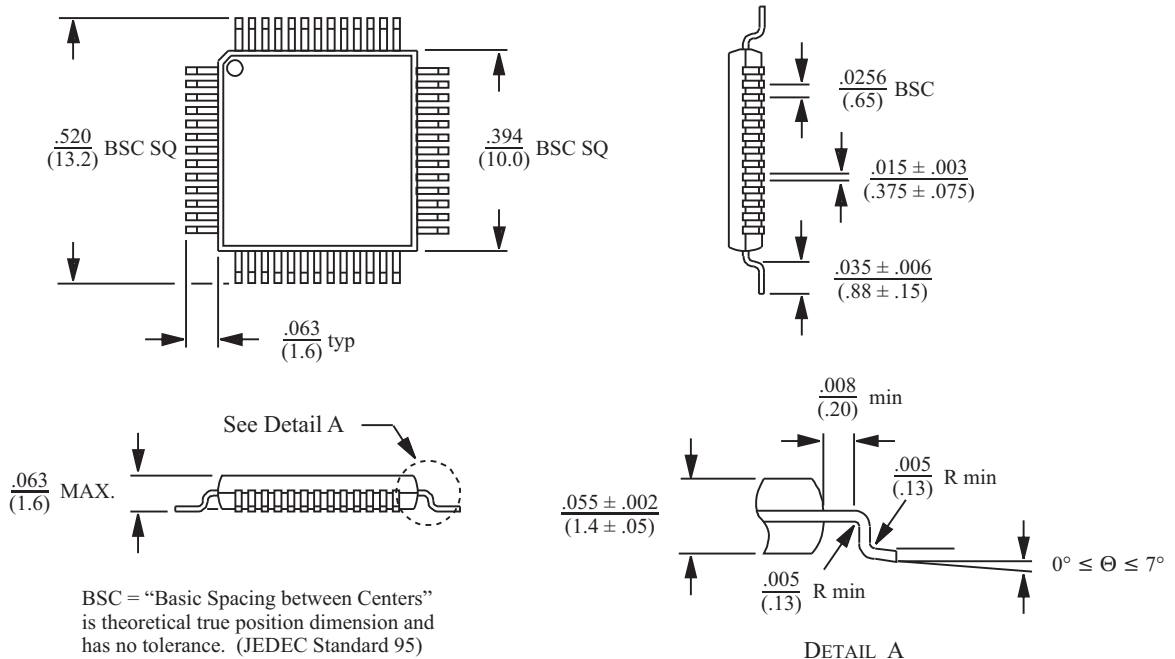


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

52-PIN PLASTIC QUAD FLAT PACK (PQFP)

inches (millimeters)

Package Type: 52PTQS



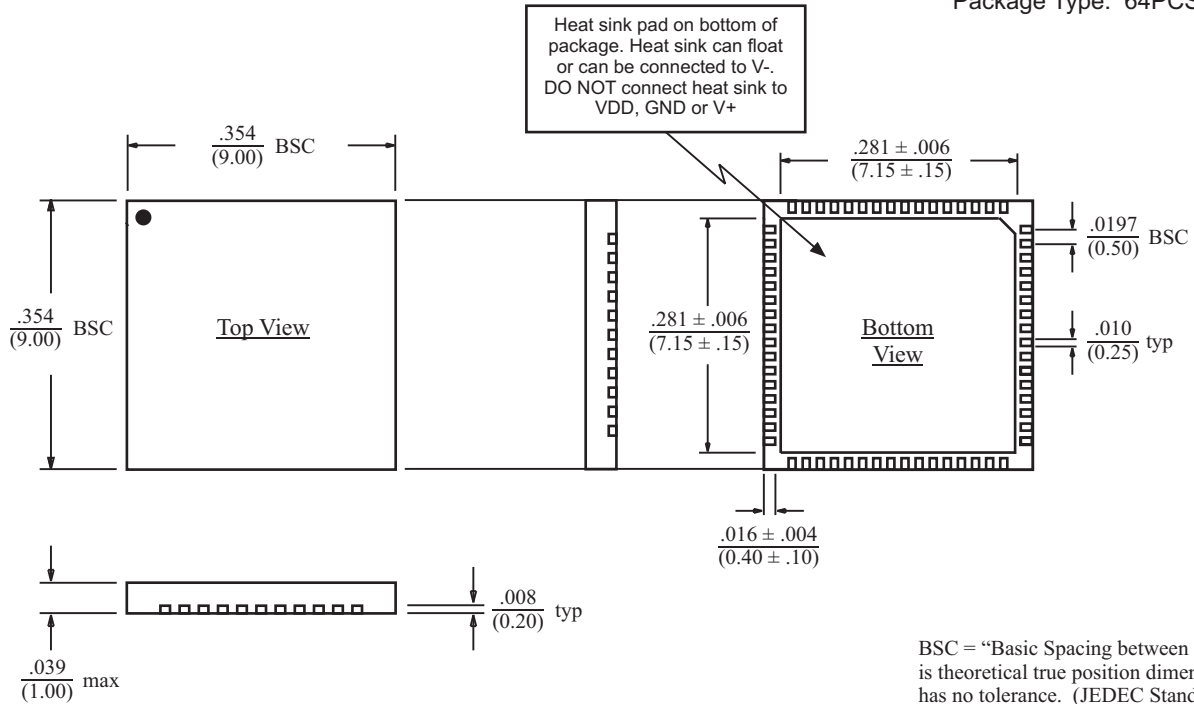
BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

DETAIL A

64-PIN PLASTIC CHIP-SCALE PACKAGE

inches (millimeters)

Package Type: 64PCS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)