HIP0060

1.5A, 50V Quad Low Side Power Driver with Serial Bus Control and Fault Protection

July 1997

Features

- Quad NDMOS Output Drivers in a High Voltage Power BiMOS Process
- Over-Stress Protection - Each Output
  - Over-Current Limiting . . . . . .1.5A Min
  - Internal Zener Drain-to-Gate Over-Voltage Clamp Protection . . . . . 50V Typ
  - Thermal Shutdown Protection
  - Open-Load Detection
- Low Quiescent Current . . . . . 10mA Max
- Serial Diagnostic Link with SPI Bus
- Diagnostic Interrupt Fault Flag
- 5V CMOS Logic Input Control
- Common Reset for Fault Bits and Output Drivers
- Ambient Operating Temperature Range. . . . . -40^{O}C to 125^{O}C

Applications

- Automotive and Industrial Systems
- Fuel Injection Drivers
- Solenoids, Relays and Lamp Drivers
- Logic and µP Controlled Drivers
- Robotic Controls

Description

The HIP0060 is a 5V logic controlled Quad Low Side Power Driver. The outputs are individually protected for over-current (OC), over-temperature (OT) and over-voltage (OV). If an OC short circuit in the output load is sensed (I_S) in one output power driver, that output current will be independently limited while the other outputs remain in operation. Over-current is limited by direct gate feedback. Over-voltage protection is provided by a drain-to-gate zener diode that clamps inductive switching pulses.

The output drivers are individually controlled through a Gate Control Latch. Temperature is sensed at each output. If a thermal fault exists, a status flag is set and the output is latched off. Open-load (OL) and over-temperature (OT) faults sets a status flag bit as diagnostic output to the SPI bus. For all fault bits (8), an ORed one-shot interrupt signal is output to the $\overline{INT}$ pin. An $\overline{RST}$ reset clears the fault flags and disables all outputs while active. The Serial Peripheral Interface (SPI) bus pins are the Serial Input (SI), Serial Output (SO), Serial Data Clock (SCK) and the Chip Select ($\overline{CS}$).

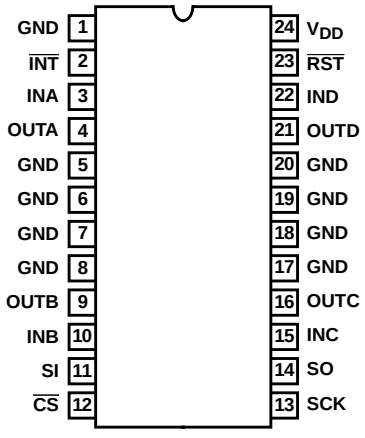
The HIP0060 is fabricated in a Power BiMOS IC process, and is intended for use in automotive and other applications having a wide range of temperature and electrical stress conditions. It is particularly suited for driving lamps, relays, and solenoids in applications where low operating power, high breakdown voltage, and higher output current at high temperatures is required.

Ordering Information

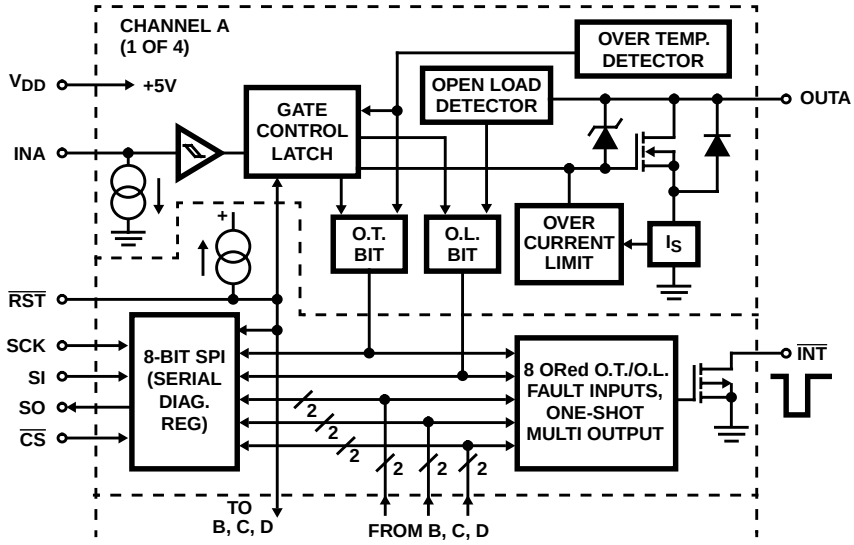
PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HIP0060AB	-40 to 125	24 Ld SOIC	M24.3

Pinout

HIP0060 (SOIC)
TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

File Number **4045**

Absolute Maximum Ratings

Max Output Voltage, V_{OUT} (Note 2) . . . . . V_{OC}
Max Output Load Current, I_{LOAD} (Per Output, Note 3) . . . . . I_{CL}
Logic Input Voltage . . . . . -0.3V to 7V
Logic Supply Voltage, V_{DD} . . . . . -0.3V to +7V

Operating Conditions

Ambient Temperature Range . . . . . -40^oC to 125^oC
Junction Temperature Range . . . . . -40^oC to 150^oC

Thermal Information

Thermal Resistance (Typical, Notes 1, 4)	θ_{JA} ($^oC/W$)
SOIC - PC Board Mount, Min. Copper	60
SOIC - PC Board Mount, 2 sq. in. Copper	35

Maximum Storage Temperature Range -55^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. The MOSFET Output Drain is internally clamped with a Drain-to-Gate zener diode that turns on the MOSFET; holding the Drain at the Output Clamp voltage V_{OC}.
3. The output drive is protected by an internal current limit. The I_{CL} over-current limiting threshold parameter specification defines the maximum current. The maximum current with all outputs ON may be further limited by dissipation.
4. Device dissipation is based on thermal resistance capability of the package in a normal operating environment. The junction to ambient thermal resistance of $60^oC/W$ is defined here as a PC Board mounted device with minimal copper. With approximately 2 square inches of copper area as a heat sink, it is practical to achieve $35^oC/W$ thermal resistance. Further reduction in the thermal resistance can be achieved with additional PC Board Copper ground area or an external heat sink structure next to the ground leads at the center of the package.

Electrical Specifications

V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = -40^oC to 125^oC; Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUTS DRIVERS (DR0 TO DR7)						
Output Channel Resistance	r_{DSON}	I_{OUT} = 0.5A	-	-	0.8	Ω
Over-Current Limiting Threshold	I_{CL}		1.5	-	3.5	A
Output Clamping Voltage	V_{OC}		40	50	60	V
Output Clamping Energy	E_{OC}	1ms Single Pulse Width, T_A = 25^oC, (Refer to Figure 3 for SOA Limits).	-	85	-	mJ
Output OFF Leakage Current	I_{LK}	V_{OUT} = 14.5V	-	-	180	µA
Open-Load Fault Threshold	R_{OLD}	V_{OUT} = 14.5V, Output Off	4	-	200	kΩ
Output Rise Time	t_R	R_L = 30Ω, V_{OUT} = 14.5V	1	-	12	µs
Output Fall Time	t_F	R_L = 30Ω, V_{OUT} = 14.5V	1	-	12	µs
Turn-On Delay	t_{ON}	R_L = 30Ω, V_{OUT} = 14.5V	-	-	12	µs
Turn-Off Delay	t_{OFF}	R_L = 30Ω, V_{OUT} = 14.5V	-	-	12	µs
POWER SUPPLY						
Power On Reset Threshold	$V_{DD(POR)}$		3.2	-	4.4	V
V_{DD} Logic Supply Current	I_{DD}	All Outputs ON or OFF	-	-	10	mA
LOGIC INPUTS (INx, SI, SCK, $\overline{RST}$, $\overline{CS}$)						
High Level Input Voltage	V_{IH}		$0.7xV_{DD}$	-	-	V
Low Level Input Voltage	V_{IL}		-	-	$0.2xV_{DD}$	V
Input Hysteresis	V_{ILHYS}		0.8	-	-	V
High Output Voltage, SO, $\overline{INT}$	V_{OL}	Current Sink = 1.6mA	-	-	0.4	V
Low Output Voltage, SO	V_{OH}	Current Source = -0.8mA	V_{DD}-0.8	-	-	V
Input Pull-Down Current, INx	I_{INPD}		75	-	250	µA
Reset Input Pull-Up Current, $\overline{RST}$	I_{RPU}		20	-	120	µA

Electrical Specifications V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = -40°C to 125°C; Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIAGNOSTIC						
Pulse Width, $\overline{INT}$	$t_{\overline{INT}}$		3	-	25	µs
Fault Response Time	t_{FAULT}		-	-	16	µs
OVER-TEMPERATURE PROTECTION						
Over-Temperature Shutdown	T_{SD}		160	-	-	°C
SERIAL PERIPHERAL INTERFACE TIMING	(Capacitance Each Pin, C_L = 200pF)					
SCK Period	t_{CYC}		500	-	-	ns
SCK Clock High/Low Time	t_{WSCKH}, t_{WSCKL}		200	-	-	ns
SCK Rise/Fall Time	t_{rSCK}, t_{fSCK}		-	-	30	ns
Enable Lead/Lag Time	t_{LEAD}, t_{LAG}		250	-	-	ns
Output Data Valid Time	t_V		-	-	170	ns
Data Setup Time	t_{SU}		-	-	30	ns
Disable Time	t_{DIS}		-	-	250	ns

Description of Diagnostics

OC (Over-Current) Fault Mode

In a short circuit or over-current fault condition when an output is switched on, the output current is limited to the I_{CL} maximum as defined in the Electrical Specifications. An OC fault condition does not shutdown the output. The current is sensed and feedback is directed to the gate of the MOS Output Driver. The gate voltage is reduced to maintained the specified level of current limiting. In this mode, the drain voltage will increase and cause increased dissipation.

OT (Over-Temperature) Fault Mode

Under a high dissipation over-temperature fault condition, the output temperature is detected and compared to a preset threshold level. When the OT threshold is exceeded, thermal shutdown for that output occurs. The Gate Control Latch drive to the output is switched off and a status flag (the OT Bit) for the fault is set. The output shutdown action is independent of the IN input state. However, the Gate Control Latch and OL Bit will be reset on the next rising edge of the IN input and, if the fault still exists, the shutdown action will repeat.

Diagnostic action for an OT fault includes feedback of the fault status to the Serial Diagnostic Register for a SPI bus data output. Also, as shown in the Block Diagram, the OT fault status bit information is ORed into a one-shot that drives an open drain to provide an $\overline{INT}$ interrupt signal output. The $\overline{INT}$ output has a specified timing from the one-shot multi and is defined in the Electrical Specifications as t_{INT}.

OL (Open-Load) Fault Mode

An open-load fault mode sequence consists of setting a status flag (the OL Bit) when an output open load condition is detected. If the output impedance is greater than a preset threshold, as detected when the input is off; the status bit is set. The OL Bit is reset on the next falling edge of the IN input signal. The off-on detection sequence will repeat as long as the output impedance is higher than the detection threshold, as detected in the off state.

Diagnostic action for an OL fault mode differs from the OT fault mode by not forcing an output shutdown through the Gate Controlled Latch. Also, because the OL fault is detected in the off state, the status flag is reset on the falling edge of the input instead of the rising edge. The OL output information to the Serial Diagnostic Register and the $\overline{INT}$ pin is the same as the OT fault mode action.

ORed Fault Bits

It is important to note that the trigger input to the one-shot is locked-out for the t_{INT} duration and any fault that may have occurred in the t_{INT} window will not be displayed at the $\overline{INT}$ output. However, all 8 fault bits may still be read as data from the SO output when clock by the SCK input. The $\overline{INT}$ fault output is provided as an interrupt signal to flag the immediate occurrence of a fault and take appropriate action as defined by the microcontroller to the SPI bus and the users programming. The $\overline{INT}$ fault output may be ORed with other ICs to provide a system microcontroller interrupt to indicate the presence of a fault.

Serial Diagnostic Link

A serial diagnostic link via the SPI bus provides the means to clock fault data in and out of the fault register to the microcontroller. When the microcontroller receives an $\overline{INT}$ interrupt signal, data is clocked from the Serial Diagnostic Register to determine what fault bit has been set. Appropriate action for the fault may then be taken, as defined by the programming of the microcontroller.

Serial Diagnostic Register

Fault bits consist of one OT bit and one OL bit for each switching channel (A, B, C and D). Data is transferred out of SO MSB first on the rising edge of SCK after $\overline{CS}$ goes low. Data is shifted into the input shift register on the falling edge of SCK. The defined order of the DO0 to DO7 fault bits is as follows:

BIT	NAME	CONDITION REQUIRED TO SET BIT
DO0	OTA	OT in Output Driver A, $T_J \geq T_{LIM}$
DO1	OTB	OT in Output Driver B, $T_J \geq T_{LIM}$
DO2	OTC	OT in Output Driver C, $T_J \geq T_{LIM}$
DO3	OTD	OT in Output Driver D, $T_J \geq T_{LIM}$
DO4	OLA	OL in Output Driver A, OFF Load > R_{OLD}
DO5	OLB	OL in Output Driver B, OFF Load > R_{OLD}
DO6	OLC	OL in Output Driver C, OFF Load > R_{OLD}
DO7	OLD	OL in Output Driver D, OFF Load > R_{OLD}

HIP0060 devices may be linked in cascade for the purposes of SPI control. Serial data is clocked in and out of each HIP0060 and then back to the host microcontroller. All linked devices have a common control sequence. When $\overline{CS}$ goes low, fault data is shifted to the Serial Diagnostic Register. SCK must be low when $\overline{CS}$ goes low. Also, when $\overline{CS}$ goes low, SO changes from a three-state to a low state and remains low until SCK goes high. Serial data is transferred by SCK. After the serial data is transferred, SCK must remain low as $\overline{CS}$ goes high. The serial data transfer must be a continuous sequence while $\overline{CS}$ is low.

Serial Peripheral Interface

The Serial Peripheral Interface (SPI) bus is system controlled by a host micro. The SPI bus controls the Serial Diagnostic Link with the $\overline{CS}$ (Chip Select), SCK, SI, SO and $\overline{RST}$ (Reset) lines. Figures 4 and 5 define the timing and protocol for the bus.

Reset Operation

The $\overline{RST}$ input is an active low reset input. When $\overline{RST}$ is low, the internal diagnostic flags are cleared but not the shift register. When $\overline{RST}$ is low, all outputs and output switches are disabled. To clear the shift register, $\overline{CS}$ is switched from high to low during or after a reset while there are no active faults, jamming data from the cleared fault flags into the shift register. The $\overline{RST}$ input has an internal pull-up to sustain a logic high when floating.

The V_{DD} input is the power supply to the 5V logic and the POR function. When the V_{DD} is less than the $V_{DD(POR)}$ threshold, the output drivers are shutoff. To insure that the diagnostic link shift register is correct after V_{DD} is less than $V_{DD(POR)}$, a manual reset must be executed.

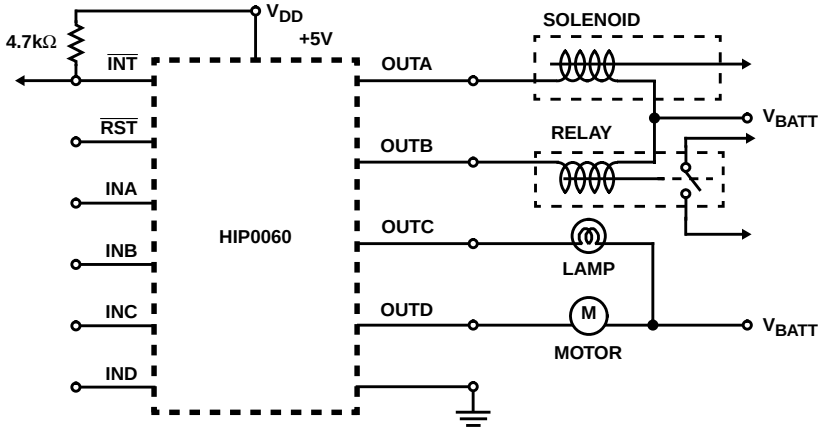


FIGURE 1. TYPICAL HIP0060 APPLICATION AS A LOW SIDE SWITCH FOR INDUCTIVE LOADS, LAMPS AND SMALL LINEAR MOTORS OR STEPPER MOTORS

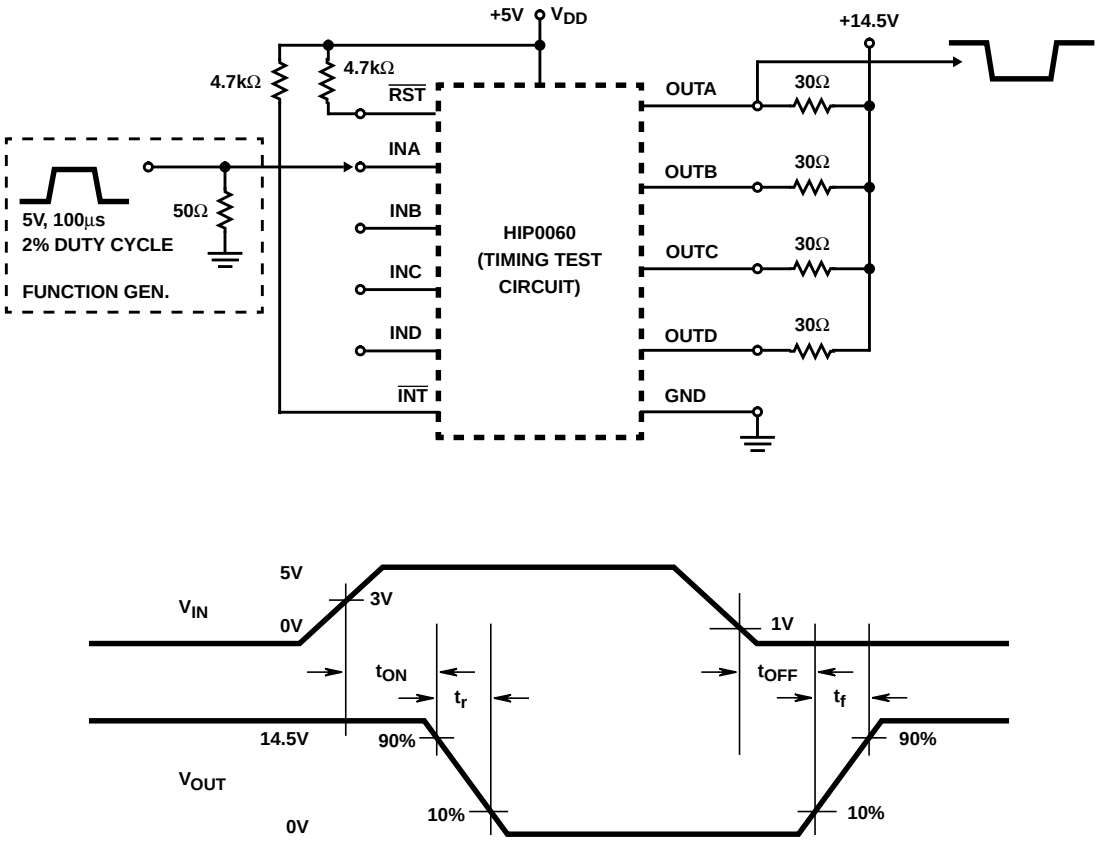


FIGURE 2. INPUT TO OUTPUT SWITCHING TIME DIAGRAM FOR EACH SWITCHING CHANNEL. THE CONDITIONS SHOWN REFER TO THE TIMING TEST CIRCUIT

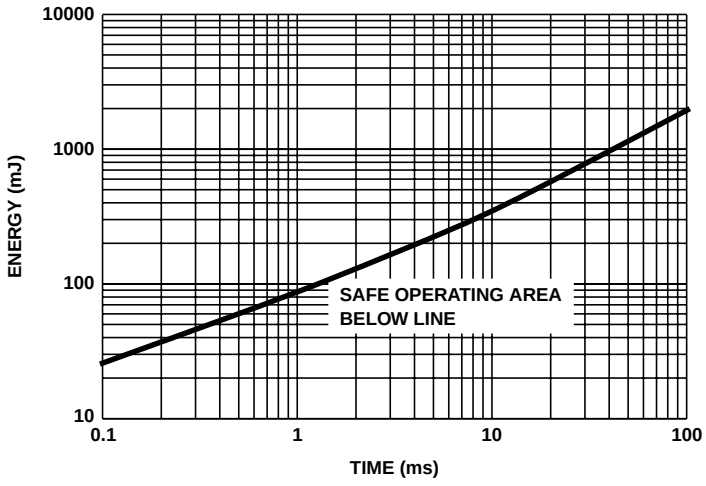


FIGURE 3. MAXIMUM SINGLE PULSE ENERGY SAFE OPERATING AREA FOR EACH CLAMPED OUTPUT DRIVER, $T_A = 25^oC$

Timing Diagrams

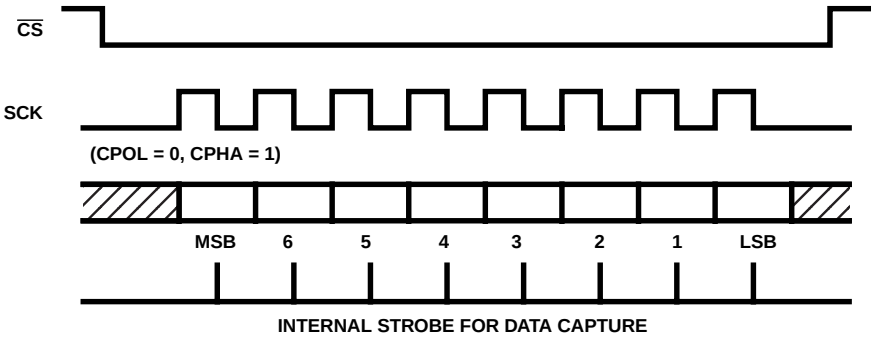


FIGURE 4. DATA AND CLOCK TIMING DIAGRAM

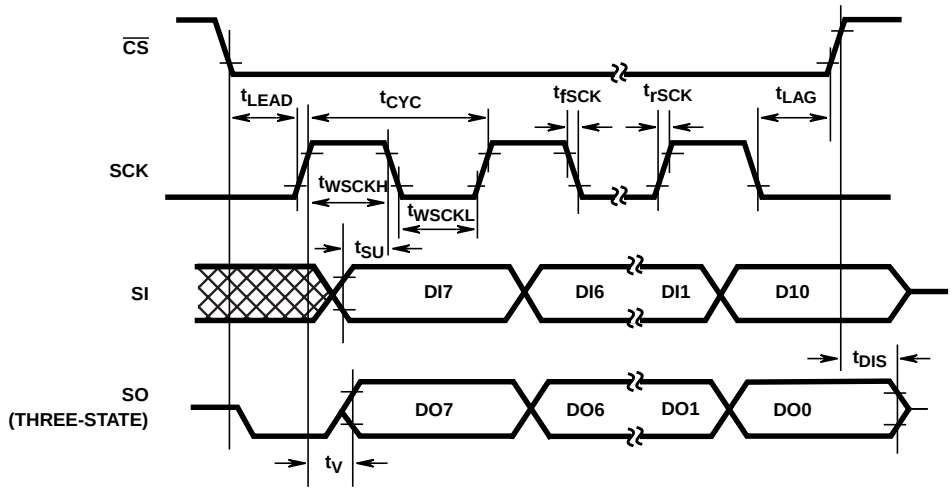
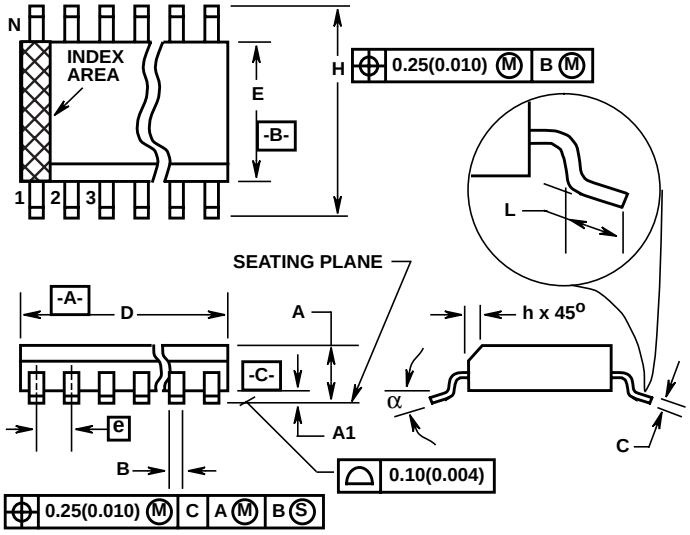


FIGURE 5. BYTE TIMING DIAGRAM WITH ASYNCHRONOUS RESET. REFER TO THE ELECTRICAL SPECIFICATION FOR THE HIGH AND LOW INPUT AND OUTPUT THRESHOLD LEVELS SHOWN FOR TIMING REFERENCE

Small Outline Plastic Packages (SOIC)



M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact