DATA SHEET

UAA3535HL
Low power GSM/DCS/PCS multi-band transceiver

Objective specification
File under Integrated Circuits, IC17

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Philips Semiconductors

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Low power GSM/DCS/PCS multi-band transceiver UAA3535HL

FEATURES

- Multi-band application for GSM, DCS and PCS cellular phone systems
- Low noise and wide dynamic range low IF receiver
- More than 35 dB on-chip image rejection in receive mode
- More than 64 dB gain control range in receive mode
- Integrated channel filter
- Integrated TX low-pass filter
- High precision I/Q modulator
- Multi-band TX modulation loop architecture including offset mixer and phase-frequency detector
- Dual PLL with on-chip fully integrated IF VCO
- Fully differential design minimizing crosstalk and spurious signals
- Functional down to 2.4 V and up to 3.6 V
- 3-wire serial bus interface
- LQFP48 package.

APPLICATIONS

- GSM 900 MHz, DCS 1800 MHz and PCS 1900 MHz hand-held transceivers.

GENERAL DESCRIPTION

The UAA3535HL is intended for Global Systems for Mobile communication (GSM), Digital Cellular communication Systems (DCS) and Personal Communication Services (PCS). The circuit integrates the receiver and most of the transmitter section of hand-held transceivers for these applications.

The receiver consists of two sections. The first section is the RF receiver front-end, which amplifies the GSM, DCS or PCS aerial signal, then converts the chosen channel down to a low Intermediate Frequency (IF) of 100 kHz, and also provides more than 35 dB image suppression. Some selectivity is provided at this stage by an on-chip low-pass filter and channel selectivity is provided by a high performance integrated band-pass filter.

The second section is the IF section, which further amplifies the chosen channel and performs gain control to adjust the output level to the desired value. The IF gain can be varied over more than 64 dB gain range.

The transmitter also consists of two sections. The first is a high precision I/Q modulator which converts the baseband modulation up to the transmit IF. The second is a modulation loop architecture which converts the signal to RF.

The Local Oscillator (LO) signals are provided by an on-chip Voltage Controlled Oscillator (VCO) for operation of the IF section and are provided externally for operation of the RF section. The frequencies of the RF and IF VCOs are set by internal PLL circuits, which are programmable via a 3-wire serial bus. Comparison frequencies are 200 kHz (100 kHz step programmability) and 13 MHz for the RF and IF PLL respectively, and are derived from a 13 MHz reference signal which has to be supplied externally. The quadrature-phase RF LO signals required for I/Q mixers in reception are generated internally. The quadrature LO signals required for operation of the I/Q modulator are generated inside the IF VCO.

The circuit can be powered-up into one of three different modes: RX, TX or SYN mode, depending on the logic state of pins RXON, TXON and SYNON, respectively. It is also possible to set the IC in one of these modes by software, using the 3-wire bus serial programming. In RX (TX) mode, all sections required for receive (transmit) are turned on. The SYN mode is used to power-up the synthesizers prior to the RX or TX mode. In the SYN mode, some internal LO buffers are also powered-up in such a way that VCO pulling is minimized when switching on the receiver or the transmitter. Additional band selection is done using the 3-wire bus serial programming, allowing the required enabling of the Low Noise Amplifiers (LNAs) and charge pumps current programming.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA3535HL	LQFP48	plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4$ mm	SOT313-2

BLOCK DIAGRAM

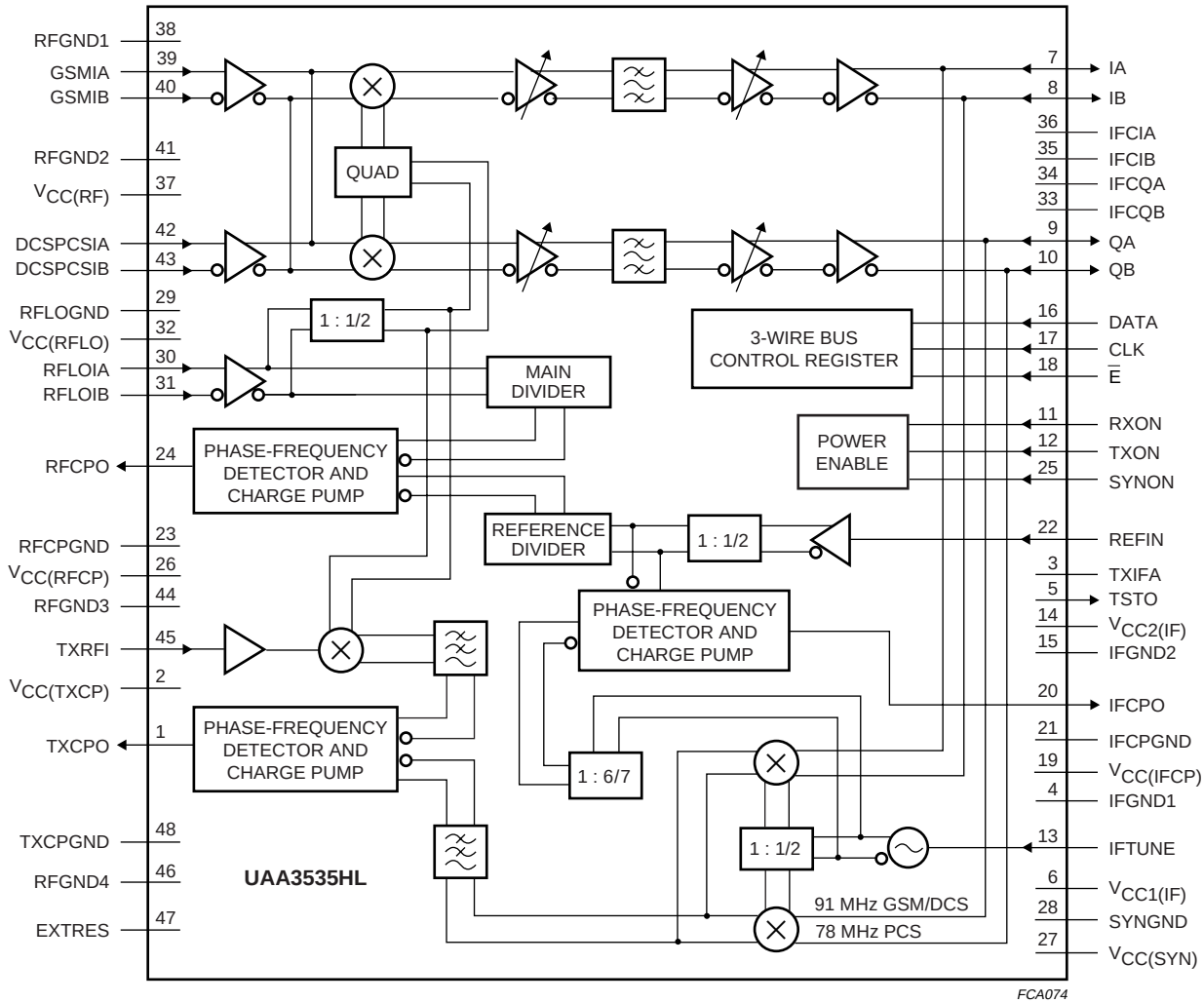


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TXCPO	1	transmit modulation loop GSM charge pump output
$V_{CC(TXCP)}$	2	transmit modulation loop charge pump supply voltage
TXIFA	3	transmit IF test pin
IFGND1	4	IF ground 1
TSTO	5	test mode output
$V_{CC1(IF)}$	6	IF supply voltage 1
IA	7	I path A baseband input/output
IB	8	I path B baseband input/output
QA	9	Q path A baseband input/output
QB	10	Q path B baseband input/output
RXON	11	RX mode control input
TXON	12	TX mode control input
IFTUNE	13	transmit IF VCO tune input
$V_{CC2(IF)}$	14	IF supply voltage 2
IFGND2	15	IF ground 2
DATA	16	3-wire bus data input
CLK	17	3-wire bus clock input
$\overline{E}$	18	3-wire bus enable control input (active LOW)
$V_{CC(IFCP)}$	19	transmit IF charge pump supply voltage
IFCPO	20	transmit IF charge pump output
IFCPGND	21	transmit IF charge pump ground
REFIN	22	synthesizers reference input
RFCPGND	23	RF charge pump ground
RFCPO	24	RF charge pump output
SYNON	25	SYN mode control input
$V_{CC(RFCP)}$	26	RF charge pump supply voltage
$V_{CC(SYN)}$	27	synthesizers supply voltage
SYNGND	28	synthesizers ground
RFLOGND	29	RF LO ground
RFLOIA	30	RF LO input A
RFLOIB	31	RF LO input B
$V_{CC(RFLO)}$	32	RF LO supply voltage
IFCQB	33	RX IF Q test pin B
IFCQA	34	RX IF Q test pin A
IFCIB	35	RX IF I test pin B
IFCIA	36	RX IF I test pin A
$V_{CC(RF)}$	37	RF front-end and transmit modulation loop supply voltage
RFGND1	38	RF front-end and transmit modulation loop ground 1
GSMIA	39	receiver GSM RF input A
GSMIB	40	receiver GSM RF input B
RFGND2	41	RF front-end and transmit modulation loop ground 2
DCSPCSIA	42	receiver DCS/PCS RF input A
DCSPCSIB	43	receiver DCS/PCS RF input B
RFGND3	44	RF front-end and transmit modulation loop ground 3
TXRFI	45	input from RF transmit VCOs
RFGND4	46	RF front-end and transmit modulation loop ground 4
EXTRES	47	reference resistor for transmit modulation loop
TXCPGND	48	transmit modulation loop charge pump ground

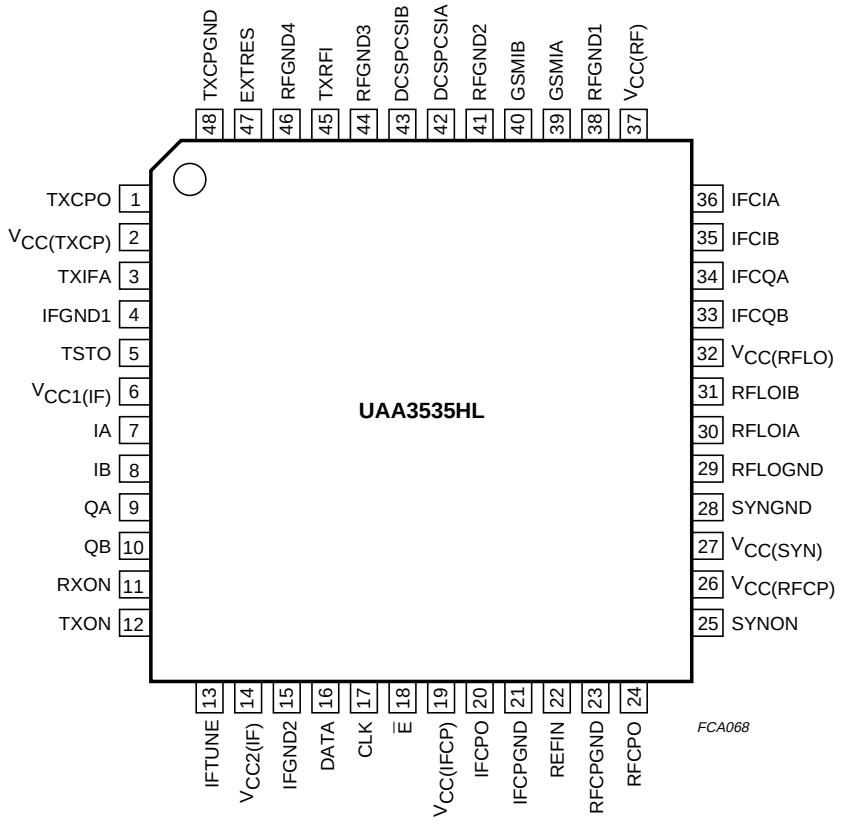


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

RF receiver

The receiver front-end converts the aerial RF signal from EGSM (Extended GSM; 925 to 960 MHz), DCS (1805 to 1880 MHz) or PCS (1930 to 1990 MHz) bands down to an IF signal of 100 kHz. The first stages are symmetrical LNAs that are matched to 50 Ω using external baluns. The LNAs are followed by an I/Q down-mixer. The I/Q down-mixer consists of two mixers in parallel but driven by quadrature out of phase LO signals.
The In-phase (I) and Quadrature- phase (Q) IF signals are then low-pass filtered to provide protection from high frequency offset interferers. The IF I and Q signals are then fed into the channel filter.

Channel filter and AGC

The front-end IF I and Q outputs are first applied to an amplifier circuit with provision for three 8 dB gain step adjustment possibilities and then to an integrated band-pass channel filter. The filter is a fifth-order band-pass filter centred around 100 with 220 kHz bandwidth. After filtering the IF I and Q signals are further amplified with provision for eleven 4 dB gain steps and DC offset compensation.

I/Q modulator

I and Q baseband signals are applied to the I/Q modulator where the modulation spectrum is shifted up to the transmit IF frequency. For low harmonic distortion, low carrier leakage and high image rejection, the phase error must be kept as small as possible. The IF output of the modulator is fed to an integrated low-pass filter where unwanted spurious signals are suppressed, prior to being fed to the phase detector.

Transmit modulation loop

The analog transmit modulation loop consists of an on-chip offset mixer, a phase-frequency detector, an off-chip loop filter and a transmit VCO. The analog PLL copies the modulation to the off-chip transmit VCO and acts as a tracking filter. A PLL of at least third-order is required to meet noise requirements at 20 MHz offset from the carrier. The PLL bandwidth must be greater than 600 kHz in order to keep a low dynamic phase error and to minimize the acquisition time.

RF and IF LO sections

The RF LO input covering the 1788 to 2002 MHz bandwidth is connected to an external RF VCO module. The RF LO section includes the LO buffering for the RF PLL, a divider-by-2 or 1 for GSM and DCS/PCS respectively which drives a quadrature generation network for use in the RX I/Q down-mixer or the transmit modulation loop offset mixer. The IF LO section consists of a fully integrated IF VCO which internally provides the I/Q modulator with the necessary quadrature signals.

Dual PLL

A high performance dual PLL is included on-chip which enables the frequencies of the RF VCO to be synthesized off-chip and that of the IF VCO on-chip. Very low close-in phase noise is achieved which allows the PLL loop bandwidth to be widened to achieve a shorter settling time. The charge pump circuit has very low leakage current, in the nA range, so that the spurious signals are hardly detectable.

The ‘main’ path consists of a programmable divider chain that divides the RF and IF LO signals down to frequencies of 200 kHz (100 kHz step programmability) and 13 MHz respectively. Their phase is then compared in a digital Phase-Frequency Detector (PFD) with that of a reference signal derived from an external 13 or 26 MHz clock signal. The phase error information is fed back to the VCO via the charge pump circuit that ‘sinks’ into or ‘sources’ current from the loop filter capacitor, thereby changing the VCO frequency so that the loop becomes ‘phase locked’.

Operating modes

Basic operating modes

The circuit can be powered-up into different operating modes depending on the voltage level applied at pins RXON, TXON and SYNON (hardware control). This defines the three main modes; RX, TX and SYN. Table 1 describes the different operating modes as defined by hardware control.

The operation mode status depends on the control bits SYNON, RXON and TXON (see Table 1).

When the receiver is on, it is possible to switch-off the low noise amplifier to perform DC offset compensation in the receiver (see Section “LNA power control”).

When in TX mode, it is possible to enable the IF synthesizer and VCO independently from the rest of the TX section via bit TXIFON via the control bus.

Table 1 Basic operating mode control

MODE	CONTROL PIN LEVEL			POWER STATUS		
	SYNON	RXON	TXON	SYNTHESIZER	RECEIVER	TRANSMITTER
SYN	HIGH	LOW	LOW	on	off	off
RX	HIGH	HIGH	LOW	on	on	off
TX	HIGH	LOW	HIGH	on	off	on
Idle	LOW	LOW	LOW	off	off	off

IF SYNTHESIZER AND VCO CONTROL

The IF synthesizer is only necessary in transmit mode. The TX IF VCO and synthesizer section can be powered-up with the control bit TXIFON; see Table 2. If TXIFON is not used, the IF VCO and synthesizer section will be enabled with the signal TXON.

Table 2 IF synthesizer and VCO power control

BIT TXIFON	IF SYNTHESIZER AND VCO MODE
0	off
1	on

LNA POWER CONTROL

When the receiver is on, it is possible to switch-off the low noise amplifier separately. Separate control of the low noise amplifier is accomplished by the control bit LNA; see Table 3.

Table 3 LNA power control

BIT LNA	LNA MODE
0	off
1	on

BAND SELECTION CONTROL

The receiver includes two RF front-end and RF LO sections; one for GSM where the RF LO is divided-by-2 and fed to the 925 to 960 MHz front-end, and the other one for DCS and/or PCS where the RF LO is not divided and fed to the 1805 to 1990 MHz front-end. The selection of these 2 modes is accomplished by the control bit BND; see Table 4.

Table 4 Band selection control

BIT BND	BAND MODE
0	GSM
1	DCS and/or PCS

SIDEBAND SELECTION CONTROL

The receiver includes an image rejection front-end which allows the use of a RF LO 100 kHz below the RF input frequency (infradyne) or 100 kHz above the RF input frequency (supradyne). Between these two states the proper image should be selected for rejection.
The selection of these 2 modes is accomplished by the control bit SBD; see Table 5.

Table 5 Sideband selection control

BIT SBD	SIDEBAND MODE
0	supradyne
1	infradyne

TX CHARGE PUMP CURRENT CONTROL

The transmit modulation loop includes a transmit charge pump where sink and source currents are determined by an external resistor. When determined, this nominal current can be divided-by-1 or 2 to cope with different transmit VCO gains. The selection of these 2 modes is accomplished by the control bit TXI; see Table 6.

Table 6 TX charge pump current control

BIT TXI	TX CHARGE PUMP CURRENT MODE
0	nominal current
1	nominal current divided-by-2

REFERENCE DIVIDER CONTROL

The reference divider can be programmed to divide the external reference frequency by 65 or 130. The selection of these 2 modes is accomplished by the control bit REFDIV; see Table 7.

Table 7 Reference divider control

BIT REFDIV	REFERENCE DIVIDER MODE
0	divide-by-65
1	divide-by-130

IF DIVIDER CONTROL

The IF divider can be programmed to divide the integrated IF VCO frequency by 1 or 2. The selection of these 2 modes is accomplished by the control bit IFDIV; see Table 8.

Table 8 IF divider control

BIT IFDIV	IF DIVIDER MODE
0	IF = f_{VCO}
1	IF = f_{VCO} divided by 2

TXIF FILTER CONTROL

The transmit section integrates two switchable low-pass filters, one for a 45.5 MHz IF and the other one for 91 MHz IF. The selection of these 2 modes is accomplished by the control bit FILT; see Table 9.

Table 9 TXIF filter control

BIT FILT	TXIF FILTER MODE
0	IF 45.5 MHz
1	IF 91 MHz

IF SYNTHESIZER DIVIDER CONTROL

The IF synthesizer divider can be programmed to divide the semi-integrated IF VCO frequency by 6 or 7. The selection of these 2 modes is accomplished by the control bit IFO; see Table 10.

Table 10 IF synthesizer divider control

BIT IFO	IF SYNTHESIZER DIVIDER MODE
0	divide-by-6
1	divide-by-7

Programming

SERIAL PROGRAMMING BUS

A simple 3-wire unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. This is allowed when CLK is in either state without causing any consequences to the register data. Only the last 17 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power-down of both synthesizers.

DATA FORMAT

Data is entered with the most significant bit first.
The leading bits make up the data field, while the trailing 4 bits are an address field. The address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch. To ensure that data is correctly loaded on first power-up, $\overline{E}$ should be held LOW and only taken High after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is inhibited during the period when data is read by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer.

The allocation of the register bits is given in Table 11.

REGISTER PRESET CONDITIONS

The UAA3535HL programming registers have a preset state. The preset values can be found in Table 12. Conditions for guaranteed preset values at power-on are as follows:

- DATA, CLOCK, $\overline{E}$, SYNON, RXON and TXON must be at 0 V
- Preset value is guaranteed 2 ms after $V_{CC(SYN)}$ rises to 90% of 2.6 V
- $\overline{E}$ should stay at 0 V up to the end of the first programming word.

Table 11 Register bit allocation; notes 1 and 2 and 3

REGISTER ALLOCATION																				
DATA FIELD																	ADDRESS FIELD			
BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	LAST 4 BITS			
X	X	RF 14	RF 13	RF 12	RF 11	RF 10	RF 9	RF 8	RF 7	RF 6	RF 5	RF 4	RF 3	RF 2	RF 1	RF 0	0	0	1	1
X	X	X	X	X	0	0	0	0	0	LNA	G5	G4	G3	G2	G1	G0	0	0	1	0
X	X	X	0	FILT	REF DIV	IFO	IF DIV	TXI	SBD	BND	1	1	TXIF ON	SYN ON	RX ON	TX ON	0	0	0	1
for test purpose only; bit usage to be defined; this is a forbidden address																	0	0	0	0

Notes

1. The 15-bit RF divider is programmable through the 15 bits RF0 to RF14, in steps of 100 kHz.
2. X = don’t care.
3. The 6-bit AGC attenuator is programmable through the 6 bits G0 to G5 in 17 steps of 4 dB (see Table 13).

Table 12 Preset values; note 1

REGISTER ALLOCATION																				
DATA FIELD																	ADDRESS FIELD			
BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	LAST 4 BITS			
X	X	1	0	0	1	0	1	0	0	0	0	0	0	1	1	0	0	0	1	1
X	X	X	X	X	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1	0
X	X	X	0	0	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	1
for test purpose only; bit usage to be defined; this is a forbidden address																	0	0	0	0

Note

1. X = don’t care.

Table 13 AGC gain look-up table; note 1

G5[2]	G4[2]	G3	G2	G1	G0	ATTENUATION (dB)[3]
1	1	1	1	1	1	0
1	1	1	1	1	0	4
1	0	1	1	1	1	8
1	0	1	1	1	0	12
0	1	1	1	1	1	16
0	1	1	1	1	0	20
0	1	1	1	0	1	24
0	1	1	1	0	0	28
0	1	0	1	1	1	32
0	1	0	1	1	0	36
0	0	0	1	1	1	40
0	0	0	1	1	0	44
0	0	0	1	0	1	48
0	0	0	1	0	0	52
0	0	0	0	1	1	56
0	0	0	0	1	0	60
0	0	0	0	0	1	64
0	0	0	0	0	0	68

Notes

1. Codes not included in the table are forbidden.
2. Steps at the input of the band-pass filter.
3. The figure represents the total attenuation in the receive path, with respect to the maximum gain.

LIMITING VALUES

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	+3.6	V
$V_{CC(TXCP)}$; $V_{CC(RFCP)}$	supply voltage for RX and TX charge pumps	–0.3	+4.25	V
P_{max}	maximum power dissipation	–	1	W
T_{amb}	ambient temperature	–30	+70	°C
T_{stg}	storage temperature	–40	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case	65	K/W

DC CHARACTERISTICS

$V_{CC} = V_{CC(TXCP)} = V_{CC(RFCP)} = 2.6$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CC}	supply current	normal mode; total power-down; note 1	–	10	50	μA
		preset mode; total power-down; note 2	–	100	200	μA
		RX and SYN mode	–	51.5	60	mA
		TX, TXIF and SYN mode	–	54	66	mA
		SYN mode	–	17	20	mA
		TXIF and SYN mode	–	29	37	mA
$V_{CC(RF)}$	RF front-end and transmit modulation loop supply voltage		2.4	–	3.3	V
$I_{CC(RF)}$	RF front-end and transmit modulation loop supply current	RX mode; one LNA and quadrature mixer active	–	17	–	mA
		RX mode; one LNA active	–	6	–	mA
		TX mode; transmit modulation loop active without charge pump	–	6	–	mA
$V_{CC1(IF)}$	IF supply voltage 1		2.4	–	3.3	V
$I_{CC1(IF)}$	IF supply current 1	RX mode; I/Q low IF band-pass filter active	–	7	–	mA
		TX mode; I/Q modulator active	–	9	–	mA
$V_{CC2(IF)}$	IF supply voltage 2		2.4	–	3.3	V
$I_{CC2(IF)}$	IF supply current 2	RX mode; I/Q AGC active	–	4	–	mA
		TXIF mode; TX IF VCO active	–	9	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC(RFLO)}$	RF LO supply voltage		2.4	–	3.3	V
$I_{CC(RFLO)}$	RF LO supply current	RX and SYN mode; RF LO buffer and divider section active	–	10	–	mA
		TX and SYN mode; RF LO buffer and divider section active	–	10	–	mA
		SYN mode; RF LO buffer active	–	6	–	mA
$V_{CC(SYN)}$	synthesizers supply voltage		2.4	–	3.3	V
$I_{CC(SYN)}$	synthesizers supply current	SYN mode; RF synthesizer active	–	9.5	–	mA
		TXIF mode; IF synthesizer active	–	0.5	–	mA
$V_{CC(IFCP)}$	transmit IF charge pump supply voltage		2.4	–	3.3	V
$I_{CC(IFCP)}$	transmit IF charge pump supply current	TXIF mode; IF LO charge pump active; in lock	–	1.5	–	mA
$V_{CC(TXCP)}$	transmit modulation loop charge pump supply voltage		2.4	–	4.25	V
$I_{CC(TXCP)}$	transmit modulation loop charge pump supply current	TX mode; TX RF charge pump active; in lock; external resistance is 1800 Ω	–	1.0	–	mA
$V_{CC(RFCP)}$	RF charge pump supply voltage		2.4	–	4.25	V
$I_{CC(RFCP)}$	RF charge pump supply current	SYN mode; RF LO charge pump active; in lock	–	4.5	–	mA
Baseband section: pins IA, IB, QA and QB						
$V_{I(CM)}$	common mode input-output voltage I	$V_I = \frac{V_{IA} + V_{IB}}{2}$	1.15	1.25	1.35	V
$V_{Q(CM)}$	common mode input-output voltage Q	$V_Q = \frac{V_{QA} + V_{QB}}{2}$	1.15	1.25	1.35	V
Logic input levels: pins DATA, CLK, $\overline{E}$, TXON, RXON and SYNON						
V_{IH}	HIGH-level input voltage		0.9	–	–	V
V_{IL}	LOW-level input voltage		–	–	0.3	V

Notes

1. $V_{CC(TXCP)} = V_{CC(RFCP)} = 4.2$ V; pins TXON, RXON and SYNON are HIGH impedance; pins DATA, CLK and $\overline{E}$ are HIGH impedance.
2. $V_{CC(TXCP)} = V_{CC(RFCP)} = 4.2$ V; pins TXON, RXON and SYNON are LOW; pins DATA, CLK and $\overline{E}$ are HIGH.

AC CHARACTERISTICS

$V_{CC} = V_{CC(CP)} = 2.6$ V; $T_{amb} = -30$ to $+70$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF receiver section; measured in a 50 Ω impedance system, including external input baluns and matching networks to 50 Ω						
PINS: GSMIA AND GSMIB						
$f_{i(RF)}$	RF input frequency		925	–	960	MHz
$R_{i(dif)}$	differential input resistance	parallel RC input model	–	75	–	Ω
$C_{i(dif)}$	differential input capacitance	parallel RC input model	–	1.5	–	pF
F	noise figure	for R_i; maximum AGC; notes 1 and 2	–	3.5	4	dB
α_{off}	LNA off-state attenuation	bit LNA = 0; note 1	–	45	–	dB
P_{off}	LNA off-state power handling	bit LNA = 0; notes 1 and 3	3	–	–	dBm
$DES3_i$	input referred 3 dB desensitization	Δf = 3 MHz; T_{amb} = 25 °C; note 1	–25	–	–	dBm
PINS: DCSPCSIA AND DCSPCSIB						
$f_{i(RF)}$	RF input frequency		1805	–	1990	MHz
$R_{i(dif)}$	differential input resistance	parallel RC input model	–	120	–	Ω
$C_{i(dif)}$	differential input capacitance	parallel RC input model	–	1.0	–	pF
F	noise figure	for R_i; maximum AGC; notes 1 and 2	–	4	4.5	dB
α_{off}	LNA off-state attenuation	bit LNA = 0; note 1	–	45	–	dB
P_{off}	LNA off-state power handling	bit LNA = 0; notes 1 and 3	6	–	–	dBm
$DES3_i$	input referred 3 dB desensitization	Δf = 3 MHz; T_{amb} = 25 °C; note 1	–28	–	–	dBm
PINS: GSMIA, GSMIB, DCSPCSIA AND DCSPCSIB						
s_{11}	input reflection coefficient	note 2	–	–15	–10	dB
$SPUR_{P(RFin)}$	power level of spurious signals at RF input	900 to 1000 MHz band	–	–	–57	dBm
		1800 to 2000 MHz band	–	–	–47	dBm
		out of preceding bands	–	–	–45	dBm
CP1	1 dB input compression point	minimum AGC; T_{amb} = 25 °C; note 1	–25	–	–	dBm
$IP3_i$	input referred third-order intercept	maximum AGC; T_{amb} = 25 °C; note 1	–18	–	–	dBm
$IP2_i$	input referred second-order intercept	maximum AGC; note 4	–	30	–	dBm
$DES3_i$	input referred 3 dB desensitization	Δf = 3 MHz; T_{amb} = 25 °C; note 1	–23	–	–	dBm
IR	image rejection	f_{IF} = 200 kHz; T_{amb} = 25 °C; note 1	35	38	–	dB
$\Delta G_{v(RF)}$	gain mismatch GSM and DCS paths	note 5	–	–	2	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PINS IA, IB, QA AND QB (RX MODE)						
$G_{v(min)}$	minimum voltage conversion gain	gain set to minimum; notes 1 and 5	19	25	31	dB
$G_{v(max)}$	maximum voltage conversion gain	gain set to maximum; notes 1 and 5	89	93	97	dB
$G_{v(step)}$	voltage conversion gain step	note 5	–	4	–	dB
$\Delta G_{v(I/Q)}$	gain mismatch I and Q paths	note 5	–	–	0.5	dB
$\Delta\Phi$	quadrature-phase error I and Q paths	peak error	–	–	5	deg
LE_{AGC}	gain control linearity	over full gain range; note 2	–2	–	+2	dB
		over any 20 dB gain range	–0.5	–	+0.5	dB
$V_{o(peak)}$	maximum output voltage per pin	3% T.H.D.; R_L = 100 kΩ per pin	0.75	–	–	V
$I_{o(peak)}$	maximum output current per pin		25	50	–	µA
V_{offset}	output offset voltage	under static conditions	–300	–	+300	mV
HP_{-3dB}	–3 dB high-pass corner frequency		4	6	8	kHz
$B_{IF(-3dB)}$	–3 dB IF filter bandwidth	100 kHz centre frequency	220	–	250	kHz
$\Delta t_{d(g)}$	group delay variation	30 kHz < f_o < 170 kHz	–	1.5	2	µs
$\alpha_{5(IF)}$	IF filter attenuation (fifth-order)	f_o = 100 kHz ± 200 kHz	17	31	–	dB
		f_o = 100 kHz ± 400 kHz	54	64	–	dB
		f_o = 100 kHz ± 600 kHz	73	82	–	dB
Transmit IF section (initial conditions: $V_{mod(peak)}$ = 0.5 V; f_{mod} = 67.7 kHz; unless otherwise specified)						
PINS IA, IB, QA AND QB (TX MODE)						
f_{mod}	modulation frequency	3 dB low-pass cut-off frequency	1	–	–	MHz
$V_{mod(peak)}$	modulation level	single-ended; peak value	–	0.5	0.55	V
$R_{i(D)}$	dynamic input resistance	single-ended	–	25	–	kΩ
IF LO oscillator (measured and guaranteed on demonstration board at T_{amb} = 25 °C)						
f_{IFLO}	range of possible operation	with programming	78	–	91	MHz
K_{VCO}	VCO gain	V_{tune} from 0.6 V to V_{CC} – 0.6 V	–	30	–	MHz/V
V_{tune}	tuning voltage	referenced to $V_{CC(IFCP)}$	0.4	–	V_{CC} – 0.4	V
Δf_{VCC}	frequency variation with respect to the supply voltage	pushing	–	–	1	MHz/V
Δf_{TRON}	frequency variation	pulling	–5	–	+5	kHz
Transmit modulation loop section						
OFFSET MIXER; PIN TXRFI						
f_{RF}	RF input frequency		880	–	1910	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_i	input resistance	single-ended	–	50	–	Ω
C_i	input capacitance	single-ended	–	–	–	pF
P_i	input power		–23	–20	–17	dBm
s_{11}	input reflection coefficient		–	–10	–	dB
F	noise figure	T_{amb} = 25 °C	–	10	–	dB
CP1	1 dB input compression point	T_{amb} = 25 °C	–	–20	–	dBm
$SPUR_{P(RFin)}$	power level of spurious signals at RF input	LO leakage	–	–50	–45	dBm
		other	–	–	–45	dBm
PHASE DETECTOR; PIN TXCPO						
$I_{CP(max)}$	charge pump maximum sink or source current	GSM mode; external resistance of 1800 Ω 1% for minimum output current; TXI = 0; note 6	1	2	4	mA
		DCS and PCS mode; external resistance of 1800 Ω 1% for minimum output current; TXI = 1; note 6	0.5	1	2	mA
KΦ	phase-frequency detector gain	for I_{CP} = 1 mA	–	0.16	–	mA/rad
ΔKΦ	phase-frequency detector gain variation	over output voltage range	–	–	10	%
V_o	output voltage		0.4	–	$V_{CC(CP)}$ – 0.4	V
R_o	output resistance	$V_o = \frac{V_{CC(PHD)}}{2}$	–	10	–	kΩ
$R_{o(pd)}$	output resistance power down	TX mode disabled	–	1	–	kΩ
LO_o	local oscillator feedthrough	note 7	–	–40	–32	dBc
$IM3_o$	third-order products level	offset +3 × 67.7 kHz or –3 × 67.7 kHz; note 7	–	–55	–50	dBc
IM_o	image level	f_{IFLO} – 67.7 kHz; note 7	–	–45	–37	dBc
Φ_{NOISE}	phase noise output power density	Δf = 400 kHz; T_{amb} = 25 °C; note 7	–	–	–117	dBc/Hz
		Δf = 1.8 MHz; T_{amb} = 25 °C; note 7	–	–	–117	dBc/Hz
		Δf = 20 MHz; T_{amb} = 25 °C	–	–	–136	dBc/Hz
$SPUR_{L(4fm)}$	level of spurious signals at 4 × f_{mod}	f_{mod} = 67.7 kHz; notes 7 and 8	–	–	–50	dBc
$SPUR_{L(8fm)}$	level of spurious signals at 8 × f_{mod}	f_{mod} = 67.7 kHz; note 7	–	–	–55	dBc
RF LO buffer						
RF SOURCE CONNECTED AT PIN RFLOIA AND RFLOIB						
$f_{i(RF)}$	RF input frequency		1788	–	2002	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{i(dif)}$	differential input resistance	parallel RC input model	–	50	–	Ω
$C_{i(dif)}$	differential input capacitance	parallel RC input model	–	0.2	–	pF
s_{11}	input reflection coefficient		–	–15	–10	dB
P_{LO}	power available from the LO source		–8	–5	–2	dBm
RF and IF synthesizers						
REFERENCE INPUT; PIN REFIN						
f_{ref}	reference frequency	REFDIV = 0	–	13	–	MHz
		REFDIV = 1	–	26	–	MHz
$V_{i(rms)}$	input voltage level (RMS value)		60	–	220	mV
R_i	input resistance	f_{ref} = 13 MHz	–	10	–	kΩ
RF SYNTHESIZER; PIN RFCPO						
f_{RFLO}	synthesizer frequency		1700	–	2100	MHz
$f_{comp(RF)}$	comparison frequency		–	200	–	kHz
$f_{comp(leak)}$	200 kHz comparison frequency leakage	with recommended loop filter	–	–50	–	dBc
$f_{step(RF)}$	frequency step programmability	$f_{comp(RF)}$ = 200 kHz	–	100	–	kHz
Φ_{noise}	close-in phase noise	Δf = 2 kHz	–	–80	–76	dBc/Hz
$SPUR_{P(RF)}$	power level of spurious signals	f > 400 kHz	–	–	–70	dBc
$I_{CP(nom)}$	nominal charge pump output current	sink or source	1.7	2.0	2.3	mA
KΦ	phase-frequency detector gain	I_{CP} = 2 mA	–	0.32	–	mA/rad
ΔKΦ	phase-frequency detector gain variation	over V_{CP} range	–	–	10	%
$I_{L(CP)}$	charge pump leakage current	in off state	–5	–	+5	nA
V_{CP}	charge pump output voltage	I_{CP} within specified range	0.4	–	V_{CC} – 0.4	V
R_o	output resistance	SYN mode disabled; power-down	–	1	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF SYNTHESIZER; PINS IFTUNE AND IFCPO						
f_{IFLO}	synthesizer frequency		70	–	100	MHz
$f_{comp(IF)}$	comparison frequency		–	13	–	MHz
Φ_{noise}	close-in phase noise	Δf = 400 kHz	–	–	–117	dBc/Hz
$SPUR_{P(IF)}$	power level of spurious signals		–	–	–70	dBc
I_{CP}	charge pump output current	sink or source	0.85	1.0	1.15	mA
$K\Phi$	phase-frequency detector gain	for I_{CP} = 1 mA	–	0.16	–	mA/rad
$\Delta K\Phi$	phase-frequency detector gain variation	over V_{CP} range	–	–	10	%
I_L	charge pump leakage current	off state	–5	–	+5	nA
V_{CP}	charge pump output voltage		0.4	–	V_{CC} – 0.4	V
R_o	output resistance	TXIFON and TXON mode disabled; power-down	–	1	–	kΩ
DIVIDERS RATIOS						
$D/D_{RF(main)}$	RF main divider ratio	ratio between RFLOI frequency and $f_{comp(RF)}$	8940	–	10 010	
$D/D_{IF(main)}$	IF main divider ratio	ratio between IF VCO frequency and $f_{comp(IF)}$	6	–	7	
$D/D_{RF(REFDIV)}$	RF reference divider ratio	REFDIV = 0	–	65	–	
		REFDIV = 1	–	130	–	
$D/D_{IF(REFDIV)}$	IF reference divider ratio	REFDIV = 0	–	1	–	
		REFDIV = 1	–	2	–	
General						
t_{ON}	turn-on time	90% of the final current	–	–	200	µs

Notes

1. Measured and guaranteed only on OM 5178 demonstration board.
2. This value includes printed-circuit board and balun losses.
3. The power level of the spurious signals in this measurement is less than specified under $SPUR_{P(RFin)}$.
4. $IP2_i$ related to an IM2 measurement in low gain mode.
5. Voltage gain defined as the differential baseband RMS output voltage (either at pins IA and IB or pins QA and QB measured in standard load) divided by the RMS input voltage at the RF baluns.
6. This range is obtained through variation of the external reference resistor.
7. Measured at external transmit VCO output.
8. This is based on an adjustment in such a way, that a difference of 36 dBc is obtained in the level of the wanted signal at the frequency $f_{IF} + f_{mod}$ and the level of the signal at the frequency $3f_{IF} – f_{mod}$, measured at the input of the phase-frequency comparator for IF frequencies of 45.5 and 91 MHz.

SERIAL TIMING CHARACTERISTICS

Initial parameter values: V_{CC} = 2.6 V ±5%; T_{amb} = –30 to +70 °C; unless otherwise specified; see Fig.3.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock: pin CLK					
t_r	rise time	–	10	20	ns
t_f	fall time	–	10	20	ns
T_{cy}	clock cycle time	200	–	–	ns
Enable programming: pin $\overline{E}$					
$t_{su(E)}$	delay to rising clock edge	200	–	–	ns
$t_{h(E)}$	delay from last falling clock edge	100	–	–	ns
$t_{W(E)}$	minimum inactive pulse width	4000	–	–	ns
$t_{su(E)}$	enable set-up time to next clock edge	200	–	–	ns
Register serial input data: pin DATA					
$t_{su(D)}$	input data to clock set-up time	50	–	–	ns
$t_{h(D)}$	input data to clock hold time	50	–	–	ns

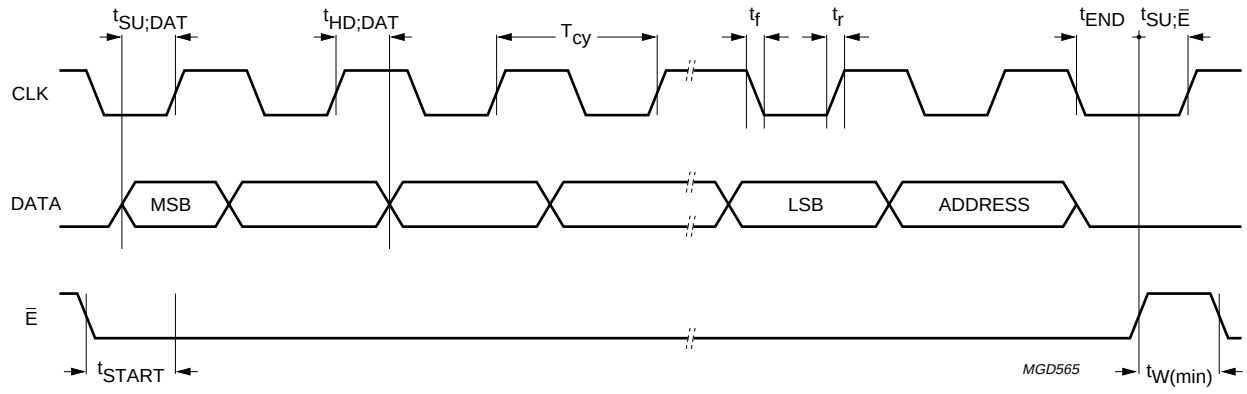


Fig.3 Timing diagram 3-wire serial bus.

APPLICATION INFORMATION

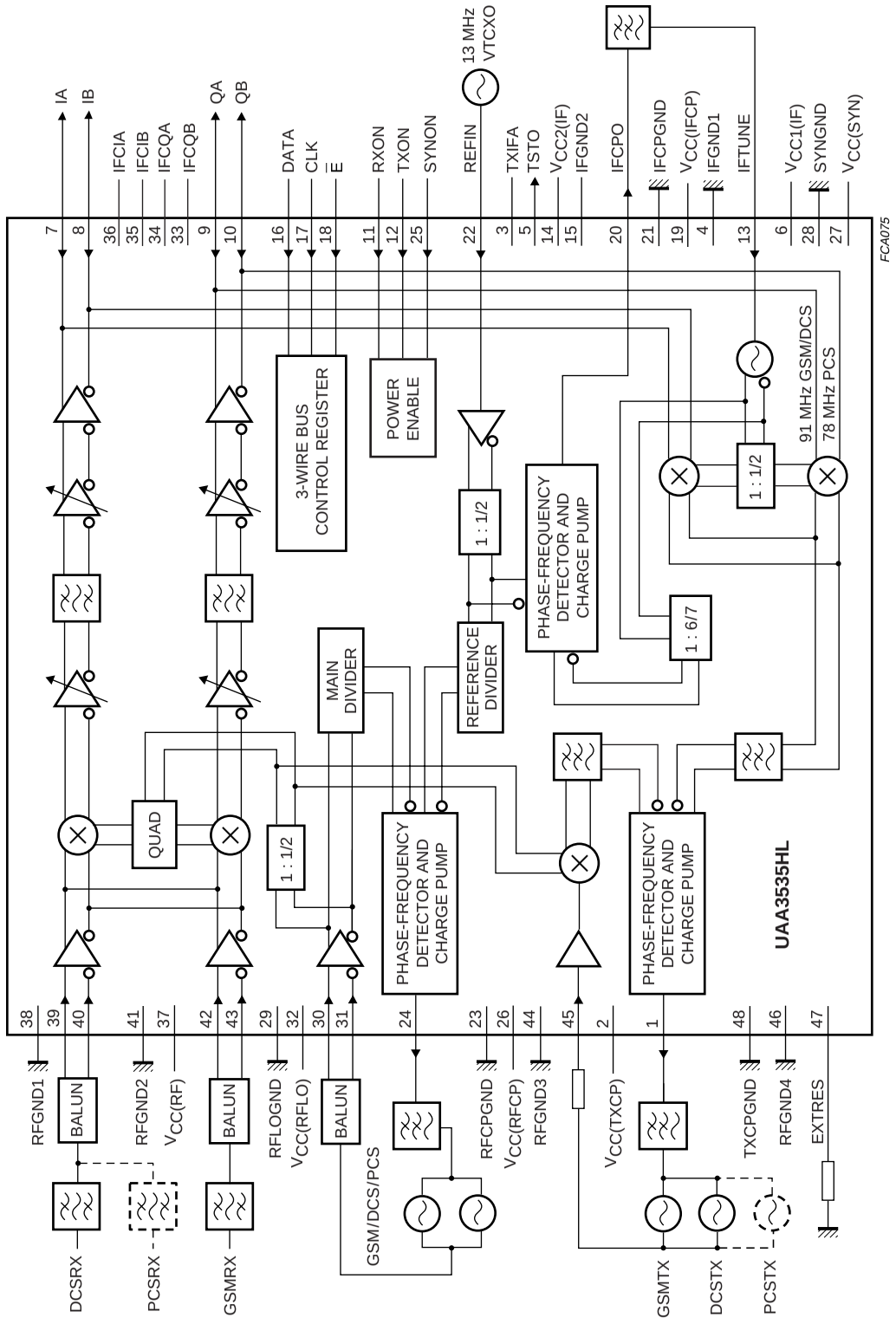
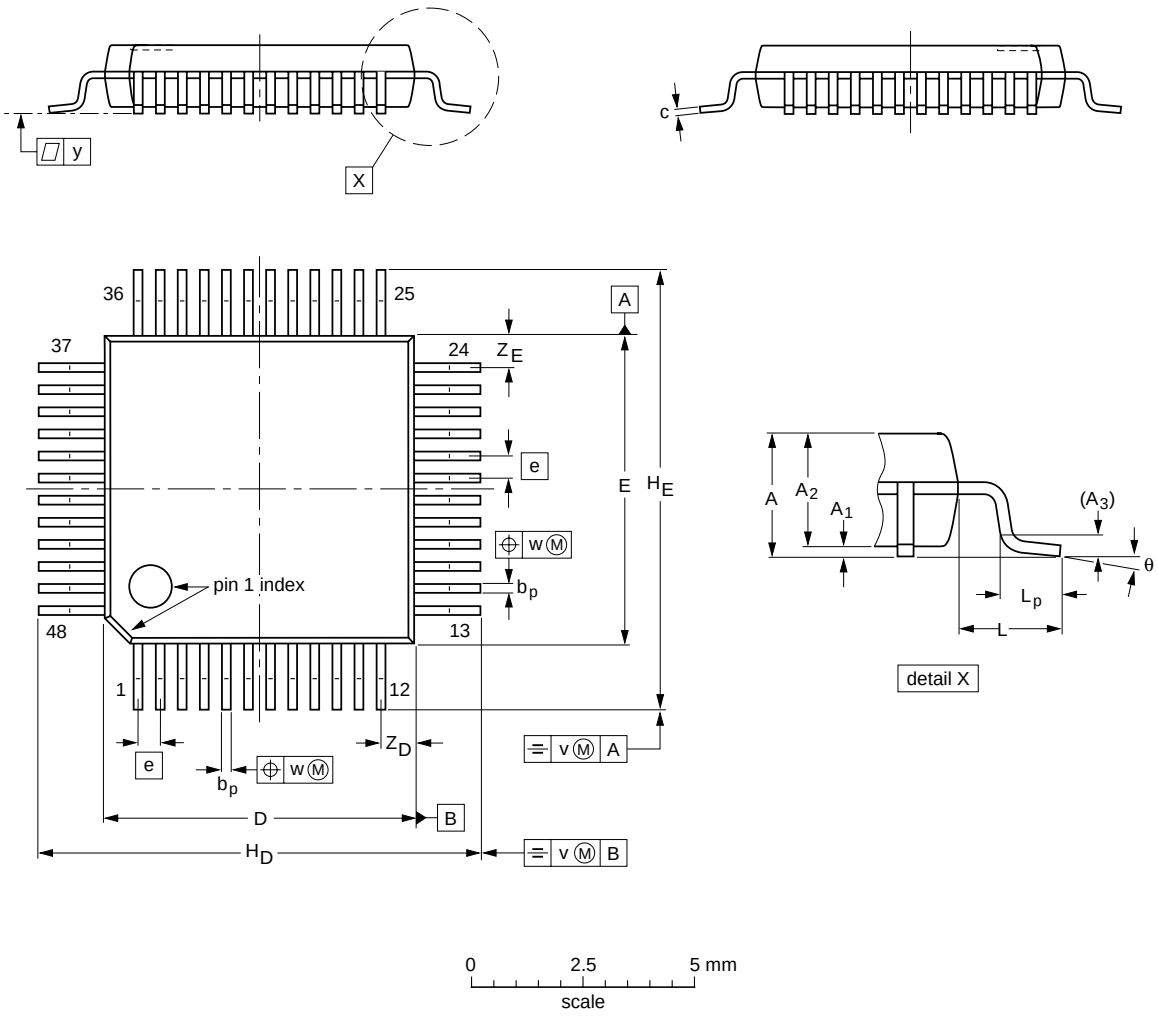


Fig.4 Application diagram.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				~~99-12-27~~ 00-01-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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