

ANALOG Narrow-Band Power-Line Communications DEVICES Master Modem IC with Networking Stack **Master Modem IC with Networking Stack**

ADE8165

FEATURES

Narrow-band power-line communications IC Integrates PHY through networking layer Simple host interface

Application layer

Supports DL/T 645-1997 or -2007 China-specific protocol as well as passthrough option

Networking layer

Master/slave architecture

Designed to work with ADE8155 slave PLC modem ICs

Supports

Dynamic routing

Automatic discovery of authenticated devices

Logical address management

Data link layer

Automatic baud rate negotiation

Up to 63-byte packet support

Physical laver

CPFSK modulation

Choice of two frequency bands

Carrier frequencies: 105.5 kHz and 118.7 kHz Carrier frequencies: 74.9 kHz and 84.2 kHz

Up to 800 bps on a 1-phase network and 2400 bps on a

3-phase network

Zero-crossing synchronized receive/transmit

6-byte physical address for logical address assignment

Communication interface

UART

Option to use DL/T 645-1997 or -2007 China-specific

application layer interface

Package and temperature range

40-lead 6 mm × 6 mm LFCSP

Fully specified for -40°C to +85°C operation

GENERAL DESCRIPTION

The ADE81651 incorporates a high performance ADC and DAC to create a very robust CPFSK power-line communications IC complete with networking functionality. The ADE8165 master modem IC is designed to work with the ADE8155 slave modem IC for a complete power-line communication system.

In an advanced metering infrastructure (AMI) scenario, the ADE8155 slave modem IC is used to connect the energy meter to the power line. Then the ADE8165 master PLC modem is used near the transformer to communicate with multiple meters on one phase. The power-line communication is independent on each phase; therefore, three ADE8165 master PLC modem ICs are used in a PLC module within the concentrator to read meters on all three phases.

A UART communication interface is supported.

For more information on the ADE8165, contact your local sales office at Analog Devices, Inc.

¹ US patents pending.

FUNCTIONAL BLOCK DIAGRAM SPICSL **EXTERNAL** (27) A0/MOSI MEMORY 28 A1/MISO INTERFACE (29) SPISCLK 23) RX WITH NETWORK MANAGEMENT FUNCTIONS 2 TX 30) RS485_OE 10) EVENT DLL 33) RXEN ZX (2) PHY (21) TXEN VMON (39 RX LED PLC RX+ 12-BIT DEMODULATOR MODULATOR DAC PLC_TX PLC RX-LDO **ADE8165** osc (35) RST AVDD XTAL1 DGND DGND AGND AGND Figure 1.

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