# STD22NM20N

## N-CHANNEL 200V - 0.088Ω - 22A DPAK
## ULTRA LOW GATE CHARGE MDmesh™ II MOSFET

**Table 1: General Features**

| TYPE | $V_{DSS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| STD22NM20N | 200 V | < 0.105 Ω | 22 A |

- WORLDWIDE LOWEST GATE CHARGE
- TYPICAL $R_{DS}$(on) = 0.088 Ω
- HIGH dv/dt and AVALANCHE CAPABILITIES
- LOW INPUT CAPACITANCE
- LOW GATE RESISTANCE

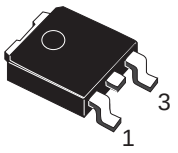
### DESCRIPTION

This 200V MOSFET with a new advanced layout brings all unique advantages of MDmesh technology to lower voltages. The device exhibits worldwide lowest gate charge for any given on-resistance. Its use is therefore ideal as primary switch in isolated DC-DC converters for Telecom and Computer applications. Used in combination with secondary-side low-voltage STripFET™ products, it contributes to reducting losses and boosting effeciency.

### APPLICATIONS

The MDmesh™ family is very suitable for increasing power density allowing system miniaturization and higher efficiencies

**Figure 1: Package**




**DPAK**

**Figure 2: Internal Schematic Diagram**

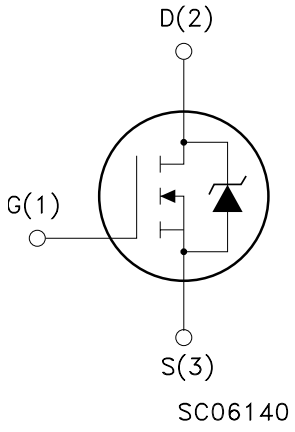



**Table 2: Order Codes**

| SALES TYPE | MARKING | PACKAGE | PACKAGING |
|---|---|---|---|
| STD22NM20NT4 | D22NM20N | DPAK | TAPE & REEL |

Rev. 5

### Table 3: Absolute Maximum ratings

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source Voltage ($V_{GS}$ = 0) | 200 | V |
| $V_{DGR}$ | Drain-gate Voltage ($R_{GS}$ = 20 kΩ) | 200 | V |
| $V_{GS}$ | Gate- source Voltage | ± 20 | V |
| $I_D$ | Drain Current (continuous) at $T_C$ = 25°<br>Drain Current (continuous) at $T_C$ = 100° | 22<br>13.7 | A<br>A |
| $I_{DM}$ (*) | Drain Current (pulsed) | 88 | A |
| $P_{TOT}$ | Total Dissipation at $T_C$ = 25°C | 100 | W |
| | Derating Factor | 0.8 | W/°C |
| dv/dt (2) | Peak Diode Recovery voltage slope | 14 | V/ns |
| $T_j$<br>$T_{stg}$ | Storage Temperature<br>Max Operating Junction Temperature | 150<br>-65 to 150 | °C<br>°C |

(*) $I_{SD}$ ≤ 22A, di/dt ≤ 400A/µs, $V_{DD}$ = 80% $V_{(BR)DSS}$

### Table 4: Thermal Data

| | | | |
|---|---|---|---|
| Rthj-case | Thermal Resistance Junction-case Max | 1.25 | °C/W |
| Rthj-amb | Thermal Resistance Junction-ambient Max | 100 | °C/W |
| Rthj-amb$T_l$ | Thermal Resistance Junction-pcb (*)<br>Maximum Lead Temperature For Soldering Purpose | 43<br>275 | °C/W<br>°C |

(*) When mounted on 1 inch² FR-4 board, 2 oz Cu, t ≤ 10 sec

### Table 5: Avalanche Characteristics

| Symbol | Parameter | Max Value | Unit |
|---|---|---|---|
| $I_{AS}$ | Avalanche Current, Repetitive or Not-Repetitive<br>(pulse width limited by $T_j$ max) | 22 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy<br>(starting $T_j$ = 25 °C, $I_D$ = 22 A, $V_{DD}$ = 50 V) | 380 | mJ |

## ELECTRICAL CHARACTERISTICS ($T_{CASE}$ =25°C UNLESS OTHERWISE SPECIFIED)

### Table 6: On/Off

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source Breakdown Voltage | $I_D$ = 1mA, $V_{GS}$ = 0 | 200 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current ($V_{GS}$ = 0) | $V_{DS}$ = Max Rating<br>$V_{DS}$ = Max Rating, $T_C$ = 125 °C | | | 1<br>10 | µA<br>µA |
| $I_{GSS}$ | Gate-body Leakage Current ($V_{DS}$ = 0) | $V_{GS}$ = ± 20V | | | 100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3.5 | 4.2 | 5 | V |
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{GS}$ = 10V, $I_D$ = 11 A | | 0.088 | 0.105 | Ω |

### Table 7: Dynamic

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (2) | Forward Transconductance | $V_{DS}$ = 15 V, $I_D$=11 A | | 8 | | S |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input Capacitance<br>Output Capacitance<br>Reverse Transfer Capacitance | $V_{DS}$ = 25V, f = 1 MHz, $V_{GS}$ = 0 | | 800<br>330<br>130 | | pF<br>pF<br>pF |
| $C_{oss\ eq.}$ (**) | Equivalent Output Capacitiance | $V_{GS}$ = 0 V, $V_{DS}$ = 0 V to 400 V | | 225 | | pF |
| $R_G$ | Gate Input Resistance | f= 1MHz Gate DC Bias = 0<br>Test Sgnal Level = 20 mV<br>Open Drain | | 5 | | Ω |
| $t_{d(on)}$<br>$t_r$<br>$t_{r(Voff)}$<br>$t_f$ | Turn-on Delay Time<br>Rise Time<br>Turn-off Delay Time<br>Fall Time | $V_{DD}$ = 100 V, $I_D$ = 11 A<br>$R_G$ = 4.7Ω $V_{GS}$ = 10 V<br>(see Figure 15) | | 40<br>15<br>40<br>11 | | ns<br>ns<br>ns<br>ns |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total Gate Charge<br>Gate-Source Charge<br>Gate-Drain Charge | $V_{DD}$ = 100 V, $I_D$ = 20 A,<br>$V_{GS}$ = 10 V<br>(see Figure 19) | | 32<br>6<br>25 | 50 | nC<br>nC<br>nC |

(**) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

### Table 8: Source Drain Diode

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$<br>$I_{SDM}$ (1) | Source-drain Current<br>Source-drain Current (pulsed) | | | | 22<br>88 | A<br>A |
| $V_{SD}$ (2) | Forward On Voltage | $I_{SD}$ = 20 A, $V_{GS}$ = 0 | | | 1.3 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse Recovery Time<br>Reverse Recovery Charge<br>Reverse Recovery Current | $I_{SD}$ = 20 A, di/dt = 100 A/µs<br>$V_{DD}$ = 100V, $T_j$ = 25°C<br>(see test circuit, Figure 17) | | 160<br>960<br>12.8 | | ns<br>µC<br>A |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse Recovery Time<br>Reverse Recovery Charge<br>Reverse Recovery Current | $I_{SD}$ = 20 A, di/dt = 100 A/µs<br>$V_{DD}$ = 100V, $T_j$ = 150°C<br>(see test circuit, Figure 17) | | 225<br>1642<br>15 | | ns<br>µC<br>A |

(1) Pulse width limited by safe operating area.
(2) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

**Figure 3: Safe Operating Area**

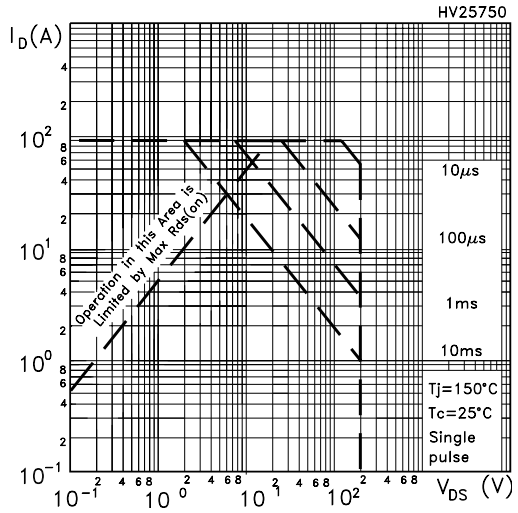



**Figure 4: Output Characteristics**

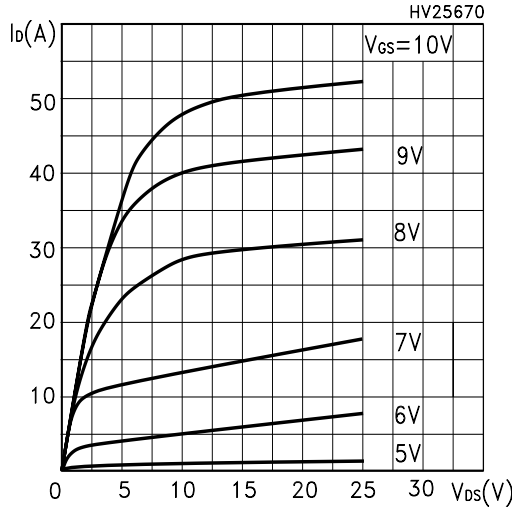



**Figure 5: Transconductance**

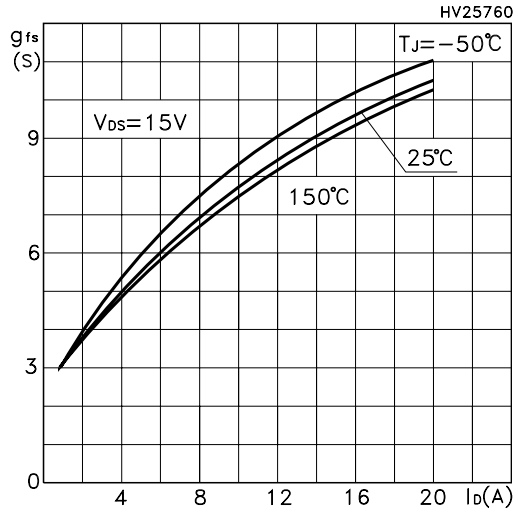



**Figure 6: Thermal Impedance**

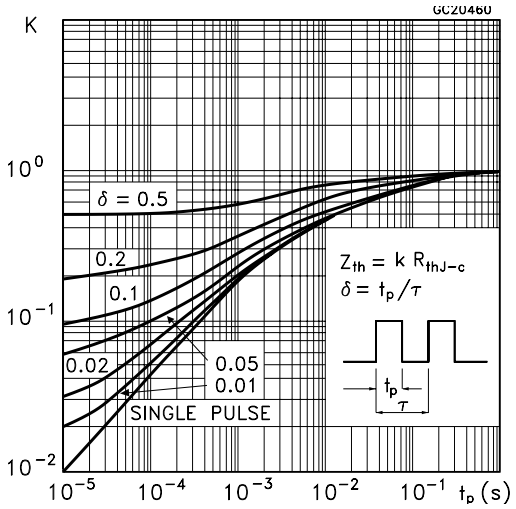



**Figure 7: Transfer Characteristics**

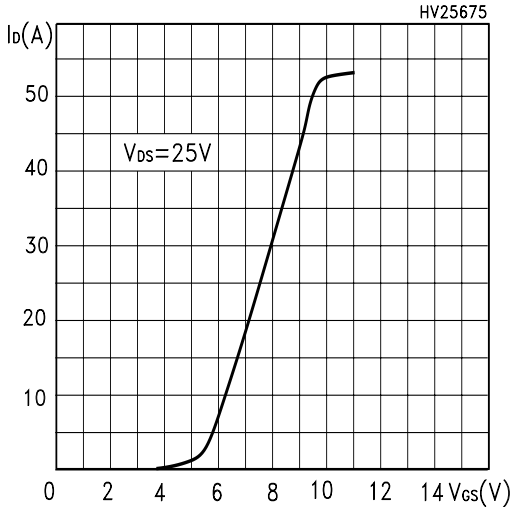



**Figure 8: Static Drain-source On Resistance**

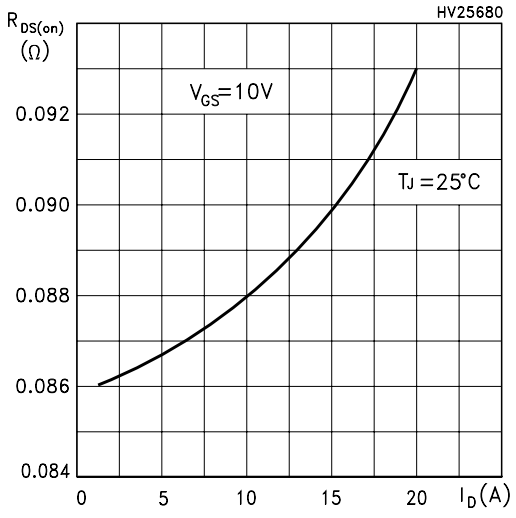


**Figure 9: Gate Charge vs Gate-source Voltage**

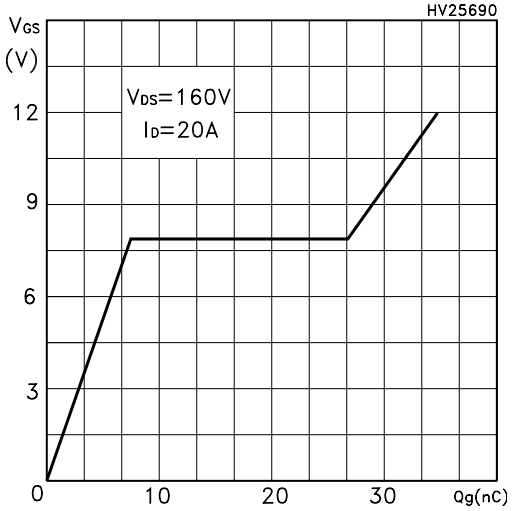



**Figure 10: Normalized Gate Thereshold Voltage vs Temperature**

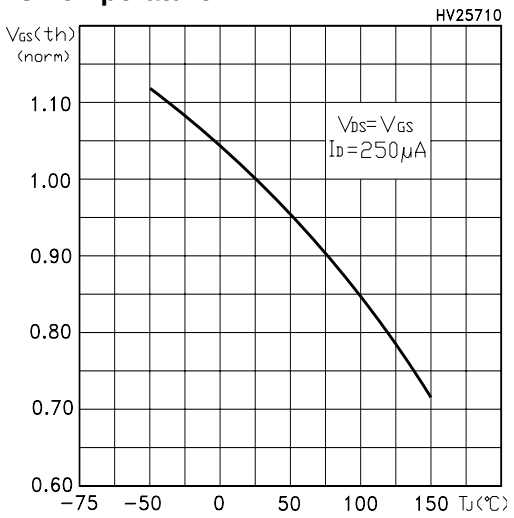



**Figure 11: Source-Drain Diode Forward Characteristics**

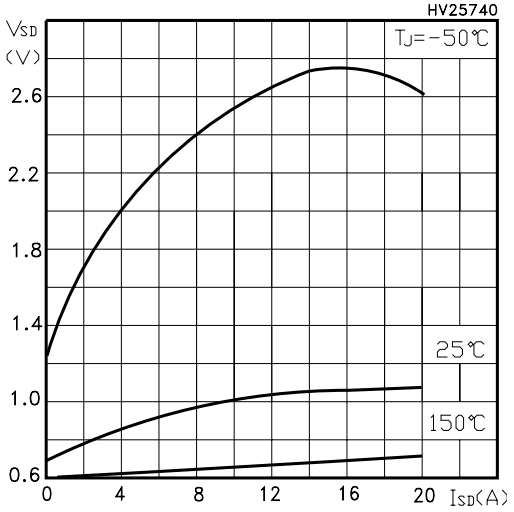



**Figure 12: Capacitance Variations**

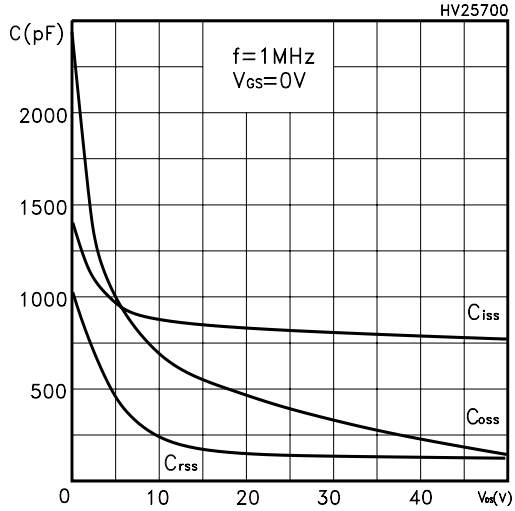



**Figure 13: Normalized On Resistance vs Temperature**

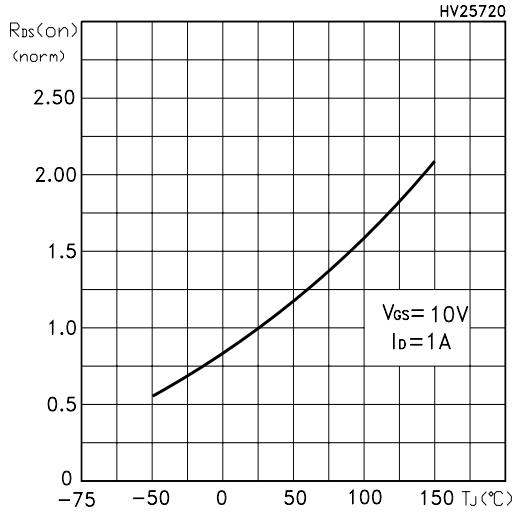



**Figure 14: Normalized BVdss vs Temperature**

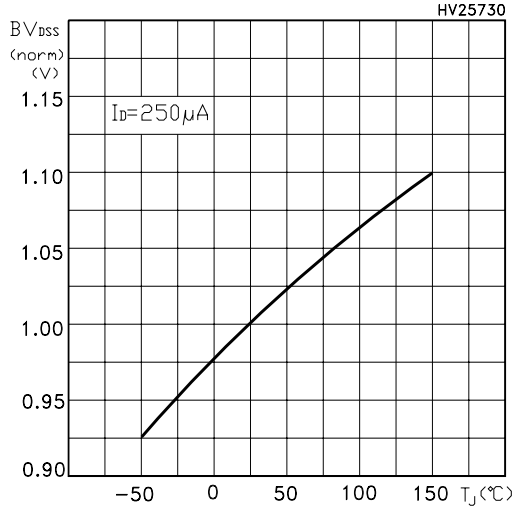


**Figure 15: Unclamped Inductive Load Test Circuit**

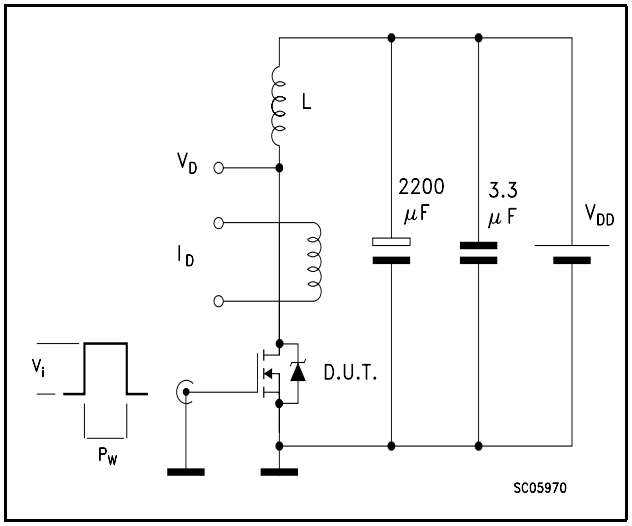



**Figure 16: Switching Times Test Circuit For Resistive Load**

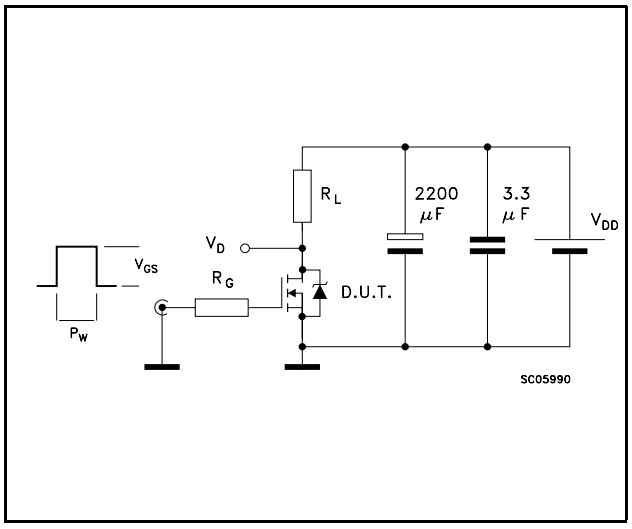



**Figure 17: Test Circuit For Inductive Load Switching and Diode Recovery Times**

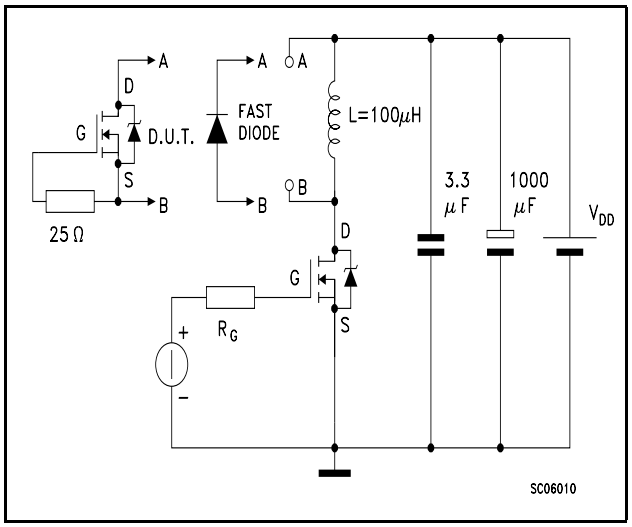



**Figure 18: Unclamped Inductive Wafeform**

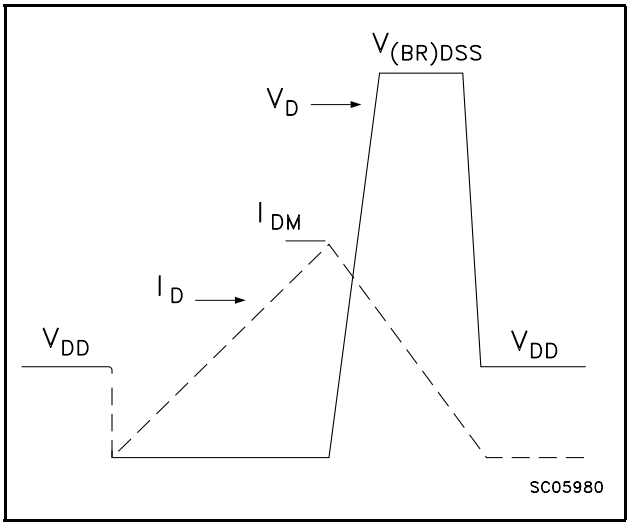
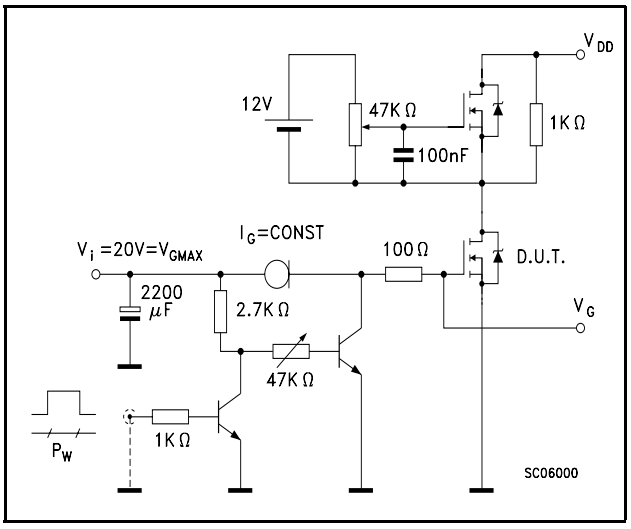
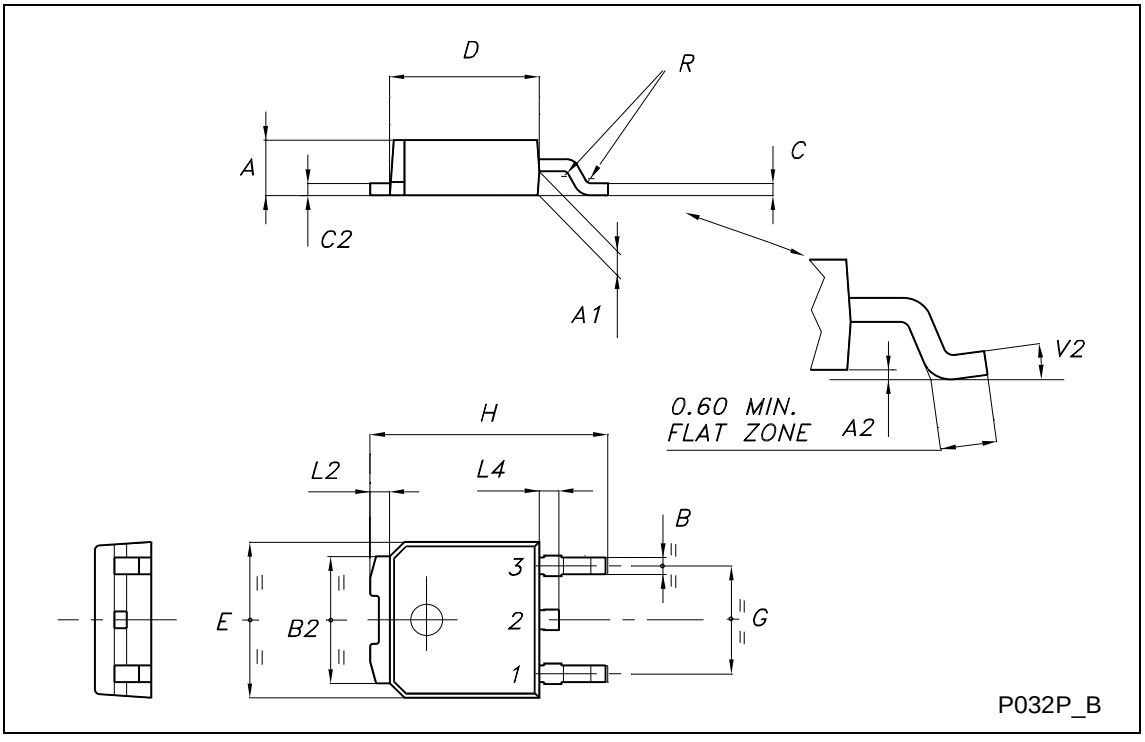



**Figure 19: Gate Charge Test Circuit**



## TO-252 (DPAK) MECHANICAL DATA

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 2.20 | | 2.40 | 0.087 | | 0.094 |
| A1 | 0.90 | | 1.10 | 0.035 | | 0.043 |
| A2 | 0.03 | | 0.23 | 0.001 | | 0.009 |
| B | 0.64 | | 0.90 | 0.025 | | 0.035 |
| B2 | 5.20 | | 5.40 | 0.204 | | 0.213 |
| C | 0.45 | | 0.60 | 0.018 | | 0.024 |
| C2 | 0.48 | | 0.60 | 0.019 | | 0.024 |
| D | 6.00 | | 6.20 | 0.236 | | 0.244 |
| E | 6.40 | | 6.60 | 0.252 | | 0.260 |
| G | 4.40 | | 4.60 | 0.173 | | 0.181 |
| H | 9.35 | | 10.10 | 0.368 | | 0.398 |
| L2 | | 0.8 | | | 0.031 | |
| L4 | 0.60 | | 1.00 | 0.024 | | 0.039 |
| V2 | $0^o$ | | $8^o$ | $0^o$ | | $0^o$ |

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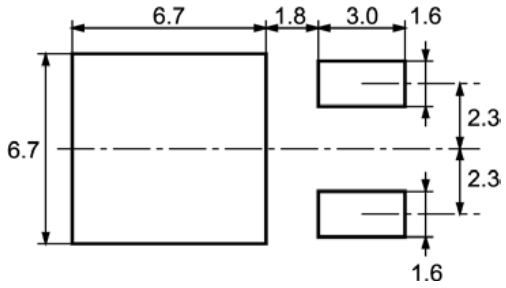
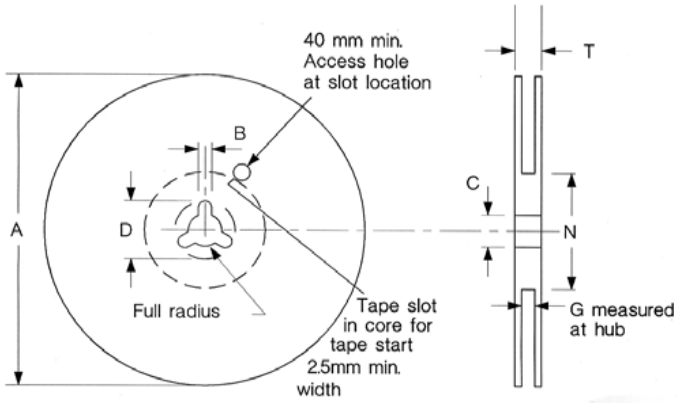
## DPAK FOOTPRINT




All dimensions are in millimeters

## TAPE AND REEL SHIPMENT




REEL MECHANICAL DATA

| DIM. | mm | | inch | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | | 330 | | 12.992 |
| B | 1.5 | | 0.059 | |
| C | 12.8 | 13.2 | 0.504 | 0.520 |
| D | 20.2 | | 0.795 | |
| G | 16.4 | 18.4 | 0.645 | 0.724 |
| N | 50 | | 1.968 | |
| T | | 22.4 | | 0.881 |

| BASE QTY | BULK QTY |
|---|---|
| 2500 | 2500 |

TAPE MECHANICAL DATA

| DIM. | mm | | inch | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A0 | 6.8 | 7 | 0.267 | 0.275 |
| B0 | 10.4 | 10.6 | 0.409 | 0.417 |
| B1 | | 12.1 | | 0.476 |
| D | 1.5 | 1.6 | 0.059 | 0.063 |
| D1 | 1.5 | | 0.059 | |
| E | 1.65 | 1.85 | 0.065 | 0.073 |
| F | 7.4 | 7.6 | 0.291 | 0.299 |
| K0 | 2.55 | 2.75 | 0.100 | 0.108 |
| P0 | 3.9 | 4.1 | 0.153 | 0.161 |
| P1 | 7.9 | 8.1 | 0.311 | 0.319 |
| P2 | 1.9 | 2.1 | 0.075 | 0.082 |
| R | 40 | | 1.574 | |
| W | 15.7 | 16.3 | 0.618 | 0.641 |

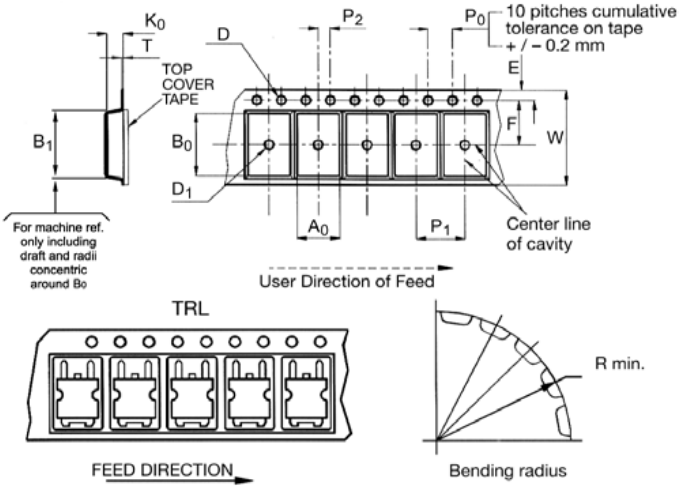


**Table 9: Revision History**

| Date | Revision | Description of Changes |
|---|---|---|
| 31-May-2004 | 1 | First Release. |
| 15-Mar-2005 | 2 | Update version. |
| 09-May-2005 | 3 | Complete version. |
| 09-Jun-2005 | 4 | New update |
| 04-Nov-2005 | 5 | Corrected value on Table 8 |