



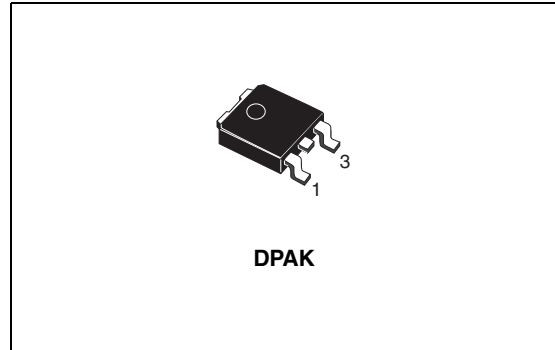
# STD16NE10L

N-channel 100V - 0.07Ω - 16A - DPAK  
STripFET™ Power MOSFET

## General features

Type	V <sub>DSSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD16NE10L	100V	<0.10Ω	16A

- Avalanche rugged technology
- Low gate charge
- High current capability
- 175°C operating temperature
- Low threshold drive



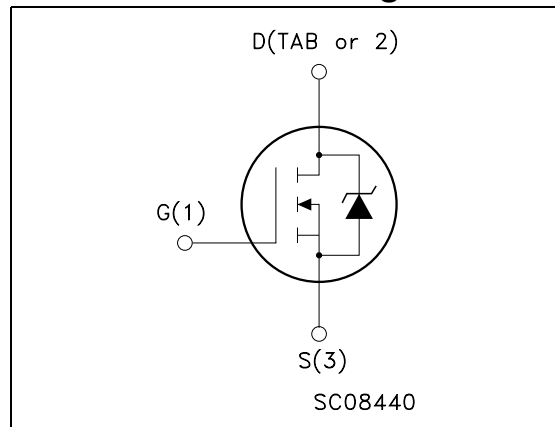
## Description

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

## Applications

- Switching application

## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STD16NE10LT4	D16NE10L	DPAK	Tape & reel

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## Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	100	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20K\Omega$ )	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	16	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	11	A
$I_{DM}^{(1)}$	Drain current (pulsed)	64	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	90	W
	Derating factor	0.6	W/ $^\circ\text{C}$
$E_{AS}^{(2)}$	Single pulse avalanche energy	75	mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	7	V/ns
$T_{stg}$	Storage temperature	-55 to 175	$^\circ\text{C}$
$T_J$	Max. operating junction temperature		

1. Pulse width limited by safe operating area
2. Starting  $T_J = 25^\circ\text{C}$ ,  $I_D = 8\text{A}$ ,  $V_{DD} = 30\text{V}$
3.  $I_{SD} \leq 16\text{A}$ ,  $di/dt \leq 300\text{ A}/\mu\text{s}$ ,  $V_{DS} \leq V_{(BR)DSS}$ ,  $T_J \leq T_{JMAX}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance junction-case Max	1.67	$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance junction-ambient Max	100	$^\circ\text{C}/\text{W}$
$T_I$	Maximum lead temperature for soldering purpose	275	$^\circ\text{C}$

## 2 Electrical characteristics

( $T_{CASE} = 25^{\circ}C$  unless otherwise specified)

**Table 3. On<sup>(1)</sup> /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	100			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating},$ $T_C = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 8A$ $V_{GS} = 5V, I_D = 8A$		0.07 0.085	0.085 0.01	$\Omega$ $\Omega$

1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5%

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 8A$	5	9		S
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz},$ $V_{GS} = 0$		1750		pF
$C_{oss}$	Output capacitance			165		pF
$C_{rss}$	Reverse transfer capacitance			45		pF
$Q_g$	Total gate charge	$V_{DD} = 80V, I_D = 16A$ $V_{GS} = 5V$		24	32	nC
$Q_{gs}$	Gate-source charge			5.5		nC
$Q_{gd}$	Gate-drain charge			11		nC

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50V, I_D = 8A,$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ <i>Figure 12 on page 8</i>		40		ns
$t_r$	Rise time			80		ns
$t_{d(off)}$	Turn-off delay time				45	ns
$t_f$	Fall time				12	ns
$t_{r(Voff)}$	Off-voltage Rise Time		$V_{clamp} = 80 V, I_D = 16 A$		12	
$t_f$	Fall Time	$R_G = 4.7\Omega, V_{GS} = 4.5 V$		17		ns
$t_c$	Cross-over Time	(Inductive Load, Figure 5)		35		ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				16	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				64	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 16A, V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 16A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 40V, T_J = 150^\circ C$ <a href="#">Figure 14 on page 8</a>		100		ns
$Q_{rr}$	Reverse recovery charge			300		$\mu C$
$I_{RRM}$	Reverse recovery current			6		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

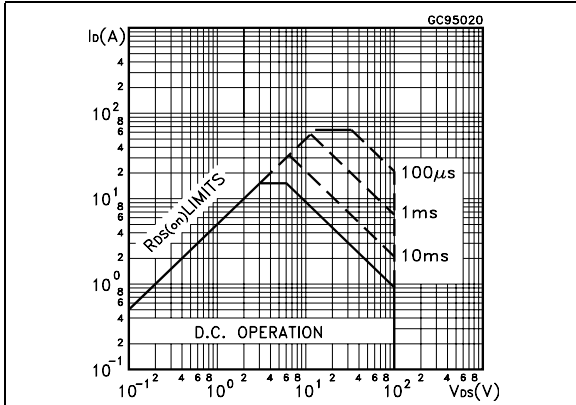


Figure 2. Thermal impedance

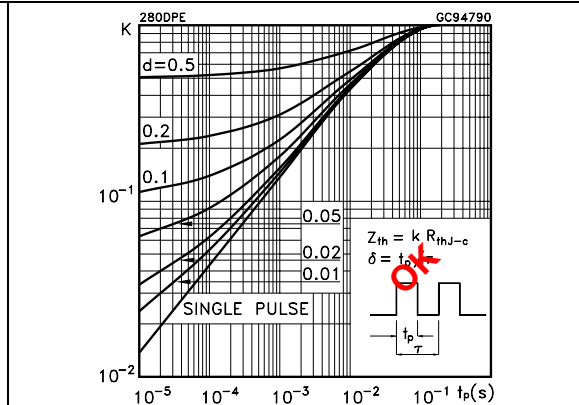


Figure 3. Output characteristics

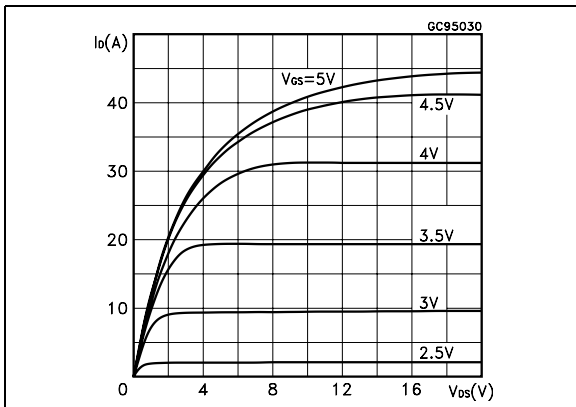


Figure 4. Transfer characteristics

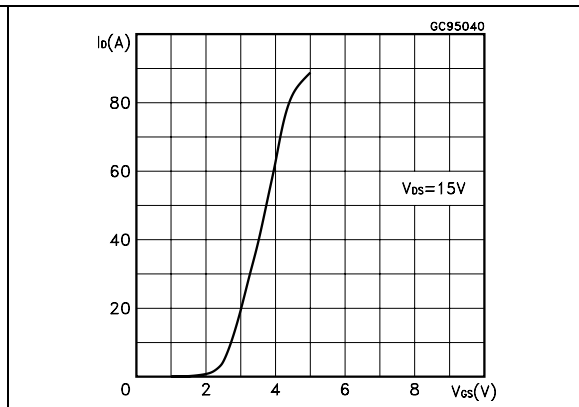


Figure 5. Transconductance

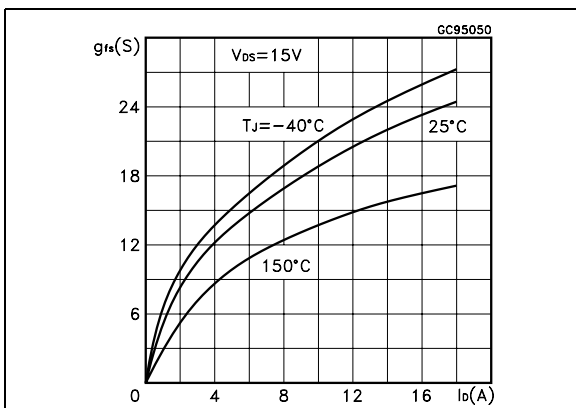


Figure 6. Static drain-source on resistance

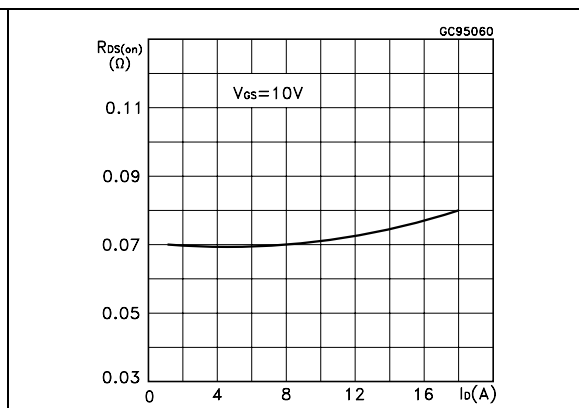


Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

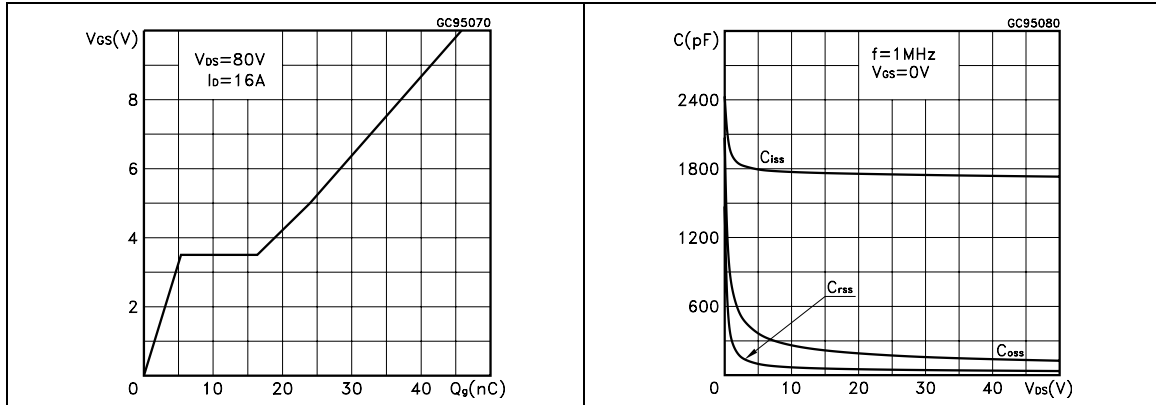


Figure 9. Normalized gate threshold voltage vs. temperature Figure 10. Normalized on resistance vs. temperature

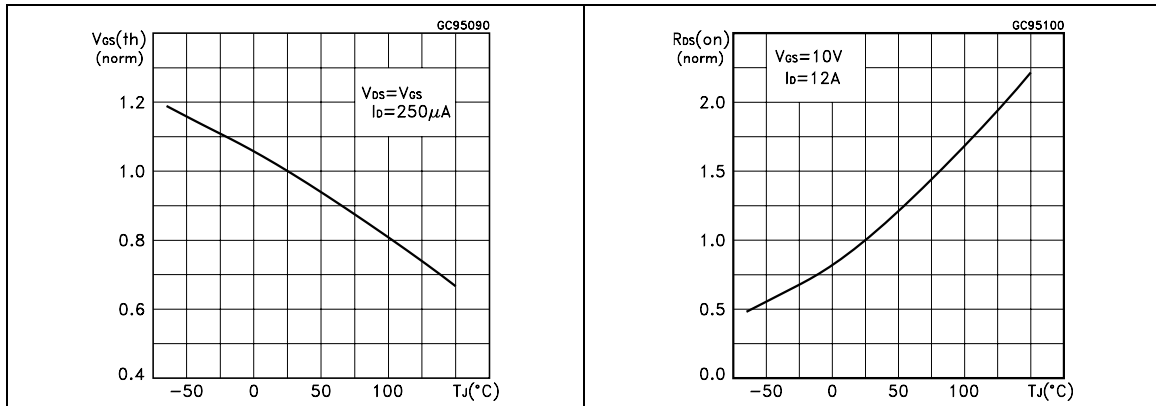
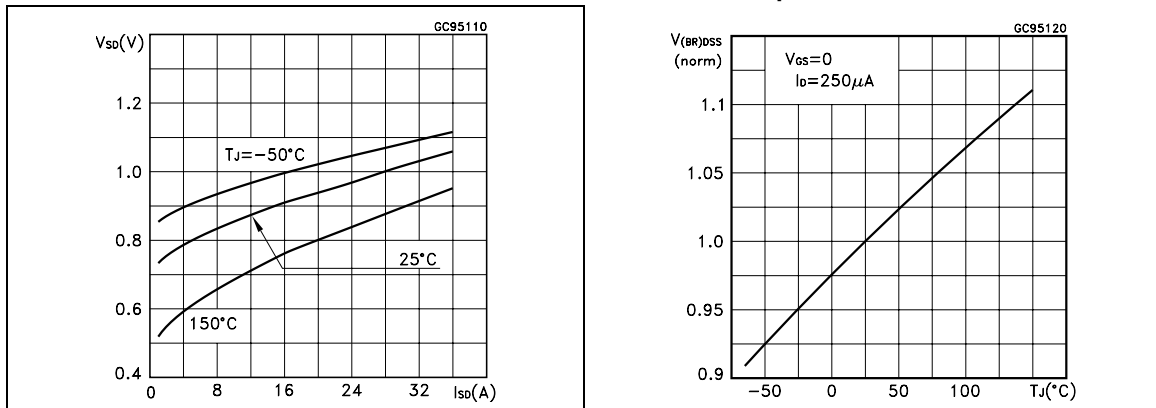


Figure 11. Source-drain diode forward characteristics Table 7. Normalized breakdown voltage temperature



### 3 Test circuit

Figure 12. Switching times test circuit for resistive load

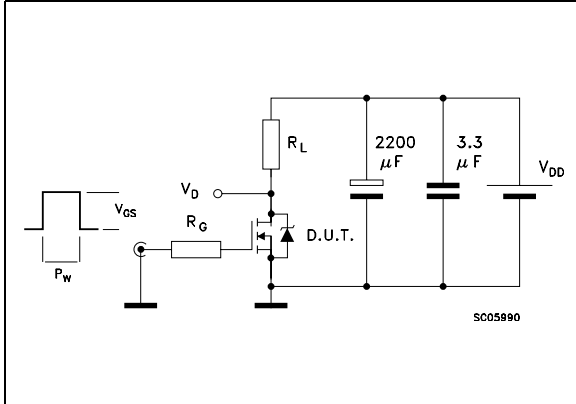


Figure 13. Gate charge test circuit

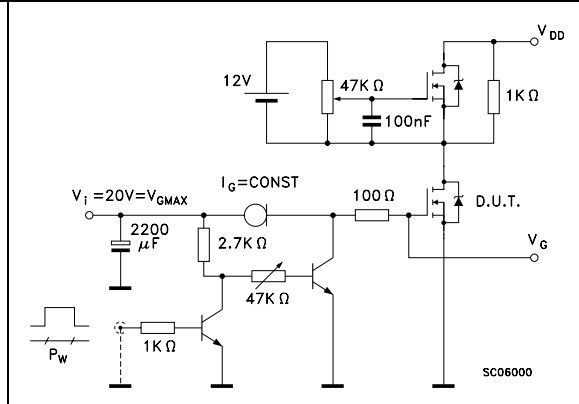


Figure 14. Test circuit for inductive load switching and diode recovery times

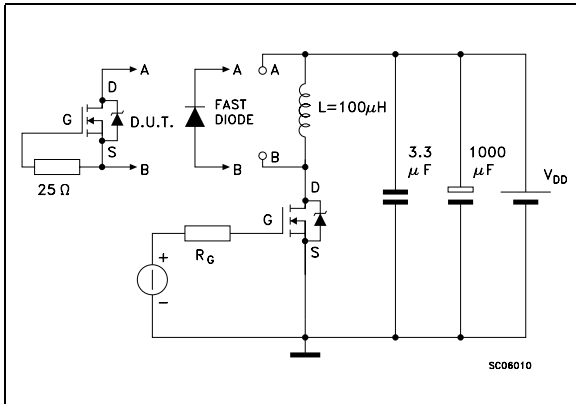


Figure 15. Unclamped Inductive load test circuit

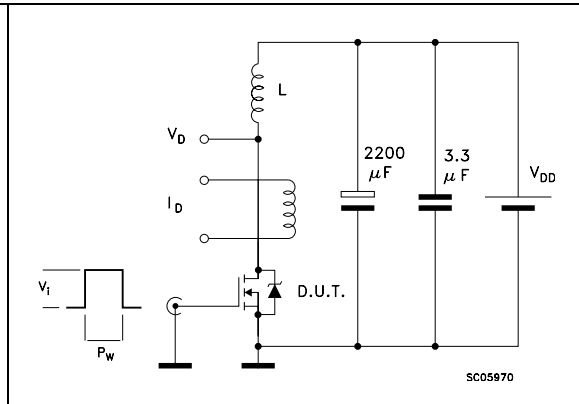
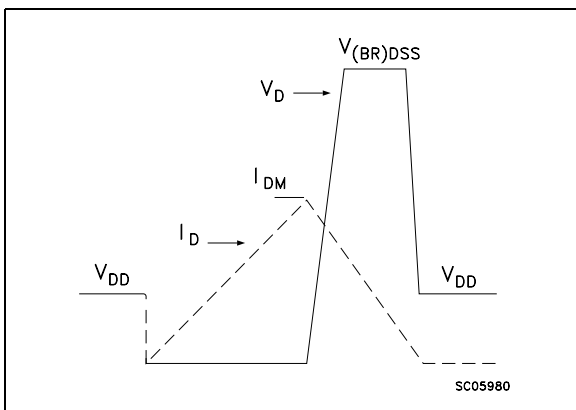


Figure 16. Unclamped inductive waveform



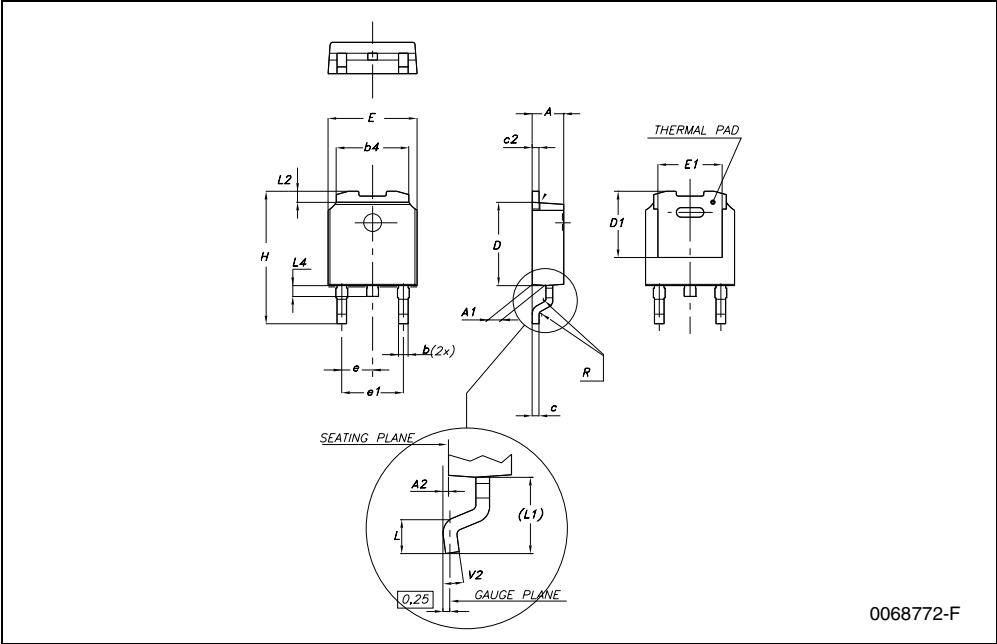


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**DPAK MECHANICAL DATA**

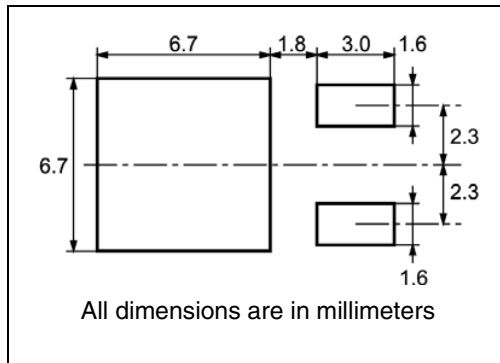
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



0068772-F

## 5 Packaging mechanical data

### DPAK FOOTPRINT



### TAPE AND REEL SHIPMENT

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

BASE QTY	BULK QTY
2500	2500

## 6 Revision history

Table 8. Revision history

Date	Revision	Changes
09-Sep-	3	Complete document
08-Aug-2006	4	New template, no content change
19-Feb-2007	5	Typo mistake on page 1

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