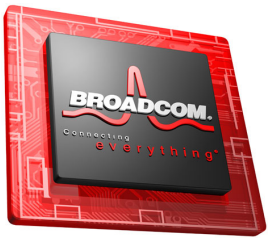
BROADCOM®
Connecting everything®

BCM3215 PRODUCT Brief



OCTAL DOWNSTREAM DOCSIS® 3.0 M-CMTS™ CORE MAC CHIP

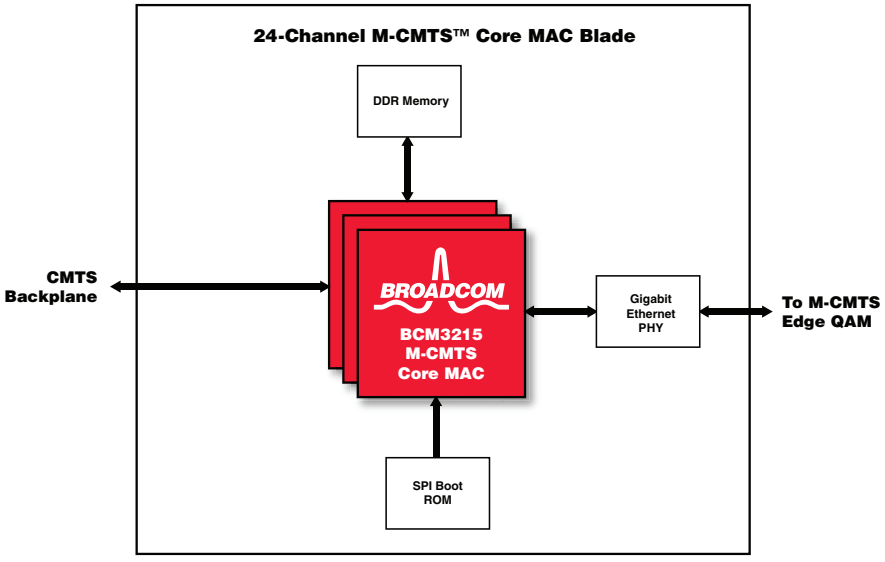
FEATURES

- Broadcom's BCM3215 is a DOCSIS® Core MAC chip with support for eight channels in M-CMTS™ applications
- Support for Downstream Edge PHY Interface (DEPI) protocols in M-CMTS applications
- Advanced packet-bonding capability support for up to N-QAM channels
- Packet port provides a high-throughput data interface to network equipment via a standard IEEE 802.3z GMII Ethernet interface
- Full DOCSIS downstream framing including Baseline Privacy, Payload Header Suppression, and MPEG Transmission Convergence
- Support for industrial temperature range of –40°C to +85°C
- Class-based queuing allows traffic prioritization of high, medium, and low priority

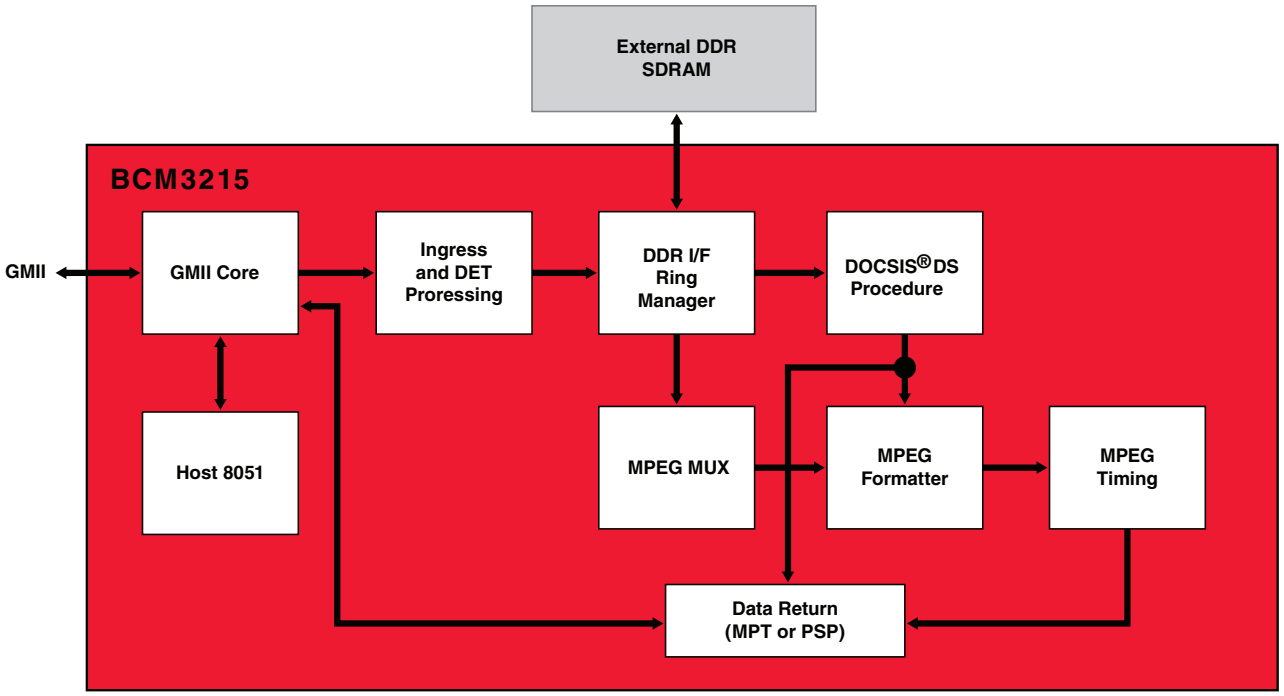
SUMMARY OF BENEFITS

- A high-performance, integrated solution for downstream transmission for data, video, and telephony applications over cable HFC networks
- Eight independent channels per package enable high-density equipment designs, reducing equipment floor space requirements.
- Provides full DOCSIS/EuroDOCSIS™ compliance for use in Modular-CMTS equipment.
- Faster line rates enable advanced data services over cable without stranding deployed equipment.
- Enables traffic prioritization for minimizing latency in delay-sensitive information such as voice and DOCSIS MAP packets.
- Enables advanced functions to be deployed in harsh environments.
  - Distributed CMTS in Hybrid Fiber Coaxial Fiber Node

Octal Downstream DOCSIS M-CMTS™ Core MAC Chip



BROADCOM



BCM3215 Block Diagram (only one channel of eight shown)

The BCM3215 is a highly integrated octal downstream core MAC chip for use in DOCSIS M-CMTS products. The chip serves as the heart of a next-generation core MAC implementation and significantly increases the density of downstream modules in digital cable modem head-end equipment. The chip features eight channels, each with integrated DOCSIS MAC and M-CMTS functions.

The BCM3215 accepts data packets from the integrated GMII and places them in priority queues. The packets then undergo payload header suppression, DOCSIS header creation, DES/AES encryption, CRC and HCS generation, MPEG encapsulation, and timestamp generation. The BCM3215 supports up to 560 Mbps of any packet size with the ability to queue packets from the GMII interface at the full 1000 Mbps rate.

All configuration of the BCM3215 is done via the GMII interface. The chip supports external DDR SDRAM buffer sizes of 64 MB, 128 MB, or 256 MB, enabling support for up to 512 variable size queues with class-based queuing for traffic prioritization of high, medium, and low priority.

The BCM3215 device's integrated feature set significantly reduces the board space in M-CMTS equipment, giving manufacturers a silicon solution that is both cost-effective and easy to use.

Connecting everything®

BROADCOM CORPORATION
16215 Alton Parkway, P.O. Box 57013
Irvine, California 92619-7013

3215-PB02-RDS 07/18/06

Phone: 949-450-8700
Fax: 949-450-8710
E-mail: info@broadcom.com
Web: www.broadcom.com