

The **QT2022/32** is a fully integrated PHY ICs designed for use in 10Gbps Ethernet and Fibre Channel LAN, WAN and SAN applications. The main physical layer functions of the receiver and transmitter are integrated onto a single chip. The QT2022 is a serial to XAUI bi-directional PHY chip that integrates the XGXS, PCS and PMA layers and supports 10GBASE-R protocol. In addition to the QT2022 features, the QT2032 includes an IEEE802.3ae WAN Interface Sublayer (WIS) for Ethernet over SONET protocol (10GBASE-W). This layer can be bypassed for LAN or SAN applications.

Features

- Complies with IEEE802.3ae specifications for LAN and WAN
- WAN Interface Sublayer (WIS) with bypass
- SONET-compliant output jitter
- Adjustable serial and XAUI output amplitude
- Comprehensive interface with XFP module
- Integrated receive LA
- LOS with adjustable threshold
- Jumbo frame support
- Multiple test features, including loopbacks and PRBS/jitter generators and checkers
- 0.9 W power consumption
- 1.2V power supply
- 15x15mm, 1mm pitch BGA
- Available in leaded or leadfree/RoHS package

Applications

- 10G Ethernet 10GBASE-LRM applications
- XENPAK, XPAK and X2 modules

In the transmit direction, the QT2022/32 converts four differential input 3.125 Gbps lanes (XAUI) into a serial 9.95-10.5 Gbps data stream.

In the receive direction the chip converts an input serial 9.95-10.5 Gbps data stream into four differential output 3.125 Gbps lanes (XAUI).

In WAN mode (10GBASE-W), maximum flexibility is provided by the transmit data clocking and jitter clean-up options. The PHY utilizes proprietary design techniques to achieve industry-leading jitter performance.

The QT2022/32 includes a standard two-wire interface for communicating with external EEPROM and DOM devices. An MDC/MDIO interface provides control and status capability for the IC.

The PHY can be used on a system card interfacing an XFP module, or inside the XENPAK, XPAK or X2 optical modules.

The QT2022/32 fully compliant with the IEEE802.3ae 10GE and ANSI INCITS/T11 10GFC standards, as well as the XENPAK, XPAK, X2 and XFP Multi Source Agreements (MSA).

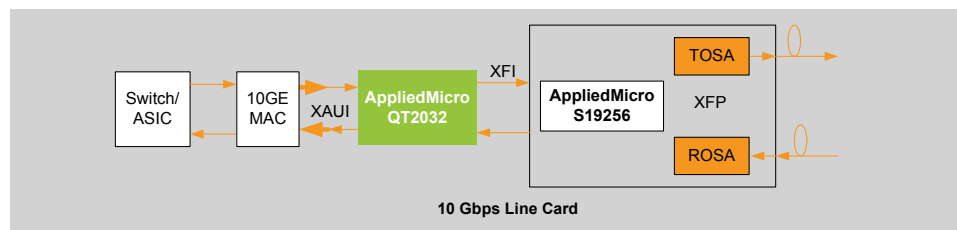
Module Application

The 10 Gbps serial receiver includes a post amplifier (LA) with a high sensitivity of 10mVpp and integrated LOS detector.

System Board Application

The serial interface is compliant with XFP requirements. The built-in receive equalizer successfully recovers data over as much as 12" of standard FR4 printed circuit board. The PHY provides a reference clock to XFP module. XFP status and control information can be accessed through the QT2022/32 interface.

QT2032/22 System Block Diagram



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