HI-8783, HI-8784, HI-8785

ARINC 429 & 561 INTERFACE DEVICE
8 Bit Parallel Data In / ARINC Serial Data Out

March 2007

DESCRIPTION

The HI-8783, HI-8784, and HI-8785 are system components for interfacing 8 bit parallel data to an ARINC 429 bus. The HI-8783 is a logic device only and requires a separate line driver circuit, such as the HI-3182 or HI-8585. The HI-8784 and HI-8785 combine logic and line driver on one chip. The HI-8784 has an output resistance of 37.5 ohms, and the HI-8785 has an output resistance of 10 ohms to facilitate external lightning protection cicuitry. The technology is analog/digital CMOS.

The HI-8783 is available in a 22 pin DIP format as a second source replacement for the Micrel / California Devices DLS-111BV.

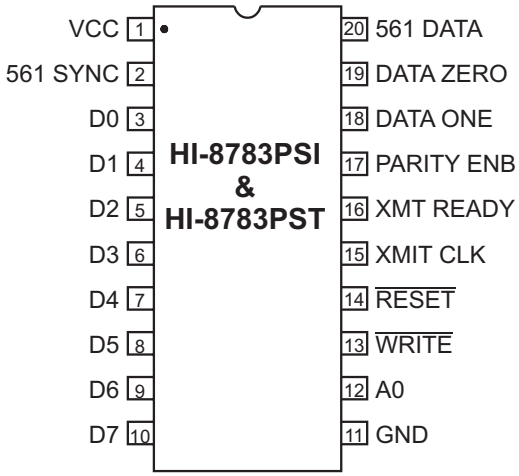
The products offer high speed data bus data transactions to a buffer register. After loading 4 bytes, data is automatically transferred and transmitted. The data rate is equal to the clock rate. Parity can be enabled in the 32nd bit. Reset is used to initialize the logic upon startup. Word gaps are transmitted automatically.

The HI-8784 and HI-8785 require +/- 10 volt supplies in addition to the 5 volt supply.

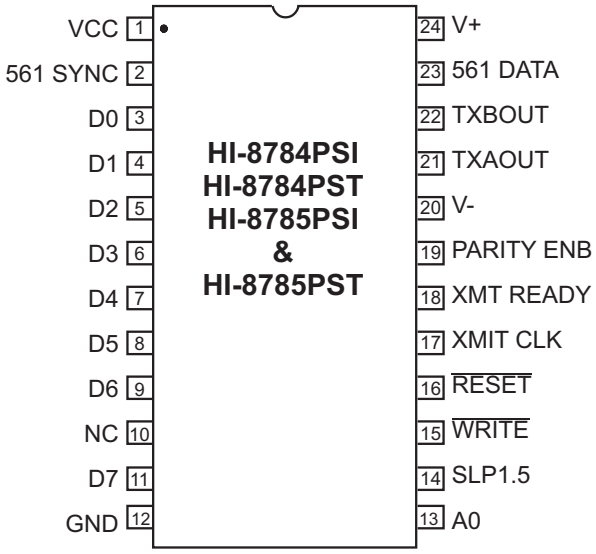
FEATURES

- Automatically converts 8 bit parallel data to ARINC 429 or 561 serial data
- High speed data bus interface
- On-chip line driver option
- SOIC packages available
- Military processing options

PIN CONFIGURATIONS



20-Pin Plastic SOIC - WB package



24-Pin Plastic SOIC - WB package

(See page 7 for additional pin configurations)

PIN DESCRIPTIONS

PIN HI-8783 (20-pin)	PIN HI-8783 (22-pin)	PIN HI-8784 HI-8785	SYMBOL	FUNCTION	DESCRIPTION
1	22	1	VCC	power supply	+5 volt rail,
2	1	2	561 SYNC	digital output	ARINC 561 Sync signal
3-10	2-8,10	3-9,11	Dn	digital inputs	Parallel 8 bit Data Input
11	11	12	GND	power supply	Ground
12	12	13	A0	digital input	Byte address, A0=1 for 1st byte, A0=0 for 2nd, 3rd & 4th bytes
-	-	14	SLP1.5	digital input	Selects the slope of the line driver. High = 1.5us
13	14	15	$\overline{\text{WRITE}}$	digital input	Write strobe, loads data on rising edge
14	15	16	$\overline{\text{RESET}}$	digital input	Registers and sequencing logic initialized when low
15	16	17	XMIT CLK	digital input	Clock input for the transmitter
16	17	18	XMT RDY	digital output	Goes high if the buffer register is empty
17	18	19	PARITY ENB	digital input	When high the 32nd bit output is odd parity
-	-	20	V-	power supply	-10 volt rail
18	19	-	DATA ONE	digital output	Goes high for each ARINC bit output that is a “one”
19	20	-	DATA ZERO	digital output	Goes high for each ARINC bit output that is a “zero”
-	-	21	TXAOUT	analog output	Line driver ouptut - A side
-	-	22	TXBOUT	analog output	Line driver output - B side
20	21	23	561 DATA	digital output	Serial output for ARINC 561 data
-	-	24	V+	power supply	+10 volt rail

FUNCTIONAL DESCRIPTION

The HI-8783 is a parallel to serial converter, which when loaded with four eight bit parallel bytes, outputs the data as a 32 bit serial word. Timing circuitry inserts a 4 bit gap at the end of each 32 bit word. An input buffer register allows load operations to take place while the previously loaded word is being transmitted.

If the PARITY ENB pin is high, the 32nd bit will be a parity bit, inserted so as to make the 32 bit word have odd parity. If the PARITY ENB pin is low, the 32nd bit will be the D7 bit of the 4th byte.

Outputs are provided for both ARINC 429/575 (DATA ONE and DATA ZERO pins) and ARINC 561 (561 DATA and 561 SYNC pins) type data.

A low signal applied to the $\overline{\text{RESET}}$ pin resets the HI-8783’s internal logic so that spurious transmission does not take place during power-up. The registers are cleared so that a continuous gap will be transmitted until the first word is loaded into the transmitter.

Input data can be loaded when the XMT RDY signal is high, which indicates the input buffer register is empty. The first 8 bit byte is the label byte and is loaded with the A0 input high, which initializes the internal byte counter. The remaining three bytes are loaded with A0 in the low state. Once A0 is set low, it must not go high until after the fourth byte is loaded. Each 8 bit byte is loaded into the input buffer register by a low pulse on the $\overline{\text{WRITE}}$ input. After the fourth byte is loaded, the XMT RDY output goes low.

The contents of the input buffer register are transferred to the output register during the fourth bit period of the gap. If the fourth gap bit period of the previous word has already been transmitted, the contents of the input buffer register will be transferred to the output shift register during the first bit period after the loading of the fourth byte, and the XMT RDY output goes high.

After the output shift register is loaded, the data is shifted out to the output logic in the order shown in figure 2.

The 561 SYNC output pulses low when the XMT CLK is low during the 8th bit of the ARINC transmission. The XMIT CLK is the same as the data rate.

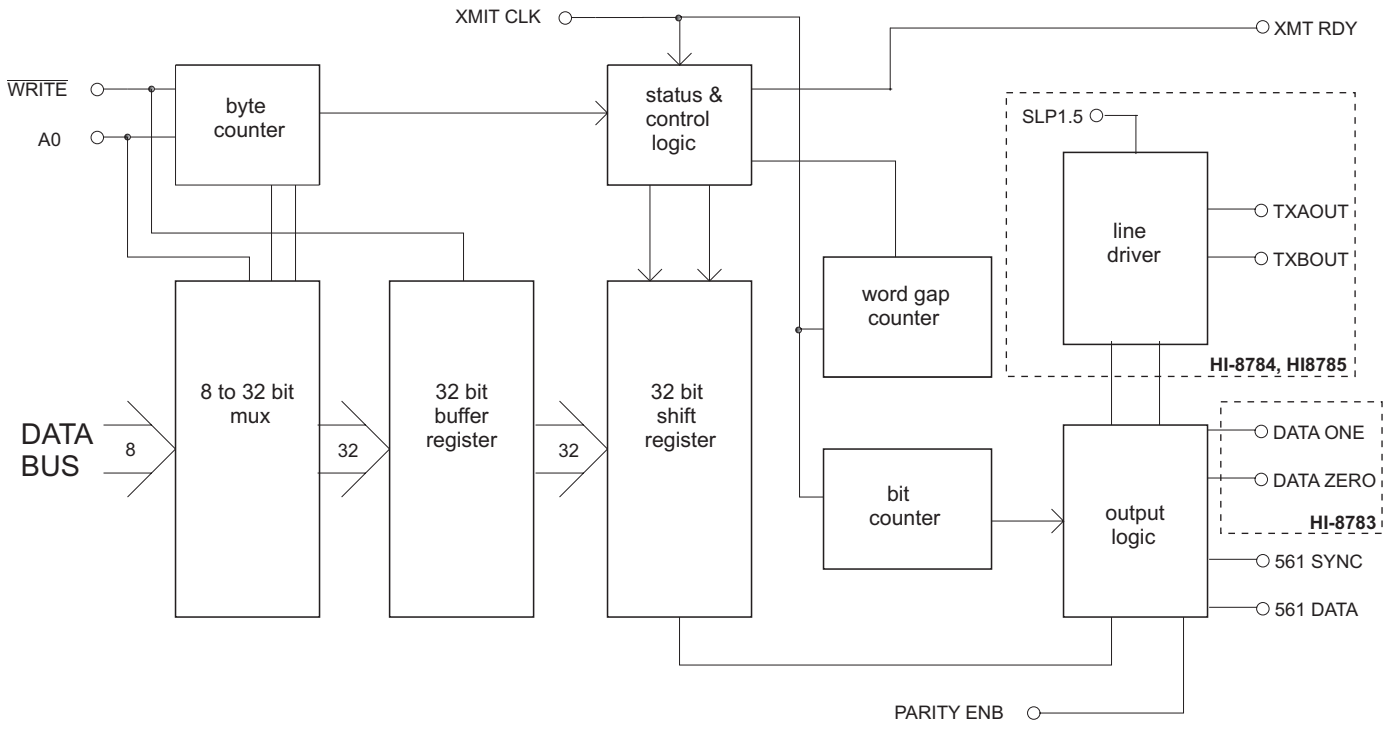


Figure 1. Block Diagram

FUNCTIONAL DESCRIPTION (Cont.)

The HI-8784 and HI-8785 have the same digital logic function as the HI-8783, but include an on-chip line driver designed to directly drive the ARINC 429 bus. The two ARINC outputs (TXAOUT and TXBOUT) provide a differential voltage to produce a +10 volt One, a -10 volt Zero, and a 0 volt Null. The slope of the ARINC outputs is controlled by the SLP1.5 pin. If SLP1.5 is high, the output rise and fall time is nominally 1.5us. If SLP1.5 is set low, the rise and fall times are 10us. DATA ONE and DATA ZERO outputs are not provided for the HI-8784 and HI-8785.

The HI-8784 has 37.5 ohms in series with each line driver output. The HI-8785 has 10.0 ohms in series. The HI-8785 is for applications where external series resistance is needed, typically for lightning protection devices.

A0	Byte	Data Bus	ARINC Bits
1	Byte 1	D0 - D7	ARINC 1 - ARINC 8
0	Byte 2	D0 - D7	ARINC 9 - ARINC 16
0	Byte 3	D0 - D7	ARINC 17 - ARINC 24
0	Byte 4	D0 - D7	ARINC 25 - ARINC 32

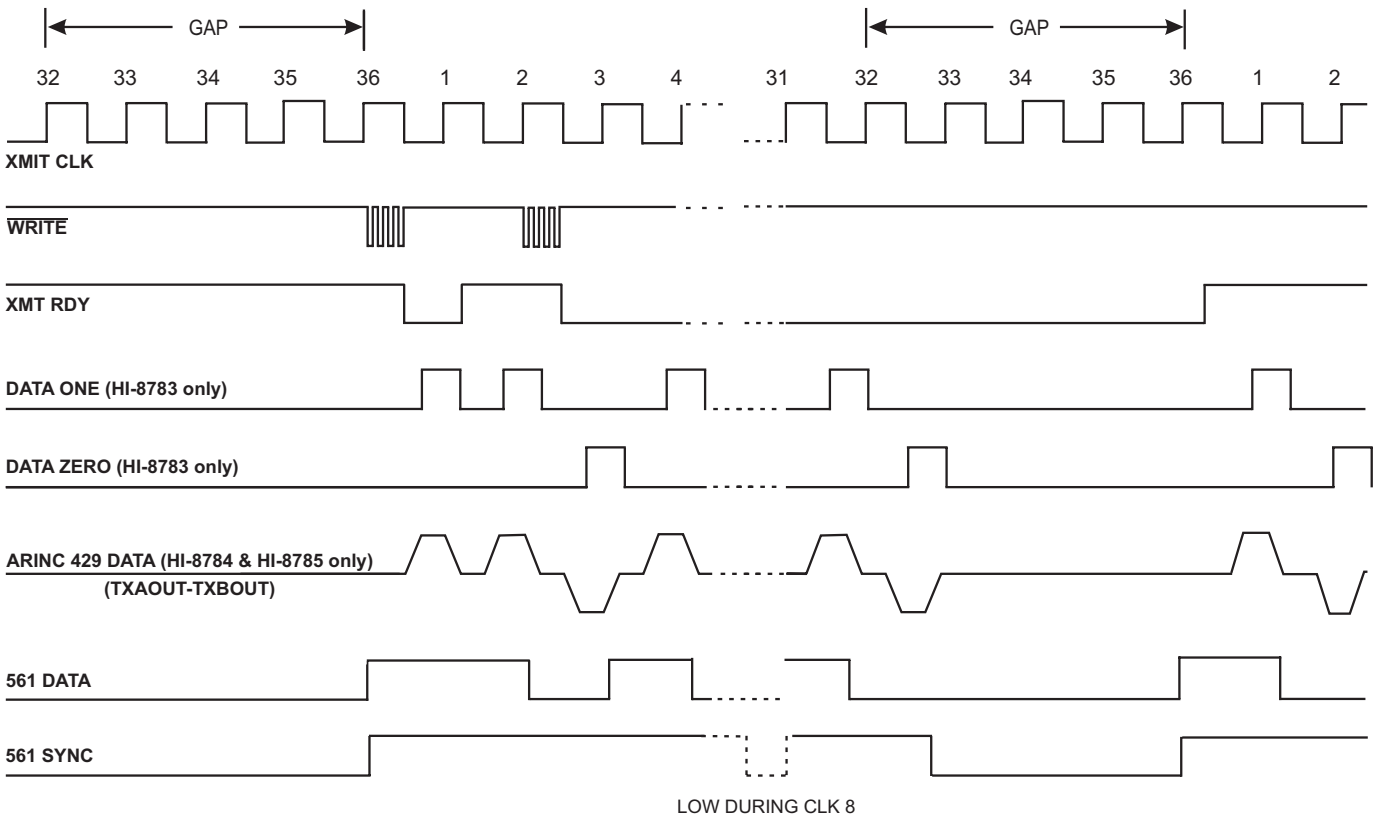
Figure 2. Order of transmitted bytes

POWER SUPPLY SEQUENCING

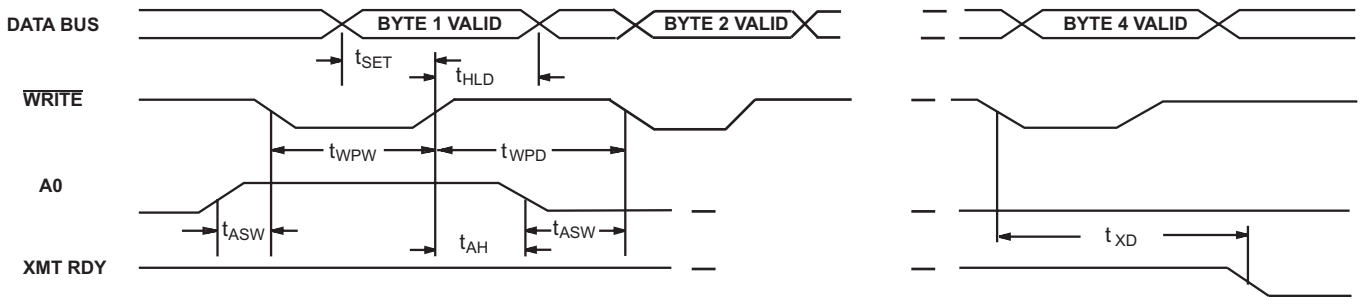
The power supplies must be controlled to prevent large currents during supply turn-on and turn-off. The required sequence is V+ followed by VDD, always ensuring that V+ is the most positive supply. The V- supply is not critical and can be asserted at any time.

TIMING DIAGRAMS

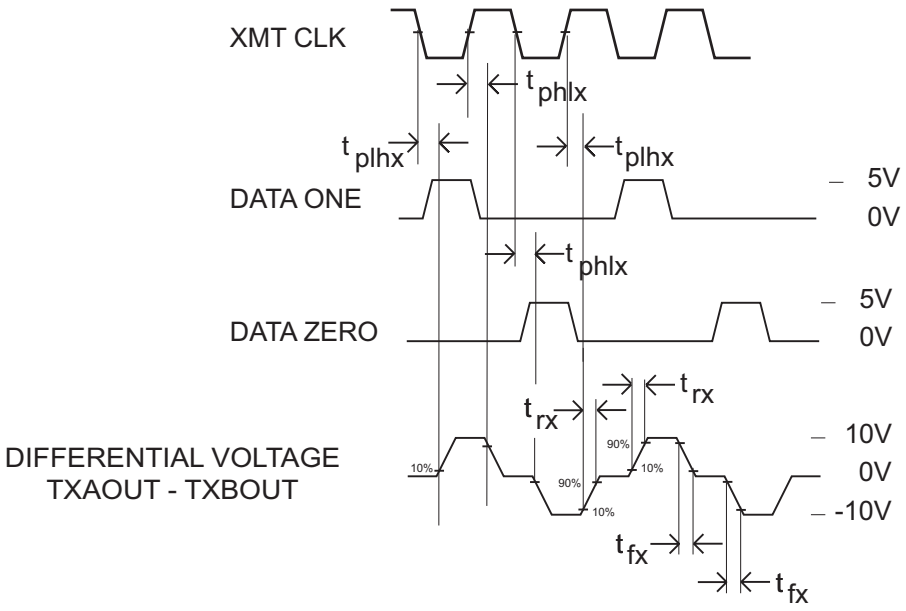
DATA TRANSMISSION - EXAMPLE PATTERN



TRANSMITTER OPERATION



LINE DRIVER OUTPUTS



ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground

Supply voltages
- V+.....12.5V
- V-.....-12.5V
- VCC..... 7V

DC current per input pin..... +10ma

Power dissipation at 25°
- plastic DIL.....1.0W, derate 10mW/°C
- ceramic DIL.....0.5W, derate 7mW/°C

Solder Temperature .....275°C for 10 sec

Storage Temperature.....-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltages
- V+.....+10V... ±5%
- V-..... -10V... ±5%
- VCC..... 5V... ±5%

Temperature Range
- Industrial Screening.....-40°C to +85°C
- Hi-Temp Screening.....-55°C to +125°C
- Military Screening.....-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS (HI-8783, HI-8784 and HI-8785)

VCC = 5.0V, VSS = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Voltage	VCC		4.75	5	5.25	V
Min. Input Voltage (HI)	VIH		2.0	1.4		V
Max. Input Voltage (LO)	VIL			1.4	0.8	V
Min. Input Current (HI)	IIH	VIH = 4.9V			1	µA
Max. Input Current (LO)	IIL	VIL = 0.1V	-1			µA
Min. Output Voltage (HI)	VOH	IOUT = -1.6mA	2.7			V
Max. Output Voltage (LO)	VIH	IOUT = 1.6mA			0.4	V
Operating Current Drain	ICC	f = 100khz		0.8	2.8	mA
Input Capacitance	CIN	Not tested			20	pF

DC ELECTRICAL CHARACTERISTICS (HI-8784 and HI-8785 only)

VCC = 5.0V, V_{SS} = 0V, V+ = 10V, V- = -10V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Voltage	V+		9.5	10	10.5	V
Operating Voltage	V-		-9.5	-10	10.5	V
Operating Current Drain (V+)	I_{DD}	no load, f = 100khz		6	20	mA
Operating Current Drain (V-)	I_{EE}	no load, f = 100khz	-20	-6		mA
Line Driver Output Levels (Ref. To GND)						
ONE		no load, VCC = 5.0V	4.5	5.0	5.5	V
NULL		"	-0.25	0	0.25	V
ZERO		"	-5.55	-5.0	-4.5	V
Line Driver Output Levels (Differential)						
ONE		no load, VCC = 5.0V	9.0	10.0	11.0	V
NULL		"	-0.5	0	0.5	V
ZERO		"	-11.0	-10.0	-9.0	V
Minimum Short Circuit Sink or Source Current	I_{OUT}	momentary magnitude	80			mA

AC ELECTRICAL CHARACTERISTICS (HI-8783, HI-8784 and HI-8785)

VCC = 5.0V, V_{SS} = 0V, T_A =Operating Temperature Range (unless otherwise specified).

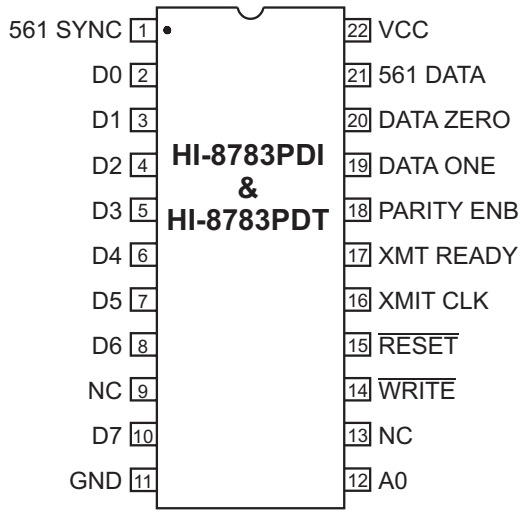
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
DATA BUS TIMING					
Setup Data Bus to $\overline{WRITE}$	t_{SET}	20			ns
Hold $\overline{WRITE}$ to Data Bus	t_{HLD}	30			ns
Hold A0 to $\overline{WRITE}$	t_{AH}	0			ns
Pulse width $\overline{WRITE}$	t_{WPW}	40		1 CLK	ns
Delay between $\overline{WRITE}$	t_{WPD}	40			ns
Setup A0 to $\overline{WRITE}$	t_{ASW}	20			ns
Delay last $\overline{WRITE}$ to XMT RDY	t_{XD}	80			ns

AC ELECTRICAL CHARACTERISTICS (HI-8784 and HI-8785 only)

V+ = 10V, V- = -10V, T_A = Operating Temperature Range (unless otherwise stated)

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Line Driver propagation delay		no load				
Output high to low	t_{phlx}		-	500	-	ns
Output low to high	t_{plhx}		-	500	-	ns
Line Driver transition times						
Output high to low	t_{fx}	SLP1.5 = logic 1	1.0	1.5	2.0	us
Output low to high	t_{rx}	SLP1.5 = logic 1	1.0	1.5	2.0	us
Output high to low	t_{fx}	SLP1.5 = logic 0	5	10	15	us
Output low to high	t_{rx}	SLP1.5 = logic 0	5	10	15	us

ADDITIONAL HI-8783 PIN CONFIGURATION



22 Pin Plastic DIP package

(See page 1 for additional pin configurations)

ORDERING INFORMATION

HI - 87XX xx x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No

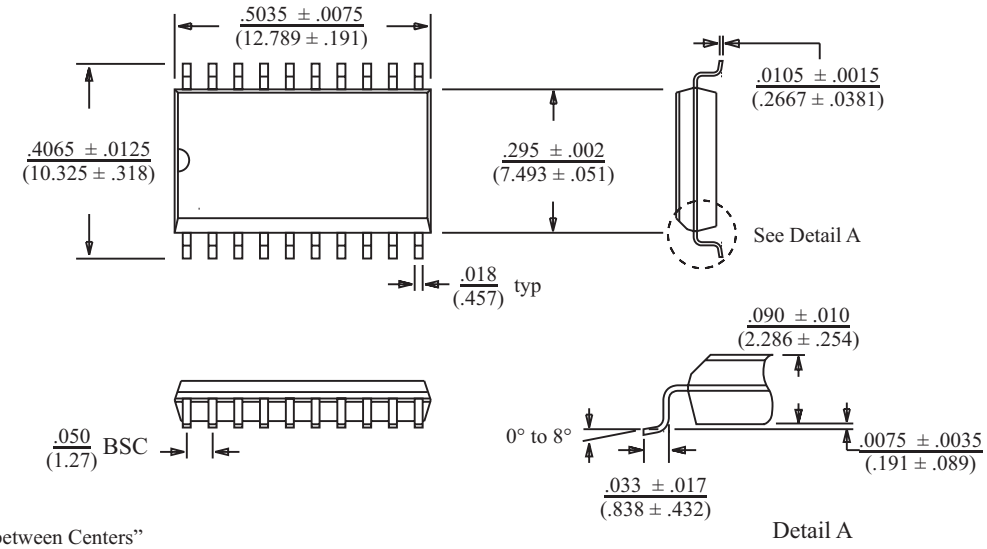
PART NUMBER	PACKAGE DESCRIPTION
PD	22 PIN PLASTIC DIP (22P) (8783 ONLY)
PS	20 PIN PLASTIC WIDE SOIC (20HW) (8783 ONLY)
	24 PIN PLASTIC WIDE SOIC (24HW) (8784 / 8785 ONLY)

PART NUMBER	INCLUDES LINE DRIVER	OUTPUT SERIES RESISTANCE	
		BUILT-IN	REQUIRED EXTERNALLY
8783	No	External Line Driver Required	
8784	Yes	37.5 Ohms	0
8785	Yes	10 Ohms	27.5 Ohms

20-PIN PLASTIC SMALL OUTLINE (SOIC) - WB
(Wide Body)

inches (millimeters)

Package Type: 20HW

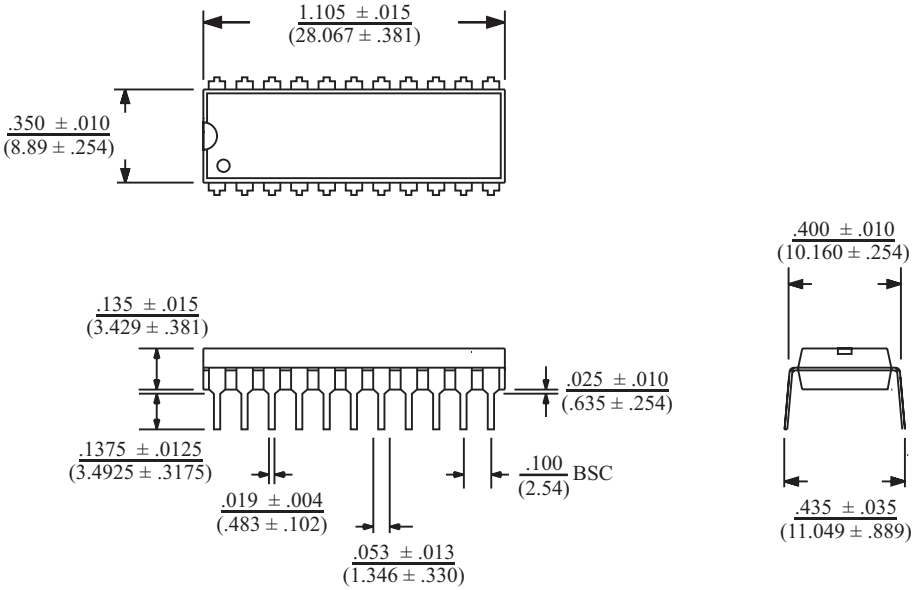


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

22-PIN PLASTIC DIP

inches (millimeters)

Package Type: 22P

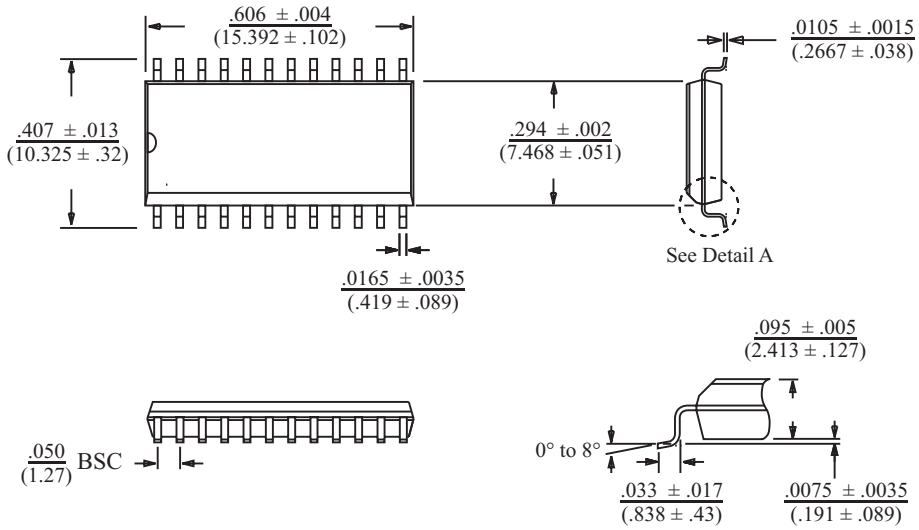


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

24-PIN PLASTIC SMALL OUTLINE (SOIC) - WB
(Wide Body)

inches (millimeters)

Package Type: 24HW



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Detail A