HOLT INTEGRATED CIRCUITS INC.

HI-8282

March 2007

ARINC 429
Serial Transmitter and Dual Receiver

GENERAL DESCRIPTION

The HI-8282 is a silicon gate CMOS device for interfacing the ARINC 429 serial data bus to a 16-bit parallel data bus. Two receivers and an independent transmitter are provided. The receiver input circuitry and logic are designed to meet the ARINC 429 specifications for loading, level detection, timing, and protocol. The transmitter section provides the ARINC 429 communication protocol. An external line driver such as the Holt HI-8585 or HI-3182 is required to translate the 5 volt logic outputs to ARINC 429 drive levels.

The 16-bit parallel data bus exchanges the 32-bit ARINC data word in two steps when either loading the transmitter or interrogating the receivers. The data bus interfaces with CMOS and TTL.

Timing of all the circuitry begins with the master clock input, CLK. For ARINC 429 applications, the master clock frequency is 1 MHz.

Each independent receiver monitors the data stream with a sampling rate 10 times the data rate. The sampling rate is software selectable at either 1MHz or 125KHz. The results of a parity check are available as the 32nd ARINC bit. The HI-8282 examines the null and data timings and will reject erroneous patterns. For example, with a 125 KHz clock selection, the data frequency must be between 10.4 KHz and 15.6 KHz.

The transmitter has a First In, First Out (FIFO) memory to store 8 ARINC words for transmission. The data rate of the transmitter is software selectable by dividing the master clock, CLK, by either 10 or 80. The master clock is used to set the timing of the ARINC transmission within the required resolution.

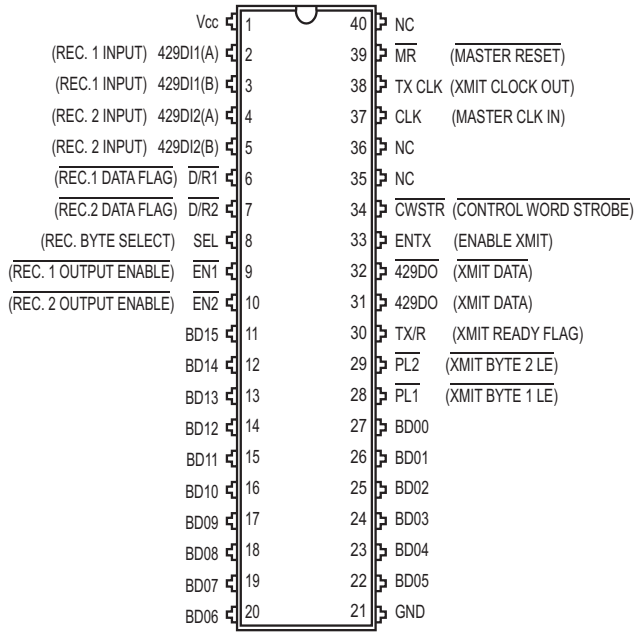
APPLICATIONS

- Avionics data communication
- Serial to parallel conversion
- Parallel to serial conversion

FEATURES

- ARINC specification 429 compliant
- 16-Bit parallel data bus
- Direct receiver interface to ARINC bus
- Timing control 10 times the data rate
- Selectable data clocks
- Receiver error rejection per ARINC specification 429
- Automatic transmitter data timing
- Self test mode
- Parity functions
- Low power, single 5 volt supply
- Industrial & full military temperature ranges
- DSCC SMD part number

PIN CONFIGURATION (Top View)



HI-8282C / CT / CM-01 / CM-03
SMD # 5962-8688002QA

40-Pin Ceramic Side-Brazed DIP

(See page 10 for additional Package Pin Configurations)

PIN DESCRIPTION

SYMBOL	FUNCTION	DESCRIPTION
VCC	POWER	+5V ±5%
429DI1 (A)	INPUT	ARINC receiver 1 positive input
429DI1 (B)	INPUT	ARINC receiver 1 negative input
429DI2 (A)	INPUT	ARINC receiver 2 positive input
429DI2 (B)	INPUT	ARINC receiver 2 negative input
$\overline{\text{D/R1}}$	OUTPUT	Receiver 1 data ready flag
$\overline{\text{D/R2}}$	OUTPUT	Receiver 2 data ready flag
SEL	INPUT	Receiver data byte selection (0 = BYTE 1) (1 = BYTE 2)
$\overline{\text{EN1}}$	INPUT	Data Bus control, enables receiver 1 data to outputs
$\overline{\text{EN2}}$	INPUT	Data Bus control, enables receiver 2 data to outputs if $\overline{\text{EN1}}$ is high
BD15	I/O	Data Bus
BD14	I/O	Data Bus
BD13	I/O	Data Bus
BD12	I/O	Data Bus
BD11	I/O	Data Bus
BD10	I/O	Data Bus
BD09	I/O	Data Bus
BD08	I/O	Data Bus
BD07	I/O	Data Bus
BD06	I/O	Data Bus
GND	POWER	0 V
BD05	I/O	Data Bus
BD04	I/O	Data Bus
BD03	I/O	Data Bus
BD02	I/O	Data Bus
BD01	I/O	Data Bus
BD00	I/O	Data Bus
$\overline{\text{PL1}}$	INPUT	Latch enable for byte 1 entered from data bus to transmitter FIFO.
$\overline{\text{PL2}}$	INPUT	Latch enable for byte 2 entered from data bus to transmitter FIFO. Must follow $\overline{\text{PL1}}$.
TX/R	OUTPUT	Transmitter ready flag. Goes low when ARINC word loaded into FIFO. Goes high after transmission and FIFO empty.
429DO	OUTPUT	"ONES" data output from transmitter.
$\overline{\text{429DO}}$	OUTPUT	"ZEROES" data output from transmitter.
ENTX	INPUT	Enable Transmission
$\overline{\text{CWSTR}}$	INPUT	Clock for control word register
CLK	INPUT	Master Clock input
TX CLK	OUTPUT	Transmitter Clock equal to Master Clock (CLK), divided by either 10 or 80.
$\overline{\text{MR}}$	INPUT	Master Reset, active low

FUNCTIONAL DESCRIPTION

CONTROL WORD REGISTER

The HI-8282 contains 10 data flip flops whose D inputs are connected to the data bus and clocks connected to $\overline{\text{CWSTR}}$. Each flip flop provides options to the user as follows:

DATA BUS PIN	FUNCTION	CONTROL	DESCRIPTION
BDO5	SELF TEST	0 = ENABLE	If enabled, an internal connection is made passing 429DO and $\overline{429DO}$ to the receiver logic inputs
BDO6	RECEIVER 1 DECODER	1 = ENABLE	If enabled, ARINC bits 9 and, 10 must match the next two control word bits
BDO7	-	-	If Receiver 1 Decoder is enabled, the ARINC bit 9 must match this bit
BDO8	-	-	If Receiver 1 Decoder is enabled, the ARINC bit 10 must match this bit
BDO9	RECEIVER 2 DECODER	1 = ENABLE	If enabled, ARINC bits 9 and 10 must match the next two control word bits
BD10	-	-	If Receiver 2 Decoder is enabled, then ARINC bit 9 must match this bit
BD11	-	-	If Receiver 2 Decoder is enabled, then ARINC bit 10 must match this bit
BD12	INVERT XMTR PARITY	1 = ENABLE	Logic 0 enables normal odd parity and Logic 1 enables even parity output in transmitter 32nd bit
BD13	XMTR DATA CLK SELECT	0 = ÷10 1 = ÷80	CLK is divided either by 10 or 80 to obtain XMTR data clock
BD14	RCVR DTA CLK SELECT	0 = ÷10 1 = ÷80	CLK is divided either by 10 or 80 to obtain RCVR data clock

ARINC 429 DATA FORMAT

The following table shows the bit positions in exchanging data with the receiver or the transmitter. ARINC bit 1 is the first bit transmitted or received.

BYTE 1																
DATA BUS	BD 15	BD 14	BD 13	BD 12	BD 11	BD 10	BD 09	BD 08	BD 07	BD 06	BD 05	BD 04	BD 03	BD 02	BD 01	BD 00
ARINC BIT	13	12	11	10	9	31	30	32	1	2	3	4	5	6	7	8

BYTE 2																
DATA BUS	BD 15	BD 14	BD 13	BD 12	BD 11	BD 10	BD 09	BD 08	BD 07	BD 06	BD 05	BD 04	BD 03	BD 02	BD 01	BD 00
ARINC BIT	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14

THE RECEIVERS

ARINC BUS INTERFACE

Figure 1 shows the input circuit for each receiver. The ARINC 429 specification requires the following detection levels:

STATE	DIFFERENTIAL VOLTAGE
ONE	+6.5 Volts to +13 Volts
NULL	+2.5 Volts to -2.5 Volts
ZERO	-6.5 Volts to -13 Volts

The HI-8282 guarantees recognition of these levels with a common mode voltage with respect to GND less than ±4V for the worst case condition (4.75V supply and 13v signal level).

Design tolerances guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the ARINC signal is out of the actual acceptance ranges, including the nulls, the chip rejects the data.

RECEIVER LOGIC OPERATION

Figure 2 (next page) is a block diagram for each receiver's logic.

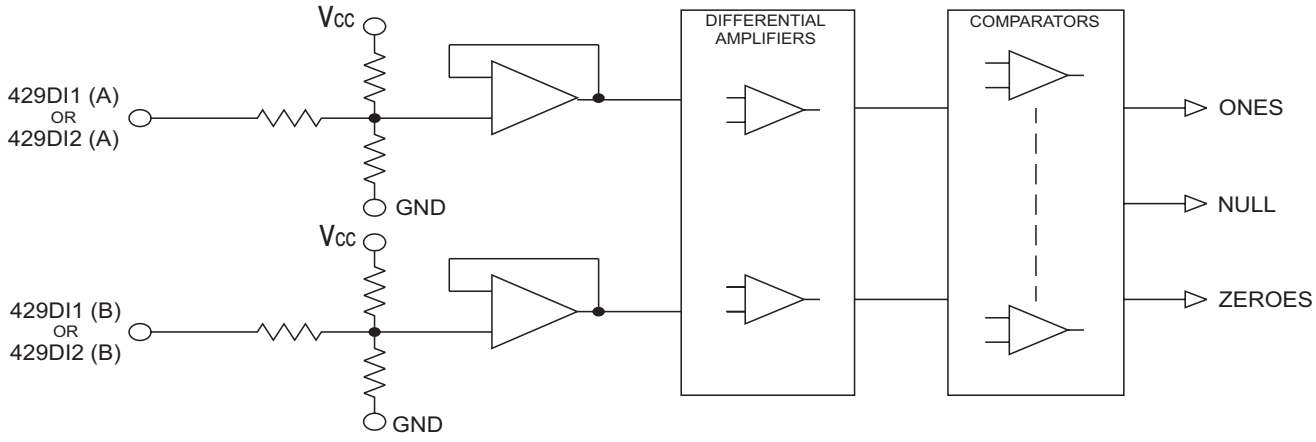


FIGURE 1. **ARINC RECEIVER INPUT**

FUNCTIONAL DESCRIPTION (cont.)

BIT TIMING

The ARINC 429 specification defines the following timing tolerances for received data:

	HIGH SPEED	LOW SPEED
BIT RATE	100K BPS ± 1%	12K -14.5K BPS
PULSE RISE TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSE FALL TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSE WIDTH	5 µsec ± 5%	34.5 to 41.7 µsec

The HI-8282 accepts signals within these tolerances and rejects signals outside these tolerances. Receiver logic achieves this as described below:

1. An accurate 1MHz clock source is required to validate receive signal timing. Less than 0.1% error is recommended.

2. The receiver uses three separate 10-bit sampling shift registers for Ones detection, Zeros detection and Null detection. When the input signal is within the differential voltage range for any shift register's state (One Zero or Null) sampling clocks a high bit into that register. When the receive signal is outside the differential voltage range defined for any shift register, a low bit is clocked. Only one shift register can clock a high bit for any given sample. All three registers clock low bits if the differential input voltage is between defined state voltage bands. Valid data bits require at least three consecutive One or Zero samples (three high bits) in the upper half of the Ones or Zeros sampling shift register, and at least three consecutive Null samples (three high bits) in the lower half of the Null sampling shift register within the data bit interval. A word gap Null requires at least three consecutive Null samples (three high bits) in the upper half of the Null sampling shift register and at least three consecutive Null samples (three high bits) in the lower half of the Null sampling shift register. This guarantees the minimum pulse width.

3. To validate the receive data bit rate, each bit must follow its preceding bit by not less than 8 samples and not more than 12 samples. With exactly 1MHz input clock frequency, the acceptable data bit rates are

	HIGH SPEED	LOW SPEED
DATA BIT RATE MIN	83K BPS	10.4K BPS
DATA BIT RATE MAX	125K BPS	15.6K BPS

4. Following the last data bit of a valid reception, the Word Gap timer samples the Null shift register every 10 input clocks (every 80 clocks for low speed). If a Null is present, the Word Gap counter is incremented. A Word Gap count of 3 enables the next reception.

RECEIVER PARITY

The receiver parity circuit counts Ones received, including the parity bit. If the result is odd, a "0" appears in the 32nd bit.

RETRIEVING DATA

Once 32 valid bits are recognized, the receiver logic generates an End of Sequence (EOS). If the receiver decoder is enabled and the 9th and 10th ARINC bits match the control word program bits or if the receiver decoder is disabled, then EOS clocks the data ready flag flip flop to a "1", $\overline{D/R1}$ or $\overline{D/R2}$ (or both) will go low. The data flag for a receiver will remain low until after both ARINC bytes from that receiver are retrieved. This is accomplished by activating $\overline{EN}$ with byte selector SEL low to retrieve the first byte and activating $\overline{EN}$ with SEL high to retrieve the second byte. $\overline{EN1}$ retrieves data from receiver 1 and $\overline{EN2}$ retrieves data from receiver 2.

If another ARINC word is received and a new EOS occurs before the two bytes are retrieved, the data is overwritten by the new word.

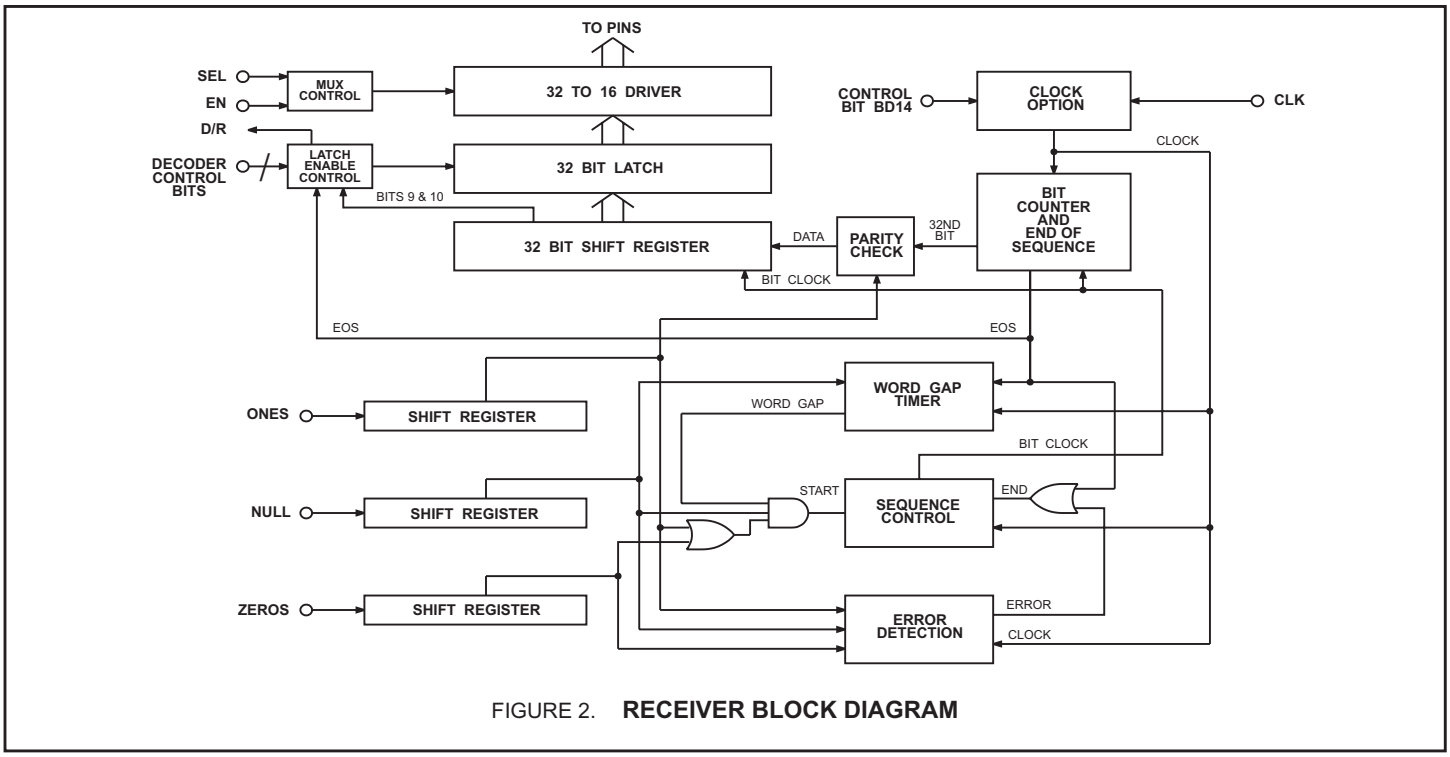


FIGURE 2. **RECEIVER BLOCK DIAGRAM**

FUNCTIONAL DESCRIPTION (cont.)

TRANSMITTER

A block diagram of the transmitter section is shown in Figure 3.

FIFO OPERATION

The FIFO is loaded sequentially by first pulsing $\overline{PL1}$ to load byte 1 and then $\overline{PL2}$ to load byte 2. The control logic automatically loads the 31 bit word in the next available position of the FIFO. If TX/R, the transmitter ready flag, is high (FIFO empty), then 8 words, each 31 bits long, may be loaded. If TX/R is low, then only the available positions may be loaded. If all 8 positions are full, the FIFO ignores further attempts to load data.

DATA TRANSMISSION

When ENTX goes high, enabling transmission, the FIFO positions are incremented with the top register loading into the data transmission shift register. Within 2.5 data clocks the first data bit appears at either 429DO or $\overline{429DO}$. The 31 bits in the data transmission shift register are presented sequentially to the outputs in the ARINC 429 format with the following timing:

	HIGH SPEED	LOW SPEED
ARINC DATA BIT TIME	10 Clocks	80 Clocks
DATA BIT TIME	5 Clocks	40 Clocks
NULL BIT TIME	5 Clocks	40 Clocks
WORD GAP TIME	40 Clocks	320 Clocks

The word counter detects when all loaded positions are transmitted and sets the transmitter ready flag, TX/R, high.

TRANSMITTER PARITY

The parity generator counts the ONES in the 31-bit word. If the BD12 control word bit is set low, the 32nd bit transmitted will make parity odd. If the control bit is high, the parity is even.

SELF TEST

If the BD05 control word bit is set low, the digital outputs of the transmitter are internally connected to the logic inputs of the receivers, bypassing the analog bus interface circuitry. Data to Receiver 1 is as transmitted and data to Receiver 2 is the complement. All data transmitted during self test is also present on the TXA(OUT) and TXB(OUT) line driver outputs.

SYSTEM OPERATION

The two receivers are independent of the transmitter. Therefore, control of data exchanges is strictly at the option of the user. The only restrictions are:

1. The received data may be overwritten if not retrieved within one ARINC word cycle.

2. The FIFO can store 8 words maximum and ignores attempts to load addition data if full.

3. Byte 1 of the transmitter data must be loaded first.

4. Either byte of the received data may be retrieved first. Both bytes must be retrieved to clear the data ready flag.

5. After ENTX, transmission enable, goes high it cannot go low until TX/R, transmitter ready flag, goes high. Otherwise, one ARINC word is lost during transmission.

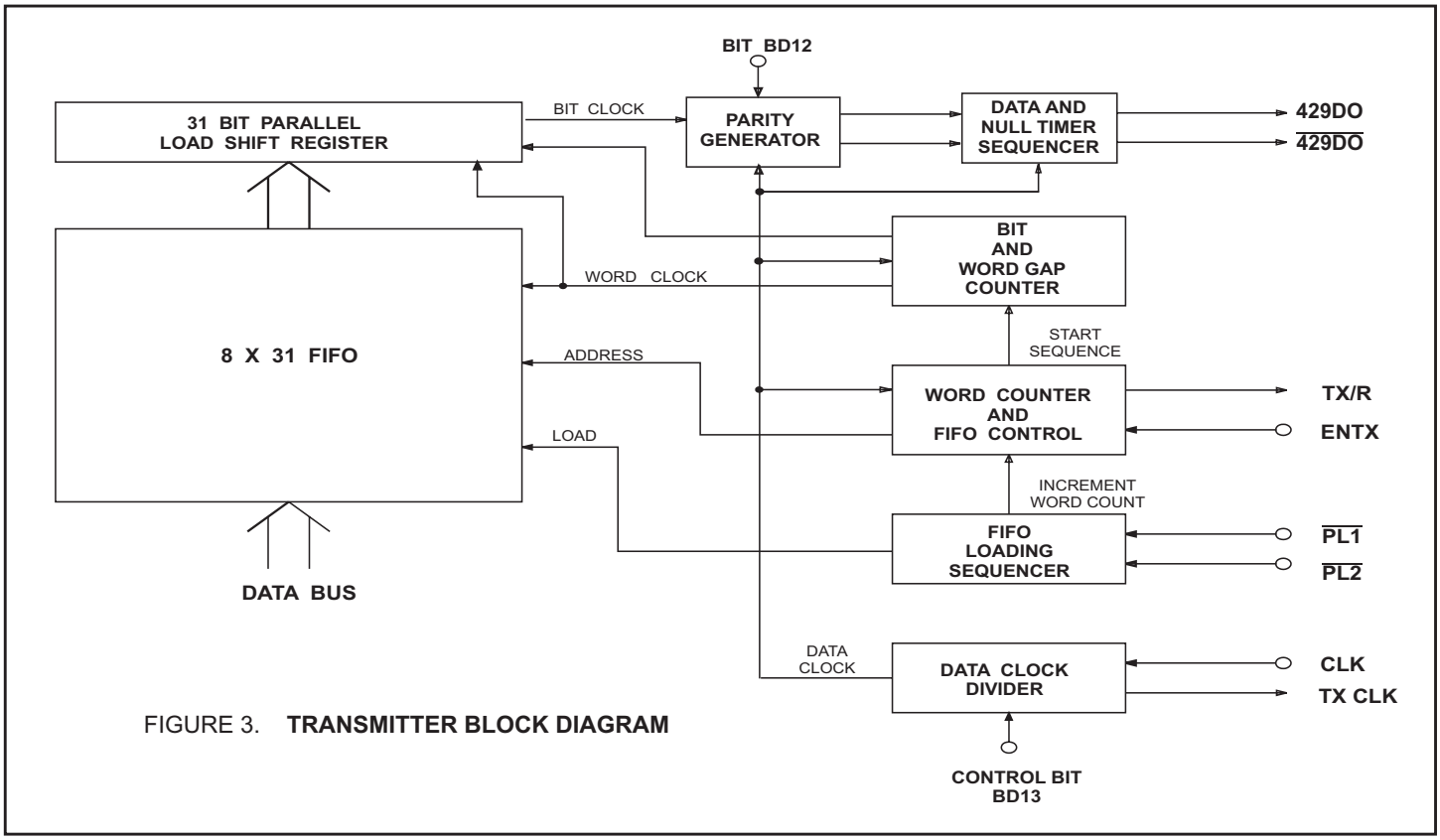


FIGURE 3. **TRANSMITTER BLOCK DIAGRAM**

FUNCTIONAL DESCRIPTION (cont.)

REPEATER OPERATION

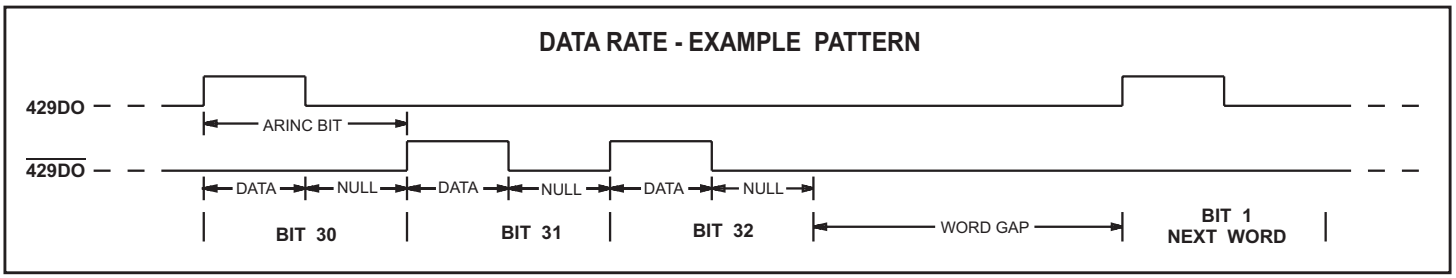
Repeater mode of operation allows a data word received by the HI-8282 to be placed directly into the Transmit FIFO for transmission. After a 32-bit word has been shifted into the receiver shift register, the $\overline{D/R}$ flag goes low. A logic "0" is placed on the SEL line and $\overline{EN}$ is strobed. This is the same procedure as for normal receiver operation, placing the lower byte (16) of the data word on the data bus. By strobing $\overline{PL1}$ at the same time as $\overline{EN}$, the byte is also transferred into the Transmit FIFO. SEL is then taken high and $\overline{EN}$ is strobed again to place the upper data word byte onto the data bus. By strobing $\overline{PL2}$ at the same time as $\overline{EN}$, the second data word byte is also transferred to the Transmit FIFO. The data word is now ready for transmission, according to the parity programmed into the Control Word register.

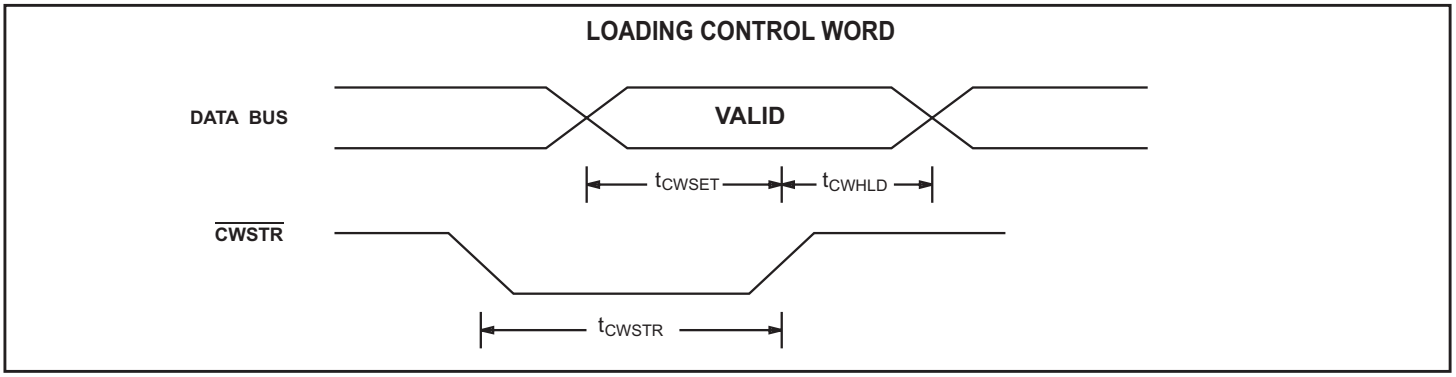
In normal (non-repeater) operation, either byte of the received data word may be read first by using the SEL input. During repeater operation however, data word lower byte must always be read first. While the data is being read, it is loading concurrently into the Transmit FIFO, which always loads lower byte first.

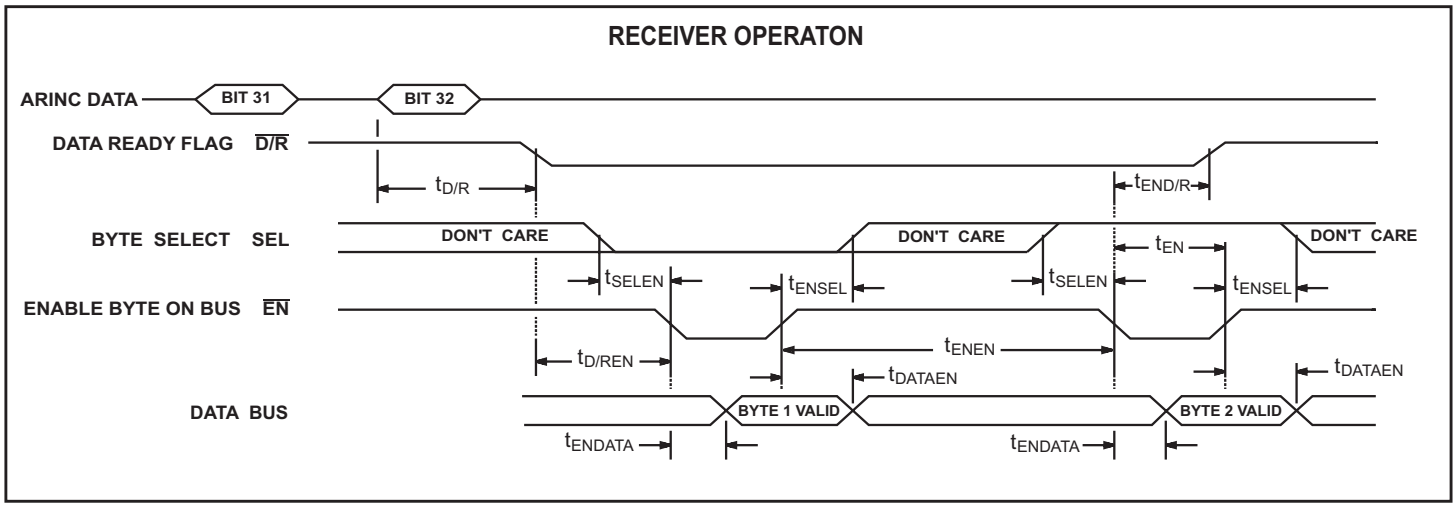
MASTER RESET ($\overline{MR}$)

Upon Master Reset, data transmission and reception are immediately terminated, all three FIFOs are cleared as are the FIFO flags at the device pins and in the Status Register. The Control Word register is not affected by a Master Reset.

TIMING DIAGRAMS

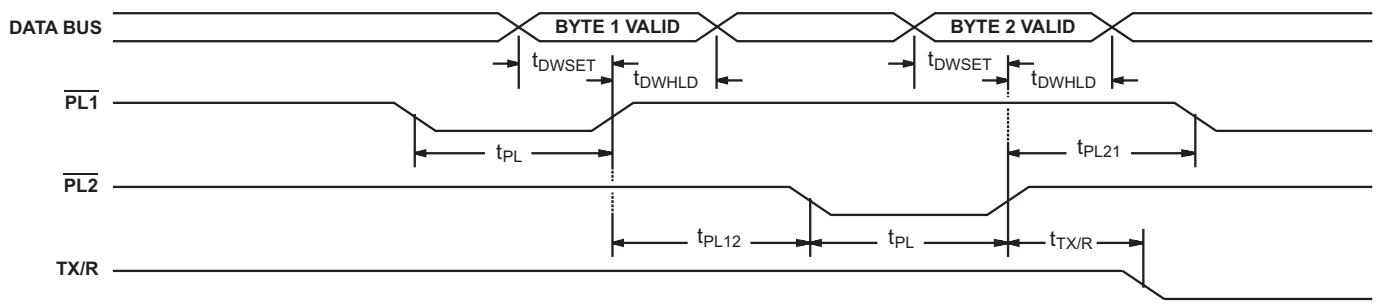




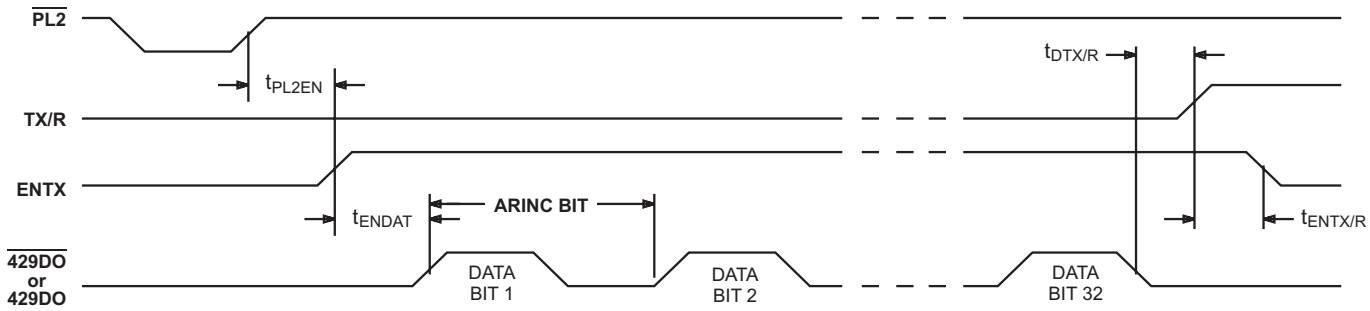


TIMING DIAGRAMS (cont.)

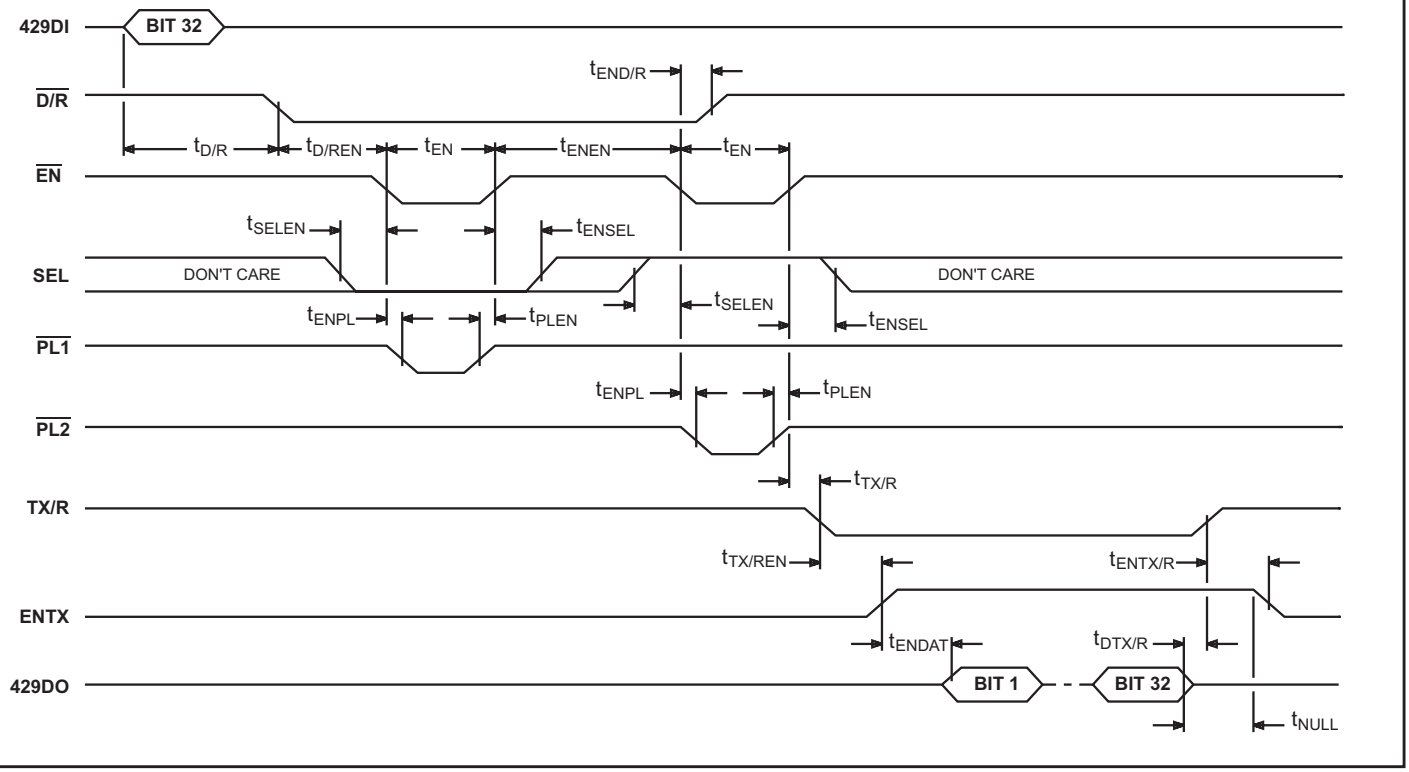
TRANSMITTER OPERATION



TRANSMITTING DATA



REPEATER OPERATION TIMING



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Vcc . . . . . -0.3V to +7V	Power Dissipation 500mW
Voltage at ARINC input pins . . . . . -29V to +29V	Operating Temperature Range: (Industrial) . . . . . -40°C to +85°C
Voltage at any other pin . . . . . -0.3V to Vcc +0.3V	(Military) . . . . . -55°C to +125°C
DC Current Drain per input pin 10mA	Storage Temperature Range: . . . . . -65°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Vcc = 5V ±5%, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER		SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
ARINC INPUTS							
Differential Input Voltage:	ONE	V_{IH}	Pins 2 to 3, 4 to 5: Common mode voltage less than ±4V with respect to GND	6.5	10.0	13.0	V
	ZERO	V_{IL}		-13.0	-10.0	-6.5	V
	NULL	V_{NUL}		-2.5	0	2.5	V
Input Resistance:	Differential	R_I		12			KΩ
	To GND	R_G		12	27		KΩ
	To Vcc	R_H		12	27		kΩ
Input Current:	Input Sink	I_{IH}				200	µA
	Input Source	I_{IL}		-450			µA
Input Capacitance: (Guaranteed but not tested)	Differential	C_I	Pins 2 to 3, 4 to 5			20	pF
	To GND	C_G				20	pF
	To Vcc	C_H				20	pF
BI-DIRECTIONAL INPUTS							
Input Voltage:	Input Voltage HI	V_{IH}		2.1			V
	Input Voltage LO	V_{IL}				0.7	V
Input Current:	Input Sink	I_{IH}				1.5	µA
	Input Source	I_{IL}		-1.5			µA
ALL OTHER INPUTS							
Input Voltage:	Input Voltage HI	V_{IH}		3.5			V
	Input Voltage LO	V_{IL}				0.7	V
Input Current:	Input Sink	I_{IH}				10	µA
	Input Source	I_{IL}		-20			µA
OUTPUTS							
Output Voltage:	Logic "1" Output Voltage	V_{OH}	I_{OH} = -1.5mA	2.7			V
	Logic "0" Output Voltage	V_{OL}	I_{OL} = 1.8mA			0.4	V
Output Current: (Bi-directional Pins)	Output Sink	I_{OL}	V_{OUT} = 0.4V	3.0			mA
	Output Source	I_{OH}	V_{OUT} = Vcc - 0.4V	1.5			mA
Output Current: (All Other Outputs)	Output Sink	I_{OL}	V_{OUT} = 0.4V	3.6			mA
	Output Source	I_{OH}	V_{OUT} = Vcc - 0.4V	1.5			mA
Output Capacitance:		C_O				15	pF
SUPPLY INPUT							
Standby Supply Current:		I_{CC1}				20	mA
Operating Supply Current:		I_{CC2}				20	mA

AC ELECTRICAL CHARACTERISTICS

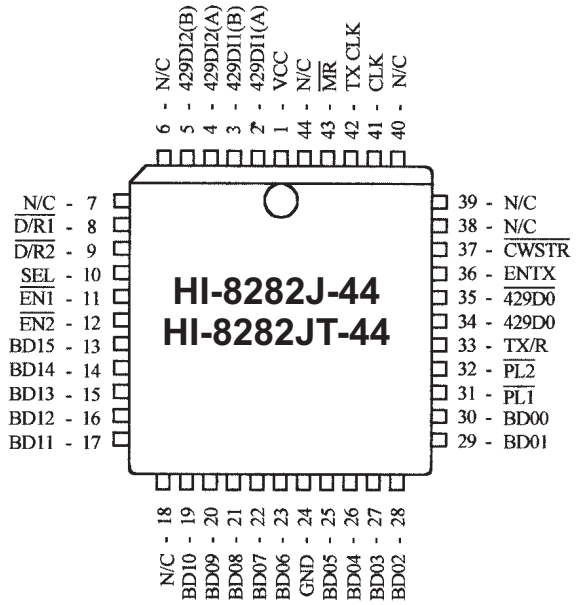
Vcc = 5V, GND = 0V, TA = Operating Temperature Range and fclk = 1MHz ±0.1% with 60/40 duty cycle

PARAMETER	SYMBOL	LIMITS			UNITS
		MIN	TYP	MAX	
CONTROL WORD TIMING					
Pulse Width - $\overline{CWSTR}$	t_{CWSTR}	130			ns
Setup - DATA BUS Valid to $\overline{CWSTR}$ HIGH	t_{CWSET}	140			ns
Hold - $\overline{CWSTR}$ HIGH to DATA BUS Hi-Z	t_{CWHLD}	0			ns
RECEIVER TIMING					
Delay - Start ARINC 32nd Bit to $\overline{D/R}$ LOW: High Speed	$t_{D/R}$			16	µs
Low Speed	$t_{D/R}$			128	µs
Delay - $\overline{D/R}$ LOW to $\overline{EN}$ L0W	$t_{D/REN}$	0			ns
Delay - $\overline{EN}$ LOW to $\overline{D/R}$ HIGH	$t_{END/R}$			200	ns
Setup - SEL to $\overline{EN}$ L0W	t_{SELEN}	20			ns
Hold - SEL to $\overline{EN}$ HIGH	t_{ENSEL}	50			ns
Delay - $\overline{EN}$ L0W to DATA BUS Valid	t_{ENDATA}			200	ns
Delay - $\overline{EN}$ HIGH to DATA BUS Hi-Z	t_{DATAEN}			30	ns
Pulse Width - $\overline{EN1}$ or $\overline{EN2}$	t_{EN}	240			ns
Spacing - $\overline{EN}$ HIGH to next $\overline{EN}$ L0W	t_{ENEN}	50			ns
FIFO TIMING					
Pulse Width - $\overline{PL1}$ or $\overline{PL2}$	t_{PL}	200			ns
Setup - DATA BUS Valid to $\overline{PL}$ HIGH	t_{DWSET}	110			ns
Hold - $\overline{PL}$ HIGH to DATA BUS Hi-Z	t_{DWHLD}	20			ns
Spacing - $\overline{PL1}$ to $\overline{PL2}$	t_{PL12}	0			ns
Spacing - $\overline{PL2}$ to $\overline{PL1}$	t_{PL21}	250			ns
Delay - $\overline{PL2}$ HIGH to TX/R LOW	$t_{TX/R}$			840	ns
TRANSMISSION TIMING					
Spacing - $\overline{PL2}$ HIGH to ENTX HIGH	t_{PL2EN}	0			µs
Delay - ENTX HIGH to TXA(OUT) or TXB(OUT): High Speed	t_{ENDAT}			25	µs
Delay - ENTX HIGH to TXA(OUT) or TXB(OUT): Low Speed	t_{ENDAT}			200	µs
Delay - 32nd ARINC Bit to TX/R HIGH	$t_{DTX/R}$			400	ns
Spacing - TX/R HIGH to ENTX L0W	$t_{ENTX/R}$	0			ns
REPEATER OPERATION TIMING					
Delay - $\overline{EN}$ LOW to $\overline{PL}$ LOW	t_{ENPL}	0			ns
Hold - $\overline{PL}$ HIGH to $\overline{EN}$ HIGH	t_{PLEN}	0			ns
Delay - TX/R LOW to ENTX HIGH	$t_{TX/REN}$	0			ns
Master Reset Pulse Width	t_{MR}	400			ns
ARINC Data Rate and Bit Timing				± 1%	

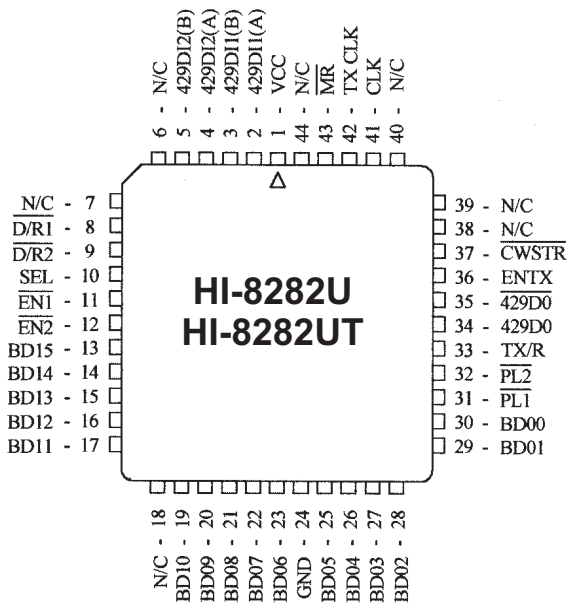
ADDITIONAL HI-8282 PIN CONFIGURATIONS

(See page 1 for the 40-pin Ceramic Side-Brazed DIP Package)

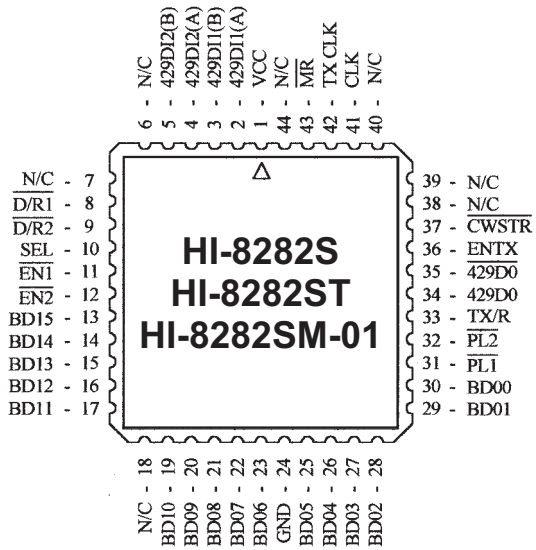
44-PIN PLASTIC PLCC



44-PIN J-LEAD CERQUAD



44-PIN CERAMIC LCC



ORDERING INFORMATION

HI - 8282 x x - xx (Ceramic)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN	NOTES
Blank	-40°C to +85°C	I	No	
T	-55°C to +125°C	T	No	
M-01	-55°C to +125°C	M	Yes	(1)
M-03	-55°C to +125°C	DSCC	Yes	(1) & (2)

PART NUMBER	PACKAGE DESCRIPTION	LEAD FINISH	NOTES
C	40 PIN CERAMIC SIDE BRAZED DIP (40C)	Gold	(3) & (1)
S	44 PIN CERAMIC LEADLESS CHIP CARRIER (44S)	Gold	(3) & (1)
U	44 PIN CERQUAD (44U) not available with 'M' flow	Tin/Lead Solder	

Notes:

(1) Process Flows M and DSCC always have Tin / Lead (Sn/Pb) solder lead finish.

(2) DSSC SMD# 5962-8688002QA. Only available in 'C' package with Sn/Pb solder lead finish.

(3) Gold terminal finish is Pb-Free, RoHS compliant.

HI - 8282J x x - 44 (Plastic)

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
Blank	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION
8282J	44 PIN PLASTIC J LEAD (44J) Note (4)

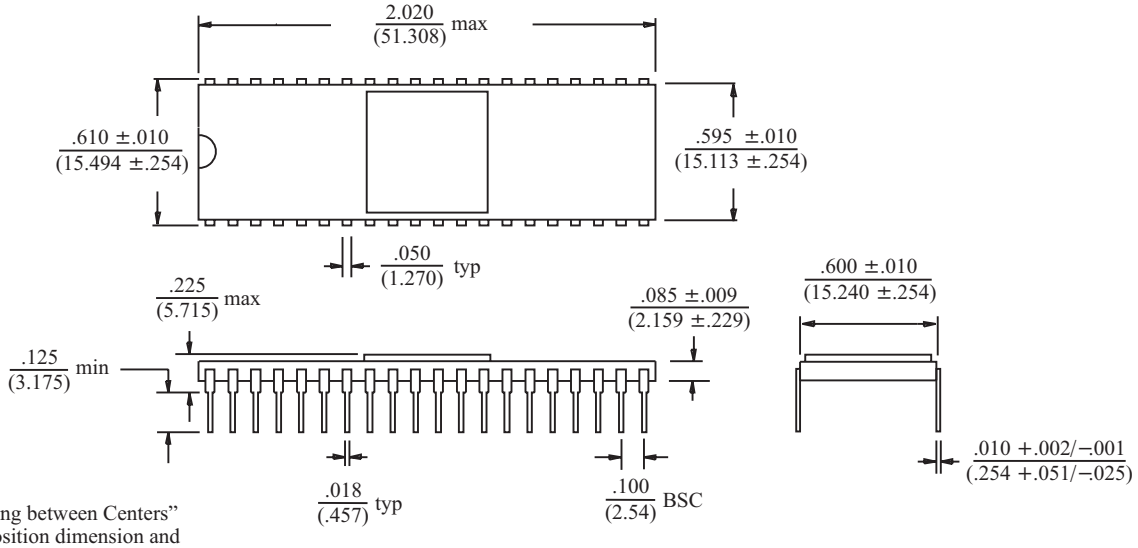
Notes:

(4) NOT RECOMMENDED FOR NEW DESIGNS. The newer HI-8282APJI and HI-8282APJT replace the HI-8282J-44 and HI-8282JT-44 respectively. The HI-8282A parts are rated as Moisture Sensitive Level 1 (MSL 1) and do not require any special handling. The older HI-8282J-44 and HI-8282JT-44 are rated as MSL 3 and require dry-packaging and /or bake-out in accordance with IPC/JEDEC J-STD-020A.

40-PIN CERAMIC SIDE-BRAZED DIP

inches (millimeters)

Package Type: 40C

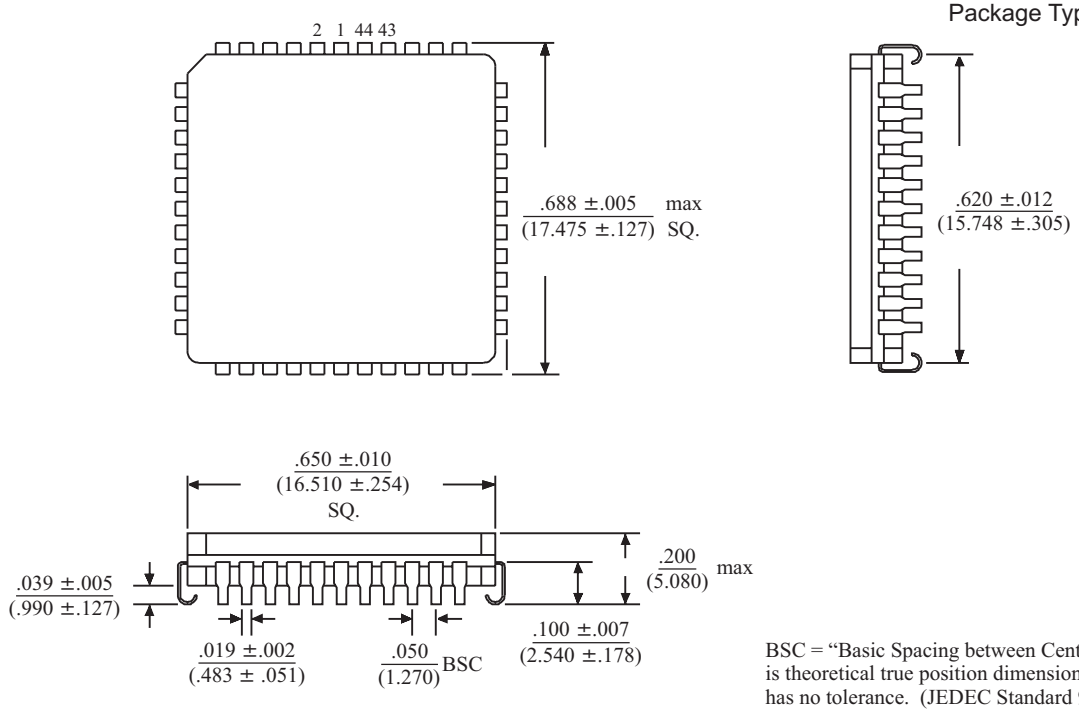


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN J-LEAD CERQUAD

inches (millimeters)

Package Type: 44U

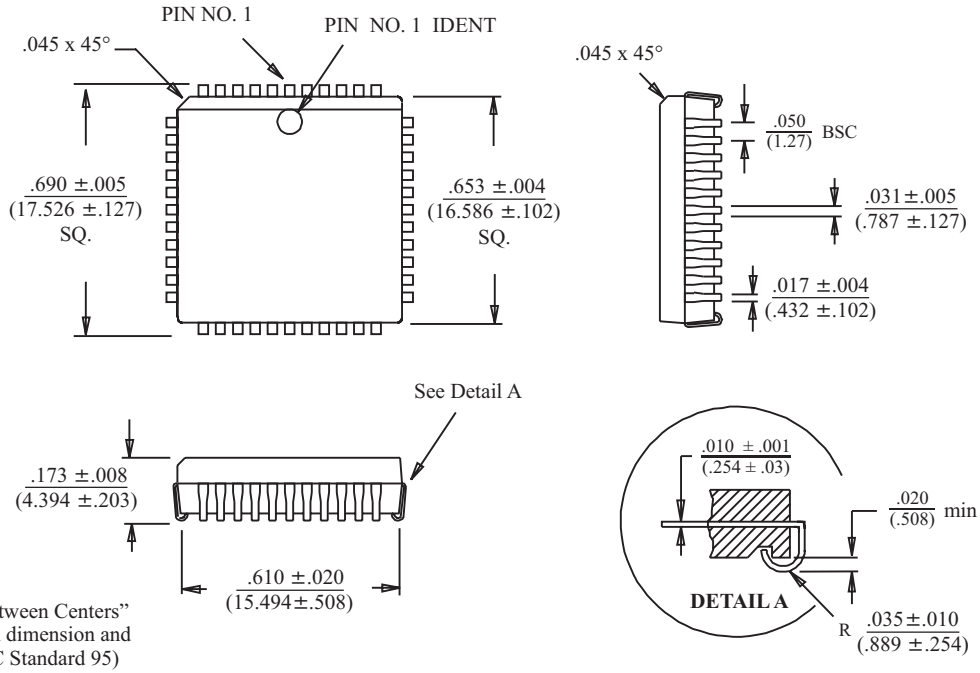


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC PLCC

inches (millimeters)

Package Type: 44J

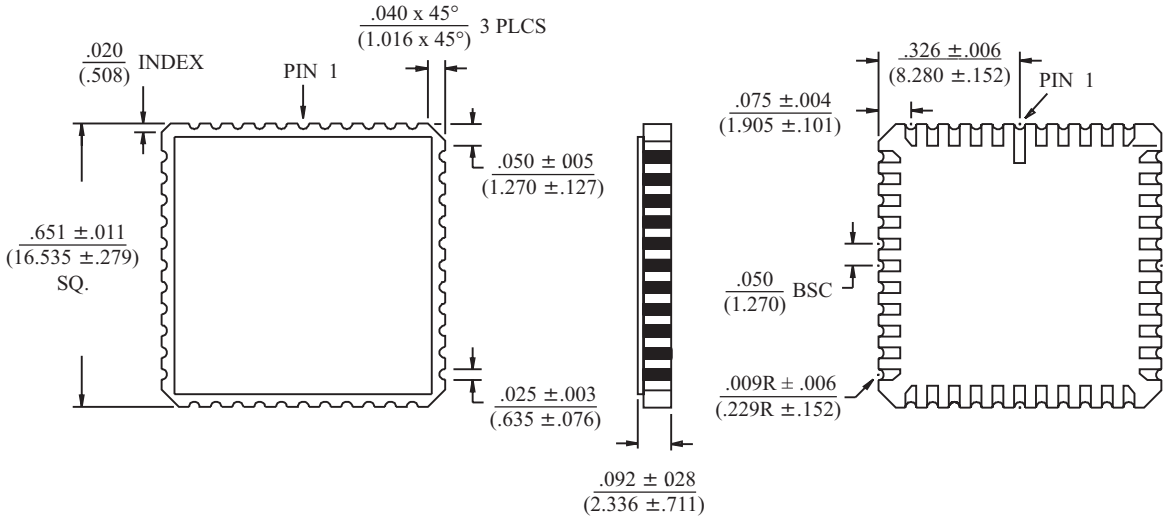


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN CERAMIC LEADLESS CHIP CARRIER

inches (millimeters)

Package Type: 44S



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)