HOLT INTEGRATED CIRCUITS

HI-8590

January 2001

ARINC 429 LINE DRIVER AND LINE RECEIVER

DESCRIPTION

The HI-8590 is a CMOS integrated circuit with independent ARINC 429 line driver and line receiver in a single 16 pin package. Both ARINC 429 functions are implemented in analog/digital CMOS.

The line driver function in the HI-8590 connects directly to the ARINC bus and translates CMOS/TTL input levels to ARINC 429 specified amplitudes using built-in zeners. The slope of the differential output signal is controlled by a single logic input without the use of any external capacitors. A internal 37.5 ohm resistor is provided in series with each line driver output. The line driver function is the same as Holt's 8 pin stand-alone HI-8585 line driver.

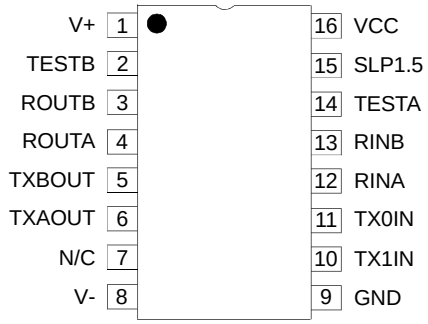
The line receiver interfaces directly to the ARINC 429 bus and translates incoming ARINC levels to levels compatible with CMOS logic. Internal comparator levels are set just below the standard 6.5 volt minimum data threshold and just above the standard 2.5 volt maximum null threshold

The TESTA and TESTB inputs of the line receiver allow bypassing the analog input circuitry for testing purposes. Also, if both test inputs are taken high, the receiver's digital outputs are tri-stated allowing wire-or possibilities. The line driver function is the same as Holt's 8 pin stand-alone HI-8588 line receiver.

FEATURES

- Direct ARINC 429 interface to line driver and line receiver
- Both functions in a single 16 pin package
- Line Driver
  - Internal zener sets output levels
  - Digital output slope control
  - CMOS/TTL logic pins
- Line Receiver
  - Input hystersis at least 2 volts
  - Test inputs bypass analog inputs
  - Output tri-state mode
- Plastic thermally enhanced surface mount (ESOIC) package
- Mil-temperature range available

PIN CONFIGURATION



SUPPLY VOLTAGES

Vcc = +5V ± 5%
V+ = 12V to 15V
V- = -12V to -15V

PIN DESCRIPTION TABLE

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	V+	POWER	+12 TO + 15 VOLTS
2	TESTB	LOGIC INPUT	CMOS
3	ROUTB	LOGIC OUTPUT	RECEIVER CMOS OUTPUT B
4	ROUTA	LOGIC OUTPUT	RECEIVER CMOS OUTPUT A
5	TXBOUT	ARINC OUTPUT	LINE DRIVER TERMINAL B
6	TXAOUT	ARINC OUTPUT	LINE DRIVER TERMINAL A
7	N/C	NO CONNECT	
8	V-	POWER	-12 TO -15 VOLTS
9	GND	POWER	GROUND
10	TX1IN	LOGIC INPUT	CMOS OR TTL
11	TX0IN	LOGIC INPUT	CMOS OR TTL
12	RINA	ARINC INPUT	RECEIVER A INPUT
13	RINB	ARINC INPUT	RECEIVER B INPUT
14	TESTA	LOGIC INPUT	CMOS
15	SLP1.5	LOGIC INPUT	CMOS OR TTL, V+ IS OK
16	VCC	POWER	+5 VOLT SUPPLY

FUNCTION TABLES

LINE DRIVER

TX1IN	TX0IN	SLP1.5	TXAOUT	TXBOUT	SLOPE
0	0	X	0V	0V	N /A
0	1	0	-5V	5V	10µs
0	1	1	-5V	5V	1.5µs
1	0	0	5V	-5V	10µs
1	0	1	5V	-5V	1.5µs
1	1	X	0V	0V	N /A

LINE RECEIVER

RINA	RINB	TESTA	TESTB	ROUTA	ROUTB
-1.25V to 1.25V	-1.25V to 1.25V	0	0	0	0
-3.25V to -6.5V	3.25V to 6.5V	0	0	0	1
3.25V to 6.5V	-3.25V to -6.5V	0	0	1	0
X	X	0	1	0	1
X	X	1	0	1	0
X	X	1	1	HI-Z	HI-Z

FUNCTIONAL DESCRIPTION

LINE DRIVER

Figure 1 is a block diagram of the line driver. The +5V and -5V levels are generated internally using on-chip zeners. Currents for slope control are set by zener voltages across on-chip resistors.

The TX0IN and TX1IN inputs receive logic signals from a control transmitter chip such as the HI-6010 or HI-8282. TXAOUT and TXBOUT hold each side of the ARINC bus at Ground until one of the inputs becomes a One. If for example TX1IN goes high, a charging path is enabled to 5V on an "A" side internal capacitor while the "B" side is enabled to -5V. The charging current is selected by the SLP1.5 pin. If SLP1.5 is high, the capacitor is nominally charged from 10% to 90% in 1.5µs. If low, the rise and fall times are 10µs.

A unity gain buffer receives the internally generated slopes and differentially drives the ARINC line. Current is limited by the series output resistors at each pin. There are no fuses in series with the ARINC outputs of the HI-8590 as exists on the HI-8382.

The HI-8590 has 37.5 ohms in series with each ARINC output just like the HI-8585. The HI-8586 has 10 ohms in series. The HI-8586 is used with the HI-8588 for applications where more series resistance is added externally, typically for lightning protection devices.

The line driver inputs TX1IN, TX0IN, & SLP1.5 must be tied to either a logic high or low if not used.

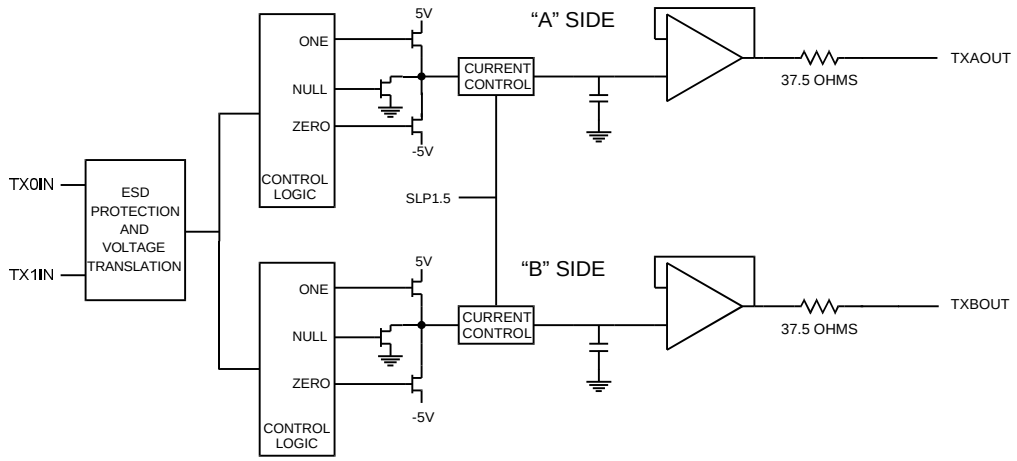


FIGURE 1 - LINE DRIVER BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION (cont.)

RECEIVER

Figure 2 shows the general architecture of the ARINC 429 receiver. The receiver operates off the VCC supply only. The inputs RINA and RINB each have series resistors, typically 35K ohms. They connect to level translators whose resistance to Ground is typically 10K ohms. Therefore, any series resistance added to the inputs will affect the voltage translation.

After level translation, the inputs are buffered and become inputs to a differential amplifier. The amplitude of the differential signal is compared to levels derived from a divider between VCC and Ground. The nominal settings correspond to a One/Zero amplitude of 6.0V and a Null amplitude of 3.3V.

The status of the ARINC receiver input is latched. A Null input resets the latches and a One or Zero input sets the latches.

The logic at the output is controlled by the test signal which is generated by the logical OR of the TESTA and TESTB pins. The receiver output pins float if both TESTA and TESTB are a logic One.

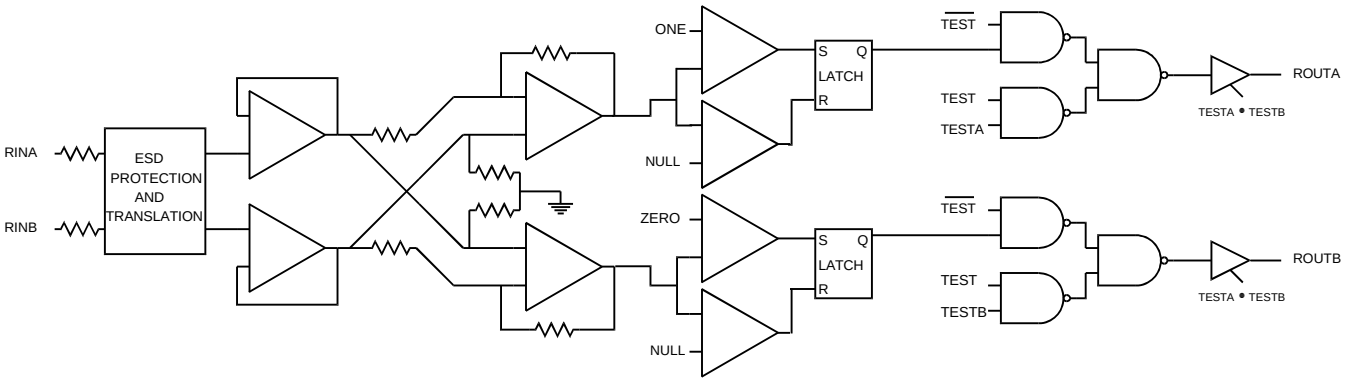


FIGURE 2 - RECEIVER BLOCK DIAGRAM

APPLICATION INFORMATION

Figure 3 shows a possible application of the HI-8590 interfacing both the ARINC transmit and receive channels of a HI-6010 which in turn interfaces to an 8-bit microprocessor bus.

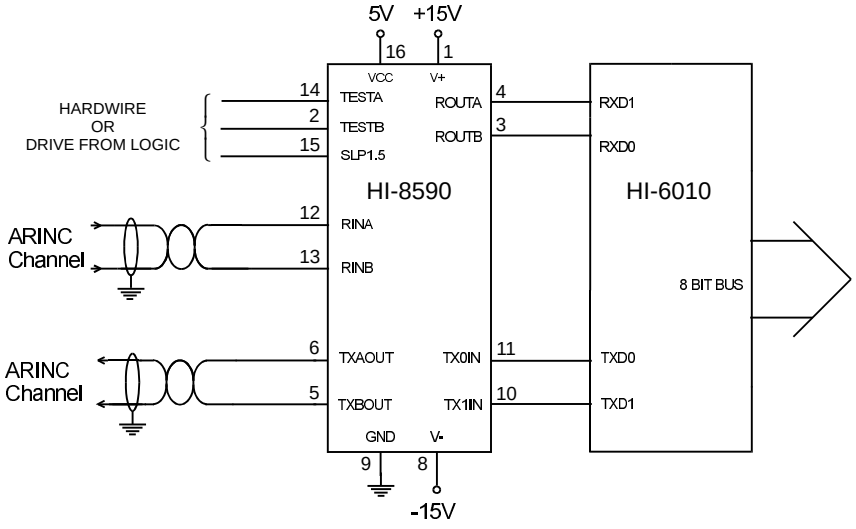


FIGURE 3 - APPLICATION DIAGRAM

ABSOLUTE MAXIMUM RATINGS

All voltages referenced to GND

Supply voltages
- V_{CC} ..... +7.0V
- V+..... +20V
- V- ..... -20V

Voltage on inputs
- ARINC pin ..... +29V to - 29V
- TX1IN, TX0IN or SLP1.5 ...-0.3 to V+ +0.3
- All other input pins.....-0.3 to V_{CC} +0.3

DC current per input pin ..... +10mA

Power dissipation at 25°C
- Plastic SO 1.0W

Thermal Resistance - Φja ..... 98°C/W

Solder Temperature
- Leads ..... +280°C for 10 sec
- Package body .....+220°C

Storage Temperature ..... -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltages
- Vcc .....+5V ± 5%
- V+.....+12V ± 5% or +15V ±10%
- V-.....-12V ± 5% or -15V ±10%

Temperature Range
- Industrial Screening ..... -40°C to +85°C
- Hi-Temp Screening ..... -55°C to +125°C

Junction Temperature, Tj ..... ≤+175°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

Vcc = 5V ±5%, V+ = 12V to 15V, V- = -12V to -15V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Line Driver						
Input voltage (TX1IN, TX0IN, SLP1.5) high low	 V_{IH} V_{IL}		 2.1 -	 - -	 V+ 0.5	 volts volts
Input current (TX1IN, TX0IN, SLP1.5) source sink	 I_{IH} I_{IL}	 V_{IN} = 0V V_{IN} = 5V	 - -	 - -	 0.1 0.1	 µA µA
ARINC output voltage (TXAOUT, TXBOUT) one or zero null	 V_{DOUT} V_{NOUT}	 magnitude at pin & no load " " " " "	 4.50 -0.25	 5.00 -	 5.50 0.25	 volts volts
ARINC output impedance (TXAOUT, TXBOUT)	Z_{OUT}	Note1	-	37.5	-	ohm

Notes :

1. The output resistance is checked by measuring the momentary short circuit current at each ARINC output pin.

DC ELECTRICAL CHARACTERISTICS (cont.)

Vcc = 5V ±5%, V+ = 12V to 15V, V- = -12V to -15V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Line Receiver						
ARINC input voltage (RINA, RINB)						
one or zero	V_{DIN}	differential voltage	6.5	10.0	13.0	volts
null	V_{NIN}	" "	-	-	2.5	volts
common mode	V_{COM}	with respect to GND	-	-	5.0	volts
Logic input voltage (TESTA, TESTB)						
high	V_{IH}		3.5	-	-	volts
low	V_{IL}		-	-	1.5	volts
ARINC input resistance						
RINA to RINB	R_{DIFF}	supplies floating	30	75	-	Kohm
RINA or RINB to GND or V_{CC}	R_{SUP}	" "	19	40	-	Kohm
Logic input current (TESTA, TESTB)						
source	I_{IH}	V_{IN} = 0V	-	-	0.1	µA
sink	I_{IL}	V_{IN} = 5V	-	-	0.1	µA
Logic output current (ROUTA, ROUTB)						
one	I_{OH}	V_{OH} = 4.6V	-	-1.6	-0.8	mA
zero	I_{OL}	V_{OL} = 0.4V	3.6	5.6	-	mA
Operating Supply Current						
V_{CC} - operating (TESTA & TESTB = 0V)	I_{CC}	RINA, RINB open V+ = +15V	-	5.3	8.5	mA
V+	I_{DD}	no load SLP1.5 = V+ TX1IN, TX0IN = 0V	-	6.0	12.0	mA
V-	I_{EE}		-12.0	-6.0	-	mA

AC ELECTRICAL CHARACTERISTICS

Vcc = 5V ±5%, V+ = 12V to 15V, V- = -12V to -15V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Line Driver						
Propagation delay		defined in Figure 4, no load				
Output high to low	t_{phlx}		-	500	-	ns
Output low to high	t_{plhx}		-	500	-	ns
Transition times						
Output high to low & low to high	t_{fx} & t_{rx}	SLP1.5 = logic 1	1.0	1.5	2.0	µs
Output high to low & low to high	t_{fx} & t_{rx}	SLP1.5 = logic 0	5	10	15	µs
Line driver input capacitance						
Logic	C_{IN}	Guaranteed but not tested	-	-	10	pF

AC ELECTRICAL CHARACTERISTICS (cont.)

Vcc = 5V ±5%, V+ = 12V to 15V, V- = -12V to -15V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Line Receiver						
Propagation delay		defined in Figure 5, C_L = 50pF				
Output high to low	t_{phlr}		-	600	-	ns
Output low to high	t_{plhr}		-	600	-	ns
Transition times						
Output high to low	t_{fr}		-	50	80	ns
Output low to high	t_{rr}		-	50	80	ns
Line receiver input capacitance (1)						
ARINC differential	C_{AD}		-	5	10	pF
ARINC single ended to GND	C_{AS}		-	-	10	pF
Logic	C_{IN}		-	-	10	pF

Notes:
1. Guaranteed but not tested

HI-8590 PACKAGE THERMAL CHARACTERISTICS

MAXIMUM ARINC LOAD

PACKAGE STYLE [1]	ARINC 429 DATA RATE	SUPPLY CURRENT (mA) [2]			JUNCTION TEMP, Tj (°C)		
		Ta = 25°C	Ta = 85°C	Ta=125°C	Ta = 25°C	Ta = 85°C	Ta=125°C
16 Lead Plastic SOIC [5]	Low Speed [3]	16.7	16.8	16.9	52	112	150
	High Speed [4]	27.1	26.3	26.1	68	121	162

TXAOUT and TXBOUT Shorted to Ground [6, 7]

PACKAGE STYLE [1]	ARINC 429 DATA RATE	SUPPLY CURRENT (mA) [2]			JUNCTION TEMP, Tj (°C)		
		Ta = 25°C	Ta = 85°C	Ta=125°C	Ta = 25°C	Ta = 85°C	Ta=125°C
16 Lead Plastic SOIC [5]	Low Speed [3]	51.3	46.4	45.7	117	168	194
	High Speed [4]	46.0	39.7	39.5	122	171	206

Notes:
1. All data taken on devices soldered to single layer copper PCB (3" X 4.5" X .062").
2. At 100% duty cycle, 15V power supplies. For 12V power supplies multiply all tabulated values by 0.8.
3. Low Speed: Data Rate = 12.5 Kbps, Load: R = 400 Ohms, C = 30 nF.
4. High Speed: Data Rate = 100 Kbps, Load: R = 400 Ohms, C = 10 nF. Data not presented for C = 30 nF as this is considered unrealistic for high speed operation.
5. 16 Lead Plastic SOIC (Thermally enhanced with built-in heat sink).
6. Similar results would be obtained with TXAOUT shorted to TXBOUT.
7. For applications requiring survival with continuous short circuit, operation above Tj = 175°C is not recommended.

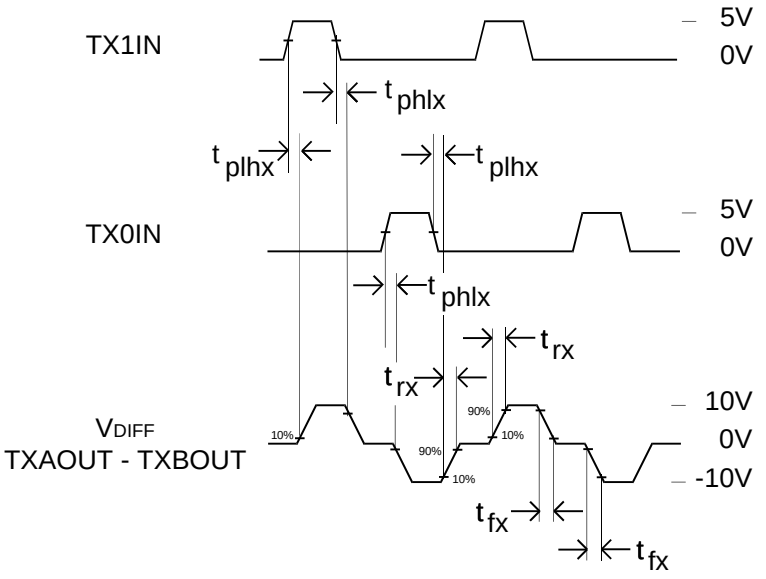


FIGURE 4 - LINE DRIVER TIMING

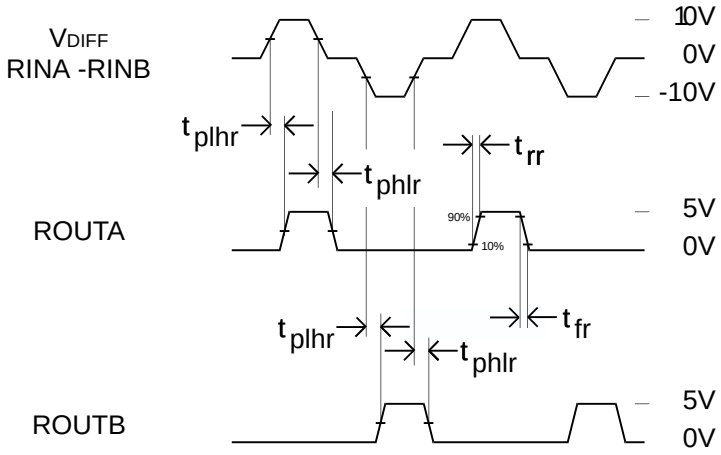


FIGURE 5 - RECEIVER TIMING

ORDERING INFORMATION

PART NUMBER	PACKAGE DESCRIPTION	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
HI-8590PSI	16 PIN PLASTIC ESOIC - WB	-40°C TO +85°C	I	NO	SOLDER
HI-8590PST	16 PIN PLASTIC ESOIC - WB	-55°C TO +125°C	T	NO	SOLDER

Legend: ESOIC - Thermally Enhanced Small Outline Package (SOIC w/built-in heat sink)
WB - Wide Body

16-PIN PLASTIC SMALL OUTLINE (ESOIC) - WB

(Wide Body, Thermally Enhanced) - HI-8590 Only

Package Type: 16HWE2