

iChip Plus™

iChip Plus CO661AL-D

Datasheet

Ver. 1.03



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Pub. No. 11-3400-01, ©Copyright February 2003

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<b>Revision History 11-3400-01</b>		
<b>Version</b>	<b>Date</b>	<b>Description</b>
1.00	December 2002	Original Release for iChip Plus CO661AL-D
1.02	February 2003	Internal Editing
1.03	February 2003	Change POBE pin description

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# 1 Introduction

## Description

CO661AL-D iChip Plus™ Internet Controller™ is part of a family of intelligent peripheral devices that provides Internet connectivity solutions to a myriad of embedded devices. iChip Plus CO661AL-D supports dial-up, wireless and 10BaseT or 10/100BaseT Ethernet Internet connectivity.

As an embedded, self-contained Internet engine, iChip Plus acts as mediator device between a host processor and an Internet communications platform. By completely offloading Internet connectivity and standard protocols, it relieves the host from the burden of handling Internet communications. From the perspective of a host device, the complexity of establishing and maintaining Internet-related sessions are reduced to simple, straightforward commands that are entirely dealt with within iChip Plus's domain.

A serial channel interfaces iChip Plus to a device's host processor via an on-chip UART. iChip Plus can also interface a host processor through an 8-bit parallel connection with some glue logic. iChip Plus directly interfaces a serial data modem, through which it supports independent communications on the Internet via a dial-up ISP connection. In addition to supporting dial-up modems, iChip Plus also supports CDMA, TDMA, GSM, GPRS, iDEN, CDPD and AMPS cellular modems.

iChip Plus also supports 10BaseT or 10/100BaseT Ethernet LANs with an additional Ethernet controller.

Available only for 3.3-volt operation, CO661AL-D includes features not available on iChip Plus CO561AD-D. It includes a host interface that supports 230 kbps bandwidth in serial mode and will support 500 Kbytes burst with up to 400 Kbytes sustained bandwidth in Parallel mode.

CO661AL-D features power save modes and will have an extended temperature range version.

Through its host Application Programming Interface (API), iChip Plus accepts commands formatted in Connect One's AT+i™ extension to the industry-standard Hayes AT command set.

Commands are available to store and manipulate functional and Internet-related non-volatile parameter data; transmit and receive textual Email messages; transmit and receive binary (MIME encoded) Email messages; serve and fetch HTML web pages; manage FTP and Telnet transactions; act as a dynamic Web server; manipulate TCP and UDP sockets; and download parameter and firmware updates for the host device or iChip Plus itself. iChip Plus supports several levels of status reporting to the host. When the host CPU issues standard AT commands, iChip Plus gains direct access to the modem and automatically operates in Transparent mode, emulating a direct host-to-modem environment (when the modem platform is selected).

iChip Plus supports 10BaseT and 10/100BaseT Ethernet LANs and all serial data modems that support the AT command set. A dedicated AT+i command enables switching iChip Plus between LAN or modem mode.

Upon receiving an AT+i command, iChip Plus operates in Internet mode, controls the modem or Ethernet controller, and independently manages standard Internet protocols. iChip Plus provides all the necessary procedures to log onto an ISP, authenticate the user and establish an Internet session.



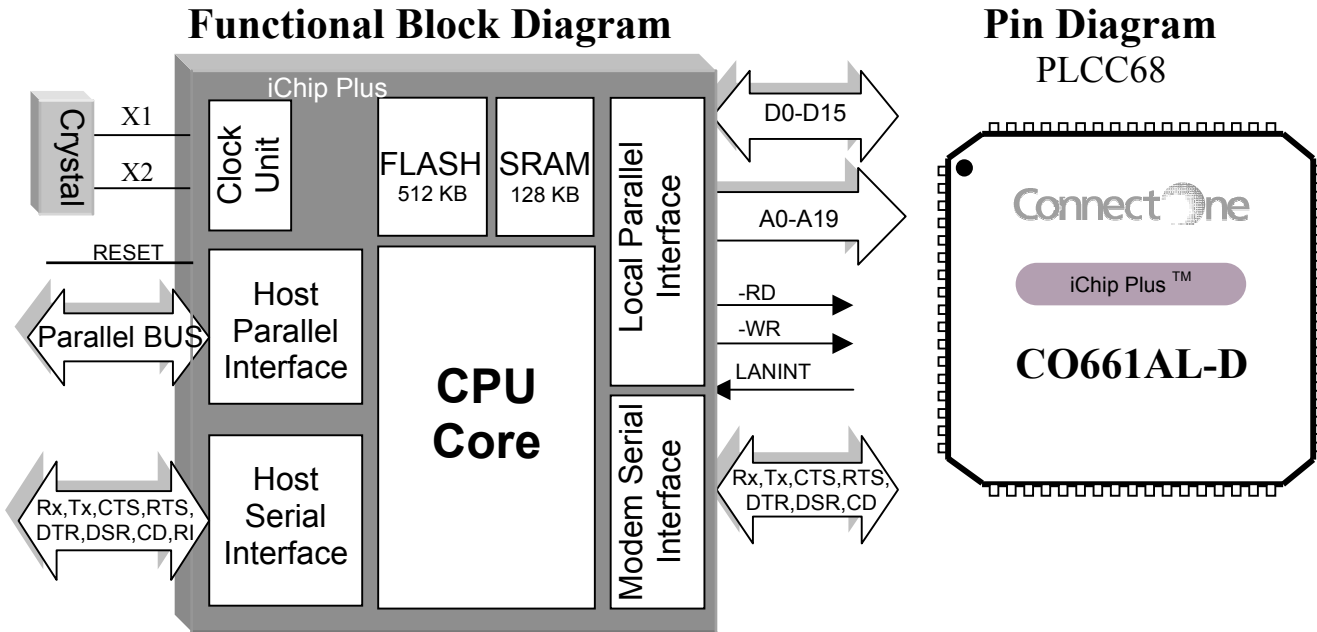


Figure 1-1 iChip Plus Functional Block Diagram

## General Features

- Microprocessor-controllable through a standard serial connection or 8-bit parallel interface.
- Supports remote firmware update by host, Email or Web.
- Includes onboard 128KB SRAM and 512KB flash memory.
- Driven by Connect One's AT+i extension to the AT command set.
- Stand-alone Internet communication capabilities.
- Binary Base64 encoding and MIME.
- Manages up to 10 simultaneous TCP or UDP sockets and up to 2 Listen (server) sockets.
- Operates at 3.3V, CMOS technology.
- Onboard non-volatile memory stores all functional and Internet-related parameters.
- Supports several layers of status reports.
- Internal self-test procedures.
- Automatic power save mode.
- Sleep Mode (with external glue logic).
- Auto baud rate detection up to 115,200 bps.
- Support for 230,400 bps (without auto baud rate).
- Supports hardware and software flow control.
- PLCC68 package.

## General Protocols

- Supports following Internet Protocols: IP, TCP, UDP, DNS, SMTP, POP3, MIME, HTTP, WAP, FTP and Telnet.
- Includes Web server and WAP server
- SerialNET mode for serial-to-Internet routing.

## Dial-up Features

- Supports dialup Internet Protocols: PPP, LCP, IPCP, and PAP or CHAP authentication.
- Supports data modems up to 56 Kbps.
- Supports CDMA, TDMA, GSM, GPRS, iDEN, CDPD and AMPS cellular modems.
- Stay-on-line feature for multiple send/receive sessions.
- Transparent mode supports direct modem commands.

## LAN Features

- Supports LAN Internet Protocols: ARP, ICMP, and DHCP.
- Provides 10BaseT and 10/100BaseT Ethernet LAN connectivity.
- Supports up to 230.4 Kbps maximum throughput with a serial host interface, and 400 Kbytes throughput with a parallel host interface.

## 2 Ordering Information

### 2.1 iChip Plus CO661AL-D Order Number:

<b>CO661AL-D</b>	<b>/20</b>	<b>P</b>	<b>C</b>	<b>-</b>	<b>3</b>
<b>Product Code</b>					
<b>Version:</b> D = Dual					
<b>Typical Clock Rate:</b> 20 = 18.432 MHz					
<b>Package:</b> P = PLCC 68 Pin					
<b>Temperature Range:</b> C = Commercial (0 to 70° C / 32 to 158° F)					
<b>Voltage:</b> 3 = 3.3V					

## **3 Functional Description**

### **3.1 Overview**

Connect One's iChip Plus Internet Controller is an integrated, firmware-driven, self-contained Internet engine that is available in a 68-pin PLCC package. iChip Plus accepts simple ASCII commands from a host CPU via a serial communication BUS and manages an Internet communication session to send and receive Email and Web and WAP pages/files, utilize FTP and Telnet, serve as a serial-to-Internet router, or to manipulate sockets through a linked modem or Ethernet communications platform.

For 10BaseT Ethernet applications, iChip Plus CO661AL-D includes the firmware and pin-out necessary to drive an external Crystal LAN CS8900A. For 10/100BaseT Ethernet applications, iChip Plus includes the firmware and pin-out necessary to drive an external SMSC LAN91C111 or ASIX AX88796L Ethernet LAN controller.

iChip Plus contains a non-volatile FLASH memory to store its firmware and Internet-related operational parameters. Remote firmware and parameter updates are supported through the local host link, by Email, using a Web browser or directly through the communications platform.

### **3.2 Technical Specifications**

#### **3.2.1 General**

iChip Plus constitutes a complete Internet messaging solution for non-PC embedded devices. It acts as a mediator device to completely offload the host processor of Internet-related software and activities. An industry-standard asynchronous serial link connects iChip Plus to the host processor. Programming, monitoring and control are fully supported using Connect One's AT+i extension to the standard AT command set.

iChip Plus connects to serial modems and to an Ethernet controller for Internet access. An AT+i command is provided to switch between the serial modem and Ethernet.

#### **3.2.2 Operation**

All iChip Plus Internet and parameter operations are controlled by AT+i commands.

##### **3.2.2.1 Transparent Mode**

In modem communications mode, iChip Plus defaults to Transparent mode, allowing the host to control the modem device directly. Control is implemented by issuing standard AT commands to iChip Plus. In this mode, iChip Plus transparently echoes the AT commands to the modem, as well as echoing the modem responses back to the host. iChip Plus supports interlacing AT+i and AT commands while the modem is in Command mode. When the modem is put into data mode, by issuing a dial command, Transparent mode is sustained throughout the data-mode session.

### **3.2.2.2 Command Mode**

iChip Plus commands are implemented using the AT+i command set. Command flow exists only on the host serial BUS between the host and iChip Plus.

### **3.2.2.3 Internet Mode**

iChip Plus enters Internet mode after being issued an Internet command such as to send or receive an Email message, open a socket, etc. iChip Plus attempts to establish an Internet connection and carry out the required activity through the communication platform link. While in this mode, AT+i commands are supported to monitor and control the process when needed.

### **3.2.2.4 Direct Modem Firmware Update Mode**

In a modem configuration, issuing an AT+iFU command enters this mode. iChip Plus monitors the modem for an incoming call by detecting the 'RING' response. When called, iChip Plus instructs the modem to answer the call and assumes a YMODEM session to receive a file containing a firmware update. The incoming file contents are downloaded and authenticated. If the new firmware image checks out the existing firmware is replaced in the on-chip flash memory and iChip Plus is reinitialized.

### **3.2.2.5 SerialNET Mode**

iChip SerialNET mode extends a local asynchronous serial link to a TCP or UDP socket across a LAN or Internet. Its main purpose is to allow simple devices, which normally interact over a serial line, to interact in a similar fashion across a network, without requiring any changes in the device itself. iChip Plus contains a set of associated operational parameters, which define the nature of the desired network connection. iChip Plus supports both Server and Client modes in SerialNET mode. AT+i commands are not required to operate SerialNET mode. Thus, SerialNET mode may be used in existing systems with little or no need to modify the application program.

## **3.2.3 Remote Internet Firmware Update**

New firmware may be uploaded from a remote location using standard Internet protocols. iChip Plus accepts Emails with new firmware attachments, as well as firmware uploads from a remote browser through iChip Plus' Web server.

## **3.2.4 Local BUS Connection to an Ethernet LAN Controller**

iChip Plus interfaces an Ethernet LAN controller connected to its 16-bit local BUS.

## **3.2.5 Host Connection**

iChip Plus can interface a host processor through one of two methods: Serial or Parallel.

### 3.2.5.1 Host Serial Connection

iChip Plus supports a full-duplex, TTL-level serial communications link with the host processor. Full EIA-232-D hardware flow control, including Tx, Rx, CTS, RTS, DTR, DSR, CD and RI lines, is supported.

CO661AL-D supports standard baud rate configurations from 2,400 bps up to 230,400<sup>1</sup> bps on the host asynchronous serial communications channel. The default baud rate may be changed permanently by using the AT+iBDRF command. Auto baud rate setting is supported for all baud rates except 230,400.

### 3.2.5.2 Host Parallel Connection

iChip Plus supports an 8-bit parallel BUS interface with some additional logic. The parallel BUS may be defined as an 80x86 (Intel) BUS or an MC68xxx (Motorola) BUS.

### 3.2.6 Serial Connection to Analog Modem

iChip Plus CO661AL-D supports a full-duplex, TTL-level serial communications link with the modem device. Full EIA-232-D hardware flow control, including Tx, Rx, CTS, RTS, DTR, DSR and CD lines, is supported. It does not support the RI line.

### 3.2.7 Hardware and Software Flow Control

Hardware flow control is supported between the host serial connection and iChip Plus. Flow control is programmed via the AT+iFLW command. The default flow control method is set to “Wait/Continue” software flow control (which is similar to XON/XOFF software flow control) between iChip Plus and the host processor.

The hardware flow control method frees the host CPU from monitoring and handling the software flow control. The host can program iChip Plus to either use hardware flow control or “Wait/Continue” software flow control. The flow control mechanism is based on the RTS/CTS signals.

The host parallel connection has built-in hardware flow control signals as part of the interface logic.

---

**Note:** 1: 230Kbps is available only from iChip Plus firmware version 704.

## 4 Hardware Interface

iChip Plus CO661AL-D may interface a host CPU in one of two methods: Serial or Parallel. The actual interface depends on the state of the –SER/PAR pin.

### 4.1 Serial Host Interface

The host interface is a serial DTE interface. Speeds of 2400, 4800, 9600, 19200, 38400, 57600, 115200 and 230400 bps are supported in the following data format:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Transmission Length (No. of Bits)
None	8	1 <sup>1</sup>	10

Table 4-1 Host Data Format

All host serial input signals (RXDH, -CTSH, -DSRH) are 5V tolerant.

### 4.2 Parallel Host Interface <sup>2</sup>

In parallel interface mode, iChip Plus connects to a host CPU through a parallel interface using a PAL (i.e., Altera “EPM7032AEC44”). The host parallel BUS may be an 80x86 (Intel) or a 68K (Motorola) BUS. With some small changes to the PAL, the user may customize an interface to any other BUS architecture. iChip Plus is connected to the interface PAL through the following signals:

- **PCS:** Parallel chip select signal. When PCS is high, the PAL is selected.
- **-RD:** When –RD is LOW, iChip Plus reads data from PAL.
- **-WR:** When –WR is LOW, iChip Plus writes data to PAL.
- **D0-D7:** Bi-directional data BUS.
- **-PRES:** Parallel reset. When LOW, generates a reset signal to the parallel interface.
- **-PERR:** Parallel error. When LOW, indicates a parallel interface error.
- **POBE:** Parallel Output Buffer Empty. When HIGH, indicates that the output buffer is empty and iChip Plus may send additional data to host. When iChip Plus sends a data byte, this signal goes LOW until the host reads the data.
- **PIBF:** Parallel Input Buffer Full. When HIGH, indicates that the input buffer is full and iChip Plus may read a data byte from the host. When iChip Plus reads the data byte, this signal goes LOW.

---

**Notes:** 1: When hardware flow control is enabled, the iChip Plus transmitter will add an additional stop bit.  
2: Parallel interface mode is available only from iChip Plus firmware version 801.

### 4.2.1 80x86 BUS

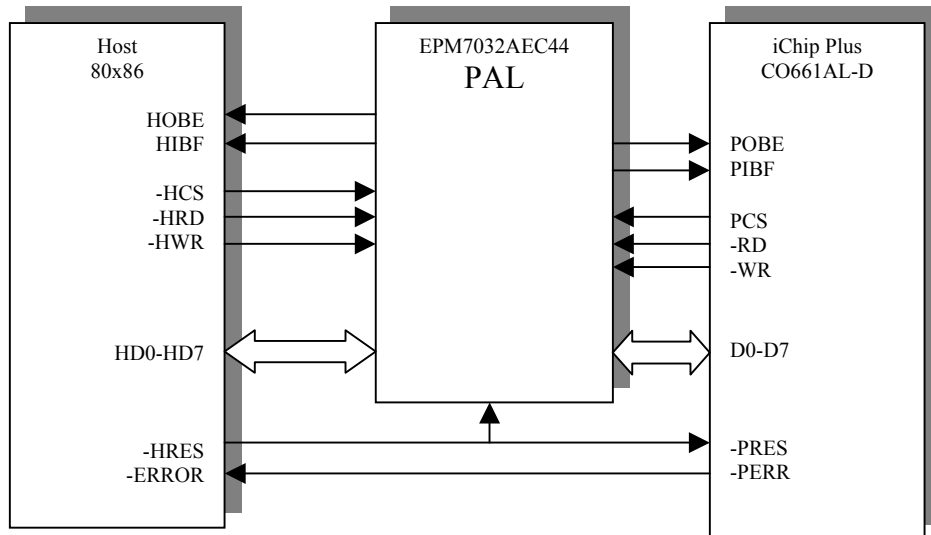


Figure 4-1 Interface to an 80x86 Type BUS

This BUS type includes the following signals:

- **-HCS:** Host Chip-Select signal. When -HCS is LOW, PAL is selected.
- **-HRD:** Host Read Data. When -HRD is LOW, a data byte is read from the PAL.
- **-HWR:** Host Write Data. When -HWR is LOW, a data byte is written to the PAL.
- **HD0 – HD7:**  
Bi-directional Host data BUS.
- **-HRES:** Parallel reset. A LOW generates a reset signal to the parallel interface. This pin may be connected to an 80x86 output port.
- **-HERR:** Parallel error. A LOW indicates a parallel interface error. This pin may be connected to an input port on the 80x86.
- **HOBE<sup>1</sup>:** Host Output Buffer Empty. When HIGH, indicates that the output buffer is empty and the host may send a data byte to iChip Plus. When the Host sends a data byte, this signal goes LOW until iChip Plus reads the data. This signal may be connected to an interrupt or I/O pin on the 80x86.
- **HIBF<sup>1</sup>:** Host Input Buffer Full. When HIGH, indicates that the input buffer is full and the host may read a data byte from iChip Plus. When the host reads the data, this signal goes LOW. This pin may be connected to an interrupt or I/O pin on the 80x86.

Note 1: HOBE and HIBF complement PIBF and POBE respectively.

## 4.2.2 MC68xxx BUS

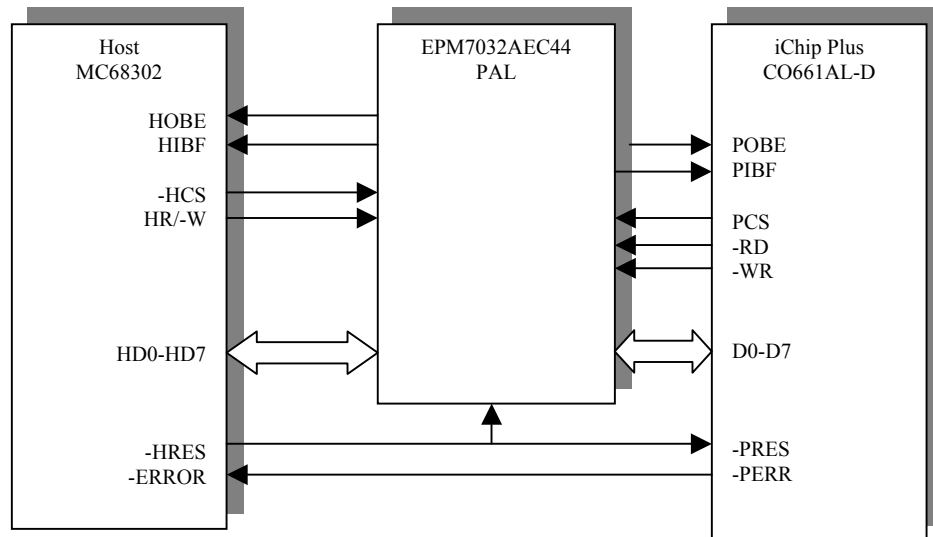


Figure 4-2 Interface to an MC68xxx Type BUS

This BUS type includes the following signals:

- **-HCS:** Host Chip-Select signal. When -HCS is LOW, PAL is selected.
- **-HR/-W:** Host read/write data from/to iChip Plus. When HR/-W is LOW, it indicates a write cycle; otherwise it is a read cycle.
- **HD0 – HD7:**  
Bi-directional Host data BUS.
- **-HRES:** Parallel reset. A LOW generates a reset signal to the parallel interface. This pin may be connected to an MC68xxx output port.
- **-HERR:** Parallel error. A LOW indicates a parallel interface error. This pin may be connected to an input port on the 80x86.
- **HOBE<sup>1</sup>:** Host Output Buffer Empty. When HIGH, indicates that the output buffer is empty and the host may send a data byte to iChip Plus. When the Host sends a data byte, this signal goes LOW until iChip Plus reads the data. This signal may be connected to an interrupt or I/O pin on the MC68xxx.
- **HIBF<sup>1</sup>:** Host Input Buffer Full. When HIGH, indicates that the input buffer is full and the host may read a data byte from iChip Plus. When the host reads the data, this signal goes low. This pin may be connected to an interrupt or I/O pin on the MC68xxx.

<sup>1</sup>Note 1: HOBE and HIBF complement PIBF and POBE respectively.



### 4.3 LAN Interface

iChip Plus directly interfaces an Ethernet LAN MAC/PHY device on its 16-bit local BUS. Currently iChip Plus supports the Crystal LAN CS8900A Ethernet controllers for 10BaseT and SMSC LAN91C111 and ASIX AX88796L Ethernet controllers for 10/100BaseT.

### 4.4 Serial Modem Interface

iChip Plus includes a dedicated port to interface a serial modem.

The modem interface is a serial DCE interface. Speeds of 2400, 4800, 9600, 19200, 38400, 57600, 115200 and 230400 bps are supported in the following data format:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Transmission Length (No. of Bits)
None	8	1	10

Table 4-2 Modem Data Format

Actual baud rate may be preprogrammed or dynamically defined as equal to the auto baud rate detected on the serial host interface (when the iChip Plus operates in Serial mode). When iChip Plus operates in Parallel mode, the modem interface baud rate must be preprogrammed.

All serial modem input signals (RXDM, -DSRM, -CTSM, -CDM) are 5V tolerant.

iChip Plus does not provide a Ring Indicator input signal.

4.5 Dual Interface

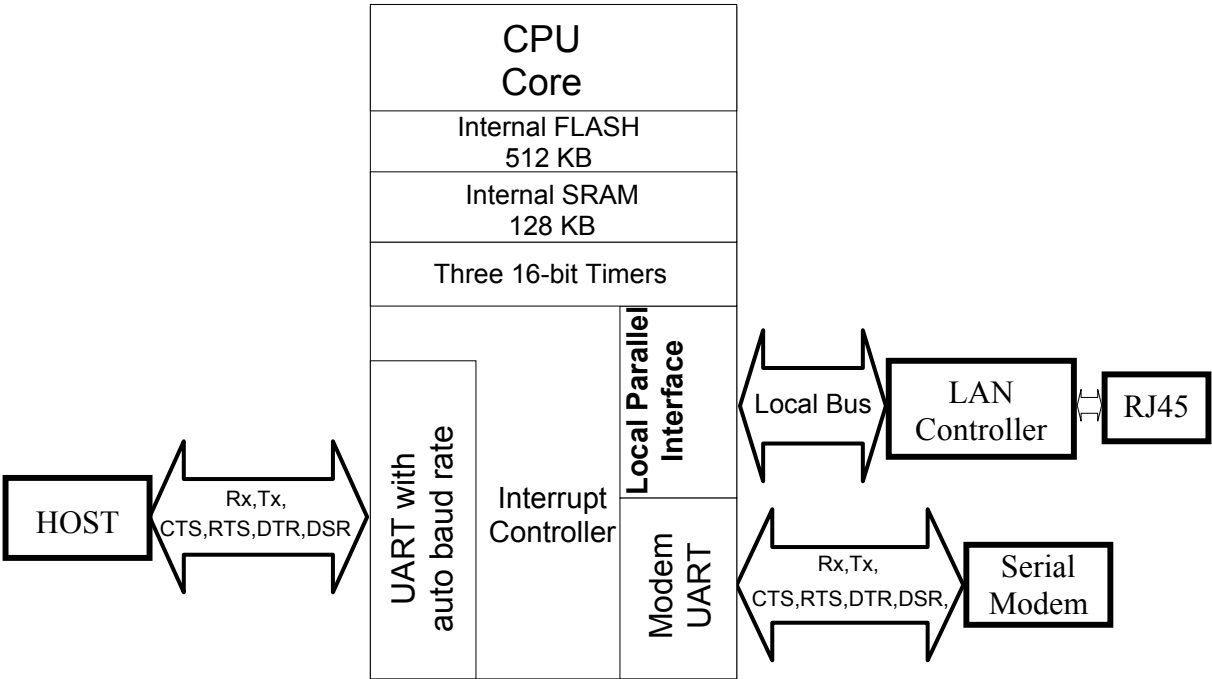


Figure 4-3: iChip Plus CO661AL-D with LAN and serial modem interface

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## 5 Pin Descriptions

### 5.1 iChip Plus CO661AL-D Pin Assignments

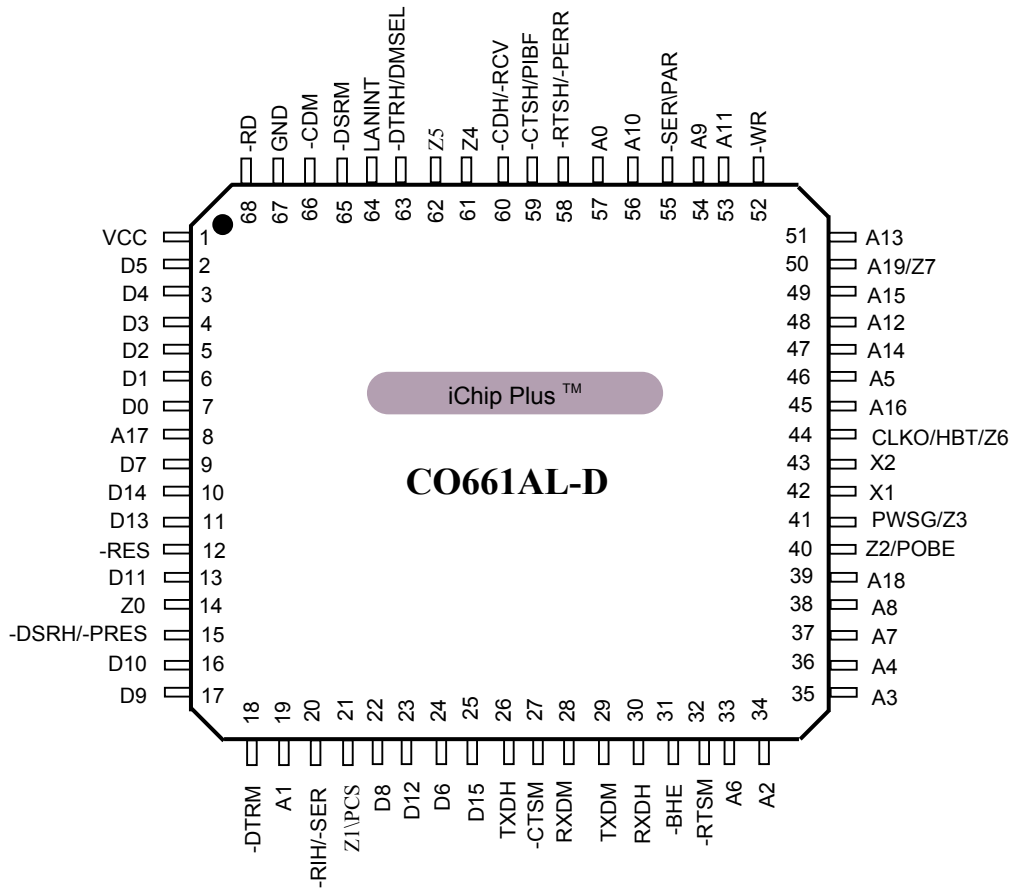


Figure 5-1 PLCC68 Package for iChip Plus CO661AL-D

## 5.2 iChip Plus Pin Functional Descriptions

### 5.2.1 Local BUS Signals

Signal	Type	Pin No.	Description															
A[18:0]	O	39, 8, 45, 49, 47, 51, 48, 53, 56, 54, 38, 37, 33, 46, 36, 35, 34, 19, 57	Address BUS: These pins supply addresses to the system. These pins should be Connected to the address BUS of the LAN controller.															
A19/Z7	O	50	Address BUS MSB. This pin should be connected to the LAN controller's address BUS MSB. In the future this pin may be changed to a General Purpose I/O (GPIO Z7).															
D[15:0]	O/I	25, 10, 11, 23, 13, 16, 17, 22, 9, 24, 2, 3, 4, 5, 6, 7	Data BUS: These pins supply data to/from the system. These pins should be connected to the data BUS of the LAN controller.															
-BHE	O	31	<p>BUS HIGH Enable: This pin and the least-significant address bit (A0) indicate to the system which bytes of the data BUS (upper, lower, or both) participate in a BUS cycle. The -BHE and A0 pins are encoded as shown in the table below.</p> <table border="1"> <thead> <tr> <th>-BHE</th> <th>A0</th> <th>Type of BUS cycle</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Word Transfer</td> </tr> <tr> <td>1</td> <td>0</td> <td>Even Byte Transfer</td> </tr> <tr> <td>0</td> <td>1</td> <td>Odd Byte Transfer</td> </tr> <tr> <td>1</td> <td>1</td> <td>N/A</td> </tr> </tbody> </table> <p>This pin should be connected to -BHE on the LAN controller.</p>	-BHE	A0	Type of BUS cycle	0	0	Word Transfer	1	0	Even Byte Transfer	0	1	Odd Byte Transfer	1	1	N/A
-BHE	A0	Type of BUS cycle																
0	0	Word Transfer																
1	0	Even Byte Transfer																
0	1	Odd Byte Transfer																
1	1	N/A																

## Pin Descriptions

Signal	Type	Pin No.	Description
-RD	O	68	READ: This pin indicates that iChip Plus is performing a read cycle. This pin should be connected to -RD on the LAN controller.
-WR	O	52	WRITE: This pin indicates that iChip Plus is performing a write cycle. This pin should be connected to -WR on the LAN controller.

## 5.2.2 Miscellaneous Signals

Signal	Type	Pin No.	Description
-RES	I	12	<p>RESET: When -RES is LOW, iChip Plus immediately terminates its present activity and clears its internal logic.</p> <p>-RES must be held LOW for at least 1 mSec after power achieves 90% VCC.</p> <p>This input is provided with a Schmidt trigger to facilitate power-on reset generation via an RC network.</p>
X1	I	42	<p>Crystal Input: This pin and the X2 pin provide connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit.</p> <p>To provide iChip Plus with an external clock source, connect the source to the X1 pin and leave the X2 pin unconnected.</p>
X2	O	43	<p>Crystal Output: This pin and the X1 pin provide connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit.</p>
CLKO/HBT/Z6	O	44	<p>AT+i Configurable Pin:</p> <p><b>CLKO</b> (default): Clock Output. This pin provides a clock-out to the system at the same frequency as X1. During reset the clock out is disabled.</p> <p><b>HBT</b>: Heart Beat. Provides a 50% duty cycle, 40 mSec frequency square wave, when iChip F/W is properly running. (Available from iChip Plus Firmware ver. 7.04).</p> <p>In the future it may be changed to a GPIO.</p> <p>This pin is configurable with the AT+iPN44 command (see AT+i Programmers Manual).</p>
-SER/PAR	I	55	<p>Serial/Parallel mode select. This pin is sampled on the rising edge of the -RES signal. If it is LOW, iChip Plus functions in Serial mode. Otherwise it functions in Parallel mode.</p>

Signal	Type	Pin No.	Description
LANINT	I	64	LAN Interrupt. When HIGH, this signal indicates that the LAN controller has information for iChip Plus.
Z0	I/O	14	GPIO for future use. This pin should be Not Connected.
Z1/PCS	I/O	21	<b>In Serial mode</b> , Z1 is available as a GPIO for future use and should be left Not Connected. <b>In Parallel mode</b> , PCS is used as a chip-select for the parallel interface PAL.
Z2/POBE	I/O	40	<b>In Serial mode</b> , Z2 is available as a GPIO for future use and should be left Not Connected. <b>In Parallel mode</b> , POBE is used as the Parallel Output Buffer Empty signal. When HIGH, iChip Plus may send a parallel data byte to the host.
PWSG/Z3	I/O	41	AT+i Configurable Pin: <b>PWSG</b> (default): Power Save Gate. This pin is used to disable iChip's oscillator (X1 Pin 42) via an external gate in order to achieve full Sleep mode with minimal power consumption (see <a href="#">Fig. 7-6</a> ). <b>Z3</b> : General Purpose I/O.
Z4	I/O	61	Reserved as a GPIO for future use. This pin should be Not Connected.
Z5	I/O	62	Reserved as a GPIO for future use. This pin should be Not Connected.
GND	P	67	Ground: iChip Plus Ground signal.
VCC	P	1	Power Supply: This pin supplies power (+3.3V) to iChip Plus.

### 5.2.3 Host Serial Interface Signals

Signal	Type	Pin No.	Description
TXDH	O	26	<b>In Serial mode</b> , Transmit Data Host: This pin supplies asynchronous serial transmit data to the host. <b>In Parallel mode</b> , this pin is used for firmware update.
RXDH	I	30	<b>In Serial mode</b> , receive Data Host: This pin supplies asynchronous serial receive data from the host. <b>In Parallel mode</b> , this pin is used for firmware update. When not used, this pin should be connected to VCC.
-CTSH /PIBF	I	59	<b>In Serial mode</b> , Clear-to-Send Host: -CTSH is active only when host hardware flow control is enabled. When -CTSH is LOW, flow control is enabled for the host serial port, i.e., iChip Plus may transmit to the host. When -CTSH is HIGH, the iChip Plus transmitter holds its data in the serial port transmit register. -CTSH is sampled only at the beginning of a frame transmission. If -CTSH is raised while a character frame is being transmitted, that frame will be completed. Connect -CTSH to -RTSH when not in use. <b>In Parallel mode</b> , Parallel Input Buffer Full: when HIGH, indicates that the host has sent a data byte, which has not yet been read.
-RTSH/-PERR	O	58	<b>In Serial mode</b> , Ready-to-Send Host: -RTSH is active only when host hardware flow control is enabled. When -RTSH is LOW, flow control is enabled for the host serial port, i.e., the host may transmit to iChip Plus. When -RTSH is HIGH, iChip Plus indicates that its receiver is busy and cannot receive data from host. Connect -RTSH to -CTSH when not in use. <b>In Parallel mode</b> , Parallel Error: When LOW, indicates to the host that an error has occurred in the parallel interface circuit.



Signal	Type	Pin No.	Description
-DSRH/-PRES	I	15	<p><b>In Serial mode</b>, Data Set Ready Host: when -DSRH is LOW, it indicates that the host is attached and ready to communicate with iChip Plus. Connect -DSRH to GND when not in use.</p> <p>In Parallel mode, Parallel Reset: when LOW, generates a reset to the parallel interface.</p>
-DTRH/DMSEL	O	63	<p>After reset this pin's functionality is DMSEL. During normal operation this pin acts as -DTRH.</p> <p>Data Terminal Ready Host: When -DTRH is LOW, it indicates to the host that iChip Plus is attached and ready to communicate. When this pin is held LOW during power up for at least 1 second, and no longer than 5 seconds, iChip Plus will enter auto baud rate mode. When this pin is held LOW during power up for more than 5 seconds, iChip Plus will automatically enter firmware update mode.</p>
-CDH/-RCV	O	60	<p>In dial-up mode, this pin functions as -CDH. In LAN mode, it functions as -RCV.</p> <p>Carrier Detect Host: This pin indicates to the host that the modem communication device detects a carrier signal.</p> <p>Receive LAN Package: when LOW, indicates that iChip Plus may receive a data packet from the LAN controller.</p> <p>During firmware update, -CDH and -RIH are used to display the firmware update status.</p>
-RIH/-SER	O	20	<p>In dial-up mode, this pin functions as -RIH. In LAN mode, it functions as -SER.</p> <p>Ring Indicator Host: This pin indicates to the host that the modem communication device detects a Ring signal.</p> <p>Serial Indicator Host: when LOW, indicates that iChip Plus may receive a legal character from the host.</p> <p>During firmware update, -CDH and -RIH are used to display the firmware update status.</p>

### 5.2.4 iChip Plus Serial Modem Signals

Signal	Type	Pin No.	Description
TXDM	O	29	Transmit Data Modem: this pin provides asynchronous serial transmit data to the modem from the serial port. During reset, this pin must remain high.
RXDM	I	28	Receive Data Modem: this pin provides asynchronous serial receive data from the modem to the asynchronous modem serial port. When this pin is not used, connect it to VCC.
-CTSM	I	27	Clear-to-Send Modem: -CTSM is active only when modem hardware flow control is enabled. When -CTSM is LOW, flow control is enabled to the modem serial port, i.e., iChip Plus may transmit to the modem. When -CTSM is HIGH, the iChip Plus transmitter holds its data in the serial port transmit register.  Connect -CTSM to -RTSM when not in use.
-RTSM	O	32	Ready-to-Send Modem: -RTSM is active only when modem hardware flow control is enabled. When -RTSM is LOW, flow control is enabled from the modem serial port, i.e., the modem may transmit to iChip Plus. When -RTSM is HIGH, iChip Plus indicates that its receiver is busy and cannot receive data from the modem. Connect -RTSM to -CTSM when not in use.
-DSRM	I	65	Data Set Ready Modem: when -DSRM is LOW, it indicates that the modem is attached and ready to communicate with iChip Plus.  Connect -DSRM to GND when not in use.
-DTRM	O	18	Data Terminal Ready Modem: when -DTRM is LOW, it indicates to the modem that iChip Plus is attached and ready to communicate.
-CDM	I	66	Carrier Detect Modem: this pin indicates to the iChip Plus that the modem detects a carrier signal.

## 6 Electrical/Mechanical Specifications

### 6.1 Environmental Specifications

#### 6.1.1 Absolute Maximum Ratings

Parameter	Rating
Voltage at local BUS pins with respect to ground	-0.5 to +3.8 Volts
Voltage at all other pins with respect to ground	-0.5 to +5.5 Volts
Operating temperature	0°C to 70°C (32 to 158°F)
Storage temperature	-60°C to 120°C (-76 to 248°F)
Soldering temperature (max. 10 sec.)	220°C (428°F)
Package dissipation	1.5 Watts

Table 6-1 Environmental Specifications – Maximum Ratings

#### 6.1.2 DC Operating Characteristics

Parameter	Min	Typical	Max	Units
DC Supply	3.0	3.3	3.6	Volts
High-level Input	2.0			Volts
Low-level Input			0.8	Volts
High-level Output <sup>1</sup>	2.4			Volts
Low-level Output <sup>2</sup>			0.4	Volts
Input leakage current			4	μA
Power supply current (Operating Mode) <sup>3</sup>		30		mA
Power supply current (Power Save Mode) <sup>3</sup>		10		mA
Input capacitance			7	pF

**Notes:** <sup>1</sup> I<sub>OH</sub> = 2mA

<sup>2</sup> I<sub>OL</sub> = 2mA

<sup>3</sup> 18.432 MHz clock

Table 6-2 DC Operating Characteristics

## 6.2 Interface Timing and Waveforms

### 6.2.1 Switching Characteristics

Parameter	Symbol	Min.	Typical	Max.	Units
Clock Out frequency	Fclk	18.43	18.432	18.434	MHz
Clock Out period	Tclk		1/Fck		us
X2 falling to address or chip select change	Txfac	4.2		10	ns
X2 rising to read active	Txrra	4.1		8.6	ns
X2 falling to read inactive	Txfri	4.1		8.6	ns
Data setup before read high	Tdsbrh	9			ns
Data setup after read high	Tdsarh	3			ns
X2 rising to write active	Txrwa	5		8.2	ns
X2 rising to data valid	Txrdv	4.1		8.6	ns
X2 rising to write inactive	Txrwi	5		8.2	ns
Data out valid after write high	Tdovaw	2.1			ns
X2 fall time <sup>1</sup>	Tckhl			5	ns
X2 rise time <sup>2</sup>	Tcklh			5	ns
X2 LOW time	Tclck	24	27	30	ns
X2 HIGH time	Tchck	24	27	30	ns
X2 to CLKO skew	Tcico	4.2		6.6	ns
Reset pulse	Trst	1			ms
RXDM high before rising reset	Trmbr	2			us
RXDM high after rising reset	Trmar	2			us
Read rising to input parallel buffer full	Trrbf	0			ns
Write rising to output parallel buffer empty	Twrbe	0			ns

Table 6-3 Switching Characteristics

<sup>1</sup> Fall time is from 2.3V to 1V.

<sup>2</sup> Rise time is from 1V to 2.3V.

### 6.2.2 Local BUS Read Cycle

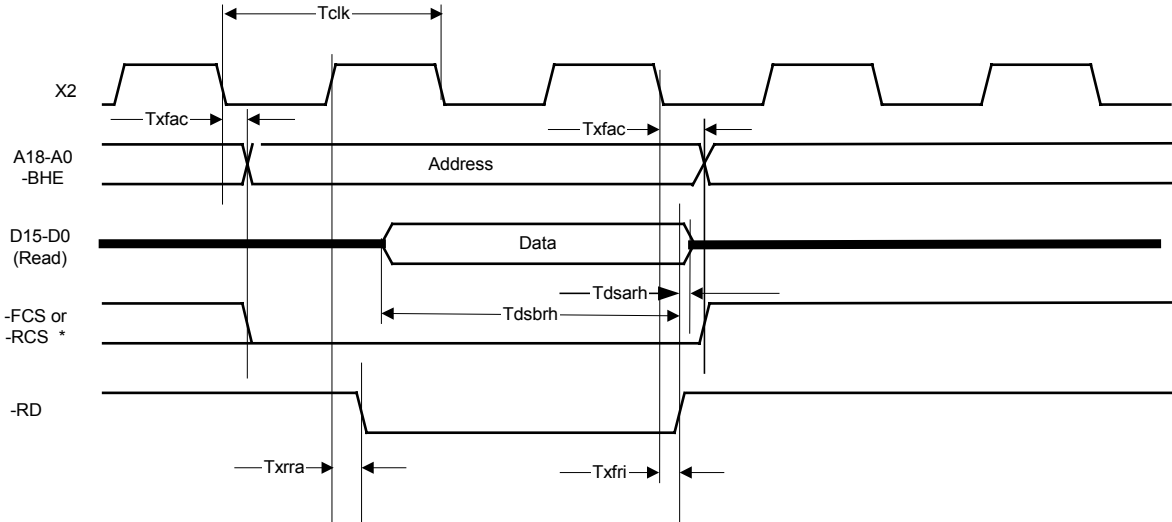


Figure 6-1 Local BUS Read Cycle

\* -FCS and -RCS are internal Flash and RAM Chip-select.

### 6.2.3 Local BUS Write Cycle

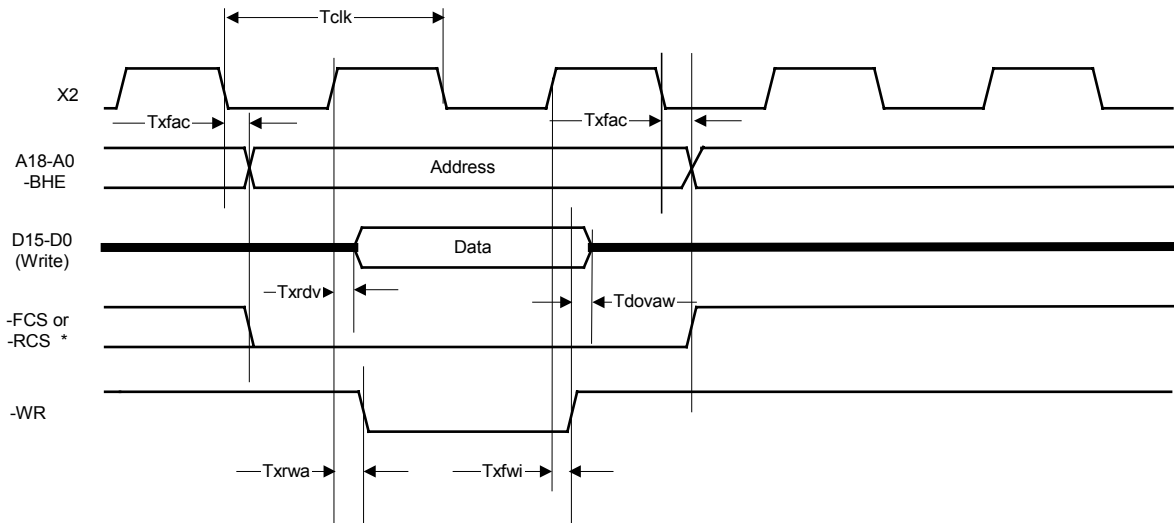


Figure 6-2 Local BUS Write Cycle

\* -FCS and -RCS are internal Flash and RAM Chip-select.

### 6.2.4 Clock Waveform

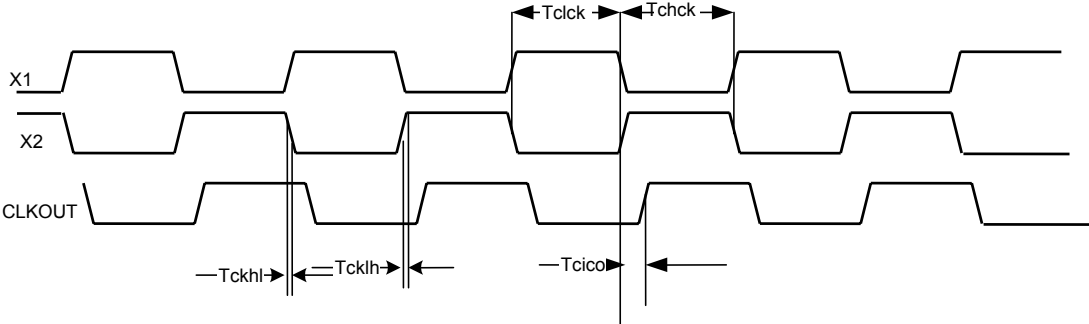


Figure 6-3 Clock Waveform

### 6.2.5 Reset Timing

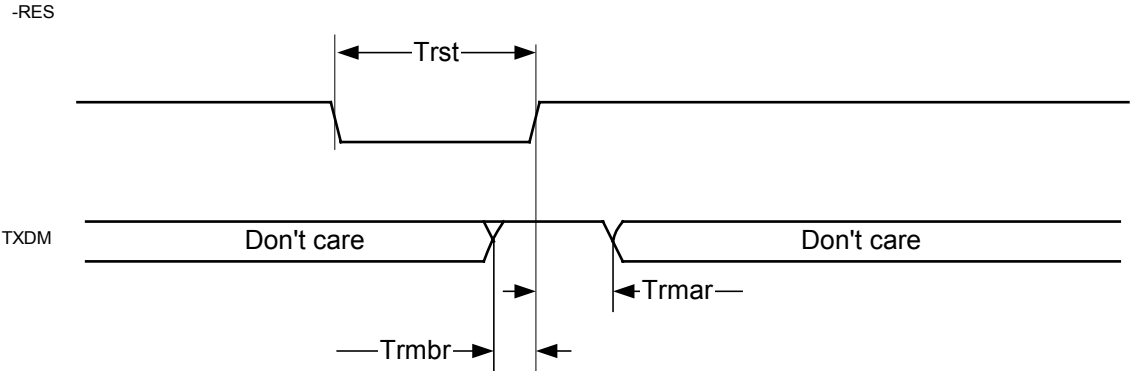


Figure 6-4 Reset Timing

Downloaded from [Elcodis.com](http://Elcodis.com) electronic components distributor

### 6.2.6 Parallel BUS Read Cycle

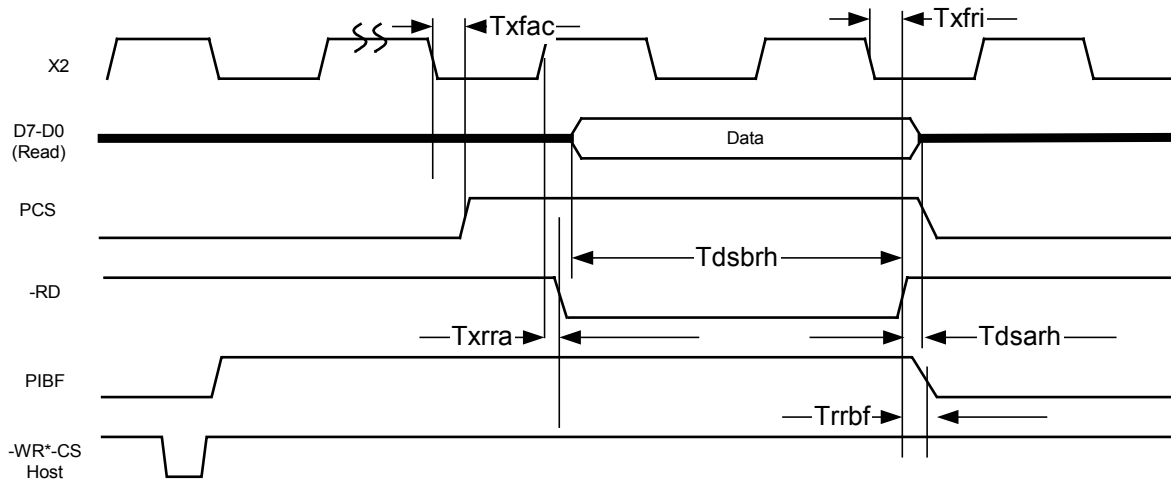


Figure 6-5 Parallel BUS Read Cycle

### 6.2.7 Parallel BUS Write Cycle

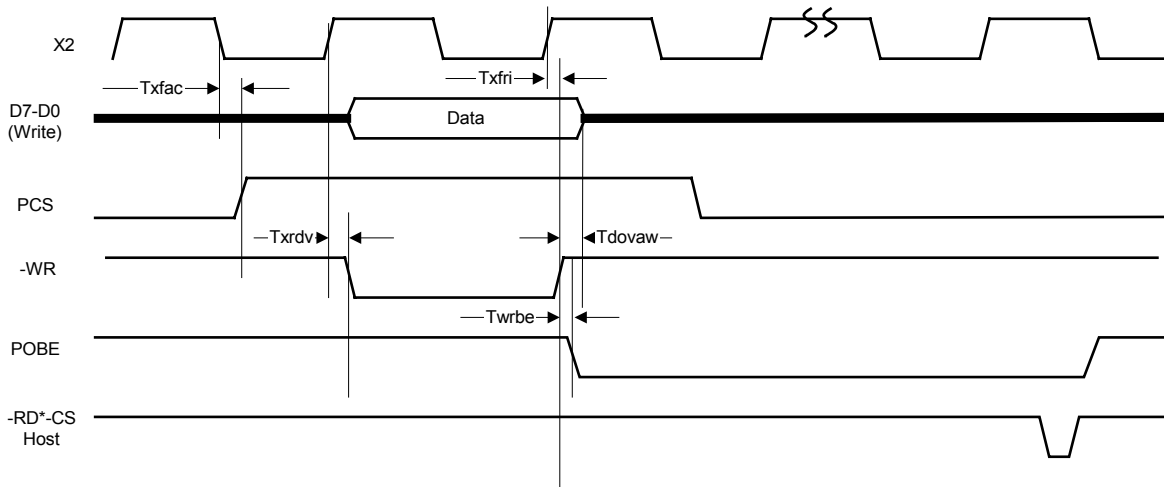


Figure 6-6 Parallel BUS Write Cycle

6.3 Mechanical Dimensions

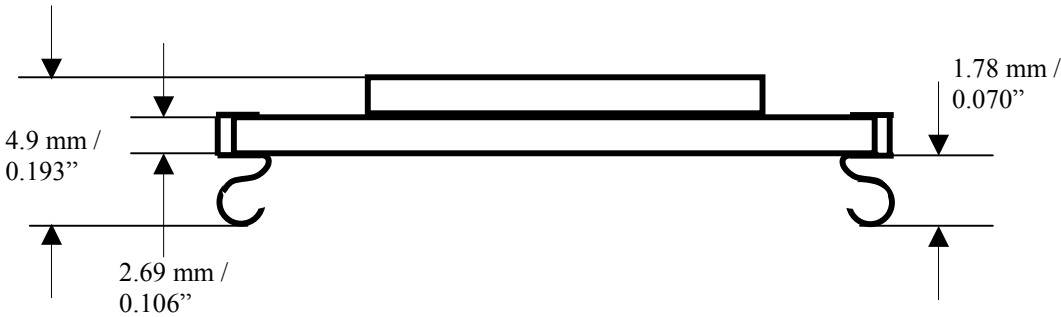
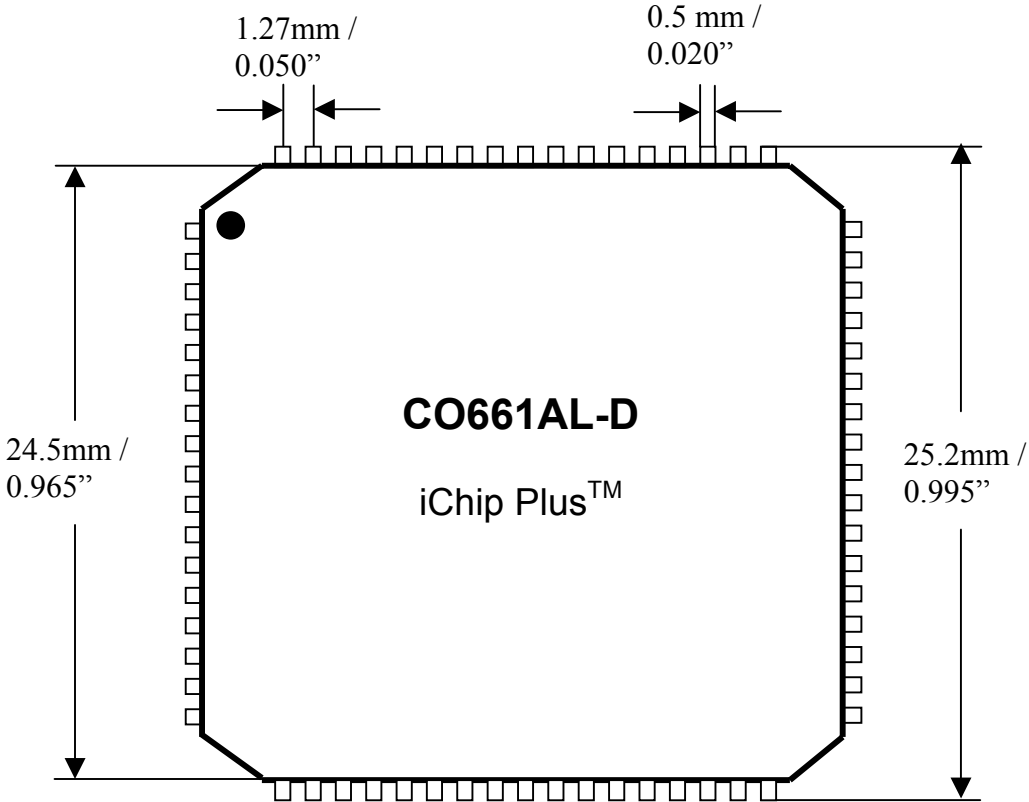


Figure 6-7 Mechanical Dimensions

Downloaded from [Elcodis.com](http://Elcodis.com) electronic components distributor



## 7 iChip Plus Designs

### 7.1 Serial Host and Ethernet controller Environment

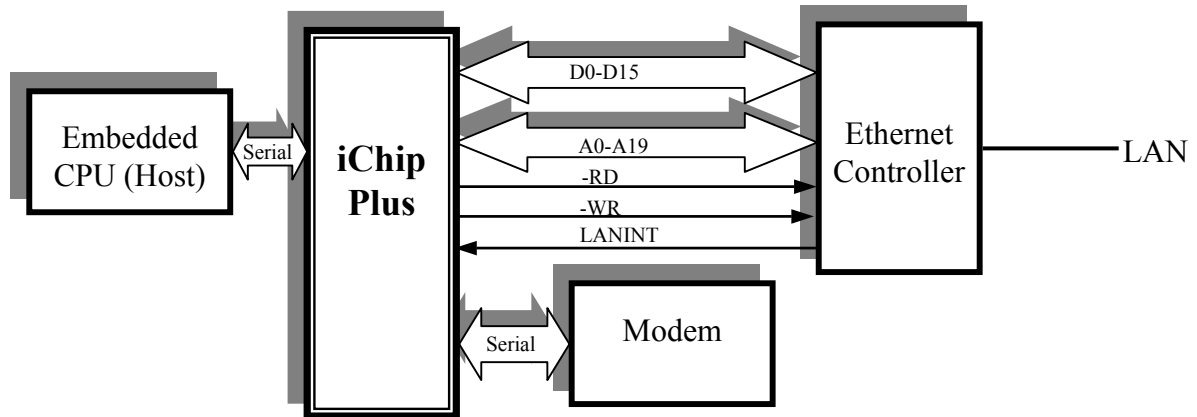


Figure 7-1 Serial Host and Ethernet Controller Environment

### 7.2 Parallel Host and Ethernet controller Environment

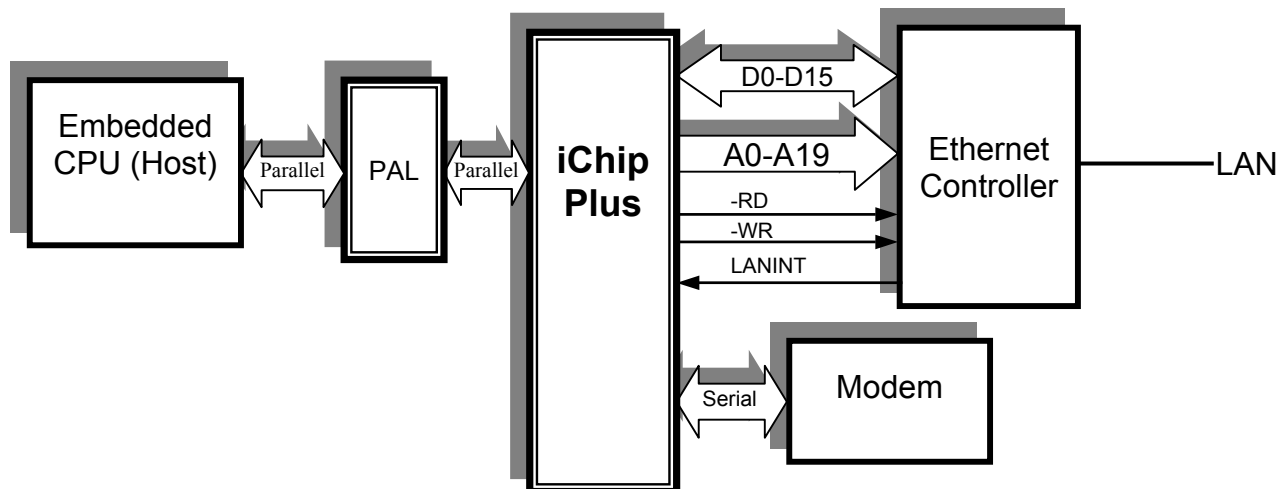


Figure 7-2 Parallel Host and Ethernet Controller Environment

### 7.3 Selecting a Crystal

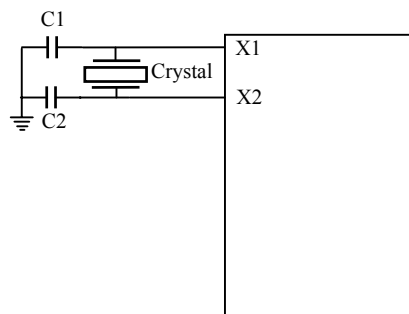


Figure 7-3 Selecting a Crystal

The characteristics of the built-in inverting amplifier set limits on the following parameters for crystals:

Crystal first overtone frequency .....	18.432 MHz
ESR (Equivalent Series Resistance) .....	40 $\Omega$ max
Drive Level .....	1 mW max
Frequency tolerance .....	+/- 100ppm
Load capacitance.....	18pF
Shunt capacitance.....	7pF Maximum

The recommended range of values for C 1 and C 2 are as follows:

C 1 .....	15 pF $\pm$ 20%
C 2 .....	22 pF $\pm$ 20%

The specific values for C1 and C2 must be determined by the designer and are dependent on the characteristics of the chosen crystal and board design.

## 7.4 Selecting the Reset Circuit

### 7.4.1 RC Network

The Reset signal may be designed with an RC network.  $\tau$  should be greater than 10 mSec. This is a low-cost solution.

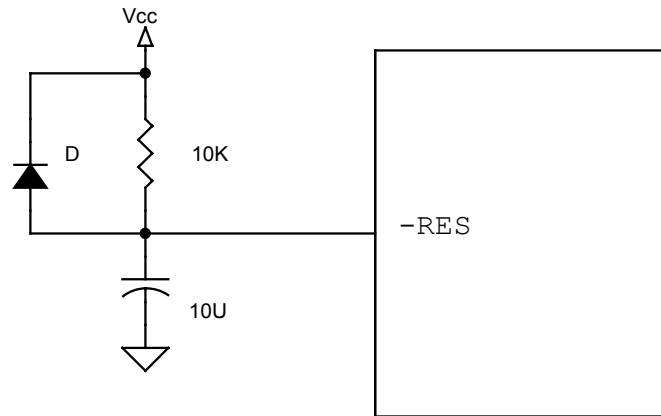


Figure 7-4 RC Reset Circuit

### 7.4.2 Supervisory Circuit

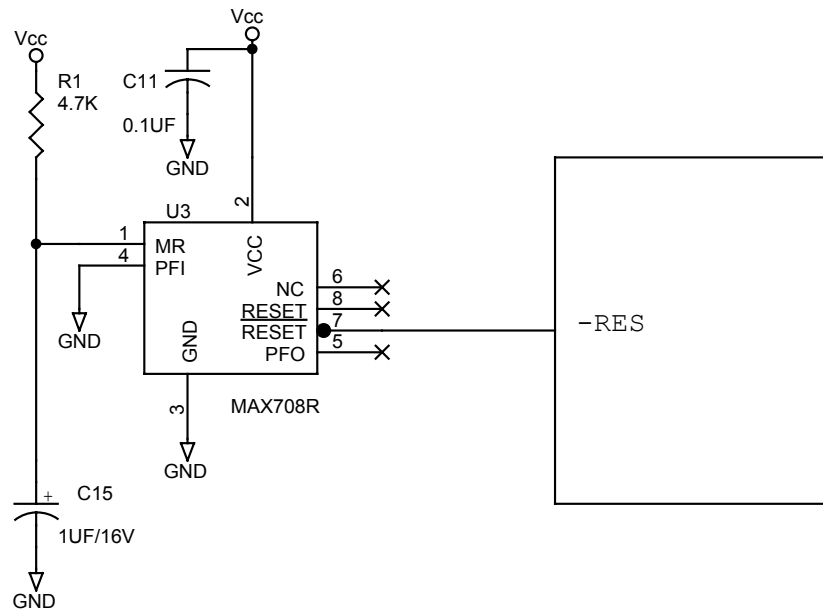


Figure 7-5 Supervisory Reset Circuit

## 7.5 Sleep Mode

CO661AL-D iChip Plus supports a sleep mode<sup>1</sup> to achieve maximum power conservation when iChip Plus is not in use. Sleep mode is based on an external circuit that gates the oscillator input to iChip Plus. The PWSG (pin 41) is an output pin used to trigger Sleep mode. While in this mode, iChip Plus current consumption is reduced to ~1 mA. The external circuit is designed to wake-up and exit Sleep mode when a transmission arrives from either the host processor or the modem or from the LAN Interrupt (See Fig. 7-6).

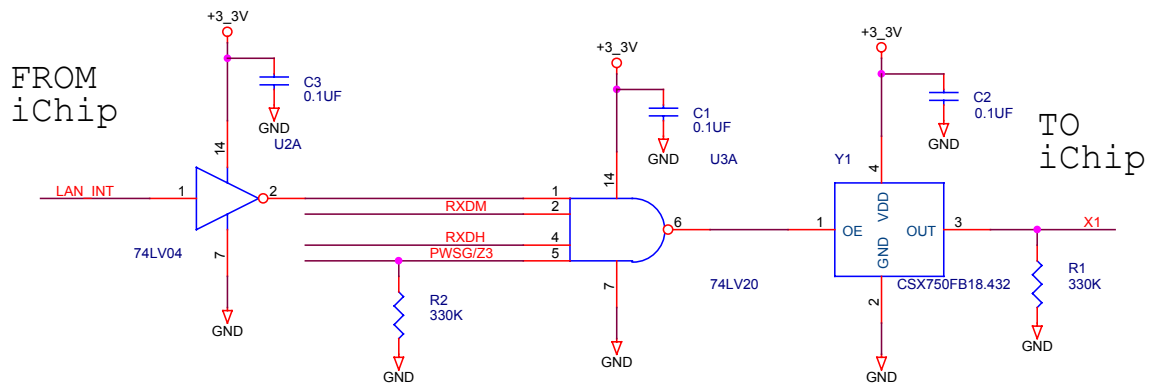


Figure 7-6 CO661AL External Sleep-Mode Circuit

**Note:** 1: Sleep mode will be available only from iChip firmware version 801

## 8 Protocol Compliance

iChip Plus CO661AL-D complies with the following Internet standards:

<b>RFC 768</b>	User Datagram Protocol (UDP)
<b>RFC 791</b>	Internet Protocol (IP)
<b>RFC 792</b>	Internet Control Message Protocol
<b>RFC 793</b>	Transmission Control Protocol (TCP)
<b>RFC 821</b>	Simple Mail Transfer Protocol (SMTP)
<b>RFC 826</b>	Ethernet Address Resolution Protocol.
<b>RFC 951</b>	Bootstrap Protocol.
<b>RFC 822</b>	Standard for the Format of ARPA Internet Text Messages.
<b>RFC 1331</b>	Point-to-Point Protocol (PPP).
<b>RFC 1332</b>	PPP Internet Protocol Control Protocol (IPCP).
<b>RFC 1334</b>	PPP Authentication Protocols (PAP).
<b>RFC 1661</b>	Point-to-Point Protocol (PPP).
<b>RFC 1939</b>	Post Office Protocol - Version 3 (POP3)
<b>RFC 1957</b>	Some Observations on the Implementations of the Post Office Protocol (POP3)
<b>RFC 2045</b>	Multipurpose Internet Mail Extensions (MIME) Part One: Format of Internet Message Bodies
<b>RFC 2046</b>	Multipurpose Internet Mail Extensions (MIME) Part Two: Media Types
<b>RFC 2047</b>	MIME (Multipurpose Internet Mail Extensions) Part Three: Message Header Extensions for Non-ASCII Text
<b>RFC 2048</b>	Multipurpose Internet Mail Extensions (MIME) Part Four: Registration Procedures
<b>RFC 2049</b>	Multipurpose Internet Mail Extensions (MIME) Part Five: Conformance Criteria and Examples
<b>RFC 2068</b>	HyperText Transfer Protocol HTTP/1.1

*Table 8-1 Internet Protocol Compliance*

## 9 List of Terms and Acronyms

<b><i>10BaseT</i></b>	10-Mbps baseband Ethernet specification using two pairs of twisted-pair cabling (Category 3, 4, or 5): one pair for transmitting data and the other for receiving data.
<b><i>10/100BaseT</i></b>	10-Mbps or 100-Mbps baseband Ethernet specification using two pairs of twisted-pair cabling (Category 5): one pair for transmitting data and the other for receiving data.
<b><i>AT+i<sup>TM</sup></i></b>	<b>Connect One's</b> Internet extension to the industry-standard Hayes AT command set. Supports simplified Internet connectivity commands in the spirit of the AT syntax.
<b><i>Base64</i></b>	<b>Encoding scheme</b> , which converts arbitrary binary data into a 64-character subset of US ASCII. The encoded data is 33% larger than the original data.
<b><i>CHAP</i></b>	<b>Challenge Authentication Protocol</b> . Extends the PAP procedure by introducing advanced elements of security.
<b><i>DNS</i></b>	<b>Domain Name System</b> . Defines the structure of Internet names and their association with IP addresses.
<b><i>iChip<sup>TM</sup></i></b>	<b>Connect One's Internet Controller for embedded Internet connectivity.</b>
<b><i>ICMP</i></b>	<b>Internet Control Message Protocol</b> . Network layer Internet protocol that reports errors and provides other information relevant to IP packet processing.
<b><i>IP</i></b>	<b>Internet Protocol</b> . Provides for transmitting blocks of data, called datagrams, from sources to destinations, which are hosts identified by fixed length addresses. Also provides for fragmentation and reassemble of long datagrams, if necessary.
<b><i>IPCP</i></b>	<b>Internet Protocol Control Protocol</b> . Establishes and configures the Internet Protocol over PPP. Also negotiates Van Jacobson TCP/IP header compression with PPP.
<b><i>ISP</i></b>	<b>Internet Service Provider</b> . Commercial company that provides Internet access to end (mostly PC) users through a dial-up connection.
<b><i>LAN</i></b>	<b>Local Area Network</b> . HIGH-speed, LOW-error data network covering a relatively small geographic area (up to a few thousand meters).
<b><i>LCP</i></b>	<b>Link Control Protocol</b> . Negotiates data link characteristics and tests the integrity of the link.

## List of Terms and Acronyms

<b><i>MIME</i></b>	<b>Multipurpose Internet Mail Extensions.</b> Extends the format of mail message bodies to allow multi-part textual and non-textual data to be represented and exchanged between Internet mail servers.
<b><i>PAP</i></b>	<b>Password Authentication Protocol.</b> Used optionally by the PPP protocol to identify the user to the ISP.
<b><i>ping</i></b>	<b>packet internet groper.</b> ICMP echo message and its reply. Often used in IP networks to test the reachability of a network device.
<b><i>POP3</i></b>	<b>Post Office Protocol Version 3.</b> Allows a workstation/PC to dynamically retrieve mail from a mailbox kept on a remote server.
<b><i>PPP</i></b>	<b>Point-to-Point Protocol.</b> Communications protocol used to send data across serial communication links, such as modems.
<b><i>RFC</i></b>	<b>Request For Comments.</b> Collections of standards that define the way remote computers communicate over the Internet.
<b><i>SMTP</i></b>	<b>Simple Mail Transfer Protocol.</b> Provides for transferring mail reliably and efficiently over the Internet.
<b><i>TCP</i></b>	<b>Transmission Control Protocol.</b> Provides reliable stream-oriented connections over the Internet. Works in conjunction with its underlying IP protocol.
<b><i>"Leave on Server"</i></b>	<b>An option</b> designating whether retrieved Email messages are to be left intact on the server for subsequent downloads or are to be deleted from the server after a successful download.

Table 9-1 Terms and Acronyms