iChip LAN ™

iChip LAN CO661AL-L

Datasheet

Ver. 1.02

International:
Connect One Ltd.
2 Hanagar Street
Kfar Saba 44425, Israel
Tel: +972-9-766-0456
Fax: +972-9-766-0461
E-mail: info@connectone.com
http://www.connectone.com

USA:
Connect One Semiconductors, Inc.
15818 North 9th Ave.
Phoenix, AZ 85023
Tel: 408-986-9602
Fax: 602-485-3715
E-mail: info@connectone.com
http://www.connectone.com

Pub. No. 11-3800-01, ©Copyright February 2003

Information provided by Connect One Ltd. is believed to be accurate and reliable. However, Connect One assumes no responsibility for its use, nor any infringement of patents or other rights of third parties, which may result from its use. No license is granted by implication or otherwise under any patent rights of Connect One other than for circuitry embodied in Connect One's products. Connect One reserves the right to change circuitry at any time without notice. This document is subject to change without notice.

The software described in this document is furnished under a license agreement and may be used or copied only in accordance with the terms of such a license agreement. It is forbidden by law to copy the software on any medium except as specifically allowed in the license agreement. No part of this document may be reproduced or transmitted in any form or by any means, electronic or mechanical, including but not limited to photocopying, recording, transmitting via fax and/or modem devices, scanning, and/or information storage and retrieval systems for any purpose without the express written consent of Connect One.

iChip, iChip LAN, iChip Plus, Socket iChip, Embedded iModem, Internet Controller, iConnector, iLAN, iModem, Instant Internet, AT+i, and Connect One are trademarks of Connect One Ltd.

Revision History 11-3800-01		
Version	**Date**	**Description**
1.00	December 2002	Original Release for iChip LAN CO661AL-L
1.01	January 2003	Internal Editing
1.02	February 2003	Change POBE pin description

Contents

Figures

Tables

1 Introduction

Description

The CO661AL-L iChip LAN™ Internet Controller™ is part of a family of intelligent peripheral devices that provides Internet connectivity solutions to a myriad of embedded devices. iChip LAN CO661AL-L is used for 10BaseT or 10/100BaseT Ethernet LAN Internet connectivity.

As an embedded, self-contained Internet engine, iChip LAN acts as mediator device between a host processor and an Internet communications platform. By completely offloading Internet connectivity and standard protocols, it relieves the host from the burden of handling Internet communications. From the perspective of a host device, the complexity of establishing and maintaining Internet-related sessions are reduced to simple, straightforward commands that are entirely dealt with within iChip LAN's domain.

A serial channel interfaces iChip LAN to a device's host processor via an on-chip UART. iChip LAN can also interface a host processor through an 8-bit parallel connection with some glue logic. iChip LAN supports 10BaseT Ethernet LANs or 10/100BaseT with an additional Ethernet controller.

Available only for 3.3-volt operation, CO661AL-L includes features not available on CO561AD-L. It includes a host interface that supports 230 kbps bandwidth in serial mode and will support 500 Kbytes/Sec burst with up to 400 Kbytes/Sec sustained bandwidth in parallel mode. CO661AL-L features power save modes and will have an extended temperature range version.

Through its host Application Programming Interface (API), iChip LAN accepts commands formatted in Connect One's AT+i™ extension to the industry-standard Hayes AT command set. IChip LAN supports several levels of status reporting to the host. Commands are available to store and manipulate functional and Internet-related non-volatile parameter data; utilize TCP and UDP sockets; transmit and receive textual Email messages; transmit and receive binary (MIME encoded) Email messages; fetch HTML web pages; manipulate files and directories via FTP; maintain Telnet sessions and download parameter and firmware updates for the host device or iChip LAN itself. IChip LAN includes a Web server engine that hosts an internal configuration Web site as well as a customizable application Web site. iChip LAN also includes a WAP server to host a WAP site.

In addition, iChip LAN includes a communication mode known as SerialNET mode, which eliminates the need to program the host CPU with AT+i commands. SerialNET allows direct host-to-Internet connectivity without requiring any reprogramming of the host application.

Functional Block Diagram

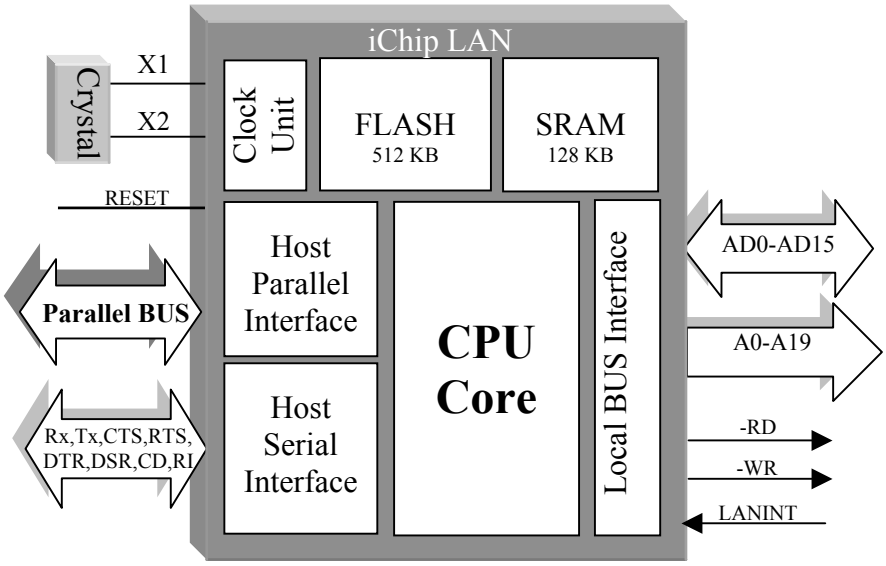


Figure 1-1 iChip LAN Functional Block Diagram

Pin Diagram

PLCC68

General Features

- Microprocessor-controllable through a standard serial connection or 8-bit parallel interface.
- Supports remote firmware update by host, Email, Web.
- Includes onboard 128KB SRAM and 512KB flash memory.
- Driven by Connect One's AT+i extension to the AT command set.
- Stand-alone Internet communication capabilities.
- Binary Base64 encoding and MIME.
- Opens up to 10 simultaneous TCP or UDP sockets and up to 2 Listen (server) sockets.
- Operates at 3.3V, CMOS technology.
- Onboard non-volatile memory stores all functional and Internet-related parameters.
- Supports several layers of status reports.
- Internal self-test procedures.
- Automatic power save mode
- Sleep Mode (with external glue logic)
- Auto baud rate detection up to 115,200 bps.
- Support for 230,400 bps (without auto baud rate).
- Supports hardware and software flow control.
- PLCC68 package.

General Protocols

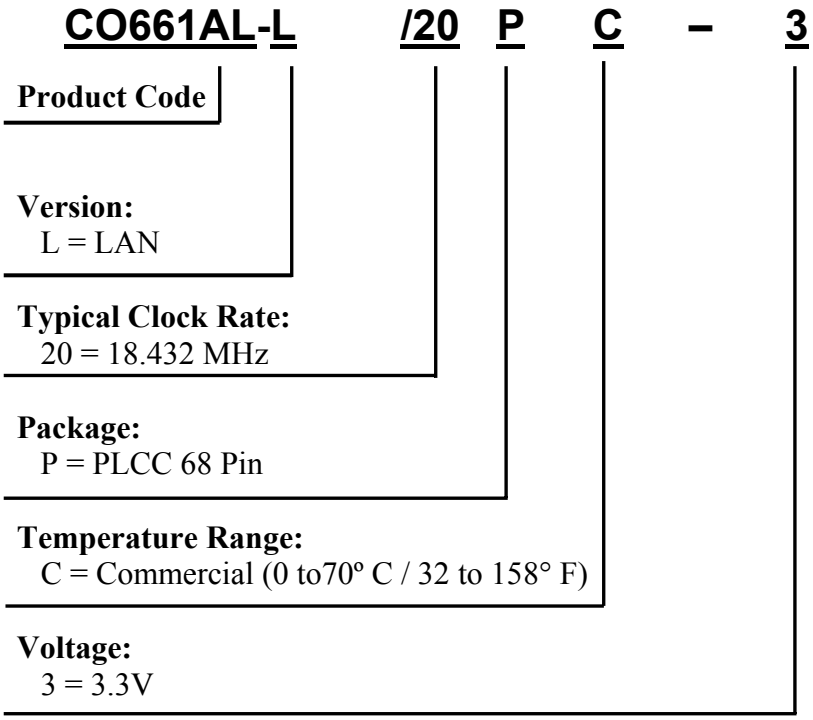
- Supports following Internet Protocols: IP, TCP, UDP, DNS, SMTP, POP3, MIME, HTTP, FTP, WAP, and Telnet
- Includes Web server and WAP server

LAN Features

- Supports LAN Internet Protocols: ARP, ICMP, and DHCP.
- Provides 10BaseT and 10/100BaseT Ethernet LAN connectivity.
- Supports up to 230.4 Kbps maximum throughput with a serial host interface and 400 Kbytes throughput with a parallel host interface.
- SerialNET mode for Serial to Ethernet routing.

2 Ordering Information

2.1 iChip LAN CO661AL-L Order Number



3 Functional Description

3.1 Overview

Connect One's iChip LAN Internet Controller is an integrated, firmware-driven, self-contained Internet engine that is available in a 68-pin PLCC package. iChip LAN accepts simple ASCII commands from a host CPU via a serial or parallel communication channel and manages an Internet communication session through an Ethernet LAN connection.

For 10BaseT Ethernet applications, iChip LAN CO661AL-L includes the firmware and pin-out necessary to drive an external Crystal LAN CS8900A. For 10/100BaseT Ethernet applications, iChip LAN includes the firmware and pin-out necessary to drive an external SMSC LAN91C111 or ASIX AX88796L LAN controller.
iChip LAN supports commands to communicate via TCP and UDP sockets; to send and receive Email, Web and WAP pages/files, utilize FTP and Telnet; or to serve as a serial-to-Internet router.

iChip LAN CO661AL-L contains non-volatile flash memory to store its firmware and Internet-related configuration parameters. Remote firmware and parameter updates are supported through the local host link, by Email or using its configuration Web site.

3.2 Technical Specifications

3.2.1 General

iChip LAN constitutes a complete Internet messaging solution for non-PC embedded devices. It acts as a mediator device to completely offload the host processor of Internet-related software and activities. An industry-standard asynchronous serial link or 8-bit parallel BUS (with some external circuitry) connects iChip LAN to the host processor. Programming, monitoring and control are fully supported using Connect One's AT+i extension to the standard AT command set.

3.2.2 Operation

All iChip LAN Internet and parameter operations are controlled by AT+i commands.

3.2.2.1 Command Mode

iChip LAN commands are implemented using the AT+i command set. Command flow exists only on the host serial channel between the host and iChip LAN.

3.2.2.2 Internet Mode

iChip LAN enters Internet mode after being issued an Internet command such as to send or receive an Email message, open a socket, etc. While in this mode, AT+i commands are supported to monitor and control the process when needed.

3.2.2.3 SerialNET Mode

iChip LAN SerialNET mode extends a local asynchronous serial link to a TCP or UDP socket across the LAN or internet . Its main purpose is to allow simple devices, which normally interact over a serial line, to interact in a similar fashion across a network, without requiring any changes in the device itself. iChip LAN contains a set of associated operational parameters, which define the nature of the desired network connection. iChip LAN supports both Server and Client modes in SerialNET mode. AT+i commands are not required to operate SerialNET mode. Thus, SerialNET mode may be used in existing systems with little or no need to modify the application program.

3.2.3 Remote Internet Firmware Update

New firmware may be uploaded from a remote location using standard Internet protocols. iChip LAN accepts Emails with new firmware attachments, as well as firmware uploads from a remote browser through iChip LAN's Web server.

3.2.4 Local BUS connection to an Ethernet LAN controller

iChip LAN interfaces an Ethernet LAN controller connected to its 16-bit local BUS.

3.2.5 Host Connection

iChip LAN can interface a host processor through one of two methods: Serial or Parallel.

3.2.5.1 Host Serial Connection

iChip LAN supports a full-duplex, TTL-level serial communications link with the host processor. Full EIA-232-D hardware flow control, including Tx, Rx, CTS, RTS, DTR, and DSR lines, is supported.

CO661AL-L supports standard baud rate configurations from 2,400 bps up to 230,400[1] bps on the host asynchronous serial communications channel. The default baud rate may be changed permanently by using the AT+iBDRF command. Auto baud rate setting is supported for all baud rates except 230,400.

3.2.5.2 Host Parallel Connection

iChip LAN supports an 8-bit parallel BUS interface with some additional logic. The parallel BUS may be defined as an 80x86 (Intel) BUS or an MC68xxx (Motorola) BUS.

Note: 1: 230Kbps is available only from iChip LAN firmware version 704.

3.2.6 Hardware and Software Flow Control

Hardware flow control is supported between the host serial connection and iChip LAN. Flow control is programmed via the AT+iFLW command. The default flow control method is set to “Wait/Continue” software flow control (which is similar to XON/XOFF software flow control) between iChip LAN and the host processor.

The hardware flow control method frees the host CPU from monitoring and handling the software flow control. The host can program iChip LAN to either use hardware flow control or “Wait/Continue” software flow control. The flow control mechanism is based on the RTS/CTS signals.

The host parallel connection has built-in hardware flow control signals as part of the interface logic.

4 Hardware Interface

iChip LAN CO661AL-L may interface a host CPU in one of two methods: Serial or Parallel. The actual interface depends on the state of the –SER/PAR pin.

4.1 Serial Host Interface

The host interface is a serial DTE interface. Speeds of 2400, 4800, 9600, 19200, 38400, 57600, 115200 and 230400 bps are supported in the following data format:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Transmission Length (No. of Bits)
None	8	1[1]	10

Table 4-1 Host Data Format

All host serial input signals (RXDH, -CTSH, -DSRH) are 5V tolerant.

4.2 Parallel Host Interface [2]

In parallel interface mode, iChip LAN connects to a host CPU through a parallel interface using a PAL (i.e., Altera "EPM7032AEC44"). The host parallel BUS may be an 80x86 (Intel) or a 68K (Motorola) BUS. With some small changes to the PAL, the user may customize an interface to any other BUS architecture. iChip LAN is connected to the interface PAL through the following signals:

- **PCS**: Parallel chip select signal. When PCS is high, the PAL is selected.
- **-RD**: When –RD is LOW, iChip LAN reads data from PAL.
- **-WR**: When –WR is LOW, iChip LAN writes data to PAL.
- **D0-D7**: Bi-directional data BUS.
- **-PRES**: Parallel reset. When LOW, generates a reset signal to the parallel interface.
- **-PERR**: Parallel error. When LOW, indicates a parallel interface error.
- **POBE**: Parallel Output Buffer Empty. When HIGH, indicates that the output buffer is empty and iChip LAN may send additional data to host. When iChip LAN sends a data byte, this signal goes LOW until the host reads the data.
- **PIBF**: Parallel Input Buffer Full. When HIGH, indicates that the input buffer is full and iChip LAN may read a data byte from the host. When iChip LAN reads the data byte, this signal goes LOW.

Notes: 1: When hardware flow control is enabled, the iChip LAN transmitter will add an additional stop bit.
2: Parallel interface mode will be available only from iChip LAN firmware version 801.

4.2.1 80x86 BUS

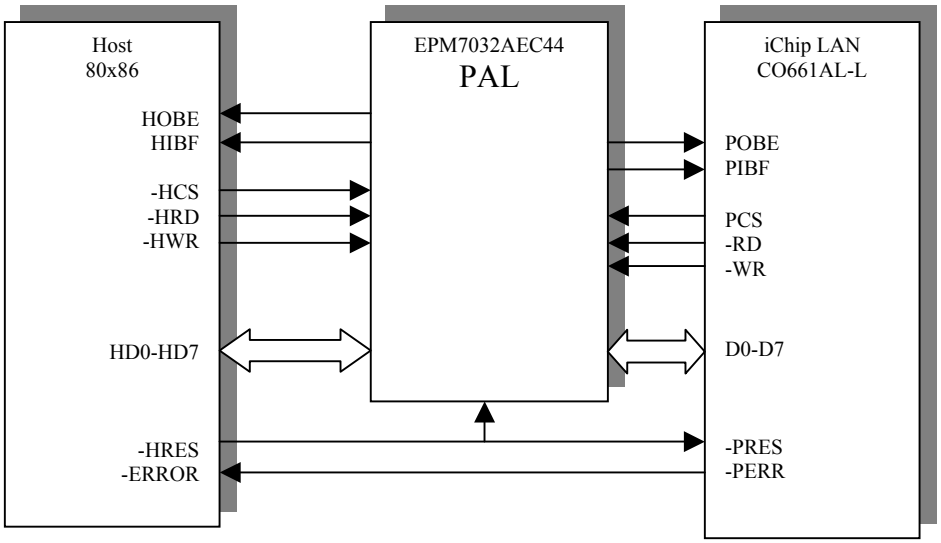


Figure 4-1 Interface to an 80x86 Type BUS

This BUS type includes the following signals:

- **-HCS**: Host Chip-Select signal. When -HCS is low, PAL is selected.
- **-HRD**: Host Read Data. When –HRD is LOW, a data is read from the PAL.
- **-HWR**: Host Write Data. When –HWR is LOW, a data byte is written to the PAL.
- **HD0 – HD7**:
  Bi-directional Host data BUS.
- **-HRES**: Parallel reset. A LOW generates a reset signal to the parallel interface. This pin may be connected to an 80x86 output port.
- **-HERR**: Parallel error. A LOW indicates a parallel interface error. This pin may be connected to an input port on the 80x86.
- **HOBE**[1]: Host Output Buffer Empty. When HIGH, indicates that the output buffer is empty and the host may send a data byte to iChip LAN. When the Host sends a data byte, this signal goes LOW until iChip LAN reads the data. This signal may be connected to an interrupt or I/O pin on the 80x86.
- **HIBF**[1]: Host Input Buffer Full. When HIGH, indicates that the input buffer is full and the host may read a data byte from iChip LAN. When the host reads the data, this signal goes LOW. This pin may be connected to an interrupt or I/O pin on the 80x86.

Note 1: HOBE and HIBF complement PIBF and POBE respectively.

4.2.2 MC68xxx BUS

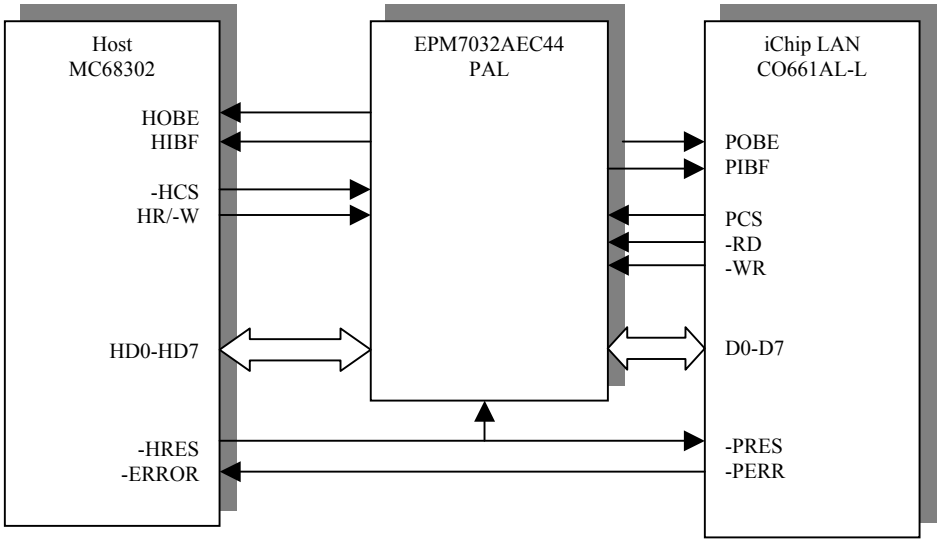


Figure 4-2 Interface to an MC68xxx Type BUS

This BUS type includes the following signals:

- **-HCS**: Host Chip-Select signal. When -HCS is LOW, PAL is selected.
- **-HR/-W**:Host read/write data from/to iChip LAN. When HR/-W is LOW, it indicates a write cycle; otherwise it is a read cycle.
- **HD0 – HD7**:
  Bi-directional Host data BUS.
- **-HRES**: Parallel reset. A LOW generates a reset signal to the parallel interface. This pin may be connected to an MC68xxx output port.
- **-HERR**: Parallel error. A LOW indicates a parallel interface error. This pin may be connected to an input port on the 80x86.
- **HOBE**[1]: Host Output Buffer Empty. When HIGH, indicates that the output buffer is empty and the host may send a data byte to iChip LAN. When the Host sends a data byte, this signal goes LOW until iChip LAN reads the data. This signal may be connected to an interrupt or I/O pin on the MC68xxx.
- **HIBF**[1]: Host Input Buffer Full. When HIGH, indicates that the input buffer is full and the host may read a data byte from iChip LAN. When the host reads the data, this signal goes low. This pin may be connected to an interrupt or I/O pin on the MC68xxx.

Note 1: HOBE and HIBF complement PIBF and POBE respectively.

4.3 LAN Interface

iChip LAN directly interfaces an Ethernet LAN MAC/PHY device on its 16-bit local BUS. Currently iChip LAN supports the Crystal LAN CS8900A Ethernet controllers for 10BaseT and SMSC LAN91C111 and ASIX AX88796L Ethernet controllers for 10/100BaseT.

5 Pin Descriptions

5.1 iChip LAN CO661AL-L Pin Assignments

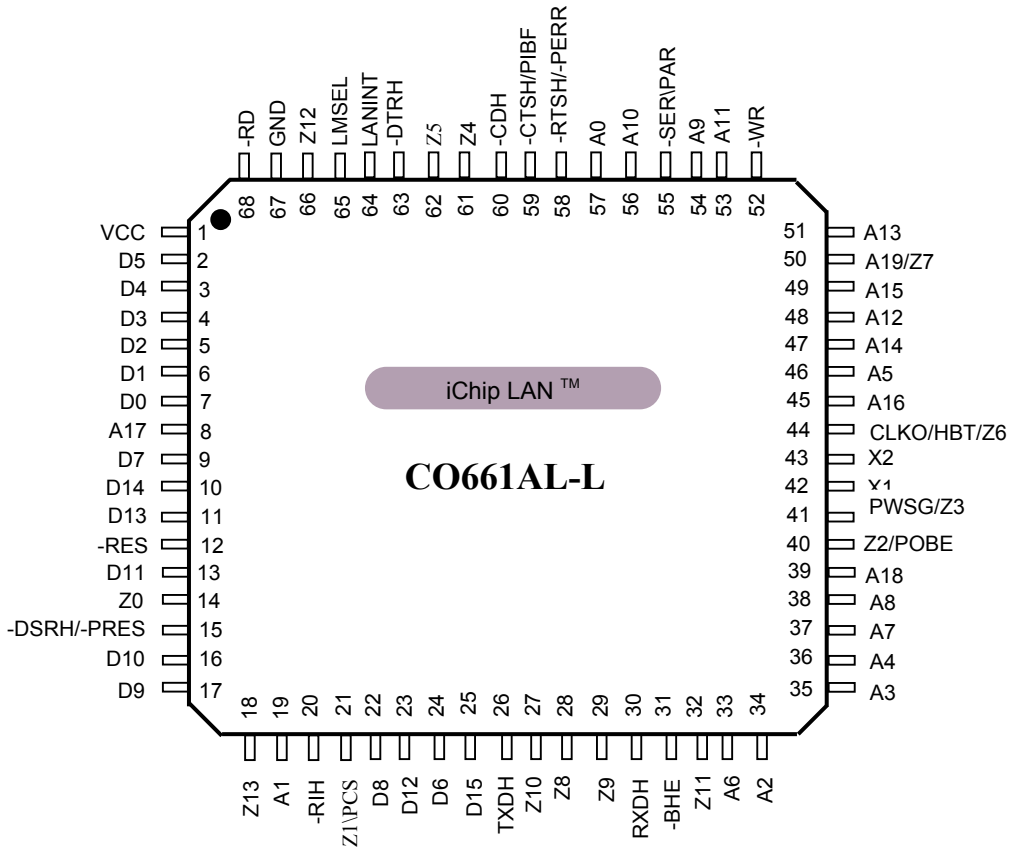


Figure 5-1 PLCC68 Package for iChip LAN CO661AL-L

5.2 iChip LAN Pin Functional Descriptions

5.2.1 Local BUS Signals

<table>
<tr><th>Signal</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>A[18:0]</td><td>O</td><td>39, 8, 45, 49, 47, 51, 48, 53, 56, 54, 38, 37, 33, 46, 36, 35, 34, 19, 57</td><td>Address BUS: These pins supply addresses to the system.
These pins should be connected to the address BUS of the LAN controller.</td></tr>
<tr><td>A19/Z7</td><td>O</td><td>50</td><td>Address BUS MSB.
This pin should be connected to the LAN controller’s address BUS MSB.
In the future, this pin may be changed to a General Purpose Output (GPIO Z7).</td></tr>
<tr><td>D[15:0]</td><td>O/I</td><td>25, 10, 11, 23, 13, 16, 17, 22, 9, 24, 2, 3, 4, 5, 6, 7</td><td>Data BUS: These pins supply data to/from the system.
These pins should be connected to the data BUS of the LAN controller.</td></tr>
<tr><td>-BHE</td><td>O</td><td>31</td><td>BUS HIGH Enable: This pin and the least-significant address bit (A0) indicate to the system which bytes of the data BUS (upper, lower, or both) participate in a BUS cycle. The -BHE and A0 pins are encoded as shown in the table below.
<table>
<tr><th>-BHE</th><th>AD0</th><th>Type of BUS cycle</th></tr>
<tr><td>0</td><td>0</td><td>Word Transfer</td></tr>
<tr><td>1</td><td>0</td><td>Even Byte Transfer</td></tr>
<tr><td>0</td><td>1</td><td>Odd Byte Transfer</td></tr>
<tr><td>1</td><td>1</td><td>N/A</td></tr>
</table>
This pin should be connected to -BHE on the LAN controller.</td></tr>
</table>

Signal	Type	Pin No.	Description
-RD	O	68	READ: This pin indicates that iChip LAN is performing a read cycle. This pin should be connected to -RD on the LAN controller.
-WR	O	52	WRITE: This pin indicates that iChip LAN is performing a write cycle This pin should be connected to -WR on the LAN controller.

5.2.2 Miscellaneous Signals

Signal	Type	Pin No.	Description
LMSEL	I	65	LAN Mode Select: • When this pin is held LOW during power up for at least 5 seconds, iChip LAN will automatically enter firmware update mode. • During a firmware update procedure, when an external modem dials to the iChip LAN, pulling this pin down to LOW will cause the iChip LAN to immediately answer the call and begin the update session. • When this pin is held LOW during power up for less than 5 seconds, it forces iChip LAN into auto baud rate detection.
-RES	I	12	RESET: When -RES is LOW, iChip LAN immediately terminates its present activity and clears its internal logic. -RES must be held LOW for at least 1 mSec after power achieves 90% VCC. This input is provided with a Schmidt trigger to facilitate power-on reset generation via an RC network.
X1	I	42	Crystal Input: This pin and the X2 pin provide connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit. To provide iChip LAN with an external clock source, connect the source to the X1 pin and leave the X2 pin unconnected.
X2	O	43	Crystal Output: This pin and the X1 pin provide connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit.

Signal	Type	Pin No.	Description
CLKO/HBT/Z6	O	44	**AT+i Configurable Pin:** **CLKO** (default): Clock Output. This pin provides a clock-out to the system at the same frequency as X1. During reset the clock out is disabled. **HBT**: Heart Beat. Provides a 50% duty cycle, 40 mSec frequency square wave, when iChip firmware is properly running. (Available from iChip Firmware ver. 7.04). In the future it may be changed to a GPIO. This pin is configurable with the AT+iPN44 command (see AT+i Programmers Manual).
-SER/PAR	I	55	Serial/Parallel mode select. This pin is sampled on the rising edge of the –RES signal. If it is LOW, iChip LAN functions in Serial mode. Otherwise it functions in Parallel mode.
LANINT	I	64	LAN Interrupt. When HIGH, this signal indicates that the LAN controller has information for iChip LAN.
-CDH	O	60	Received LAN Package: When LOW, this signal indicates that iChip LAN received a legal packet from the LAN controller. During firmware update, -SER and -RCV are used to display the firmware update status.
-RIH	O	20	Serial Indicator Host: When LOW, this signal indicates that iChip LAN has received a character from the host. During firmware update, -SER and -RCV are used to display the firmware update status.
Z0	I/O	14	GPIO for future use. This pin should be Not Connected.
Z1/PCS	I/O	21	**In Serial mode**: Z1 is available as a GPIO for future use and should be left Not Connected. **In Parallel mode**: PCS is used as a chip-select for the parallel interface PAL.

Signal	Type	Pin No.	Description
Z2/POBE	I/O	40	**In Serial mode**: Z2 is available as a GPIO for future use and should be left Not Connected. **In Parallel mode**: POBE is used as the Parallel Output Buffer Empty signal. When HIGH, iChip LAN may send a parallel data byte to the host.
PWSG/Z3	I/O	41	**AT+i Configurable Pin:** **PWSG** (default): Power Save Gate. This pin is used to disable the iChip's oscillator (X1 Pin 42) via an external gate in order to achieve full Sleep mode with minimal power consumption (see Fig. 7-6). **Z3:** General Purpose I/O.
Z4	I/O	61	Reserved as a GPIO for future use. This pin should be Not Connected.
Z5	I/O	62	Reserved as a GPIO for future use. This pin should be Not Connected.
Z8	I/O	28	Reserved as a GPIO for future use. This pin should be Not Connected.
Z9	O	29	Reserved as a GPO for future use. This pin should be Not Connected.
Z10	I/O	27	Reserved as a GPIO for future use. This pin should be Not Connected.
Z11	I/O	32	Reserved as a GPIO for future use. This pin should be Not Connected.
Z12	I/O	66	Reserved as a GPIO for future use. This pin should be Not Connected.
Z13	I/O	18	Reserved as a GPIO for future use. This pin should be Not Connected.
GND	P	67	Ground: iChip LAN Ground signal.
VCC	P	1	Power Supply: This pin supplies power (+3.3V) to iChip LAN.

5.2.3 Host Serial Interface Signals

Signal	Type	Pin No.	Description
TXDH	O	26	**In Serial mode:** Transmit Data Host: This pin supplies asynchronous serial transmit data to the host. **In Parallel mode:** this pin is used for firmware update.
RXDH	I	30	**In Serial mode:** Receive Data Host: This pin supplies asynchronous serial receive data from the host. **In Parallel mode:** this pin is used for firmware update. When not used, this pin should be connected to VCC.
-CTSH /PIBF	I	59	**In Serial mode**: Clear-to-Send Host: -CTSH is active only when host hardware flow control is enabled. When -CTSH is LOW, flow control is enabled for the host serial port, i.e., iChip LAN may transmit to the host. When -CTSH is HIGH, the iChip LAN transmitter holds its data in the serial port transmit register. -CTSH is sampled only at the beginning of a frame transmission. If -CTSH is raised while a character frame is being transmitted, that frame will be completed. Connect -CTSH to -RTSH when not in use. **In Parallel mode:** Parallel Input Buffer Full, when HIGH, indicates that the host has sent a data byte, which has not yet been read.
-RTSH/-PERR	O	58	**In Serial mode**: Ready-to-Send Host: -RTSH is active only when host hardware flow control is enabled. When -RTSH is LOW, flow control is enabled for the host serial port, i.e., the host may transmit to iChip LAN. When -RTSH is HIGH, iChip LAN indicates that its receiver is busy and cannot receive data from host. Connect -RTSH to -CTSH when not in use. **In Parallel mode:** Parallel Error, when LOW, indicates to the host that an error has occurred in the parallel interface circuit.

Signal	Type	Pin No.	Description
-DSRH/-PRES	I	15	**In Serial mode:** Data Set Ready Host: When -DSRH is LOW, it indicates that the host is attached and ready to communicate with iChip LAN. Connect -DSRH to GND when not in use. **In Parallel mode:** Parallel Reset, when LOW, generates a reset to the parallel interface.
-DTRH	O	63	Data Terminal Ready Host: When -DTRH is LOW, it indicates to the host that iChip LAN is attached and ready to communicate.

6 Electrical/Mechanical Specifications

6.1 Environmental Specifications

6.1.1 Absolute Maximum Ratings

Parameter	Rating
Voltage at local bus pins with respect to ground	-0.5 to +3.8 Volts
Voltage at all other pins with respect to ground	-0.5 to +5.5 Volts
Operating temperature	0°C to 70°C (32 to 158°F)
Storage temperature	-60°C to 120°C (–76 to 248°F)
Soldering temperature (max. 10 sec.)	220°C (428°F)
Package dissipation	1.5 Watts

Table 6-1 Environmental Specifications – Maximum Ratings

6.1.2 DC Operating Characteristics

Parameter	Min	Typical	Max	Units
DC Supply	3.0	3.3	3.6	Volts
High-level Input	2.0			Volts
Low-level Input			0.8	Volts
High-level Output[1]	2.4			Volts
Low-level Output[2]			0.4	Volts
Input leakage current			4	µA
Power supply current (Operating Mode)[3]		30		mA
Power supply current (Power-save Mode)[3]		10		mA
Input capacitance			7	pF

Notes: [1] I_{OH} =2mA
[2] I_{OL} = 2mA
[3] 18.432 MHz clock

Table 6-2 DC Operating Characteristics

6.2 Interface Timing and Waveforms

6.2.1 Switching Characteristics

Parameter	Symbol	Min.	Typical	Max.	Units
Clock Out frequency	Fclk	18.43	18.432	18.434	MHz
Clock Out period	Tclk		1/Fck		us
X2 falling to address or chip select change	Txfac	4.2		10	ns
X2 rising to read active	Txrra	4.1		8.6	ns
X2 falling to read inactive	Txfri	4.1		8.6	ns
Data setup before read high	Tdsbrh	9			ns
Data setup after read high	Tdsarh	3			ns
X2 rising to write active	Txrwa	5		8.2	ns
X2 rising to data valid	Txrdv	4.1		8.6	ns
X2 rising to write inactive	Txrwi	5		8.2	ns
Data out valid after write high	Tdovaw	2.1			ns
X2 fall time [1]	Tckhl			5	ns
X2 rise time [2]	Tcklh			5	ns
X2 LOW time	Tclck	24	27	30	ns
X2 HIGH time	Tchck	24	27	30	ns
X2 to CLKO skew	Tcico	4.2		6.6	ns
Reset pulse	Trst	1			ms
Read rising to input parallel buffer full	Trrbf	0			ns
Write rising to output parallel buffer empty	Twrbe	0			ns

Table 6-3 Switching Characteristics

[1] Fall time is from 2.3V to 1V.
[2] Rise time is from 1V to 2.3V.

6.2.2 Local BUS Read Cycle

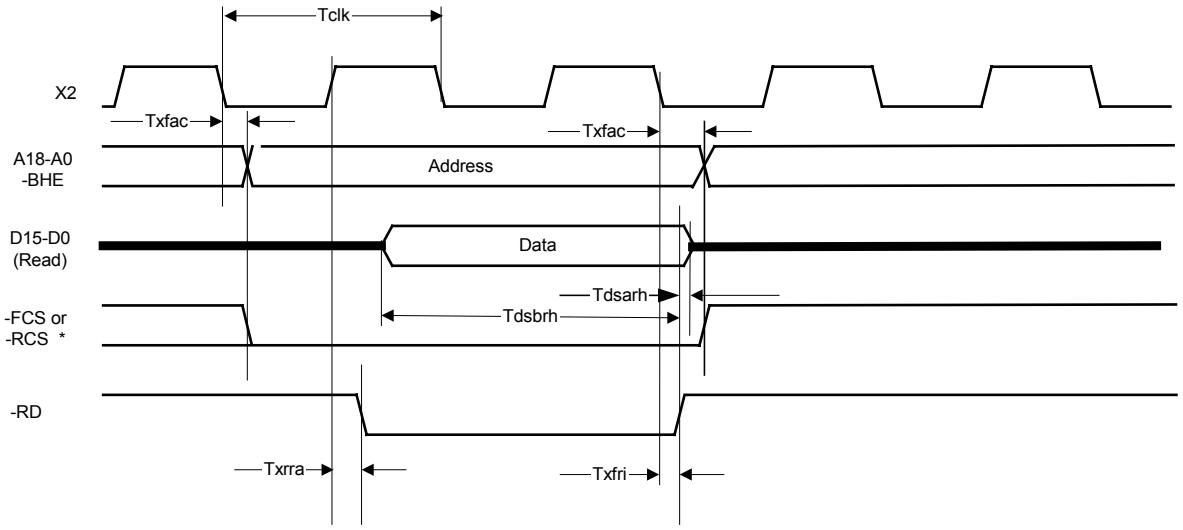


Figure 6-1 Local BUS Read Cycle

* -FCS and –RCS are internal Flash and RAM chip-select.

6.2.3 Local BUS Write Cycle

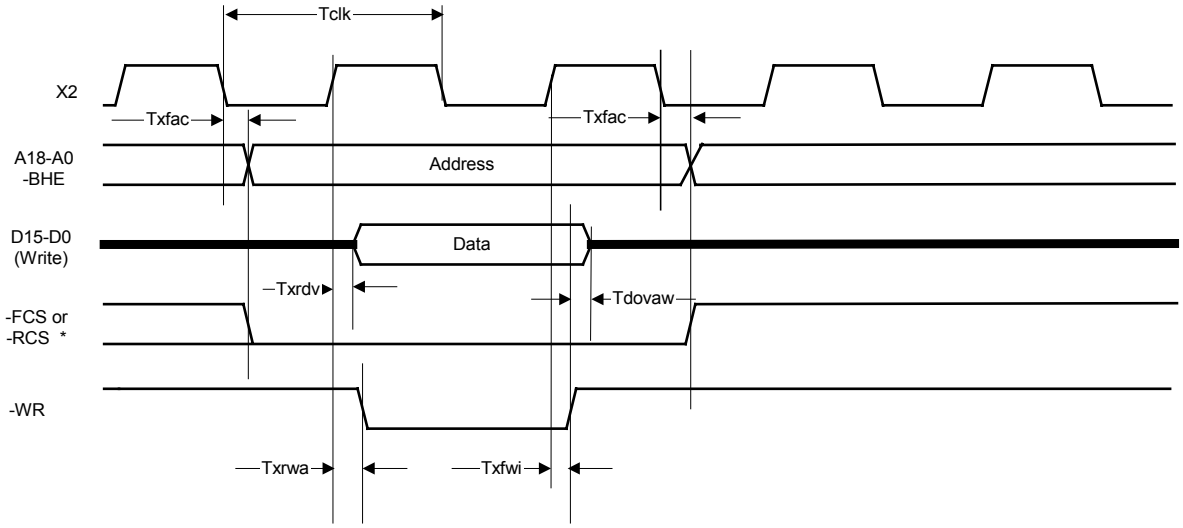


Figure 6-2 Local BUS Write Cycle

* -FCS and –RCS are internal Flash and RAM chip-select.

6.2.4 Clock Waveform

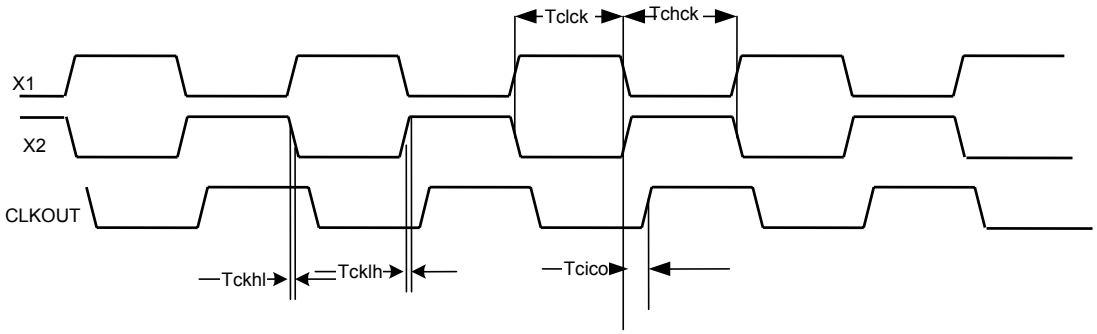


Figure 6-3 Clock Waveform

6.2.5 Reset Timing

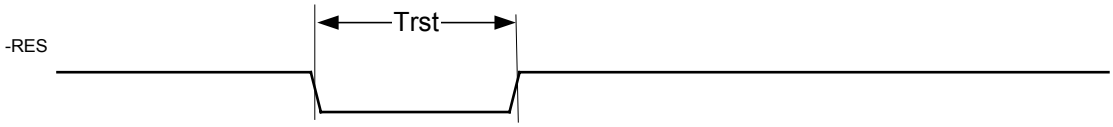


Figure 6-4 Reset Timing

6.2.6 Parallel BUS Read Cycle

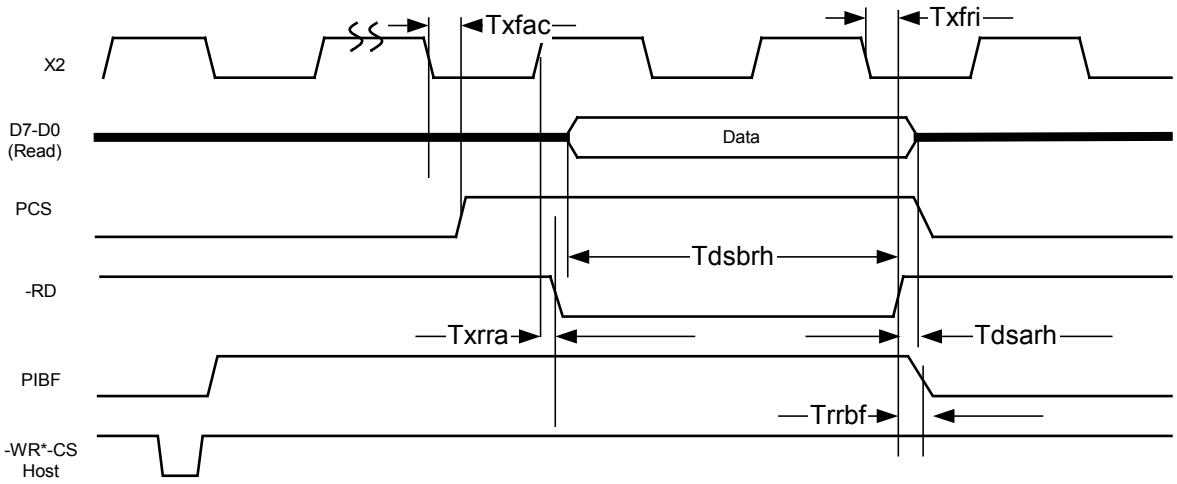


Figure 6-5 Parallel BUS Read Cycle

6.2.7 Parallel BUS Write Cycle

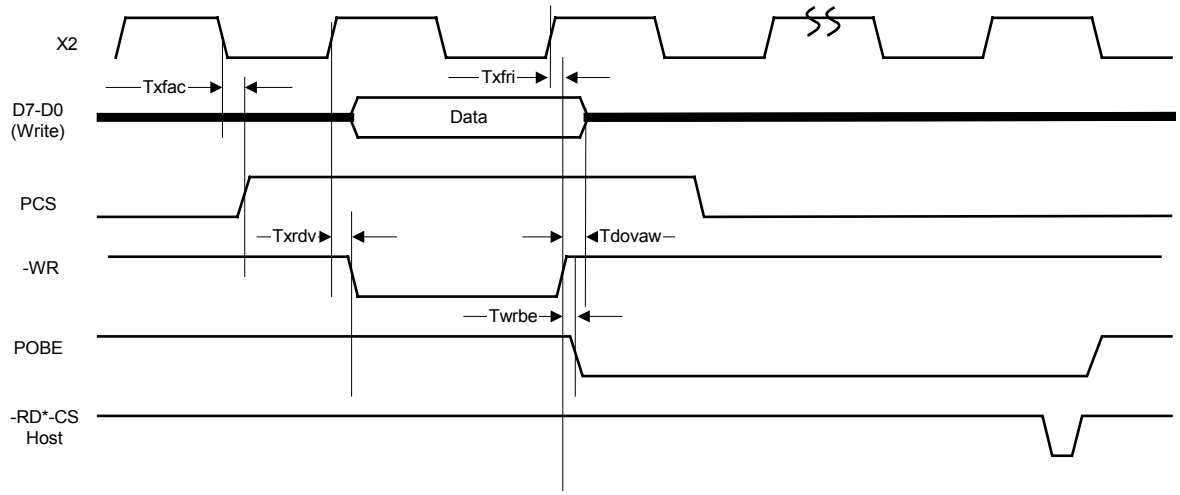


Figure 6-6 Parallel BUS Write Cycle

6.3 Mechanical Dimensions

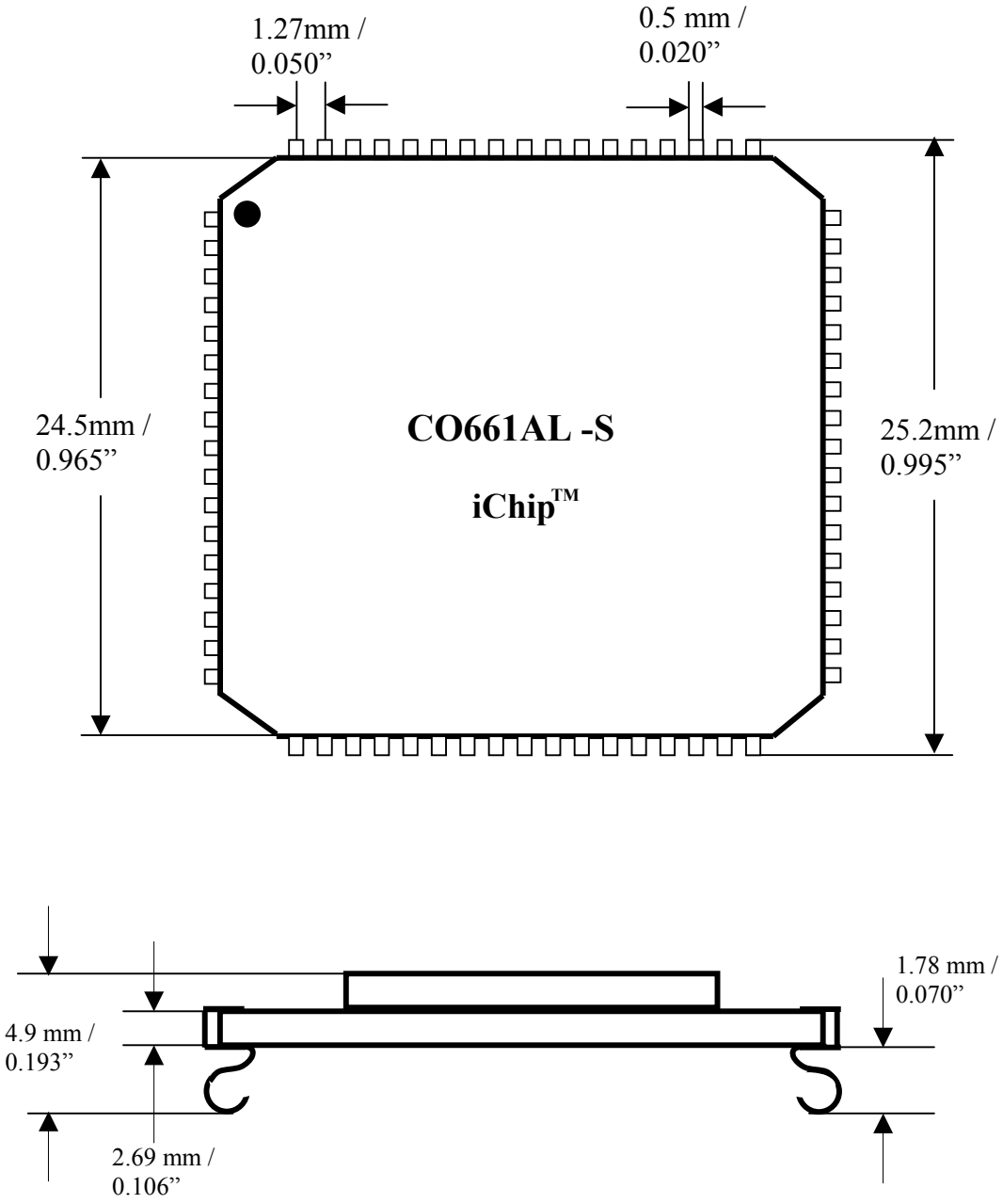


Figure 6-7 Mechanical Dimensions

7 iChip LAN Designs

7.1 Serial Host and Ethernet Controller Environment

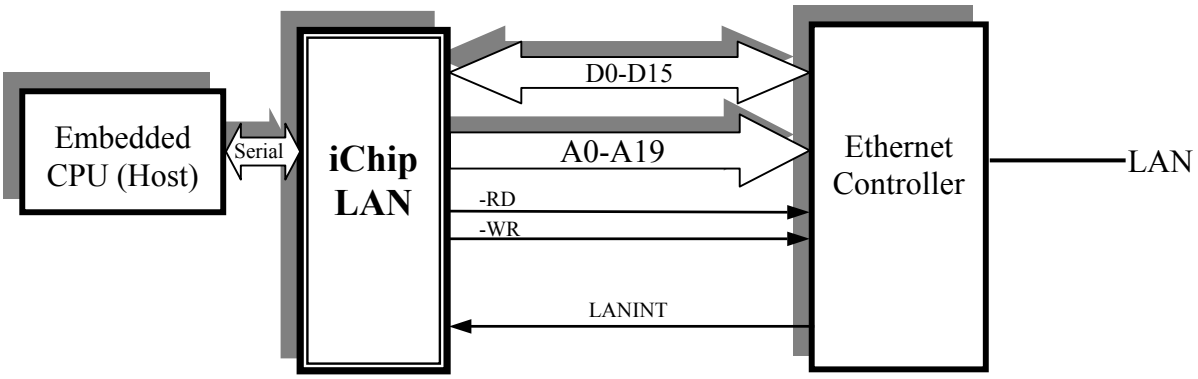


Figure 7-1 Serial Host and Ethernet Controller Environment

7.2 Parallel Host and Ethernet Controller Environment

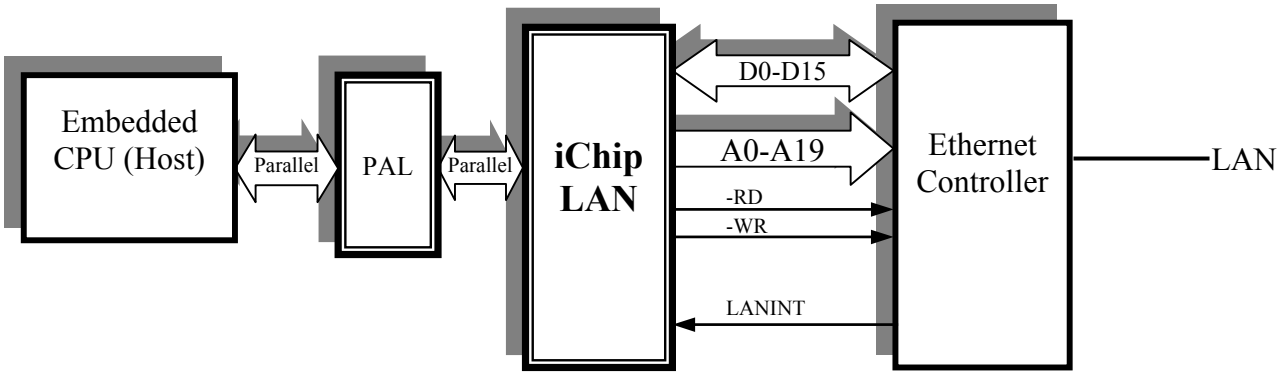


Figure 7-2 Parallel Host and Ethernet Controller Environment

7.3 Selecting a Crystal

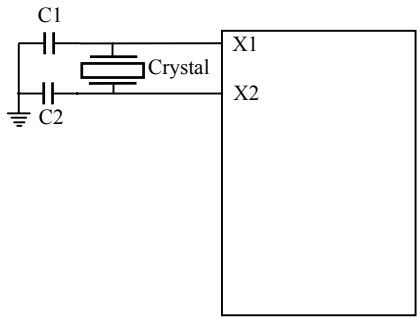


Figure 7-3 Selecting a Crystal

The characteristics of the built-in inverting amplifier set limits on the following parameters for crystals:
Crystal first overtone frequency ..... 18.432 MHz
ESR (Equivalent Series Resistance) ..... 40 Ω max
Drive Level ..... 1 mW max
Frequency tolerance ..... +/- 100ppm
Load capacitance..... 18pF
Shunt capacitance..... 7pF Maximum

The recommended range of values for C 1 and C 2 are as follows:
C 1 ..... 15 pF ± 20%
C 2 ..... 22 pF ± 20%
The specific values for C1 and C2 must be determined by the designer and are dependent on the characteristics of the chosen crystal and board design.

7.4 Selecting the Reset Circuit

7.4.1 RC Network

The Reset signal may be designed with an RC network. τ should be greater than 10 mSec. This is a low-cost solution.

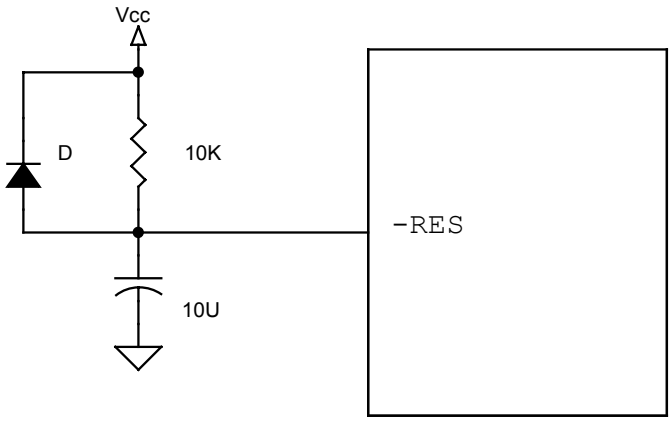


Figure 7-4 RC Reset Circuit

7.4.2 Supervisory Circuit

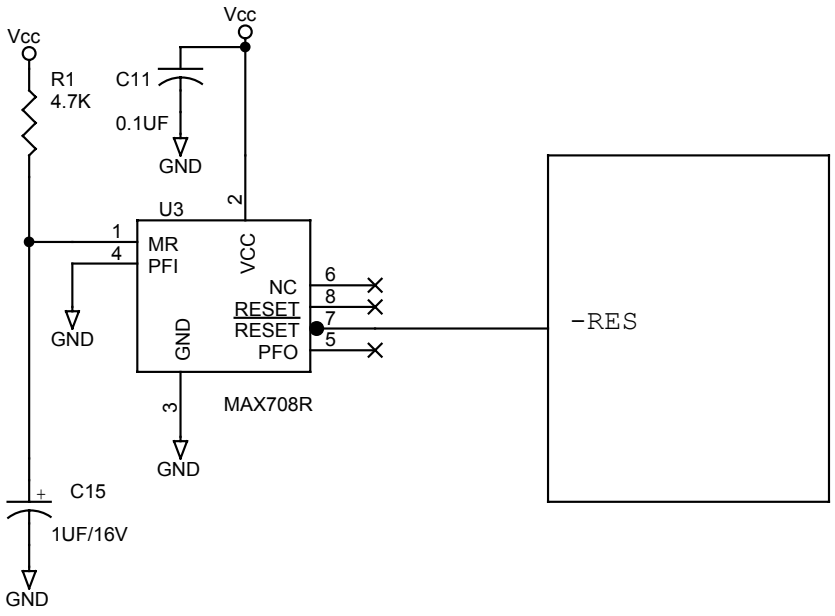


Figure 7-5 Supervisory Reset Circuit

7.5 Sleep Mode [1]

The CO661AL-L iChip LAN supports a Sleep mode to achieve maximum power conservation when the iChip is not in use. Sleep mode is based on an external circuit that gates the oscillator input to the iChip. The PWSG (pin 41) is an output pin used to trigger Sleep mode. While in this mode, iChip current consumption is reduced to ~1 mA. The external circuit is designed to wake-up and exit sleep mode when a transmission arrives from the host processor (see Fig. 7-6).

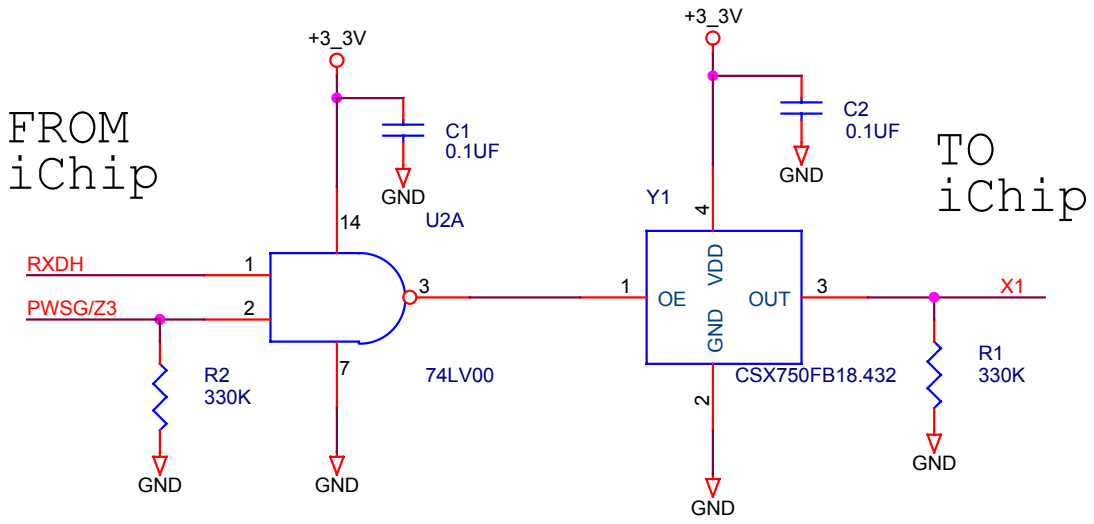


Figure 7-6 CO661AL External Sleep Mode Circuit

Note: 1: Sleep mode will be available only from iChip firmware version 801

8 Protocol Compliance

iChip LAN CO661AL-L complies with the following Internet standards:

RFC 768	User Datagram Protocol (UDP)
RFC 791	Internet Protocol (IP)
RFC 792	Internet Control Message Protocol
RFC 793	Transmission Control Protocol (TCP)
RFC 821	Simple Mail Transfer Protocol (SMTP)
RFC 826	Ethernet Address Resolution Protocol (iChip LAN)
RFC 951	Bootstrap Protocol (iChip LAN)
RFC 822	Standard for the Format of ARPA Internet Text Messages
RFC 1331	Point-to-Point Protocol (PPP) (iChip)
RFC 1332	PPP Internet Protocol Control Protocol (IPCP) (iChip)
RFC 1334	PPP Authentication Protocols (PAP) (iChip)
RFC 1661	Point-to-Point Protocol (PPP) (iChip)
RFC 1939	Post Office Protocol - Version 3 (POP3)
RFC 1957	Some Observations on the Implementations of the Post Office Protocol (POP3)
RFC 2045	Multipurpose Internet Mail Extensions (MIME) Part One: Format of Internet Message Bodies
RFC 2046	Multipurpose Internet Mail Extensions (MIME) Part Two: Media Types
RFC 2047	MIME (Multipurpose Internet Mail Extensions) Part Three: Message Header Extensions for Non-ASCII Text
RFC 2048	Multipurpose Internet Mail Extensions (MIME) Part Four: Registration Procedures
RFC 2049	Multipurpose Internet Mail Extensions (MIME) Part Five: Conformance Criteria and Examples
RFC 2068	HyperText Transfer Protocol HTTP/1.1

Table 8-1 Internet Protocol Compliance

9 List of Terms and Acronyms

10BaseT	10-Mbps baseband Ethernet specification using two pairs of twisted-pair cabling (Category 3, 4, or 5): one pair for transmitting data and the other for receiving data.
10/100BaseT	10-Mbps or 100-MBPS baseband Ethernet specification using two pairs of twisted-pair cabling (Category 5): one pair for transmitting data and the other for receiving data.
AT+i™	**Connect One's** Internet extension to the industry-standard Hayes AT command set. Supports simplified Internet connectivity commands in the spirit of the AT syntax.
Base64	**Encoding scheme**, which converts arbitrary binary data into a 64-character subset of US ASCII. The encoded data is 33% larger than the original data.
CHAP	**Challenge Authentication Protocol.** Extends the PAP procedure by introducing advanced elements of security.
DNS	**Domain Name System**. Defines the structure of Internet names and their association with IP addresses.
iChip™	**Connect One's Internet Controller for embedded Internet connectivity.**
ICMP	**Internet Control Message Protocol**. Network layer Internet protocol that reports errors and provides other information relevant to IP packet processing.
IP	**Internet Protocol**. Provides for transmitting blocks of data, called datagrams, from sources to destinations, which are hosts identified by fixed length addresses. Also provides for fragmentation and reassemble of long datagrams, if necessary.
IPCP	**Internet Protocol Control Protocol**. Establishes and configures the Internet Protocol over PPP. Also negotiates Van Jacobson TCP/IP header compression with PPP.
ISP	**Internet Service Provider**. Commercial company that provides Internet access to end (mostly PC) users through a dial-up connection.
LAN	**Local Area Network**. HIGH-speed, LOW-error data network covering a relatively small geographic area (up to a few thousand meters).
LCP	**Link Control Protocol**. Negotiates data link characteristics and tests the integrity of the link.

MIME	**Multipurpose Internet Mail Extensions**. Extends the format of mail message bodies to allow multi-part textual and non-textual data to be represented and exchanged between Internet mail servers.
PAP	**Password Authentication Protocol**. Used optionally by the PPP protocol to identify the user to the ISP.
ping	**packet internet groper**. ICMP echo message and its reply. Often used in IP networks to test the reachability of a network device.
POP3	**Post Office Protocol Version 3**. Allows a workstation/PC to dynamically retrieve mail from a mailbox kept on a remote server.
PPP	**Point-to-Point Protocol**. Communications protocol used to send data across serial communication links, such as modems.
RFC	**Request For Comments**. Collections of standards that define the way remote computers communicate over the Internet.
SMTP	**Simple Mail Transfer Protocol**. Provides for transferring mail reliably and efficiently over the Internet.
TCP	**Transmission Control Protocol**. Provides reliable stream-oriented connections over the Internet. Works in conjunction with its underlying IP protocol.
"Leave on Server"	**An option** designating whether retrieved Email messages are to be left intact on the server for subsequent downloads or are to be deleted from the server after a successful download.

Table 9-1 Terms and Acronyms