iChip ™

iChip CO661AL-S

Datasheet

Ver. 1.05

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Revision History 11-3600-02		
Version	**Date**	**Description**
1.00	December 2002	Original Release for iChip CO661AL-S
1.04	January 2003	Internal Editing
1.05	February 2003	Change POBE pin description

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1 Introduction

Description

The CO661AL-S iChip™ Internet Controller™ is part of a family of intelligent peripheral devices that provides Internet connectivity solutions to a myriad of embedded devices. iChip CO661AL-S is designed for use with dial-up and wireless modems. As an embedded, self-contained Internet engine, iChip acts as mediator device between a host processor and an Internet communications platform. By completely offloading Internet connectivity and standard protocols, it relieves the host from the burden of handling Internet communications. From the perspective of a host device, the complexity of establishing and maintaining Internet-related sessions are reduced to simple, straightforward commands that are entirely dealt with within iChip's domain.

A serial channel interfaces iChip CO661AL-S to a device's host processor via an on-chip UART. CO661AL-S can also interface a host processor through an 8-bit parallel connection with some glue logic. iChip CO661AL-S directly interfaces a serial data modem for transparent modem communication, and also supports independent communications on the Internet via a dial-up or wireless connection to an Internet Service Provider (ISP). iChip CO661AL-S supports AMPS, CDMA, CDPD, GPRS, GSM, iDEN, and TDMA cellular modems.

Available only for 3.3-volt operation, CO661AL-S includes features not available on CO561AD-S. It includes a host interface that supports up to 230 kbps bandwidth in serial mode and will support a 500 Kbytes/Sec burst rate in parallel mode. CO661AL-S features power save modes and will have an extended temperature range version.

Through its host Application Programming Interface (API), iChip accepts commands formatted in Connect One's AT+i™ extension to the industry-standard Hayes AT command set. iChip supports several levels of status reporting to the host. Commands are available to store and manipulate functional and Internet-related non-volatile parameter data; utilize TCP and UDP sockets; transmit and receive textual Email messages; transmit and receive binary (MIME encoded) Email messages; fetch HTML web pages; manipulate files and directories via FTP; maintain Telnet sessions and download parameter and firmware updates for the host device or iChip itself. iChip includes a Web server engine that hosts an internal configuration Web site as well as a customizable application Web site. iChip also includes a WAP server to host a WAP site.

When the host CPU issues standard AT commands, iChip CO661AL-S provides direct access to the modem by automatically operating in Transparent mode, emulating a direct host-to-modem environment. When the host CPU issues AT+i commands, iChip enters Internet mode and controls the modem connection to an ISP. iChip provides all the necessary procedures to log onto an ISP, authenticate the user and establish an Internet session. Upon receiving an AT+i command, iChip independently manages standard Internet protocols to transmit and receive data over PPP. iChip also includes a mode known as SerialNET mode, which eliminates the need to program the host CPU with AT+i commands, and enables serial-to-Internet routing.

Functional Block Diagram

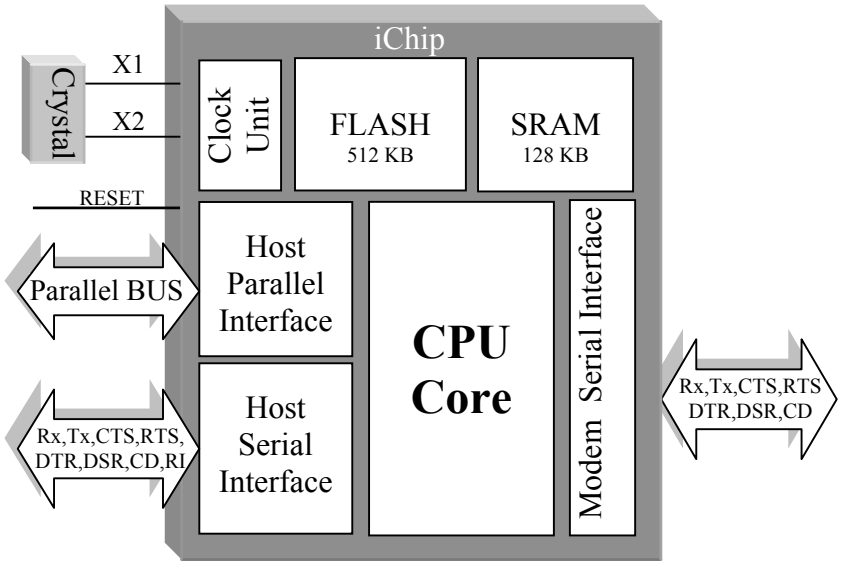
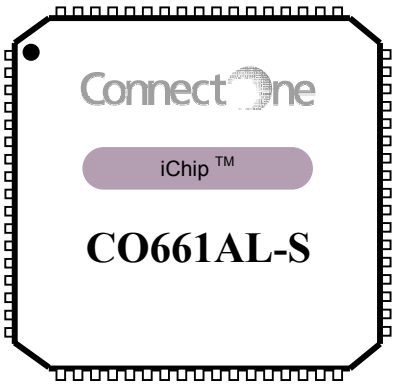


Figure 1-1 iChip Functional Block Diagram

Pin Diagram

PLCC68



General Features

- Microprocessor-controllable through a standard serial connection or 8-bit parallel interface.
- Supports remote firmware update by host, Email, Web or direct modem-to-modem communications.
- Includes onboard 128KB SRAM and 512KB flash memory.
- Driven by Connect One's AT+i extension to the AT command set.
- Stand-alone Internet communication capabilities.
- Binary Base64 encoding and MIME.
- Opens up to 10 simultaneous TCP or UDP sockets and up to 2 Listen (server) sockets.
- Operates at 3.3V, CMOS technology.
- Onboard non-volatile memory stores all functional and Internet-related parameters.
- Supports several layers of status reports.
- Internal self-test procedures.
- Automatic power save mode
- Sleep Mode (with external glue logic)
- Auto baud rate detection up to 115,200 bps.
- Support for 230,400 bps (without auto baud rate).
- Supports hardware and software flow control.
- PLCC68 package.

General Protocols

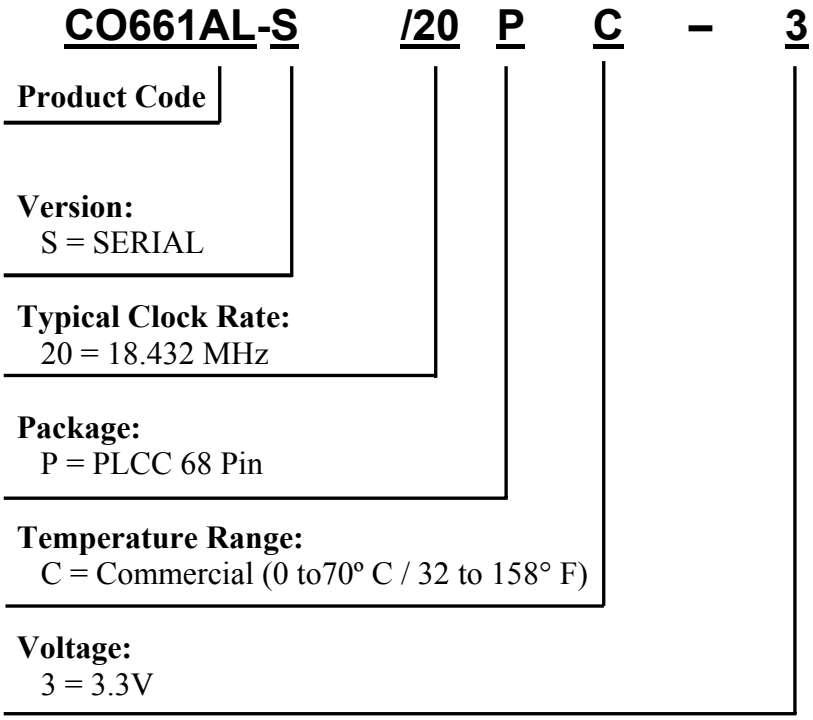
- Supports following Internet Protocols: IP, TCP, UDP, DNS, SMTP, POP3, MIME, HTTP, FTP, WAP, and Telnet
- Includes Web server and WAP server

Dial-up Features

- Supports dialup Internet Protocols: PPP, LCP, IPCP, and PAP or CHAP authentication.
- Supports data modems up to 56 Kbps.
- Supports AMPS, CDMA, TDMA, GSM, CDPD, GPRS and iDEN cellular modems.
- Stay-on-line feature for multiple send/receive sessions.
- SerialNET mode for serial-to-Internet routing.
- Transparent mode supports all direct modem commands.

2 Ordering Information

2.1 iChip CO661AL-S Order Number:



3 Functional Description

3.1 Overview

Connect One's iChip Internet Controller is an integrated, firmware-driven, self-contained Internet engine that is available in a 68-pin PLCC package. iChip accepts simple ASCII commands from a host CPU via a serial or parallel communication channel and manages an Internet communication session through a PSTN or cellular modem. iChip supports commands to communicate via TCP and UDP sockets; to send and receive Email, Web and WAP pages/files; utilize FTP and Telnet; or to serve as a serial-to-Internet router.

iChip CO661AL-S contains non-volatile flash memory to store its firmware and Internet-related configuration parameters. Remote firmware and parameter updates are supported through the local host link, by Email, using a Web browser or by direct modem communications.

3.2 Technical Specifications

3.2.1 General

iChip constitutes a complete Internet messaging solution for non-PC embedded devices. It acts as a mediator device to completely offload the host processor of Internet-related software and activities. An industry-standard asynchronous serial link connects iChip to the host processor. Programming, monitoring and control are fully supported using Connect One's AT+i extension to the standard AT command set.

An additional industry-standard asynchronous serial link connects iChip CO661AL-S to a standard serial modem. iChip supports transparent direct host-to-modem operations using the standard AT command set.

3.2.2 Operation

All iChip Internet and parameter operations are controlled by AT+i commands.

3.2.2.1 Transparent Mode

iChip CO661AL-S defaults to Transparent mode, allowing the host to control the modem device directly. Control is implemented by issuing standard AT commands to iChip. In this mode, iChip CO661AL-S transparently echoes the AT commands to the modem, as well as echoing the modem responses back to the host. In addition, hardware flow control signals are emulated on the host side to reflect the levels set by the modem and vice-versa. iChip CO661AL-S supports interlacing AT+i and AT commands, while the modem is in Command mode.

When the modem is put into data mode (by issuing a dial command), Transparent mode is sustained throughout the data mode session.

3.2.2.2 Command Mode

iChip commands are implemented using the AT+i command set. Command flow exists only on the host serial channel between the host and iChip.

3.2.2.3 Internet Mode

iChip enters Internet mode after being issued an Internet command such as to send or receive an Email message, open a socket, etc. iChip attempts to establish an Internet connection and carry out the required activity over PPP. While in this mode, AT+i commands are supported to monitor and control the process when needed.

3.2.2.4 SerialNET Mode

iChip SerialNET mode extends a local asynchronous serial link to a TCP or UDP socket across the Internet. Its main purpose is to allow simple devices, which normally interact over a serial line, to interact in a similar fashion across a network, without requiring any changes in the device itself. iChip contains a set of associated operational parameters, which define the nature of the desired network connection. iChip supports both Server and Client modes in SerialNET mode. AT+i commands are not required to operate SerialNET mode. Thus, SerialNET mode may be used in existing systems with little or no need to modify the application program.

3.2.2.5 Direct Modem Firmware Update Mode

Issuing the AT+iFU command enters Firmware Update mode. iChip CO661AL-S monitors the modem for an incoming call by detecting the 'RING' response. When called, iChip CO661AL-S instructs the modem to answer the call and assumes a YMODEM session to receive a file containing a firmware update. The incoming file contents are downloaded and authenticated. If the new firmware image checks out, the existing firmware is replaced in the on-chip flash memory and iChip CO661AL-S is reinitialized.

3.2.3 Remote Internet Firmware Update

New firmware may be uploaded from a remote location using standard Internet protocols. iChip accepts Emails with new firmware attachments, as well as firmware uploads from a remote browser through iChip's Web server.

3.2.4 Serial Connection to Analog Modem

iChip CO661AL-S supports a full-duplex, TTL-level serial communications link with the modem device. Full EIA-232-D hardware flow control, including Tx, Rx, CTS, RTS, DTR, DSR and CD lines, is supported. However, it does not support the RI line.

3.2.5 Host Connection

iChip can interface a host processor through one of two methods: Serial or Parallel.

3.2.5.1 Host Serial Connection

iChip supports a full-duplex, TTL-level serial communications link with the host processor. Full EIA-232-D hardware flow control, including Tx, Rx, CTS, RTS, DTR, DSR, RI and CD lines, is supported.

CO661AL-S supports standard baud rate configurations from 2,400 bps up to 230,400 bps on the host asynchronous serial communications channel. The default baud rate may be changed permanently by using the AT+iBDRF command. Auto baud rate setting is supported for all baud rates except 230,400.

3.2.5.2 Host Parallel Connection

iChip supports an 8-bit parallel BUS interface with some additional logic. The parallel BUS may be defined as an 80x86 (Intel) BUS or an MC68xxx (Motorola) bus.

3.2.6 Serial Hardware and Software Flow Control

Hardware flow control is supported on a host serial connection and between iChip and a serial modem. Flow control is programmed via the AT+iFLW command. The default flow control methods are set to “Wait/Continue” software flow control (which is similar to XON/XOFF software flow control) between iChip and the host, and no flow control between iChip and the modem.

The hardware flow control method frees the host CPU from monitoring and handling the software flow control. The host can program iChip to either use hardware flow control or to use “Wait/Continue” software flow control between iChip and the host CPU. The flow control mechanism is based on the RTS/CTS signals.

Flow control between iChip and the modem can be individually programmed to hardware flow control or no flow control.

The host parallel connection has built-in hardware flow control signals as part of the interface logic.

4 Hardware Interface

iChip CO661AL-S may interface a host CPU in one of two methods: Serial or Parallel. The actual interface depends on the state of the –SER/PAR pin.

4.1 Serial Host Interface

The host interface is a serial DTE interface. Speeds of 2400, 4800, 9600, 19200, 38400, 57600, 115200 and 230400 bps are supported in the following data format:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Transmission Length (No. of Bits)
None	8	1[1]	10

Table 4-1 Host Data Format

All host serial input signals (RXDH, -CTSH, -DSRH) are 5V tolerant.

4.2 Parallel Host Interface [2]

In Parallel interface mode, iChip connects to a host CPU through a parallel interface using a PAL (i.e., Altera "EPM7032AEC44"). The host parallel BUS may be an 80x86 (Intel) or a 68K (Motorola) BUS. With some small changes to the PAL, the user may customize an interface to any other BUS architecture. iChip is connected to the interface PAL through the following signals:

- **PCS**: Parallel chip select signal. When PCS is high, the PAL is selected.
- **-RD**: When –RD is LOW, iChip reads data from PAL.
- **-WR**: When –WR is LOW, iChip writes data to PAL.
- **D0-D7**: Bi-directional data BUS.
- **-PRES**: Parallel reset. When LOW, generates a reset signal to the parallel interface.
- **-PERR**: Parallel error. When LOW, indicates a parallel interface error.
- **POBE**: Parallel Output Buffer Empty. When HIGH, indicates that the output buffer is empty and iChip may send additional data to host. When iChip sends a data byte, this signal goes LOW until the host reads the data.
- **PIBF**: Parallel Input Buffer Full. When HIGH, indicates that the input buffer is full and iChip may read a data byte from the host. When iChip reads the data byte, this signal goes LOW.

Notes: 1: When hardware flow control is enabled, the iChip transmitter will add an additional stop bit.
2: Parallel interface mode will be available only from iChip firmware version 801

4.2.1 80x86 BUS

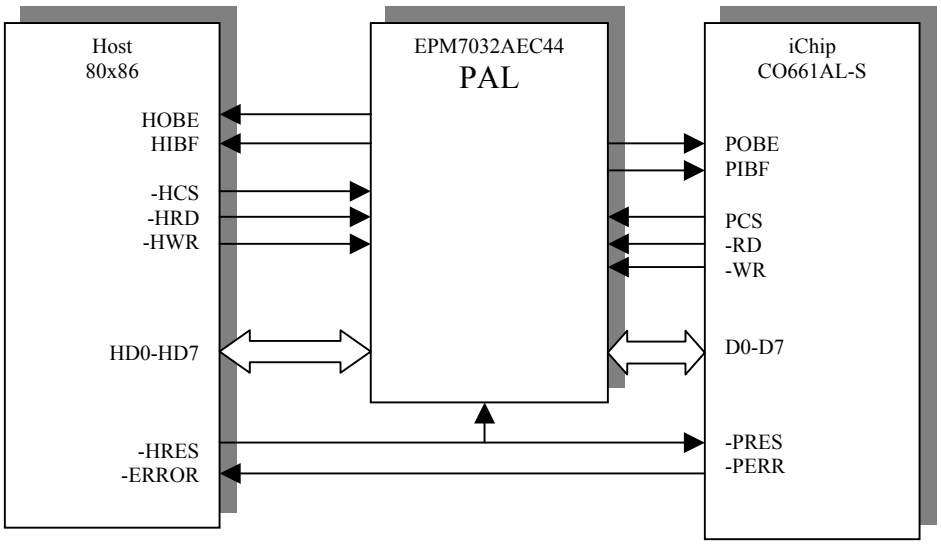


Figure 4-1 Interface to an 80x86 Type BUS

This BUS type includes the following signals:

- **-HCS**: Host Chip-Select signal. When -HCS is LOW, the PAL is selected.
- **-HRD**: Host Read Data. When –HRD is LOW, a data byte is read from the PAL.
- **-HWR**: Host Write Data. When –HWR is LOW, a data byte is written to the PAL.
- **HD0 – HD7**:
  Bi-directional Host data BUS.
- **-HRES**: Parallel reset. A LOW generates a reset signal to the parallel interface. This pin may be connected to an 80x86 output port.
- **-HERR**: Parallel error. A LOW indicates a parallel interface error. This pin may be connected to an input port on the 80x86.
- **HOBE**[1]: Host Output Buffer Empty. When HIGH, indicates that the output buffer is empty and the host may send a data byte to iChip. When the Host sends a data byte, this signal goes LOW until iChip reads the data. This signal may be connected to an interrupt or I/O pin on the 80x86.
- **HIBF**[1]: Host Input Buffer Full. When HIGH, indicates that the input buffer is full and the host may read a data byte from iChip. When the host reads the data, this signal goes LOW. This pin may be connected to an interrupt or I/O pin on the 80x86.

Note 1: HOBE and HIBF complement PIBF and POBE respectively.

4.2.2 MC68xxx BUS

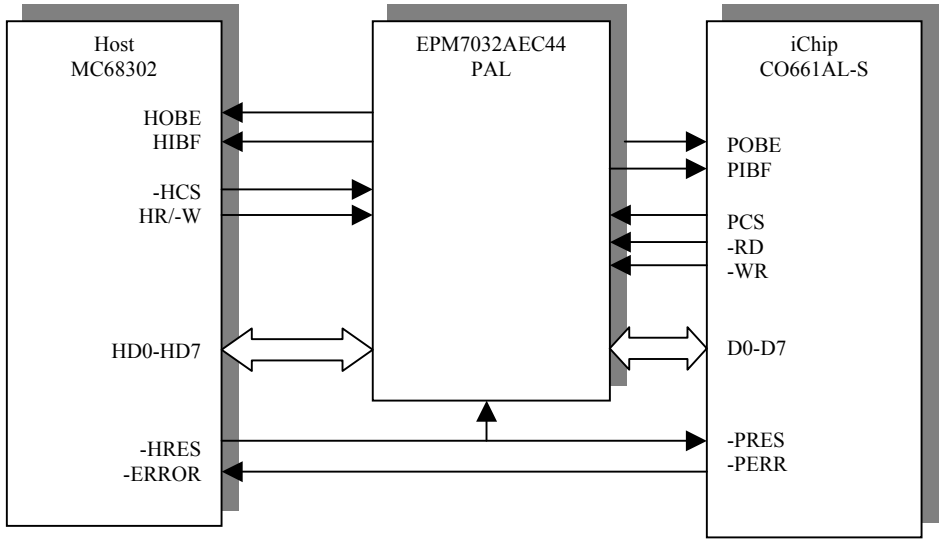


Figure 4-2 Interface to an MC68xxx Type BUS

This BUS type includes the following signals:

- **-HCS**: Host Chip-Select signal. When -HCS is LOW, PAL is selected.
- **-HR/-W**:Host read/write data from/to iChip. When HR/-W is LOW, it indicates a write cycle; otherwise it is a read cycle.
- **HD0 – HD7**:
  Bi-directional Host data BUS.
- **-HRES**: Parallel reset. A LOW generates a reset signal to the parallel interface. This pin may be connected to an MC68xxx output port.
- **-HERR**: Parallel error. A LOW indicates a parallel interface error. This pin may be connected to an input port on the 80x86.
- **HOBE**[1]:Host Output Buffer Empty. When HIGH, indicates that the output buffer is empty and the host may send a data byte to iChip. When the Host sends a data byte, this signal goes LOW until iChip reads the data. This signal may be connected to an interrupt or I/O pin on the MC68xxx.
- **HIBF**[1]: Host Input Buffer Full. When HIGH, indicates that the input buffer is full and the host may read a data byte from iChip. When the host reads the data, this signal goes low. This pin may be connected to an interrupt or I/O pin on the MC68xxx.

Note 1: HOBE and HIBF complement PIBF and POBE respectively.

4.3 Serial Modem Interface

iChip CO661AL-S includes a dedicated port to interface a serial modem. The modem interface is a serial DCE interface. Speeds of 2400, 4800, 9600, 19200, 38400, 57600, 115200 and 230400 bps are supported in the following data format:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Transmission Length (No. of Bits)
None	8	1	10

Table 4-2 Host Data Format

Actual baud rate may be preprogrammed or dynamically defined as equal to the auto baud rate detected on the serial host interface (when CO661AL-S operates in Serial mode). When the CO661AL-S operates in Parallel mode, the modem interface baud rate must be preprogrammed.

All serial modem input signals (RXDM, -DSRM, -CTSM, -CDM) are 5V tolerant.

iChip does not provide a Ring Indicator input signal.

5 Pin Descriptions

5.1 iChip CO661AL-S Pin Assignments

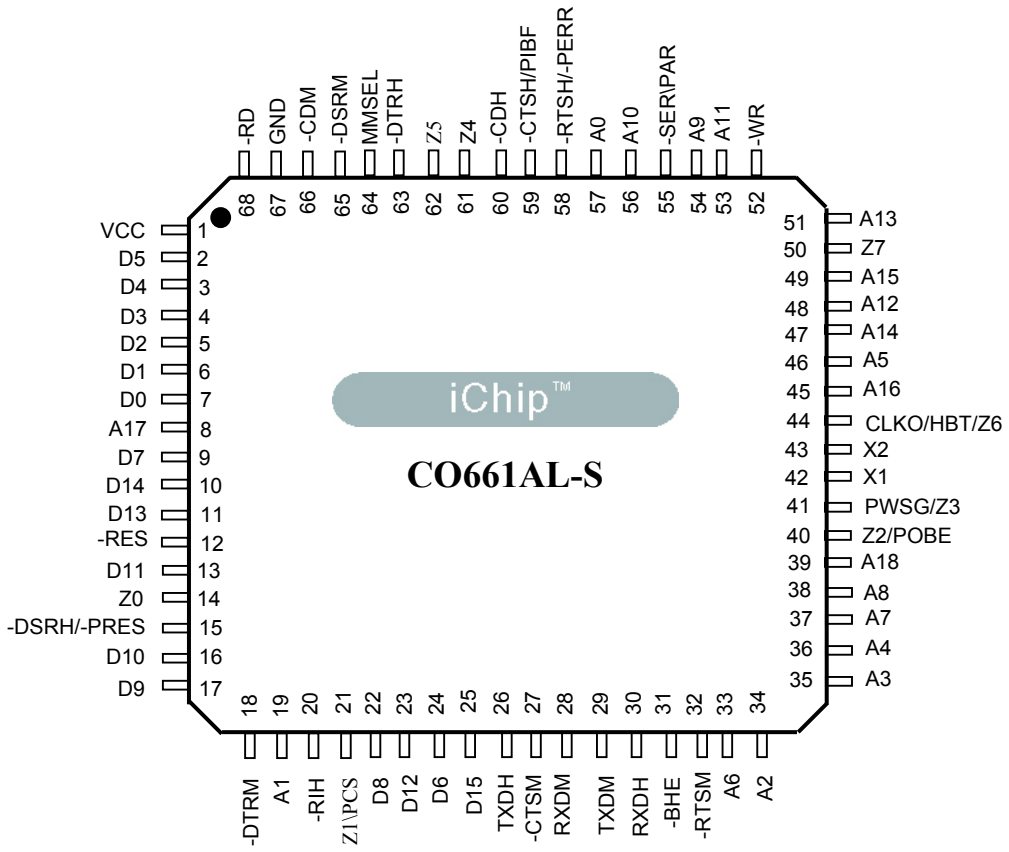


Figure 5-1 PLCC68 Package for iChip CO661AL-S

5.2 iChip Pin Functional Descriptions

5.2.1 Local BUS Signals[1]

<table>
<tr><th>Signal</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>A[18:0]</td><td>O</td><td>39, 8, 45, 49, 47, 51, 48, 53, 56, 54, 38, 37, 33, 46, 36, 35, 34, 19, 57</td><td>Address BUS: These pins supply addresses to the system.
These pins should be left Not Connected.</td></tr>
<tr><td>D[15:0]</td><td>O/I</td><td>25, 10, 11, 23, 13, 16, 17, 22, 9, 24, 2, 3, 4, 5, 6, 7</td><td>Data BUS: These pins supply data to/from the system.
These pins should be left Not Connected.</td></tr>
<tr><td>-BHE</td><td>O</td><td>31</td><td>BUS HIGH Enable: This pin and the least-significant address bit (A0) indicate to the system which bytes of the data BUS (upper, lower, or both) participate in a BUS cycle. The -BHE and A0 pins are encoded as shown in the table below.
<table>
<tr><th>-BHE</th><th>AD0</th><th>Type of BUS cycle</th></tr>
<tr><td>0</td><td>0</td><td>Word Transfer</td></tr>
<tr><td>1</td><td>0</td><td>Even Byte Transfer</td></tr>
<tr><td>0</td><td>1</td><td>Odd Byte Transfer</td></tr>
<tr><td>1</td><td>1</td><td>N/A</td></tr>
</table>
This pin should be left Not Connected.</td></tr>
</table>

Note: 1: Currently the local BUS is not in use in the CO661AL-S.

Signal	Type	Pin No.	Description
-RD	O	68	READ: This pin indicates that iChip is performing a read cycle. This pin should be left Not Connected.
-WR	O	52	WRITE: This pin indicates that iChip is performing a write cycle. This pin should be left Not Connected.

5.2.2 Miscellaneous Signals

Signal	Type	Pin No.	Description
MMSEL	I	64	Modem Mode Select: • When this pin is held LOW during power up for at least 5 seconds, iChip will automatically enter firmware update mode. • During a firmware update procedure, when an external modem dials to the iChip, pulling this pin down to LOW will cause the iChip to immediately answer the call and begin the update session. • When this pin is held LOW during power up for less than 5 seconds, it forces iChip into auto baud rate detection.
-RES	I	12	RESET: When -RES is LOW, iChip immediately terminates its present activity and clears its internal logic. -RES must be held LOW for at least 1 mSec after power achieves 90% VCC. This input is provided with a Schmidt trigger to facilitate power-on reset generation via an RC network (see Fig. 7-4).
X1	I	42	Crystal Input: This pin and the X2 pin provide connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit. To provide iChip with an external clock source, connect the source to the X1 pin and leave the X2 pin unconnected.
X2	O	43	Crystal Output: This pin and the X1 pin provide connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit.

Signal	Type	Pin No.	Description
CLKO/HBT/Z6	O	44	**AT+i Configurable Pin:** **CLKO** (default): Clock Output. This pin provides a clock-out to the system at the same frequency as X1. During reset the clock out is disabled. **HBT**: Heart Beat. Provides a 50% duty cycle, 40 mSec frequency square wave, when iChip F/W is properly running. (Available from iChip Firmware ver. 7.04). In the future it may be changed to a GPIO. This pin is configurable with the AT+iPN44 command (see AT+i Programmers Manual).
-SER/PAR	I	55	Serial/Parallel mode select. This pin is sampled on the rising edge of the –RES signal. If it is LOW, iChip functions in Serial mode. Otherwise, it functions in Parallel mode.
Z0	I/O	14	Reserved as a GPIO for future use. This pin should be Not Connected.
Z1/PCS	I/O	21	**In Serial mode**, Z1 is available as a GPIO for future use and should be left Not Connected. **In Parallel mode**, PCS is used as a chip-select for the parallel interface PAL.
Z2/POBE	I/O	40	**In Serial mode**, Z2 is available as a GPIO for future use and should be left Not Connected. **In Parallel mode**, POBE is used as the Parallel Output Buffer Empty signal. When HIGH, iChip may send a parallel data byte to the host.
PWSG/Z3	I/O	41	**AT+i Configurable Pin:** **PWSG** (default): Power-Save Gate. This pin is used to disable the iChip's oscillator (X1 Pin 42) via an external gate in order to achieve full sleep mode with minimal power consumption (see Fig. 7-6). **Z3:** General Purpose I/O.
Z4	I/O	61	Reserved as a GPIO for future use. This pin should be Not Connected.
Z5	I/O	62	Reserved as a GPIO for future use. This pin should be Not Connected.
Z7	I/O	50	Reserved as a GPIO for future use. This pin should be Not Connected.
GND	P	67	Ground: iChip Ground signal.
VCC	P	1	Power Supply: This pin supplies power (+3.3V) to iChip.

5.2.3 Host Serial Interface Signals

Signal	Type	Pin No.	Description
TXDH	O	26	Transmit Data Host: This pin supplies asynchronous serial transmit data to the host. In Parallel mode, this pin is used for firmware update.
RXDH	I	30	Receive Data Host: This pin supplies asynchronous serial receive data from the host. In Parallel mode, this pin is used for firmware update. When not used, this pin should be connected to VCC.
-CTSH /PIBF	I	59	**In Serial mode:** Clear-to-Send Host: -CTSH is active only when host hardware flow control is enabled. When -CTSH is LOW, flow control is enabled for the host serial port, i.e., iChip may transmit to the host. When -CTSH is HIGH, the iChip transmitter holds its data in the serial port transmit register. -CTSH is sampled only at the beginning of a frame transmission. If -CTSH is raised while a character frame is being transmitted, that frame will be completed. Connect -CTSH to -RTSH when not in use. **In Parallel mode:** Parallel Input Buffer Full, when HIGH, indicates that the host has sent a data byte, which has not yet been read.
-RTSH/-PERR	O	58	**In Serial mode:** Ready-to-Send Host: -RTSH is active only when host hardware flow control is enabled. When -RTSH is LOW, flow control is enabled for the host serial port, i.e., the host may transmit to iChip. When -RTSH is HIGH, iChip indicates that its receiver is busy and cannot receive data from host. Connect -RTSH to -CTSH when not in use. **In Parallel mode:** Parallel Error, when LOW, indicates to the host that an error has occurred in the parallel interface circuit.

Signal	Type	Pin No.	Description
-DSRH/-PRES	I	15	**In Serial mode:** Data Set Ready Host: When -DSRH is LOW, it indicates that the host is attached and ready to communicate with iChip. Connect -DSRH to GND when not in use. **In Parallel mode:** Parallel Reset, when LOW, generates a reset to the parallel interface.
-DTRH	O	63	Data Terminal Ready Host: When -DTRH is LOW, it indicates to the host that iChip is attached and ready to communicate.
-CDH	O	60	Carrier Detect Host: This pin indicates to the host that the modem communication device detects a carrier signal. During firmware update, -CDH and -RIH are used to display the firmware update status.
-RIH	O	20	Ring Indicator Host: This pin indicates to the host that the modem communication device detects a Ring signal. During firmware update, -CDH and -RIH are used to display the firmware update status.

5.2.4 iChip Serial Modem Signals

Signal	Type	Pin No.	Description
TXDM	O	29	Transmit Data Modem: This pin provides asynchronous serial transmit data to the modem from the serial port. This pin must remain HIGH on reset.
RXDM	I	28	Receive Data Modem: This pin provides asynchronous serial receive data from the modem to the asynchronous modem serial port. When this pin is not used, connect it to VCC.
-CTSM	I	27	Clear-to-Send Modem: -CTSH is active only when modem hardware flow control is enabled. When -CTSM is LOW, flow control is enabled for the modem serial port, i.e., iChip may transmit to the modem. When -CTSM is HIGH, the iChip transmitter holds its data in the serial port transmit register. Connect -CTSM to -RTSM when not in use
-RTSM	O	32	Ready-to-Send Modem: -RTSM is active only when modem hardware flow control is enabled. When -RTSM is LOW, flow control is enabled for the modem serial port, i.e., the modem may transmit to iChip. When -RTSM is HIGH, iChip indicates that its receiver is busy and cannot receive data from modem. Connect -RTSM to -CTSM when not in use.
-DSRM	I	65	Data Set Ready Modem: When -DSRM is LOW, it indicates that the modem is attached and ready to communicate with iChip. Connect -DSRM to GND when not in use.
-DTRM	O	18	Data Terminal Ready Modem: When -DTRM is LOW it indicates to the modem that iChip is attached and ready to communicate.
-CDM	I	66	Carrier Detect Modem: This pin indicates to iChip that the modem detects a carrier signal.

6 Electrical/Mechanical Specifications

6.1 Environmental Specifications

6.1.1 Absolute Maximum Ratings

Parameter	Rating
Voltage at local bus pins with respect to ground	-0.5 to +3.8 Volts
Voltage at all other pins with respect to ground	-0.5 to +5.5 Volts
Operating temperature	0°C to 70°C (32 to 158°F)
Storage temperature	-60°C to 120°C (–76 to 248°F)
Soldering temperature (max. 10 sec.)	220°C (428°F)
Package dissipation	1.5 Watts

Table 6-1 Environmental Specifications – Maximum Ratings

6.1.2 DC Operating Characteristics

Parameter	Min	Typical	Max	Units
DC Supply	3.0	3.3	3.6	Volts
High-level Input	2.0			Volts
Low-level Input			0.8	Volts
High-level Output[1]	2.4			Volts
Low-level Output[2]			0.4	Volts
Input leakage current			4	µA
Power supply current (Operating Mode)[3]		30		mA
Power supply current (Power-save Mode)[3]		10		mA
Power supply current (Sleep Mode)[4]			1	mA
Input capacitance			7	pF

Table 6-2 DC Operating Characteristics

Notes: 1: I_{OH} =2mA
2: I_{OL} = 2mA
3: 18.432 MHz clock
4: Oscillator blocked with external circuit

6.2 Interface Timing and Waveforms

6.2.1 Switching Characteristics

Parameter	Symbol	Min.	Typical	Max.	Units
Clock Out frequency	Fclk	18.43	18.432	18.434	MHz
Clock Out period	Tclk		1/Fck		us
X2 falling to address or chip select change	Txfac	4.2		10	ns
X2 rising to read active	Txrra	4.1		8.6	ns
X2 falling to read inactive	Txfri	4.1		8.6	ns
Data setup before read high	Tdsbrh	9			ns
Data setup after read high	Tdsarh	3			ns
X2 rising to write active	Txrwa	5		8.2	ns
X2 rising to data valid	Txrdv	4.1		8.6	ns
X2 rising to write inactive	Txrwi	5		8.2	ns
Data out valid after write high	Tdovaw	2.1			ns
X2 fall time [1]	Tckhl			5	ns
X2 rise time [2]	Tcklh			5	ns
X2 LOW time	Tclck	24	27	30	ns
X2 HIGH time	Tchck	24	27	30	ns
X2 to CLKO skew	Tcico	4.2		6.6	ns
Reset pulse	Trst	1			ms
TXDM high before raising reset	Trmbr	2			us
TXDM high after raising reset	Trmar	2			us
Read rising to input parallel buffer full	Trrbf	0			ns
Write rising to output parallel buffer empty	Twrbe	0			ns

Table 6-3 Switching Characteristics

[1] Fall time is from 2.3V to 1V.
[2] Rise time is from 1V to 2.3V.

6.2.2 Local BUS Read Cycle

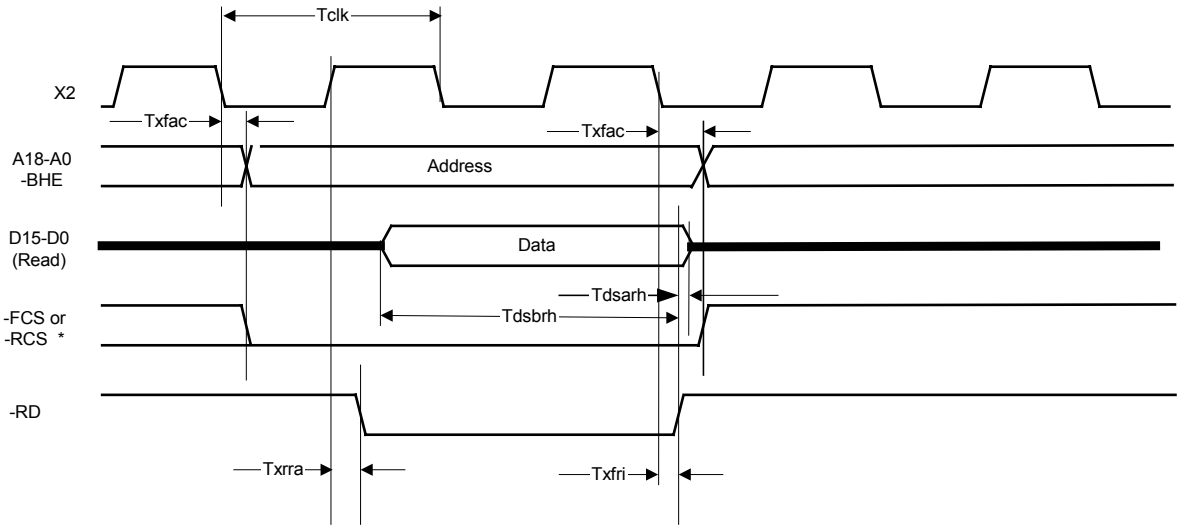


Figure 6-1 Local BUS Read Cycle

* -FCS and –RCS are internal Flash and RAM Chip-select.

6.2.3 Local BUS Write Cycle

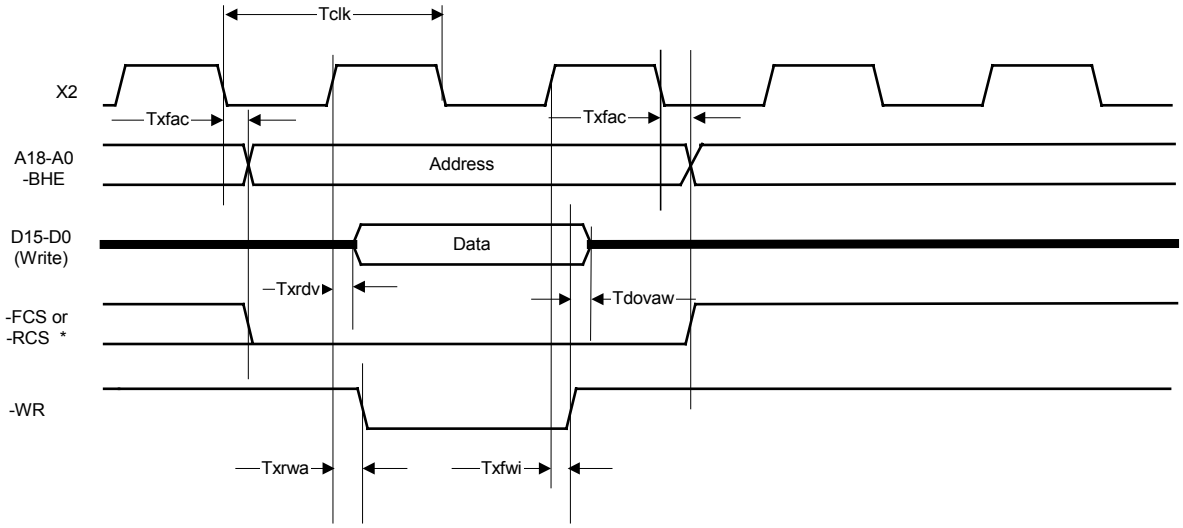


Figure 6-2 Local BUS Write Cycle

* -FCS and –RCS are internal Flash and RAM Chip-select.

6.2.4 Clock Waveform

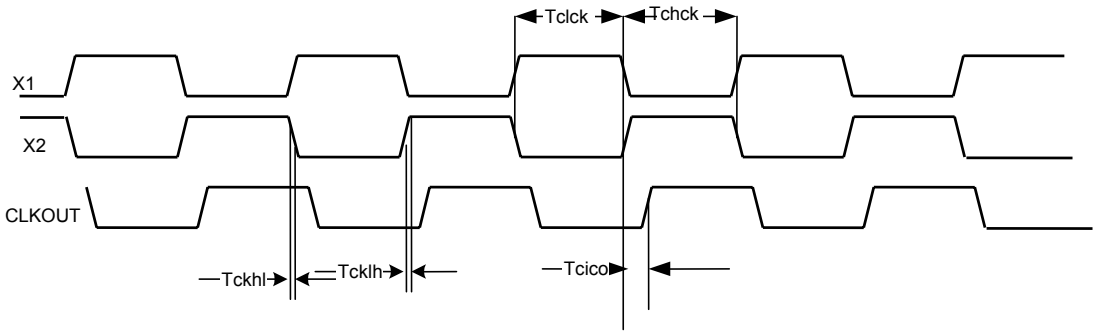


Figure 6-3 Clock Waveform

6.2.5 Reset Timing

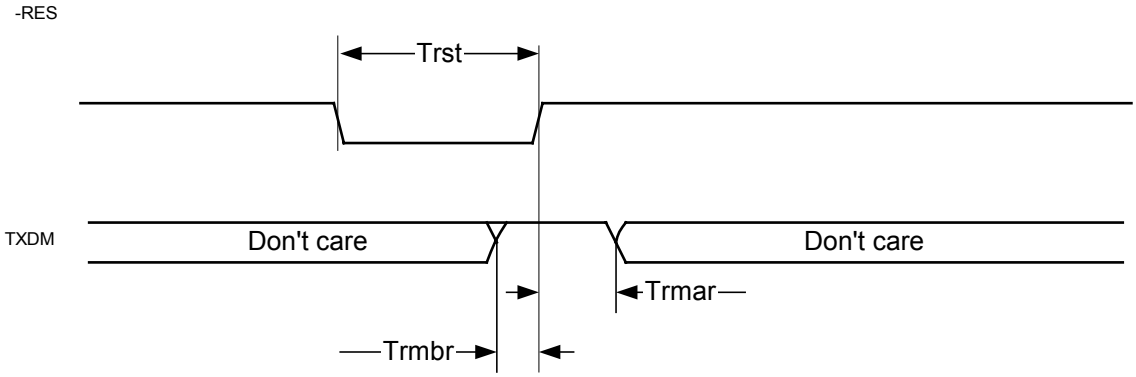


Figure 6-4 Reset Timing

6.2.6 Parallel BUS Read Cycle

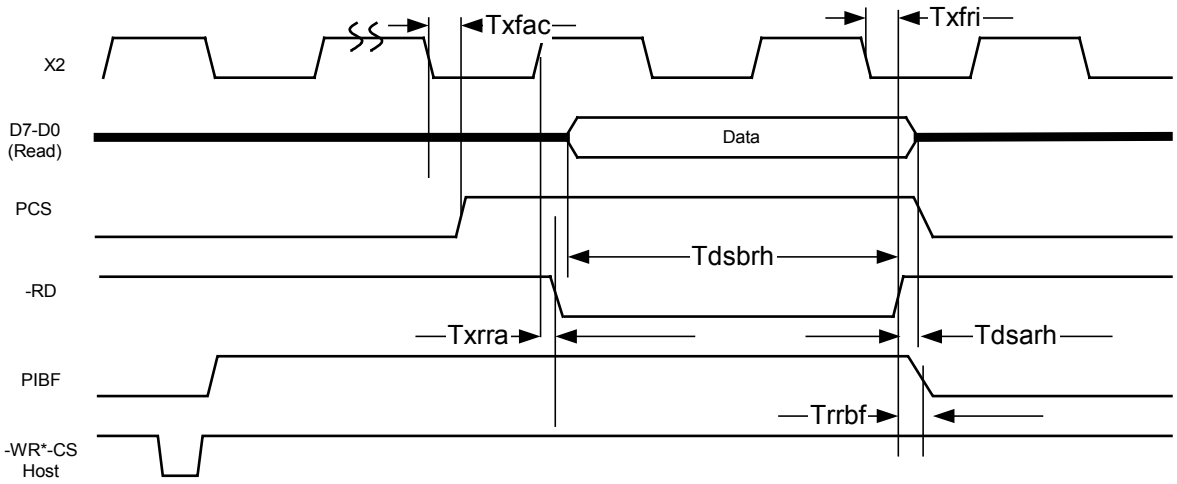


Figure 6-5 Parallel BUS Read Cycle

6.2.7 Parallel BUS Write Cycle

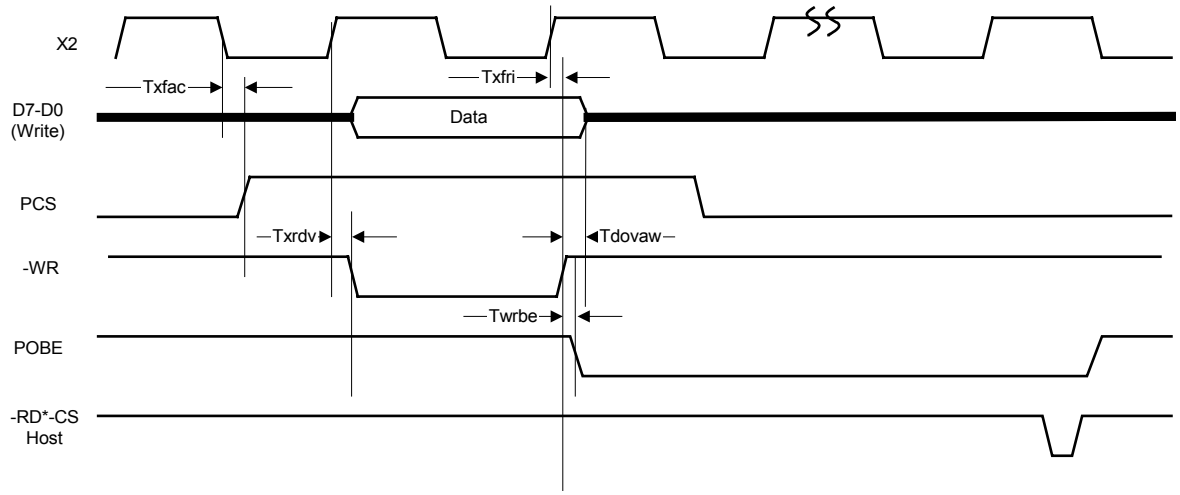


Figure 6-6 Parallel BUS Write Cycle

6.3 Mechanical Dimensions

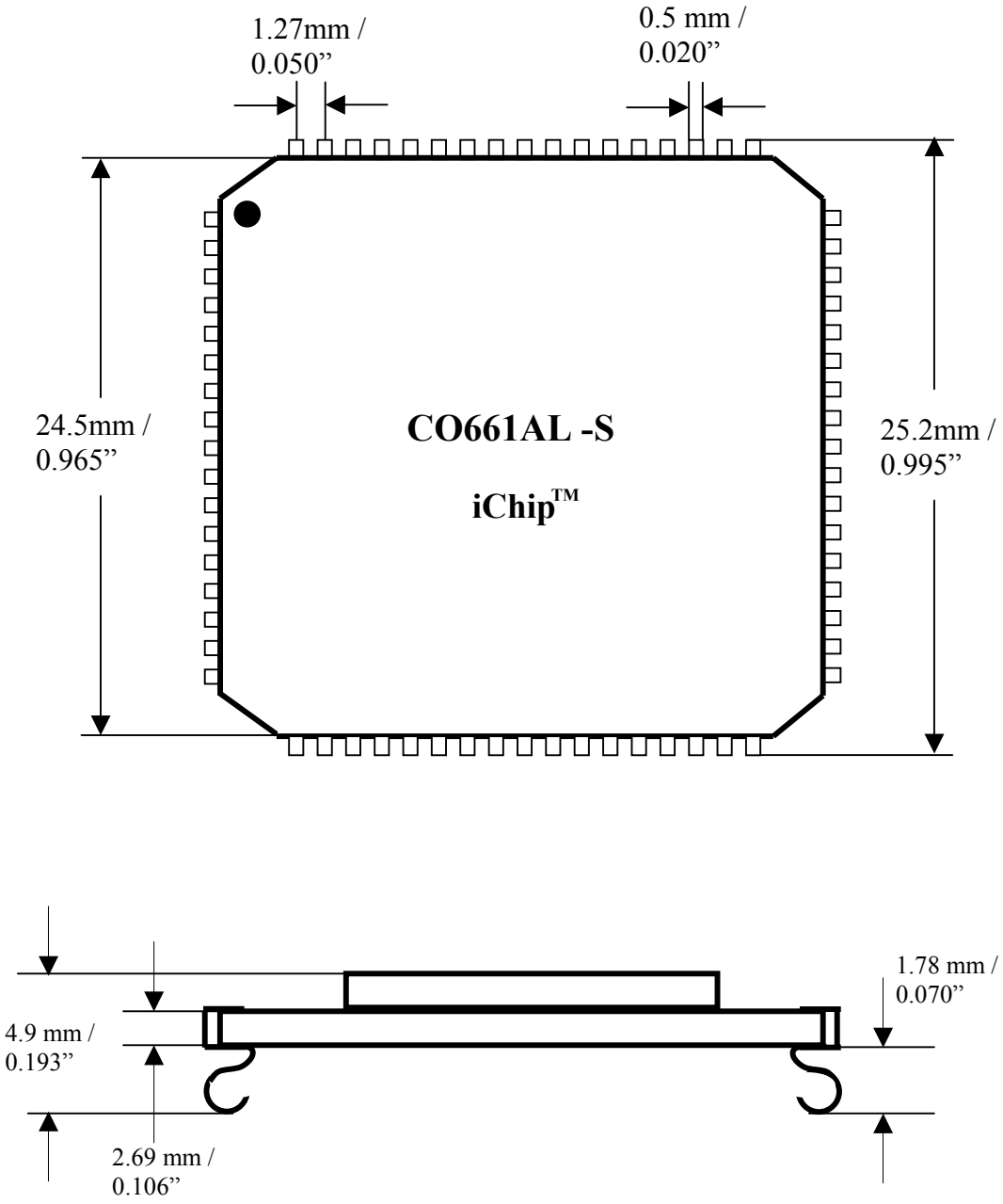


Figure 6-7 Mechanical Dimensions

7 iChip Designs

7.1 Serial Host and Modem Environment

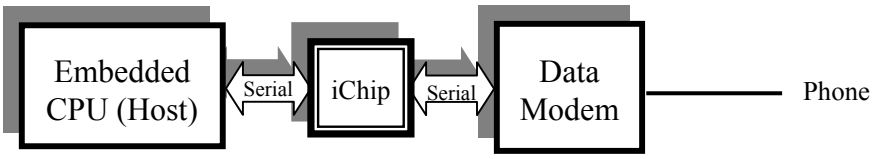


Figure 7-1 Serial Host and Modem Environment

7.2 Parallel Host and Serial Modem Environment

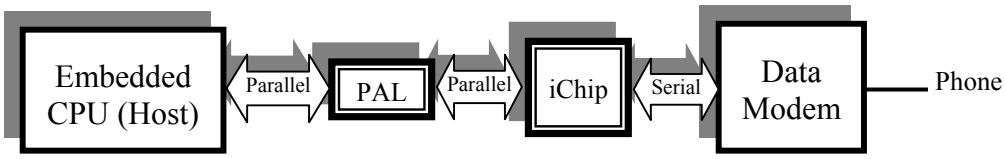


Figure 7-2 Parallel Host and Serial Modem Environment

7.3 Selecting a Crystal

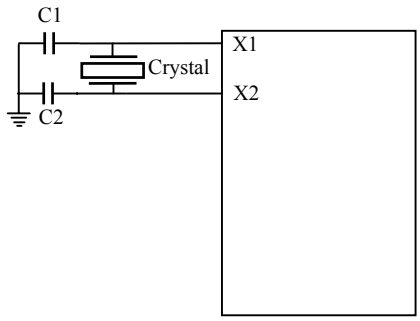


Figure 7-3 Selecting a Crystal

The characteristics of the built-in inverting amplifier set limits on the following parameters for crystals:
Crystal first overtone frequency ..... 18.432 MHz
ESR (Equivalent Series Resistance) ..... 40 Ω max
Drive Level ..... 1 mW max
Frequency tolerance ..... +/- 100ppm
Load capacitance..... 18pF
Shunt capacitance..... 7pF Maximum

The recommended range of values for C 1 and C 2 are as follows:
C 1 ..... 15 pF ± 20%
C 2 ..... 22 pF ± 20%
The specific values for C1 and C2 must be determined by the designer and are dependent on the characteristics of the chosen crystal and board design.

7.4 Selecting the Reset Circuit

7.4.1 RC Network

The Reset signal may be designed with a RC network. τ should be greater than 10 mSec. This is a low-cost solution.

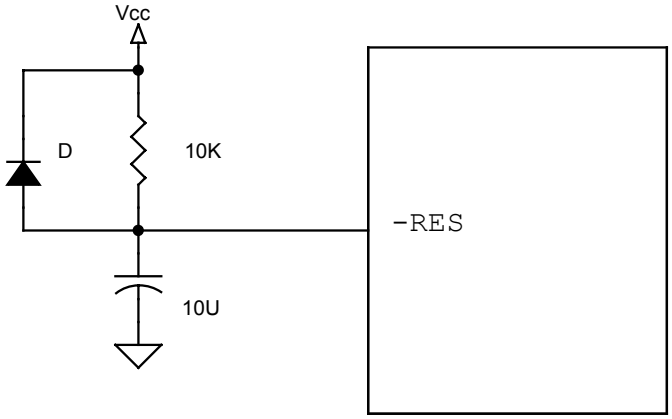


Figure 7-4 RC Reset Circuit

7.4.2 Supervisory Circuit

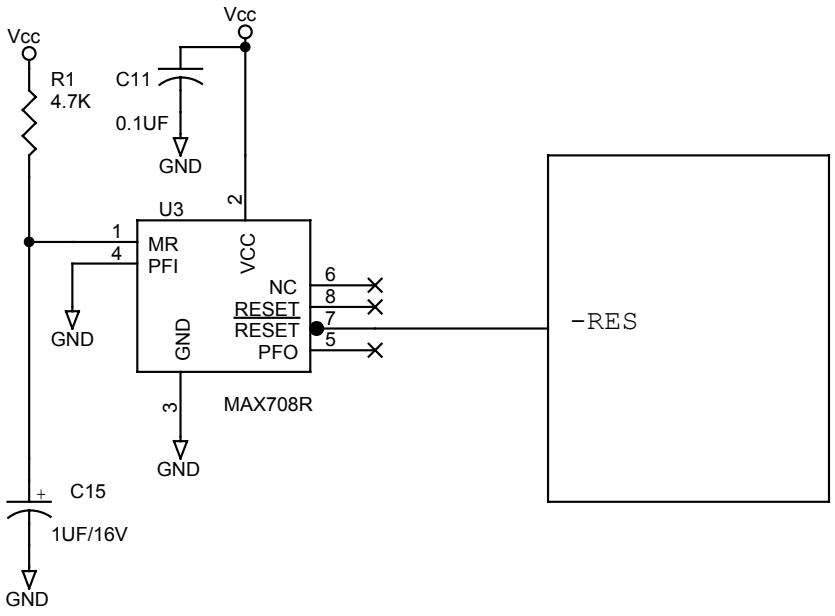


Figure 7-5 Supervisory Reset Circuit

7.5 Sleep Mode [1]

CO661AL-S iChip supports a Sleep mode to achieve maximum power conservation when iChip is not in use. Sleep mode is based on an external circuit that gates the oscillator input to iChip. The PWSG (pin 41) is an output pin used to trigger sleep mode. While in this mode, iChip current consumption is reduced to ~1 mA. The external circuit is designed to wake-up and exit Sleep mode when a transmission arrives from either the host processor or the modem (see Fig. 7-6).

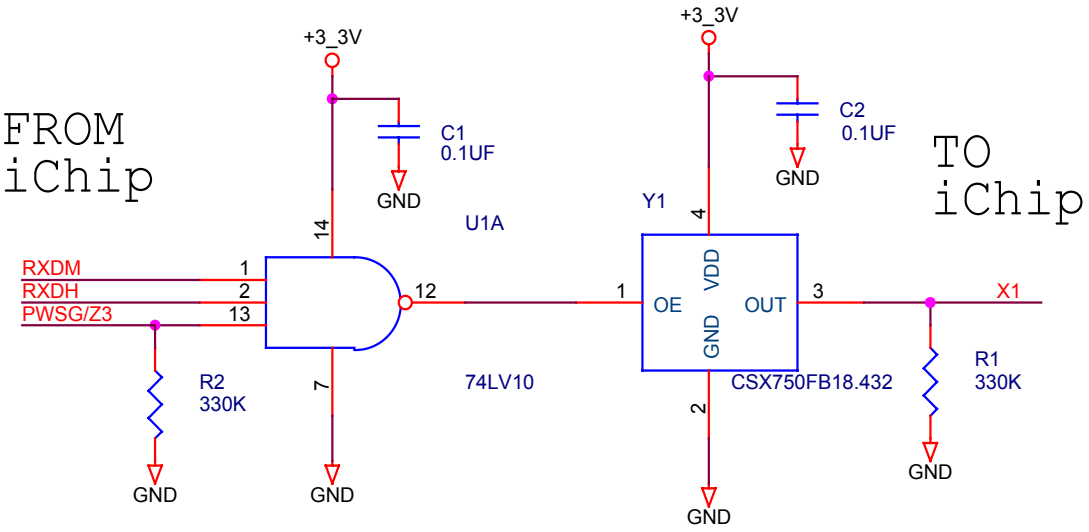


Figure 7-6 CO661AL External Sleep Mode Circuit

Note: 1: Sleep mode will be available only from iChip firmware version 8.01

8 Protocol Compliance

iChip CO661AL-S complies with the following Internet standards:

RFC 768	User Datagram Protocol (UDP)
RFC 791	Internet Protocol (IP)
RFC 792	ICMP – Internet Control Message Protocol
RFC 793	Transmission Control Protocol (TCP)
RFC 821	Simple Mail Transfer Protocol (SMTP)
RFC 822	Standard for the Format of ARPA Internet Text Messages
RFC 959	FTP – File Transfer Protocol
RFC 854	TELNET protocol specification
RFC 857	Telnet ECHO option
RFC 858	Telnet suppress go-ahead option
RFC 1034	DOMAIN NAMES (DNS) - Concepts and Facilities
RFC 1035	DOMAIN NAMES (DNS) - Implementation and Specification
RFC 1091	Telnet terminal type option
RFC 1073	Telnet window size option
RFC 1321	MD5 Message Digest Algorithm
RFC 1331	Point-to-Point Protocol (PPP)
RFC 1332	PPP Internet Protocol Control Protocol (IPCP)
RFC 1334	PPP Authentication Protocols (PAP)
RFC 1570	PPP LCP Extensions
RFC 1661	Point-to-Point Protocol (PPP)
RFC 1877	PPP IPCP Extensions for Name Server Addresses
RFC 1939	Post Office Protocol - Version 3 (POP3)
RFC 1957	Some Observations on the Implementations of the Post Office Protocol (POP3)
RFC 1994	PPP Challenge Handshake Authentication Protocol (CHAP)
RFC 2045	Multipurpose Internet Mail Extensions (MIME) Part One: Format of Internet Message Bodies
RFC 2046	Multipurpose Internet Mail Extensions (MIME) Part Two: Media Types
RFC 2047	MIME (Multipurpose Internet Mail Extensions) Part Three: Message Header Extensions for Non-ASCII Text
RFC 2048	Multipurpose Internet Mail Extensions (MIME) Part Four: Registration Procedures
RFC 2049	Multipurpose Internet Mail Extensions (MIME) Part Five: Conformance Criteria and Examples
RFC 2068	HyperText Transfer Protocol HTTP/1.1

Table 8-1 Internet Protocol Compliance

9 List of Terms and Acronyms

AT+i™	**Connect One's** Internet extension to the industry-standard Hayes AT command set. Supports simplified Internet connectivity commands in the spirit of the AT syntax.
Base64	**Encoding scheme**, which converts arbitrary binary data into a 64-character subset of US ASCII. The encoded data is 33% larger than the original data.
CHAP	**Challenge Authentication Protocol.** Extends the PAP procedure by introducing advanced elements of security.
DNS	**Domain Name System**. Defines the structure of Internet names and their association with IP addresses.
iChip™	**Connect One's Internet Controller for embedded Internet connectivity.**
ICMP	**Internet Control Message Protocol**. Network layer Internet protocol that reports errors and provides other information relevant to IP packet processing.
IP	**Internet Protocol**. Provides for transmitting blocks of data, called datagrams, from sources to destinations, which are hosts identified by fixed length addresses. Also provides for fragmentation and reassemble of long datagrams, if necessary.
IPCP	**Internet Protocol Control Protocol**. Establishes and configures the Internet Protocol over PPP. Also negotiates Van Jacobson TCP/IP header compression with PPP.
ISP	**Internet Service Provider**. Commercial company that provides Internet access to end (mostly PC) users through a dial-up connection.
LCP	**Link Control Protocol**. Negotiates data link characteristics and tests the integrity of the link.
"Leave on Server"	**An option** designating whether retrieved Email messages are to be left intact on the server for subsequent downloads or are to be deleted from the server after a successful download.
MIME	**Multipurpose Internet Mail Extensions**. Extends the format of mail message bodies to allow multi-part textual and non-textual data to be represented and exchanged between Internet mail servers.
PAP	**Password Authentication Protocol**. Used optionally by the PPP protocol to identify the user to the ISP.
ping	ICMP protocol **ECHO message** and its reply. Often used to debug IP networks and to test the accessibility of a network device.
POP3	**Post Office Protocol Version 3**. Allows a workstation/PC to dynamically retrieve mail from a mailbox kept on a remote server.
PPP	**Point-to-Point Protocol**. Communications protocol used to send data across serial communication links, such as modems.
RFC	**Request For Comments**. Collections of standards that define the way remote computers communicate over the Internet.
SMTP	**Simple Mail Transfer Protocol**. Provides for transferring mail reliably and efficiently over the Internet.

TCP	**Transmission Control Protocol**. Provides reliable stream-oriented connections over the Internet. Works in conjunction with its underlying IP protocol.
Telnet	**Network Terminal Protocol.** Provides remote terminal connectivity, which allows to execute tasks on a remote application server.

Table 9-1 Terms and Acronyms