iChip LAN™

iChip LAN CO561AD-L

Datasheet

Ver. 1.04

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Version	**Date**	**Description**
1.0	November 2002	Changed data sheet format of publication 11-3100-07. Separated CO561AD-S and CO561AD-L data sheets. Updated pin descriptions. Deleted pin LANDRQ.
1.04	January 2003	Internal Editing

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1 Introduction

Description

The CO561AD-L iChip LAN™ Internet Controller™ is part of a family of intelligent peripheral devices that provides Internet connectivity solutions to a myriad of embedded devices. iChip LAN, CO561AD-L, is used for 10BaseT Ethernet LAN Internet connectivity.

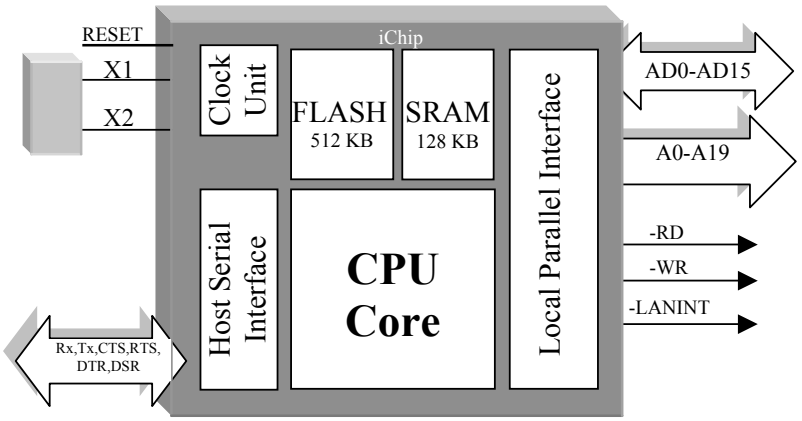
As an embedded, self-contained Internet engine, iChip LAN acts as mediator device between a host processor and an Internet communications platform. By completely offloading Internet connectivity and standard protocols, it relieves the host from the burden of handling Internet communications. From the perspective of a host device, the complexity of establishing and maintaining Internet-related sessions is reduced to simple, straightforward commands that are entirely dealt with within iChip LAN's domain.

A serial channel interfaces iChip LAN to a device's host processor via an on-chip UART. iChip LAN supports 10BaseT Ethernet LANs with the addition of an external 16-bit Cirrus Logic Crystal LAN CS8900A Ethernet controller or Realtek RTL8019AS Ethernet controller.

Through its host Application Programming Interface (API), iChip LAN accepts commands formatted in Connect One's AT+i™ extension to the industry-standard Hayes AT command set. iChip LAN supports several levels of status reporting to the host. Commands are available to store and manipulate functional and Internet-related non-volatile parameter data; utilize TCP and UDP sockets; transmit and receive textual Email messages; transmit and receive binary (MIME encoded) Email messages; fetch HTML web pages; manipulate files and directories via FTP; maintain Telnet sessions and download parameter and firmware updates for the host device or iChip LAN itself. iChip LAN includes a Web server engine that hosts an internal configuration Web site as well as a customizable application Web site. iChip LAN also includes a WAP server to host a WAP site.

In addition, iChip LAN includes a communication mode known as SerialNET mode, which eliminates the need to program the host CPU with AT+i commands. SerialNET allows direct host-to-Internet connectivity without requiring any reprogramming of the host application.

Functional Block Diagram



Pin Diagram

PLCC68

Figure 1-1 iChip LAN Functional Block Diagram

General Features

- Microprocessor-controllable through a standard serial connection.
- Supports remote firmware update by host, Email or Web.
- Includes onboard 128KB SRAM and 512KB flash memory.
- Driven by Connect One's AT+i extension to the AT command set.
- Stand-alone Internet communication capabilities.
- Binary Base64 encoding and MIME.
- Opens up to 10 simultaneous TCP or UDP sockets and up to 2 Listen (server) sockets.
- 3.3 and 5V versions available, CMOS technology.
- Onboard non-volatile memory stores all functional and Internet-related parameters.
- Supports several layers of status reports.
- Internal self-test procedures.
- Auto baud rate detection.
- Includes hardware and software flow control.
- PLCC68 package.

General Protocols

- Supports following Internet Protocols:
- IP, TCP, UDP, DNS, SMTP, POP3, MIME, HTTP, FTP, WAP, and Telnet.
- Includes Web server and WAP server

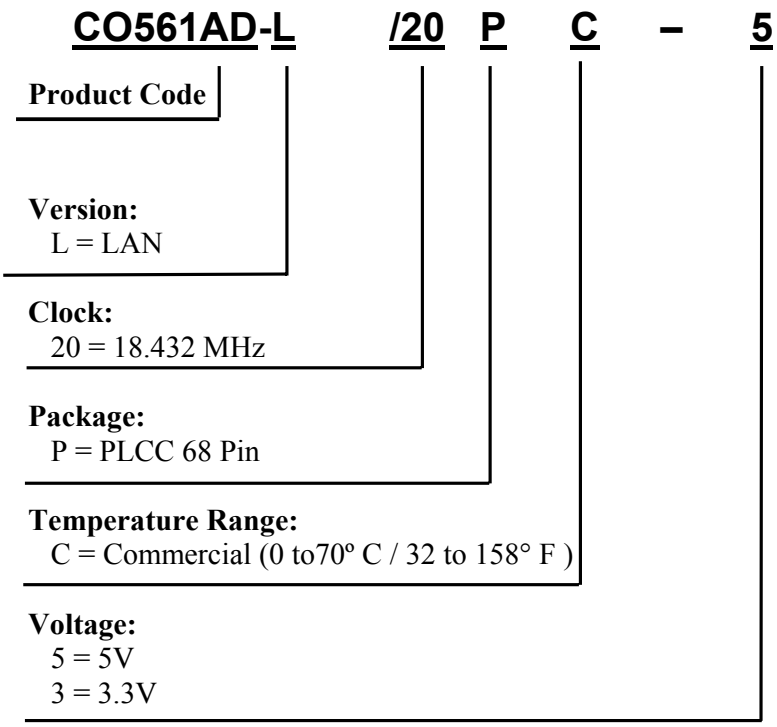
LAN Features

- Supports LAN Internet Protocols: ARP, ICMP, and DHCP.
- Provides 10BaseT Ethernet LAN connectivity via Crystal LAN CS8900A and Realtek RTL8019AS Ethernet controller.
- Supports up to 115 Kbps maximum throughput.
- Serial to Ethernet routing (SerialNET mode).

2 Ordering Information

2.1 iChip LAN Order Number

Connect One's iChip LAN devices are available in two operating voltages. The order number is formed by a combination of the elements below:



3 Functional Description

3.1 Overview

Connect One's iChip LAN Internet Controller is an integrated, firmware-driven, self-contained Internet engine that is available in a 68-pin PLCC package. iChip LAN accepts simple ASCII commands from a host CPU via a serial communication channel and manages an Internet communication session through an Ethernet LAN connection.

For 10BaseT Ethernet applications, iChip LAN CO561AD-L includes the firmware and pin-out necessary to drive external Crystal LAN CS8900A (3.3-volt or 5-volt) or Realtek RTL8019AS (5-volt) 10BaseT Ethernet controllers. iChip LAN supports commands to communicate via TCP and UDP sockets; to send and receive Email, Web and WAP pages/files, utilize FTP and Telnet; or to serve as a serial-to-Internet router.

iChip LAN CO561AD-L contains non-volatile flash memory to store its firmware and Internet-related configuration parameters. Remote firmware and parameter updates are supported through the local host link, by Email or by using a Web browser.

3.2 Technical Specifications

3.2.1 General

iChip LAN constitutes a complete Internet messaging solution for non-PC embedded devices. It acts as a mediator device to completely offload the host processor of Internet-related software and activities. An industry-standard asynchronous serial link connects iChip LAN to the host processor. Programming, monitoring and control are fully supported using Connect One's AT+i extension to the standard AT command set.

3.2.2 Data Rates

CO561AD-L supports standard baud rate configurations from 2,400 bps up to 115,200 bps on the host asynchronous serial communications channel. The default baud rate may be changed permanently by using the AT+iBDRF command. Auto baud rate setting is supported for all baud rates.

3.2.3 Operation

All iChip LAN Internet and parameter operations are controlled by AT+i commands.

3.2.3.1 Command Mode

iChip LAN commands are implemented using the AT+i command set. Command flow exists only on the host serial channel between the host and iChip LAN.

3.2.3.2 Internet Mode

iChip LAN enters Internet mode after being issued an Internet command such as to send or receive an Email message, open a socket, etc. While in this mode, AT+i commands are supported to monitor and control the process when needed.

3.2.3.3 SerialNET Mode

iChip LAN SerialNET mode extends a local asynchronous serial link to a TCP or UDP socket across a LAN or Internet. Its main purpose is to allow simple devices, which normally interact over a serial line, to interact in a similar fashion across a network, without requiring any changes in the device itself. iChip LAN contains a set of associated operational parameters, which define the nature of the desired network connection. iChip LAN supports both Server and Client modes in SerialNET mode. AT+i commands are not required to operate SerialNET mode. Thus, SerialNET mode may be used in existing systems with little or no need to modify the application program.

3.2.4 Remote Internet Firmware Update

New firmware may be uploaded from a remote location using standard Internet protocols. iChip LAN accepts Emails with new firmware attachments, as well as firmware uploads from a remote browser through iChip LAN's Web server.

3.2.5 Host Serial Connection

iChip LAN supports a full-duplex, TTL-level serial communications link with the host processor. Full EIA-232-D hardware flow control, including Tx, Rx, CTS, RTS, DTR, and DSR lines, is supported.

3.2.6 Hardware and Software Flow Control

Hardware flow control is supported between the host CPU and iChip LAN. Flow control is programmed via the AT+iFLW command. The default flow control methods are set to "Wait/Continue" software flow control between iChip LAN and the host (this method is similar to XON/XOFF software flow control).

The hardware flow control method frees the host CPU from monitoring and handling the software flow control. The host can program iChip LAN to either use hardware flow control or to use "Wait/Continue" software flow control between iChip LAN and the host CPU. Hardware flow control mechanism is based on the RTS/CTS signals.

4 Hardware Interface

4.1 Host Interface

The host interface is a serial DTE interface. Speeds of 2400, 4800, 9600, 19200, 38400, 57600 and 115200 bps are supported in the following data format:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Transmission Length (No. of Bits)
None	8	1 [1]	10

Table 4-1 Host Data Format

Note:[1] When hardware flow control is enabled the iChip transmitter will add an additional stop bit.

4.2 LAN Interface

iChip LAN directly interfaces an Ethernet LAN MAC/PHY device on its 16-bit local BUS. Currently iChip LAN supports the Crystal LAN CS8900A and Realtek RTL8019AS Ethernet controllers.

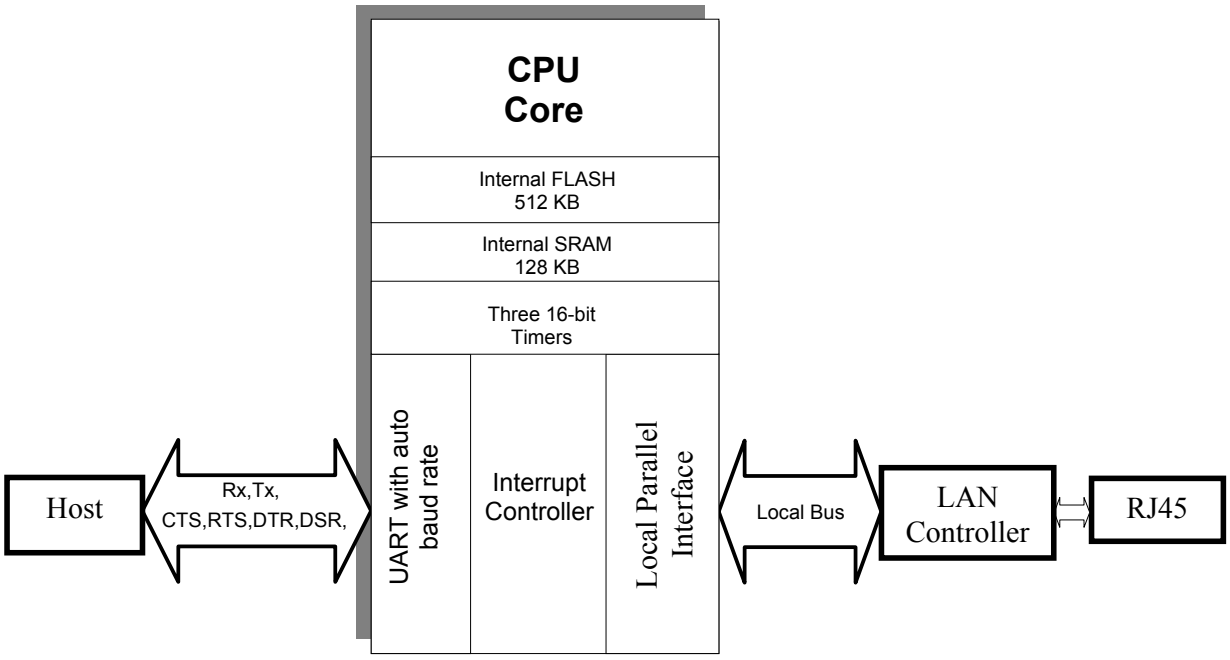


Figure 4-1 iChip LAN CO561AD-L with LAN Interface

5 Pin Descriptions

5.1 iChip LAN CO561AD-L Pin Assignments

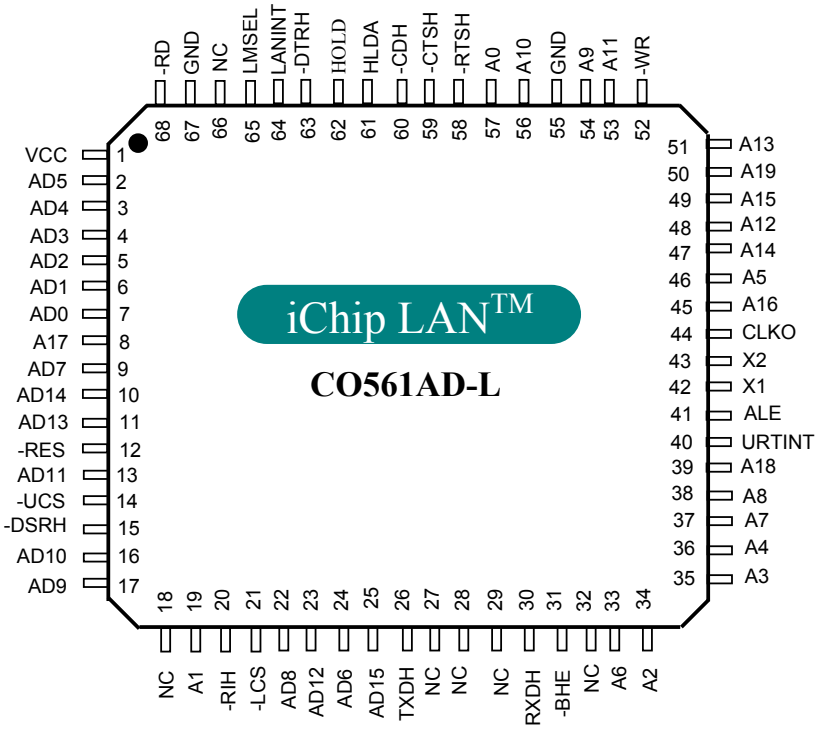


Figure 5-1 PLCC68 Package for iChip LAN CO561AD-L Serial Version

5.2 iChip LAN Pin Functional Descriptions

5.2.1 Local BUS Signals

Signal	Type	Pin No.	Description
A[19:0]	O	50, 39, 8, 45, 49, 47, 51, 48, 53, 56, 54, 38, 37, 33, 46, 36, 35, 34, 19, 57	Address BUS: These pins supply addresses to the system one-half of a CLKO period earlier than the multiplexed address and data BUS AD15–AD0. During a BUS hold or reset condition, the address BUS is in a HIGH-impedance state. These pins should be Connected to the address bus of the LAN controller.
AD[15:0]	O/I	25, 10, 11, 23, 13, 16, 17, 22, 9, 24, 2, 3, 4, 5, 6, 7	Address and Data BUS: These time-multiplexed pins supply addresses and data to the system. This BUS will supply an address to the system during the first period of a BUS cycle. They supply data to the system during the remaining periods of that cycle. During a BUS hold or reset condition, the address BUS is in a HIGH-impedance state. These pins should be connected to the data bus of the LAN controller.
ALE	O	41	Address Latch Enable: This pin indicates to the system that an address appears on the address and data BUS (AD15–AD0). The address is guaranteed to be valid on the trailing edge of ALE. This pin should be left Not Connected.
-UCS	O	14	Upper Chip Select: When –UCS is LOW, the iChip LAN accesses internal flash memory. This pin should be left Not Connected.
-LCS	O	21	Lower Chip Select: When –LCS is LOW, the iChip LAN accesses internal SRAM memory. This pin should be left Not Connected.

<table>
<tr><th>Signal</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>-BHE</td><td>O</td><td>31</td><td>BUS HIGH Enable: This pin and the least-significant address bit (AD0 or A0) indicate to the system, which bytes of the data BUS (upper, lower, or both) participate in a BUS cycle. The ~BHE and A0 pins are encoded as shown in the table below.
<table>
<tr><th>-BHE</th><th>AD0</th><th>Type of BUS cycle</th></tr>
<tr><td>0</td><td>0</td><td>Word Transfer</td></tr>
<tr><td>1</td><td>0</td><td>Even Byte Transfer</td></tr>
<tr><td>0</td><td>1</td><td>Odd Byte Transfer</td></tr>
<tr><td>1</td><td>1</td><td>N/A</td></tr>
</table>
During a BUS hold or reset condition, -BHE is in a HIGH-impedance state.
This pin should be connected to -BHE of the LAN controller.</td></tr>
<tr><td>HOLD</td><td>I</td><td>62</td><td>BUS Hold Request: when HOLD is HIGH, it indicates that an external BUS master needs control of the local BUS.
This pin should be connected to GND.</td></tr>
<tr><td>HLDA</td><td>O</td><td>61</td><td>BUS Hold Acknowledge: This pin goes HIGH to indicate to an external BUS master that the iChip LAN has released control of the local BUS.
This pin should be left Not Connected.</td></tr>
<tr><td>-RD</td><td>O</td><td>68</td><td>READ: This pin indicates that the iChip LAN is performing a memory read cycle. -RD floats during a BUS hold condition.
This pin should be connected to -RD of the LAN controller.</td></tr>
<tr><td>-WR</td><td>O</td><td>52</td><td>WRITE: This pin indicates that the iChip LAN is performing a memory write cycle. -WR floats during a BUS hold condition.
This pin should be connected to -WR of the LAN controller.</td></tr>
</table>

5.2.2 Miscellaneous Signals

Signal	Type	Pin No.	Description
URTINT	I	40	UART Interrupt: This pin is for debugging purpose only. This pin should be pulled up to VCC.
LMSEL	I	65	LAN Mode Select: • When this pin is held LOW during power up for at least 5 seconds, iChip LAN will automatically enter firmware update mode. • When this pin is held LOW during power up for less than 5 seconds, it forces the iChip LAN into auto baud rate detection.
-RES	I	12	RESET: When -RES is LOW, iChip LAN immediately terminates its present activity and clears its internal logic. -RES must be held LOW for at least 1 ms after power stabilizes. iChip LAN begins fetching instructions approximately 6.5 CLKO periods after ~RES going HIGH. This input is provided with a Schmidt trigger to facilitate power-on reset generation via an RC network.
-CDH	O	60	Received LAN Package: When LOW, this signal indicates that iChip LAN received a legal packet from the LAN controller. During firmware update, -RIH and -CDH are used to display the firmware update status.
-RIH	O	20	Serial Indicator Host: When LOW, this signal indicates that iChip LAN has received a character from the host. During firmware update, -RIH and -CDH are used to display the firmware update status.

5.2.3 Host Interface Signals

Signal	Type	Pin No.	Description
LANINT	I	64	LAN Interrupt. When high, this signal indicates that the LAN controller has information for iChip LAN.
X1	I	42	Crystal Input: This pin and the X2 pin provide connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit. To provide iChip LAN with an external clock source, connect the source to the X1 pin and leave the X2 pin unconnected.
X2	O	43	Crystal Output: This pin and the X1 pin provide connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit.
CLKO	O	44	Clock Output: This pin outputs the internal clock and has the some frequency as X2.
GND	P	67, 55	Ground: iChip LAN Ground signal.
VCC	P	1	Power Supply: This pin supplies power (+5V or +3.3V) to iChip LAN.
NC	N.C	18, 27, 28 29, 32, 66	Must be Not Connected.

Signal	Type	Pin No.	Description
TXDH	O	26	Transmit Data Host: This pin supplies asynchronous serial transmit data to the host.
RXDH	I	30	Receive Data Host: This pin supplies asynchronous serial receive data from the host. When this pin is not used, connect it to VCC.
-CTSH	I	59	Clear-to-Send Host: -CTSH is active only when host hardware flow control is enabled. When -CTSH is LOW, flow control is enabled for the host serial port, i.e., iChip LAN may transmit to the host. When -CTSH is HIGH, the iChip LAN transmitter holds its data in the serial port transmit register. -CTSH is sampled only at the beginning of a frame transmission. If -CTSH is raised while a character frame is being transmitted, that frame will be completed. Connect -CTSH to -RTSH when not in use.
-RTSH	O	58	Ready-to-Send Host: -RTSH is active only when host hardware flow control is enabled. When -RTSH is LOW, flow control is enabled for the host serial port, i.e., the host may transmit to iChip LAN. When -RTSH is HIGH, iChip LAN indicates that its receiver is busy and cannot receive data from host. Connect -RTSH to -CTSH when not in use.
-DSRH	I	15	Data Set Ready Host: When -DSRH is LOW, it indicates that the host is attached and ready to communicate with iChip LAN. Connect -DSRH to GND when not in use.
-DTRH	O	63	Data Terminal Ready Host: When -DTRH is LOW, it indicates to the host that iChip LAN is attached and ready to communicate.

6 Electrical/Mechanical Specifications

6.1 Environmental Specifications

6.1.1 Absolute Maximum Ratings

Parameter	Rating
Voltage at any pin with respect to ground	-0.5 to VCC + 0.5 Volts
Operating temperature	0°C to 70°C (32 to 158°F)
Storage temperature	-60°C to 120°C (–76 to 248°F)
Soldering temperature (max. 10 sec.)	220°C (428°F)
Package dissipation	1.5 Watts

Table 6-1 Environmental Specifications

6.1.2 DC Operating Characteristics

6.1.2.1 3.3 Volt Version

Parameter	Min	Typical	Max	Units
DC Supply	3.0	3.3	3.6	Volts
HIGH-level Input	2.0		VCC+0.5	Volts
HIGH-level Input for X1	VCC-0.8		VCC+0.5	Volts
LOW-level Input	-0.5		0.8	Volts
HIGH-level Output[1]	VCC-0.5		VCC	Volts
LOW-level Output[2]			0.45	Volts
Input leakage current			+/- 10	µA
Power supply current (Operating Mode)[3]		70	80	mA
Input capacitance			20	pF

Notes: [1] I_{OH} = 0.2mA
[2] I_{OL} = 1mA
[3] 20 MHz clock

Table 6-2 DC Operating Characteristics 3.3V Version

6.1.2.2 5 Volt Version

Parameter	Min	Typical	Max	Units
DC Supply	4.75	5.0	5.25	Volts
HIGH-level Input	2.0		VCC+0.5	Volts
LOW-level Input	-0.5		0.8	Volts
HIGH-level Output[1]	2.4		VCC	Volts
HIGH-level Input for X1	VCC-0.8		VCC+0.5	Volts
LOW-level Output[2]			0.45	Volts
Input leakage current			+/- 10	µA
Power supply current (Operating Mode)[3]		160	220	mA
Input capacitance			20	pF

Notes: [1] I_{OH} = 2.4mA
[2] I_{OL} = 2mA
[3] 20 MHz clock

Table 6-3 DC Operating Characteristics 5V Version

6.2 Interface Timing and Waveforms

6.2.1 Switching Characteristic

Parameter	Symbol	Min.	Typical	Max.	Units
Clock Out frequency	Fclk	18.430	18.432	18.434	MHz
Clock Out period	Tclk		1/Fck		us
Address valid to –RD LOW	Tavrl	72			ns
-RD active delay	Tclrl	25			ns
-RD pulse with	Trlrh	94			ns
Data in setup	Tdvcl	10			ns
Data in hold	Tcldx	3			ns
Address valid to –WR LOW	Tavwl	72			ns
Data valid delay	Tcldv	0		15	ns
Control active delay	Tcvctv	0		25	ns
Control inactive delay	Tcvctx	0		25	ns
Data hold time	Tcldox	0			ns
-WR pulse with	Twlwh	94			ns
X1 fall time (1)	Tckhl			5	ns
X1 rise time (2)	Tcklh			5	ns
X1 LOW time	Tclck	24	27	30	ns
X1 HIGH time	Tchck	24	27	30	ns
X1 to CLKO skew	Tcico			25	Ns

Table 6-4 Switching Characteristic

(1) Fall time on 5V version is from 3.5V to 1V and on 3V version is from 2V to 1V.
(2) Rise time on 5V version is from 1V to 3.5V and on 3V version is from 1V to 2V.

6.2.2 Local BUS Read Cycle

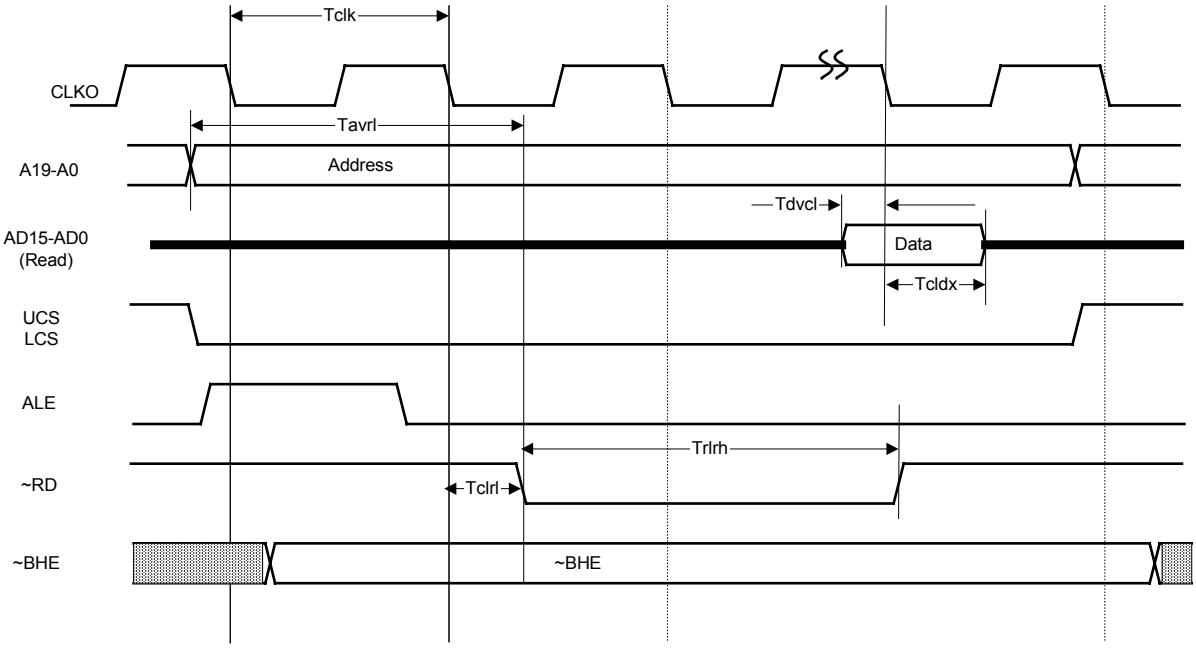


Figure 6-1 Local BUS Read Cycle

6.2.3 Local BUS Write Cycle

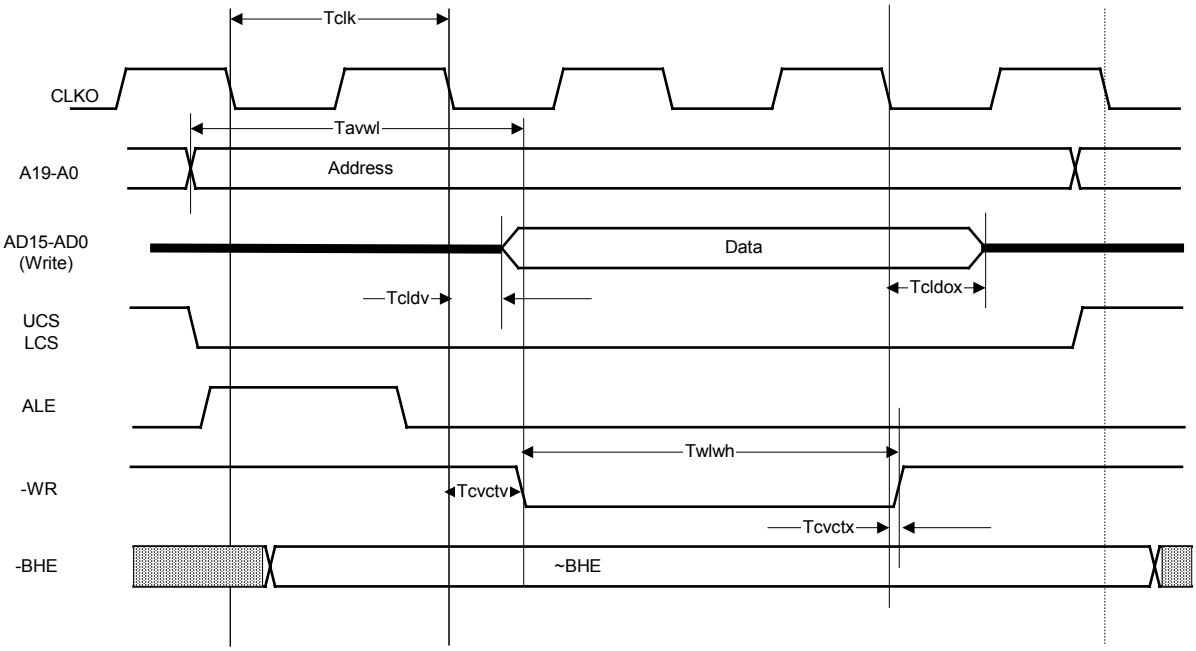


Figure 6-2 Local BUS Write Cycle

6.2.4 Clock Waveform

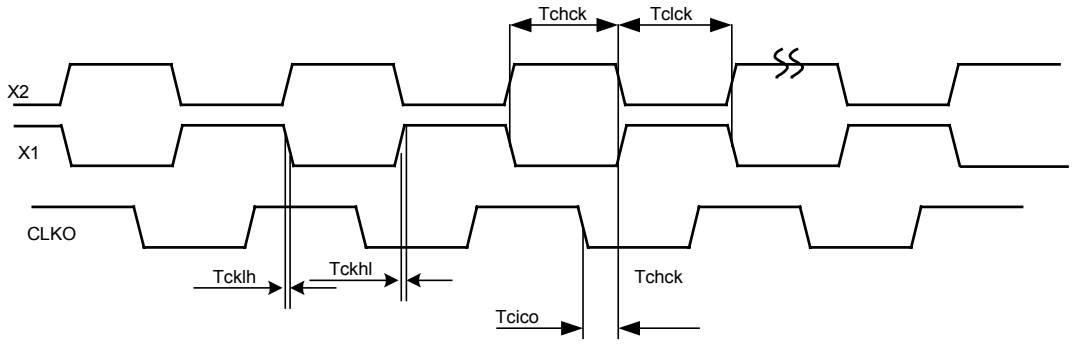


Figure 6-3 Clock Waveform

6.3 Mechanical Dimensions

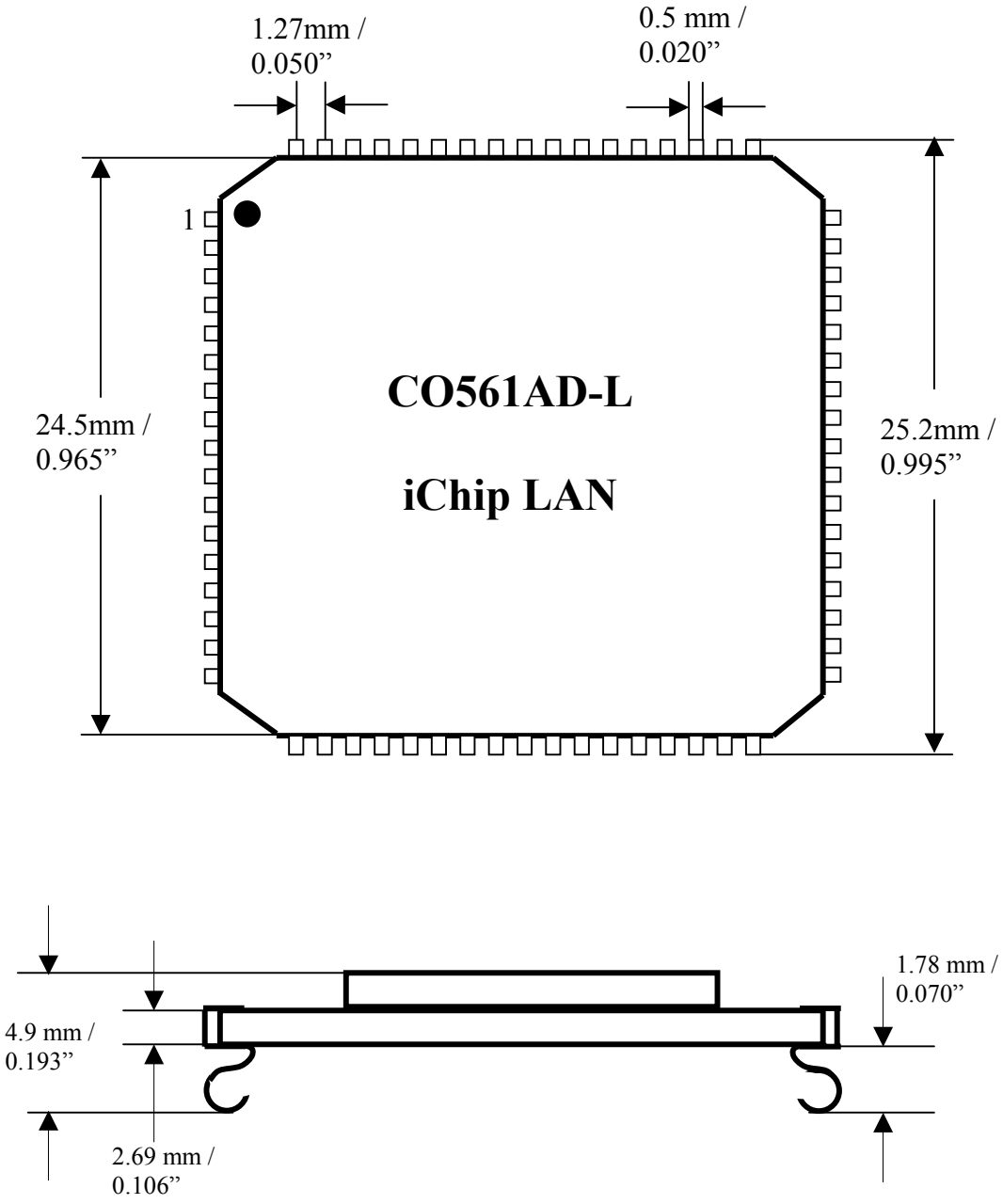


Figure 6-4 Mechanical Dimensions

7 iChip LAN Designs

7.1 Ethernet Controller Environment with Crystal CS8900A

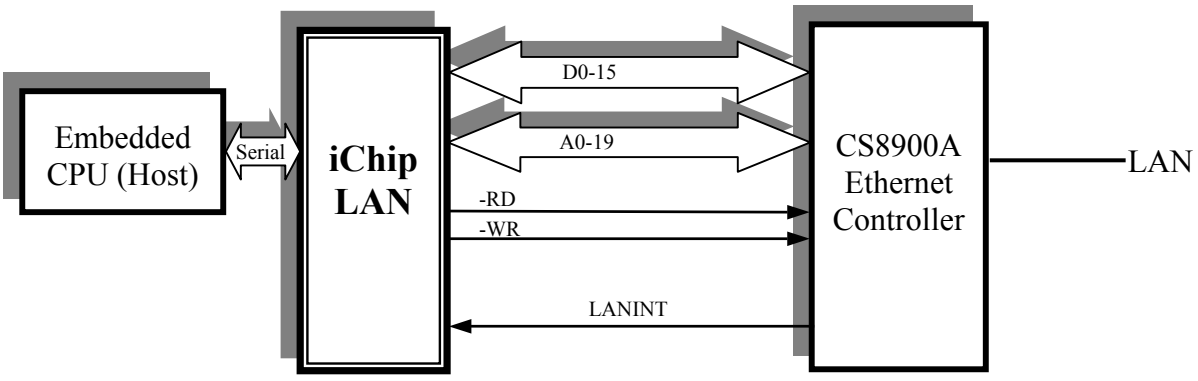


Figure 7-1 CS8900A Ethernet Controller Environment

Note: CS8900A is available for 3.3 and 5-voltiChip LAN.

7.1.1 Ethernet Controller Environment with Realtek RTL8019AS

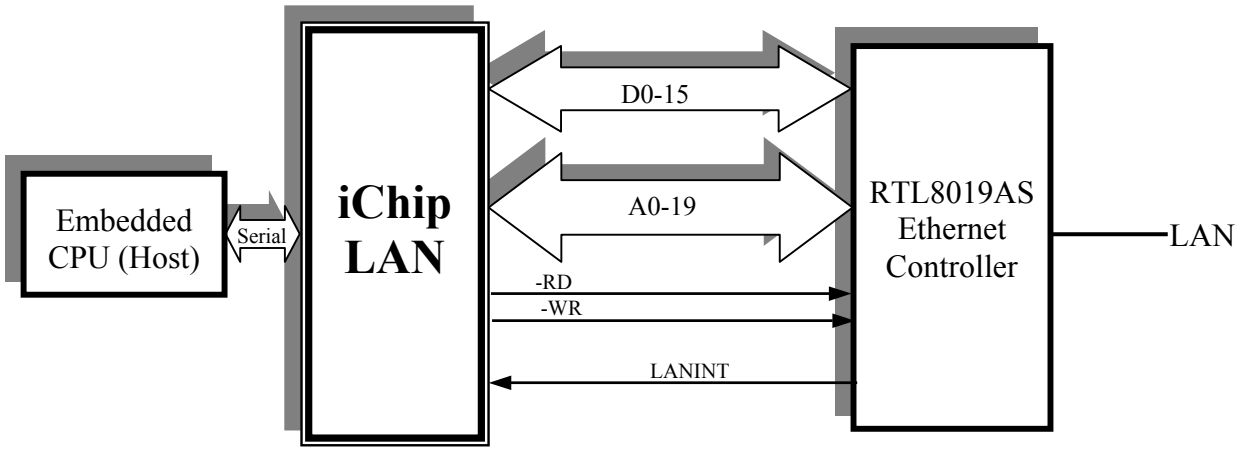


Figure 7-2 RTL8019AS Ethernet Controller Environment

Note: RTL8019AS is appropriate only for 5-volt iChip LAN.

7.2 Selecting a Crystal

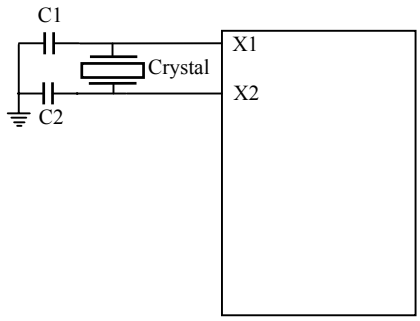


Figure 7-3 Selecting a Crystal.

The characteristics of the built-in inverting amplifier set limits on the following parameters for crystals:
Crystal first overtone frequency ..... 18.432 MHz
ESR (Equivalent Series Resistance) ..... 40 Ω max
Drive Level .....….. 1 mW max
Frequency tolerance …… +/- 100ppm
Load capacitance…….. 18pF
Shunt capacitance……. 7pF Maximum

The recommended range of values for C 1 and C 2 are as follows:
C 1 ..... 15 pF ± 20%
C 2 ..... 22 pF ± 20%
The specific values for C1 and C2 must be determined by the designer and are dependent on the characteristics of the chosen crystal and board design.

7.3 Selecting the Reset Circuit

7.3.1 RC Network

The Reset signal may be designed with a RC network. τ should be greater than 10 mSec. This is a low-cost solution.

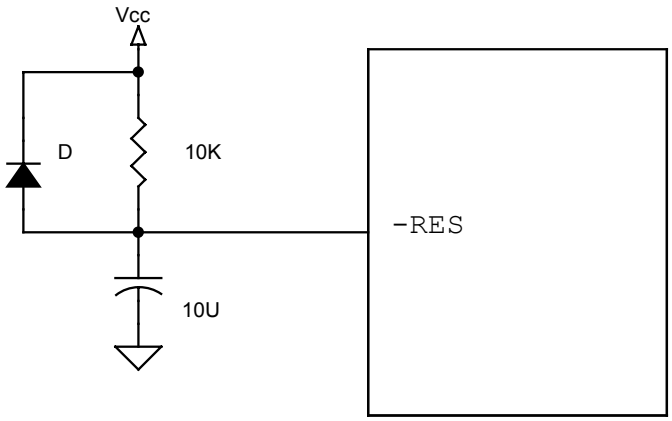


Figure 7-4 RC Reset Circuit

7.3.2 Supervisory Circuit

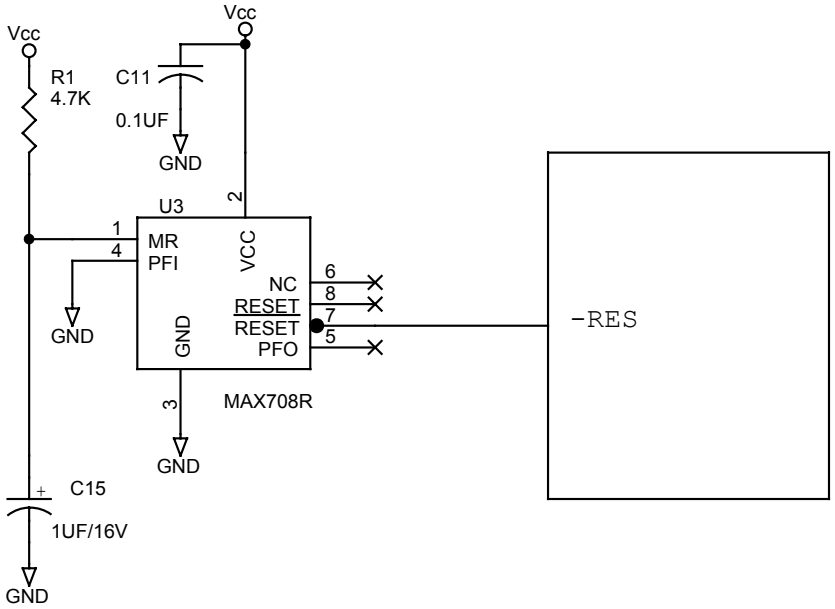


Figure 7-5 Supervisory Reset Circuit

8 Protocol Compliance

iChip LAN CO561AD-L complies with the following Internet standards:

RFC 768	User Datagram Protocol (UDP)
RFC 791	Internet Protocol (IP)
RFC 792	Internet Control Message Protocol (ICMP)
RFC 793	Transmission Control Protocol (TCP)
RFC 821	Simple Mail Transfer Protocol (SMTP)
RFC 826	Ethernet Address Resolution Protocol (ARP)
RFC 822	Standard for the Format of ARPA Internet Text Messages
RFC 1939	Post Office Protocol - Version 3 (POP3)
RFC 1957	Some Observations on the Implementations of the Post Office Protocol (POP3)
RFC 2045	Multipurpose Internet Mail Extensions (MIME) Part One: Format of Internet Message Bodies
RFC 2046	Multipurpose Internet Mail Extensions (MIME) Part Two: Media Types
RFC 2047	MIME (Multipurpose Internet Mail Extensions) Part Three: Message Header Extensions for Non-ASCII Text
RFC 2048	Multipurpose Internet Mail Extensions (MIME) Part Four: Registration Procedures
RFC 2049	Multipurpose Internet Mail Extensions (MIME) Part Five: Conformance Criteria and Examples
RFC 2068	Hypertext Transfer Protocol HTTP/1.1
RFC 959	FTP – File Transfer Protocol
RFC 854	TELNET protocol specification
RFC 857	Telnet ECHO option
RFC 858	Telnet suppress go-ahead option
RFC 1091	Telnet terminal type option
RFC 1073	Telnet window size option
RFC 1321	MD5 Message Digest Algorithm
RFC 1034	Domain Names – Concepts
RFC 1035	Domain Name Server – Implementation
RFC 2131	DHCP
RFC 2132	DHCP Options

Table 8-1 Internet Protocol Compliance

9 List of Terms and Acronyms

10BaseT	10-Mbps baseband Ethernet specification using two pairs of twisted-pair cabling (Category 3, 4, or 5): one pair for transmitting data and the other for receiving data.
AT+i™	**Connect One's** Internet extension to the industry-standard Hayes AT command set. Supports simplified Internet connectivity commands in the spirit of the AT syntax.
ARP	**Address Resolution Protocol.** Protocol intended to resolve the Ethernet MAC address of a LAN node based on its IP address.
Base64	**Encoding scheme**, which converts arbitrary binary data into a 64-character subset of US ASCII. The encoded data is 33% larger than the original data.
DHCP	**Dynamic Host Configuration Protocol.** Provides local LAN configuration parameters, such as IP address, Subnet, Gateways, DNS servers and Mail servers.
DNS	**Domain Name System**. Defines the structure of Internet names and their association with IP addresses.
FTP	**File Transfer Protocol.** Provides file send/receive and remote file directory manipulation.
iChip™	**Connect One's Internet Controller for embedded Internet connectivity.**
ICMP	**Internet Control Message Protocol**. Network layer Internet protocol that reports errors and provides other information relevant to IP packet processing.
IP	**Internet Protocol**. Provides for transmitting blocks of data, called datagrams, from sources to destinations, which are hosts identified by fixed length addresses. Also provides for fragmentation and reassemble of long datagrams, if necessary.
IPCP	**Internet Protocol Control Protocol**. Establishes and configures the Internet Protocol over PPP. Also negotiates Van Jacobson TCP/IP header compression with PPP.
ISP	**Internet Service Provider**. Commercial company that provides Internet access to end (mostly PC) users through a dial-up connection.
LAN	**Local Area Network**. HIGH-speed, LOW-error data network covering a relatively small geographic area (up to a few thousand meters).
LCP	**Link Control Protocol**. Negotiates data link characteristics and tests the integrity of the link.
"Leave on Server"	**An option** designating whether retrieved Email messages are to be left intact on the server for subsequent downloads or are to be deleted from the server after a successful download.
MIME	**Multipurpose Internet Mail Extensions**. Extends the format of mail message bodies to allow multi-part textual and non-textual data to be represented and exchanged between Internet mail servers.
PAP	**Password Authentication Protocol**. Used optionally by the PPP protocol to identify the user to the ISP.
ping	ICMP protocol **ECHO message** and its reply. Often used to debug IP networks and to test the accessibility of a network device.
POP3	**Post Office Protocol Version 3**. Allows a workstation/PC to dynamically retrieve mail from a mailbox kept on a remote server.

PPP	**Point-to-Point Protocol**. Communications protocol used to send data across serial communication links, such as modems.
RFC	**Request For Comments**. Collections of standards that define the way remote computers communicate over the Internet.
SMTP	**Simple Mail Transfer Protocol**. Provides for transferring mail reliably and efficiently over the Internet.
TCP	**Transmission Control Protocol**. Provides reliable stream-oriented connections over the Internet. Works in conjunction with its underlying IP protocol.
Telnet	**Network Terminal Protocol.** Provides remote terminal connectivity, which allows to execute tasks on a remote application server.

Table 9-1 Terms and Acronyms