Features

- Single-chip 3.5GHz WiMAX Transceiver
- Fully Differential Design
- Low-IF/Zero-IF Transceiver Architecture; Requires No External Filters
- Self Calibration Mode for RX / TX Filters
- Support Channel Bandwidths of 3.5, 5.0, 7.0, 8.75MHz, and 10MHz
- Modulation up to 64QAM
- Ultra-fast Fractional-N Synthesizer
- Sensitivity < -74 dBm at 64-QAM, CR=¾, 7MHz BW Typical
- Phase Noise Synthesizer: 0.8° (-37dBc)
- Low Supply Voltage: 3.0 V
- TX Output PRF: 0 dBm, -34 dB EVM
- RX/TX Operating Current: 270/360mA Typical
- 56-lead QFN Package
- Low External Component Count
- Integrated Self IQ Calibration (no external components or control)
- HFDD Support

Applications

- 3.5 GHz Band Wireless Communication Devices
- IEEE® 802.16-2004 Radios
- Supports OFDM up to 64QAM

Description

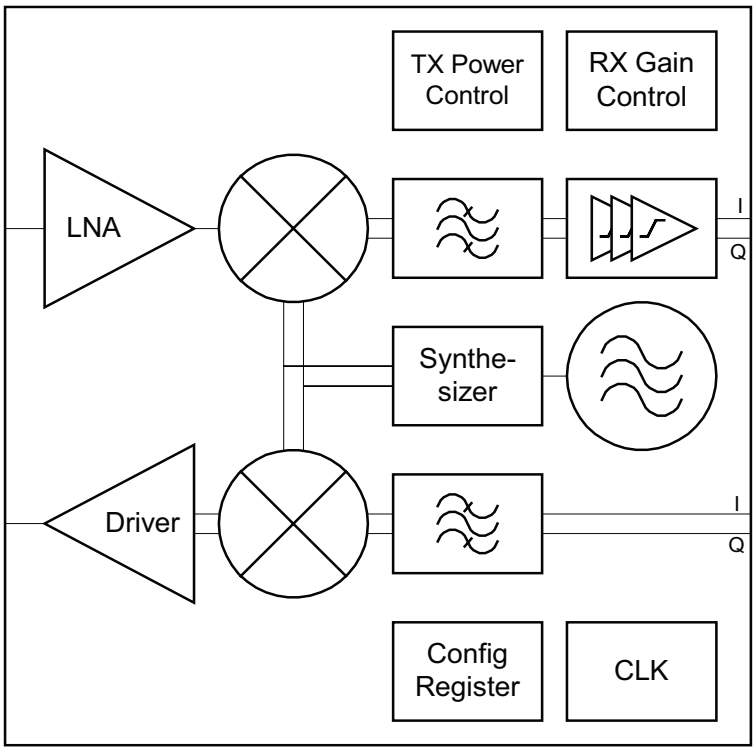
Atmel®'s AT86RF535B is a fully integrated, low cost RF 3.5GHz Low-IF/Zero-IF conversion transceiver for WiMAX applications. It combines excellent RF performance, small size, and low current consumption. The AT86RF535 chip is fabricated on the advanced SiGe BiCMOS process AT46000. The transceiver combines LNA, PA driver, RX/TX mixer, RX/TX filters, VCO, Synthesizer, RX Gain control, and TX Power control, all fully digitally controlled. Only a minimum number of external components are required.

3.5GHz WiMAX Transceiver

AT86RF535B

5190B–WiMAX–9/07

Figure 1. AT86RF535B Block Diagram



Quick Reference Data

Table 1. Quick Reference Data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{RF}	Input Center Frequency		3.4		3.8	GHz
DFRS	Frequency Resolution				19.6	Hz
V_{DD}	Supply Voltage	Applied to VDD pins	3.0	3.3	3.6	V
I_{DDRX}	Supply Current	Receive mode		270		mA
I_{DDTX}	Supply Current	Transmit mode, -5dBm, incl. Balun		360		mA
I_{DDSYN}	Supply Current	Synthesizer Mode		135		mA
I_{DDSTB}	Supply Current	Stand By Mode, CLK driver activated Clock Load 20pF		2.5		mA
SENS	Sensitivity QPSK Sensitivity 64QAM	BW=3.5MHz, CR=½, S/N=9.4dB BW=7MHz, CR=¾, S/N=24.4dB		-92 -74	-88 -70	dBm
P_{RF}	TX Output Power	FRF= 3.5 GHz, 64QAM, EVM=-34dB, incl. Balun		0		dBm
PN	Integrated Phase Noise of Synthesizer	Integrated over Frequency Range 50kHz … 1MHz		0.8		deg rms
T_{AMB}	Operating Ambient Temperature		-30	27	+70	°C

Note: All voltages are referred to GND. VDD=3.0V TAMB=27°C, unless otherwise noted.

Electrical Characteristics

Table 2. Receiver Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
System						
F_{RF}	Input Center Frequency		3.4		3.8	GHz
Z_{IN}	Differential Impedance at LNA Input	Includes a matching inductor and two series capacitors		100		Ω diff.
SENS	Sensitivity QPSK Sensitivity 64QAM	BW=3.5MHz, CR=½, S/N=9.4dB BW=7MHz, CR=¾, S/N=24.4dB			-88 -70	dBm
$P_{IN,MAX}$	Maximum Input Power	BW=7MHz, EVM=24.4dB	-20			dBm
NF_{SSB}	Noise Figure Single Side Band	high gain mode, includes balun w/o Frontend loss		5	6	dB
$G_{RX,STEP}$	RX Chain: Gain Steps			0.76		dB
$G_{RX,RANGE}$	RX Chain: Gain Range			95.5		dB
$t_{RX/TX}$	RX to TX Switching Time	TDD Mode HFDD Mode			5 50	µs
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
System						
ACR±1	Adjacent Ch. Rejection	16QAM 3/4 64QAM 3/4			-11 -4	dB
ACR±2	Nonadjacent Ch. Rejection	16QAM 3/4 64QAM 3/4			-30 -23	dB
Baseband filters, DC cancellation, RSSI, IQ outputs						
R_{OUT}	Output load resistance	Pin to GND	1			MΩ
C_{OUT}	Output load capacitance	Pin to GND		20	50	pF
V_{OMAX}	Maximum Output Voltage	Differential	1			V

V_{OUT}	I or Q output Voltage	Differential at the load specified Output buffer gain offset = +6dB		1		$V_{p,}$ diff
$G_{B,OFFSTEP}$	I, Q output buffer: Gain Offset Steps			0.76		dB
$G_{B,RANGE}$	I, Q output buffer: Gain Range		-9		+2.25	dB
BW_{3dB}	3-dB Bandwidth of Filter	1.875 MHz 2.7 MHz 3.75 MHz 5.0 MHz Note2		3.5 5.0 7.0 8.75		MHz
IMRR	Image Rejection Ratio	Note 2		-42	-36	dB
CMD	Common Mode IQ Voltage		1.2	1.25	1.35	V DC

Table 3. Transmitter Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
System						
F_{RF}	Output Center Frequency		3.4		3.8	GHz
Z_{OUT}	Differential Impedance at Driver Output			100		Ω diff
P_{OUT}	TX Output Power	For 64QAM modulated signals		0		dBm
$t_{TX/RX}$	TX to RX Switching Time	TDD Mode HFDD Mode			5 50	µs
$G_{PA,RANGE}$	TX Chain Gain Control Range		50	71.9		dB
$G_{LSB,STEP}$	TX Chain Gain Control LSB Step Size			0.76		dB
BW_{3dB}	3-dB Bandwidth of Filter	1.875 MHz 2.7 MHz 3.75 MHz 5.0 MHz Note2		3.5 5.0 7.0 8.75		MHz
L_{Carr}	Carrier Leakage	Referred to sub carrier level of 64QAM modulated signals Note 2, 3		-20	-12	dBc
IMRR	Image Rejection Ratio	Referred to sub carrier level of 64QAM modulated signals Note 2, 3		-49	-45	dBr
EVM	Error Vector Magnitude	64QAM ¾, 0dBm Output Power			-34	dB
Z_{IN}	IQ Input Impedance	Differential		10		kΩ diff
V_{IN}	IQ Input Voltage	Peak, Differential		1		Vp,diff
$V_{IN,DC}$	DC Input Voltage			1.25		V

Notes: 1. VDD=3.0V, TAMB =27°C, FRF=3.55 GHz, specific application circuit TBD, unless otherwise noted.
2. Internally adjusted by build-in self-calibration.
3. ETSI Mask Compliant

Functional Description

The AT86RF535B is based on the IEEE 802.16-2004 standard. This product will provide transmit, receive, and frequency synthesis functions using the OFDM modulation schemes, as defined in the above specifications.

The AT86RF535B consists of a frequency-agile RF transceiver intended for use in 3.5-GHz licensed bands at data rates up to 26Mbps.

Configuration and control registers and a bi-directional data communications interface are available to communicate with existing baseband devices from different vendors. The AT86RF535B addresses the requirements of base station (BS) as well as subscriber stations (SS) equipment. The device will operate down to 3.0V.

The AT86RF535 is fabricated in Atmel's AT46000 advanced SiGe BiCMOS process technology and is assembled in a 8mm x 8mm 56-lead QFN package.

RX Path

The differential low noise amplifier (DLNA) makes use of a differential bipolar stage with resistive emitter linearization. For digital gain control operation the DLNA supports the four gain modes 0, 6, 12, and 18dB. The linearity improves as the gain is reduced.

The differential inphase quadrature phase mixer (IQMIX) utilizes a differential bipolar stage with emitter degeneration for the best linearity performance. A complex driving LO source is chosen for optimal LO leakage cancellation. The IQMIX has 4, 10, 16, and 22dB of switchable gain.

The receive poly phase filter (RXPPF) is designed as a frequency shifted leapfrog structure. The filter provides three different bandwidths at three different center frequencies. The bandwidth of this filter is tuned by a built-in self-test (BIST). The PPF filter cap values are automatically adjusted upon power-up. The cap tuning can be recalled via SPI. Image rejection is also calibrated upon request via SPI.

There are also three digitally controlled gain amplifiers (DGA1-3) available to provide the necessary amplification for the receive signal. Each stage supports the four gain modes 0, 6, 12, and 18dB, respectively. An additional fine gain stage DGB enables gain tuning of approximately ± 6dB in 0.76 dB steps. An output buffer with gain offset matches the voltage swing of the radio to the respective Baseband input stage.

The gain control is complete digital and affects LNA, MIX, and the three DGAs by using the same granularity for each stage. The BB/MAC provides the gain vector at a separated serial interface.

Fast TX/RX switching is possible via TX/RX switch input pins controlled by BB/MAC.

The low-IF conversion receiver does not have to amplify DC signals, but the gain setting process produces different offsets in gain stages. An offset correction takes place after each gain step in the receiver to prevent signal saturation. Every stage has an individual offset correction circuit to maintain the correct overall dynamic range. The DC feedback (DCFB) works as an output offset compensation network, which depends on actual gain setting.

The internal gain control operation is optimized for fixed target amplitude. To adapt to different application requirements, the IQ Output Buffer DGB has a programmable gain offset from –1.5dB to 6dB in increments of 0.76dB. This allows the nominal output voltage to be set between 180mVp and 650mVp. The gain is controllable via the register setting. The IQOB is able to drive

a capacitive load on all four-output ports (RXI1, RXI2, RXQ1, RXQ2). The CMD pin is available to provide the common mode voltage of the Digital Output Buffer (DGB).

TX Path

The transmit low pass (TXLP) filter is band limited to meet the emission regulation for OFDM signals. The data signals to the four input ports (TXI1, TXI2, TXQ1, TXQ2) driving the TXLP should be digital but with defined levels.

The complex filtered BB signal is up converted with IQ low-IF up converter (IQUC). A complex driving LO source is used to minimize LO leakage. The output currents of the two mixer stages are added together. The resulting signal drives the power amplifier control block (PAC).

PAC is a Gilbert cell based current domain amplifier with the gain controlled by DC voltage across the mixer core. In that way linear to logarithmic (dB) gain control is achieved.

The BB/MAC provides the gain setting vector at a separated serial interface.

Synthesizer

The voltage controlled oscillator (VCO) operates at two times the local oscillator (LO) frequency. The VCO output feeds a specialized divide-by-two module. The divider provides the required times one LO frequency with both in-phase and quadrature components for use in the IQ Mixer (IQMIX) and the IQ upconverter (IQUC). The use of the divider at two times the LO also reduces load pull on the LO frequency each time the integrated power amplifier (PA) is enabled.

The VCO core is a differential double-grounded bipolar stage with the load for the VCO tank circuit made up of inductive and capacitive components in parallel. No external tuning devices are required. A fully differential inductor is contained on-chip. The capacitive portion of the frequency determining circuitry is made up of a binary weighted capacitor array and an analog voltage controlled varactor. The radio makes use of a hybrid phase lock loop (PLL) architecture. The coarse tuning is accomplished with the combination of Digital PLL/Binary capacitance array and the fine tuning is accomplished using the more conventional analog portion of the PLL. This use of coarse and fine tuning together reduces the analog VCO gain requirement. The reduction of tuning tolerance issues and noise are a direct effect of this type of PLL. Additionally, the characteristic impedance of the loop filter can be increased to reduce the charge pump current which helps in the integration of the active loop filter on-chip. This PLL also contains both integral and proportional charge pumps whose currents may be changed via register settings. This allows the loop parameters to be optimized for tuning speed and noise reduction.

The fractional-N synthesizer in this radio utilizes a unique phase interpolation divider (PID) rather than the more conventional modulus divider architecture. The PID allows for very good frequency resolution and fast tuning speed. It also has the speed and power advantages of an asynchronous divider and is fully programmable within a restricted frequency range.

Because of the coarse digital tuning the analog tuning gain could be reduced so that the characteristic impedance of the loop filter increases and the charge pump current is reduced. This helps to integrated the whole active loop filter (APLL).

Using of two (proportional and integral components) charge pumps and programming their currents permit changing of filter parameters.

The phase interpolation divider (PDIV) is an alternate divider architecture to a conventional modulus divider. It has the speed and power advantages of an asynchron divider and is programmable in a restricted range.

Integrated Calibration Support

Calibration of the transceiver imbalances to optimize transmit LO leakage, transmit and receive image rejection ratio (IMRR) will be performed in between RX/TX operation. It is totally independent from BB/MAC processor.

SPI Interface

Serial peripheral interface (SPI) controls the transceiver. This 4-wire bus contains the ports SDE, SCL, SDI and SDO. The SPI has an 8-bit organization. Each transmission starts with a command byte with the following structure:

MSB LSB

CMD	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0

The command bit CMD is set to “1” for WRITE operation and “0” for READ operation.

The transmission is continued with the data bytes. The number of data bytes depends on the register. The MSB of each data byte is send first.

For an 8 bit register:

MSB LSB

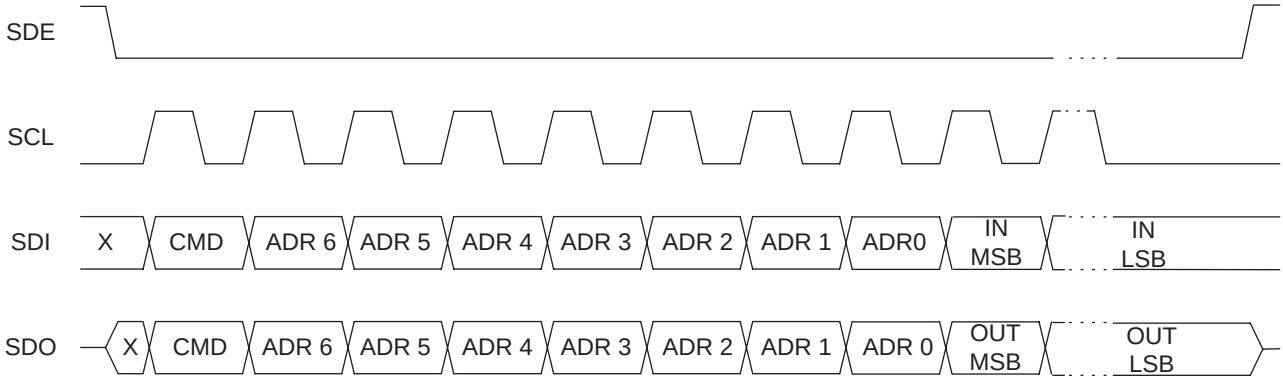
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

For a 16 bit register:

MSB LSB

DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 2. SPI transmission for multiple bytes



Pin Description and Package Drawing

Table 4. Pin Description

Pin	Pin No.	Description
FSW	1	PLL Frequency Switch for HFDD Mode Digital CMOS input levels
VSSDPLL	2	Ground Supply of Digital PLL Modules
VDDDPLL	3	Voltage Supply of Digital PLL Modules
VDDBBIF	4	Supply Voltage of Digital Base Band Interface Pads
PTX	5	Power Switch Transmit Path High active, digital CMOS input levels
RFRX1	6	RF Receive Input 1 Low noise amplifier input. The 50? matching is in part by the bond/package inductance and an external component (tbd).
RFRX2	7	RF Receive Input 2 Complementary signal to RFRX1
VSSRFRX	8	Ground Supply of Radio Frequency Receive Circuit Modules
VDDRFRX	9	Voltage Supply of Radio Frequency Receive Circuit Modules
ATB	10	Analog Test Bus Analog IO Analog output/input signal for testing purposes, connection configurable over SPI
VDDRFTX1	11	Voltage Supply of Radio Frequency Transmit Circuit Modules
VDDRFTX1	12	Voltage Supply of Radio Frequency Transmit Circuit Module
VDDRFTX2	13	Voltage Supply of Radio Frequency Transmit Circuit Modules
VDDRFTX2	14	Voltage Supply of Radio Frequency Transmit Circuit Modules
VDDPA	15	Voltage Supply of Power Amplifier Driving Module
VDDPA	16	Voltage Supply of Power Amplifier Driving Module

Table 4. Pin Description (Continued)

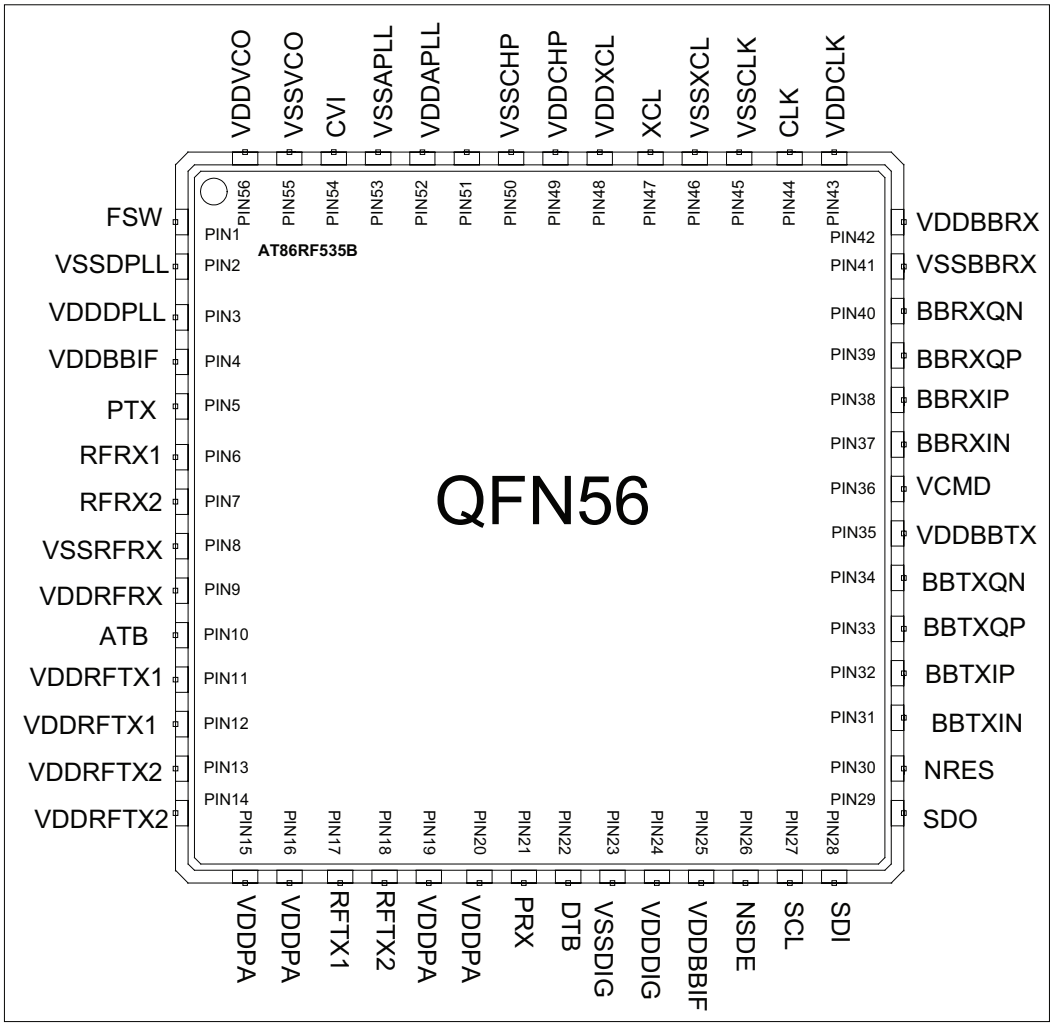
Pin	Pin No.	Description
RFTX1	17	RF Transmit Output 1 P1dB up to +15dBm @ 50? differential 3.5GHz. The 50? matching is in part by the bond/package inductance and an external component (tbd).
RFTX2	18	RF Transmit Output 2 Complementary signal to RFTX1
VDDPA	19	Voltage Supply of Power Amplifier Driving Module
VDDPA	20	Voltage Supply of Power Amplifier Driving Module
PRX	21	Power Switch of Receive Path High active, digital CMOS input levels
DTB	22	Digital Test Bus Input/Output Digital DTB input/output signal for testing purposes, connection and direction is configurable over SPI.
VSSDIG	23	Ground Supply SPI Interface Pads and of Digital Circuit Modules
VDDDIG	24	Voltage Supply of Digital Circuit Modules
VDDBBIF	25	Voltage Supply of Digital Base Band Interface Pads
NSDE	26	SPI Enable Digital Input The rising edge of SCL and a low SDE indicate the start of a data transmission to the SPI slave
SCL	27	SPI Clock Digital Input At every rising edge the SDI data is latched into the internal SPI register. SDO data change also on the rising edge.
SDI	28	SPI Data Digital Input Serial SPI data input stream is started with SDE and contain first an address byte. Read in is MSB first. The MSB of the address byte is the R/W control bit. After the address byte there follows a number of data bytes. The actual number of data bytes depends on the address.
SDO	29	SPI Data Digital Output
NRES	30	Power On Reset Low active, open drain output with internal 10k? pull up resistor
BBTXIN	31	Base Band Transmit Input I Negative Complementary signal to BBTXIP
BBTXIP	32	Base Band Transmit Input I Positive Base band transmit input signal In Phase
BBTXQP	33	Base Band Transmit Input Q Positive Complementary signal to BBTXQN
BBTXQN	34	Base Band Transmit Input Q Negative Base band transmit input signal Quad Phase
VDDBBTX	35	Voltage Supply of BB TX circuit modules
VCMD	36	Common Mode Voltage Bias Output RX Elements DC output voltage 1.0V, only active if PRX=High

Table 4. Pin Description (Continued)

Pin	Pin No.	Description
BBRXIN	37	Base Band Receive Output I Negative In Phase output negative. The base band-processed signal is level voltage programmable to adapt to different base band ADCs. The capacitive load should be less than 10pF asymmetric
BBRXIP	38	Base Band Receive Output I Positive Complementary signal to BBRXIN
BBRXQP	39	Base Band Receive Output Q Positive Quad Phase output positive. The base band-processed signal is level voltage programmable to adapt to different base band ADCs. The capacitive load should be less than 10pF asymmetric.
BBRXQN	40	Base Band Receive Output Q Negative Complementary signal to BBRXQP
VSSBBRX	41	Voltage Supply of BB Receive circuit modules
VDDBBRX	42	Voltage Supply of BB Receive circuit modules
VDDCLK	43	Ground Supply of CMOS Clock Output Driver
CLK	44	40MHz CMOS Clock Digital Output Driver
VSSCLK	45	Ground Supply of CMOS Clock Output Driver
VSSXCL	46	Ground Supply of Crystal Clock Input Buffer
XCL	47	Crystal Clock Input Buffer
VDDXCL	48	Voltage Supply of Crystal Clock Input Buffer
VDDCHP	49	Voltage Supply of Phase Frequency Detector and Charge Pump Modules
VSSCHP	50	Ground Supply of Phase Frequency Detector and Charge Pump Modules
	51	
VDDAPLL	52	Voltage Supply of PLL Analog Divider Modules
VSSAPLL	53	Ground Supply of PLL Analog Divider Modules
CVI	54	VCO Control Voltage IO (Testpin)
VSSVCO	55	Ground Supply of Synthesizer modules VCO and APLF
VDDVCO	56	Voltage Supply of Synthesizer modules VCO and APLF

Note: Additional ground supplies are generated by down bonds to exposed paddle

Figure 3. Pin Information



Revision History

Doc. Rev.	Date	Comments
5190B	9/2007	Modified Features Modified data in Quick Reference Data tables Updated to new Template
5190A	4/2007	Initial document release.

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
Wimax@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature