*National* *Semiconductor*

September 1998

# 54AC299 • 54ACT299
## 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

## General Description

The 'AC/'ACT299 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops $Q_0$, $Q_7$ to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

## Features

- $I_{CC}$ and $I_{OZ}$ reduced by 50%

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT299 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
  'AC299: 5962-88754
  'ACT299: 5962-88771

## Ordering Code:
## Logic Symbols



DS100252-1

### IEEE/IEC



DS100252-4
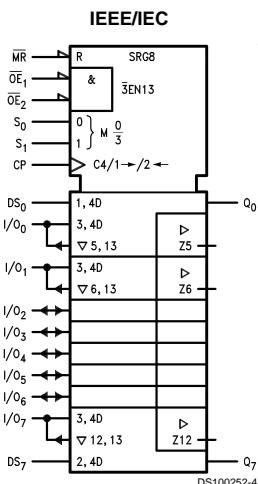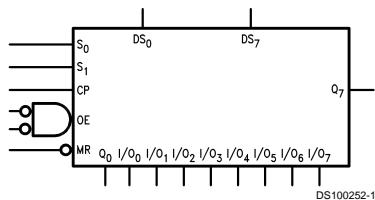
## Connection Diagrams

### Pin Assignment
### for DIP and Flatpak



DS100252-2
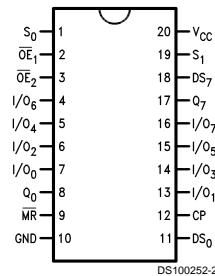
### Pin Assignment for LCC



DS100252-3
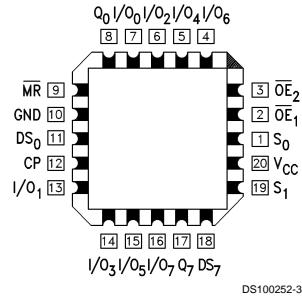
TRI-STATE® is a registered trademark of National Semiconductor Corporation.
FACT® is a registered trademark of Fairchild Semiconductor Corporation.

## Connection Diagrams (Continued)

| Pin Names | Description |
|---|---|
| CP | Clock Pulse Input |
| $DS_0$ | Serial Data Input for Right Shift |
| $DS_7$ | Serial Data Input for Left Shift |
| $S_0$, $S_1$ | Mode Select Inputs |
| $\overline{MR}$ | Asynchronous Master Reset |
| $\overline{OE}_1$, $\overline{OE}_2$ | TRI-STATE Output Enable Inputs |
| $I/O_0$–$I/O_7$ | Parallel Data Inputs or |
|  | TRI-STATE Parallel Outputs |
| $Q_0$, $Q_7$ | Serial Outputs |

## Functional Description

The 'AC/'ACT299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by $S_0$ and $S_1$, as shown in the Truth Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. $Q_0$ and $Q_7$ are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both $S_0$ and $S_1$ in preparation for a parallel load operation.

## Truth Table

| Inputs | | | | Response |
|---|---|---|---|---|
| $\overline{MR}$ | $S_1$ | $S_0$ | CP | |
| L | X | X | X | Asynchronous Reset; $Q_0$–$Q_7$ = LOW |
| H | H | H | ⌐ | Parallel Load; $I/O_n \rightarrow Q_n$ |
| H | L | H | ⌐ | Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc. |
| H | H | L | ⌐ | Shift Left, $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc. |
| H | L | L | X | Hold |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

# Logic Diagram
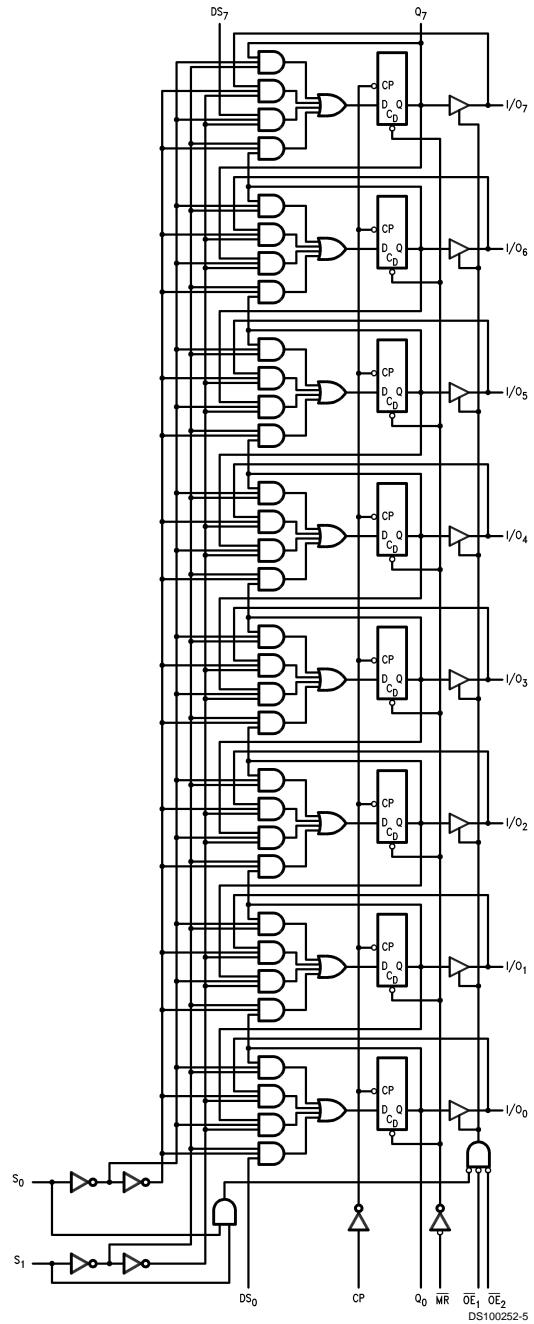


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DS100252-5

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## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $\quad V_I = -0.5V$ | −20 mA |
| $\quad V_I = V_{CC} +0.5V$ | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ +0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $\quad V_O = -0.5V$ | −20 mA |
| $\quad V_O = V_{CC} +0.5V$ | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ +0.5V |
| DC Output Source or Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current | |
| $\quad$ Per Output Pin ($I_{CC}$ or $I_{GND}$) | ±50 mA |
| Storage Temperature ($T_{STG}$) | −65˚C to +150˚C |
| Junction Temperature ($T_J$) | |
| $\quad$ CDIP | 175˚C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| $\quad$ (Unless Otherwise Specified) | |
| $\quad$ 'AC | 2.0V to 6.0V |
| $\quad$ 'ACT | 4.5V to 5.0V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | |
| $\quad$ 54AC/ACT | −55˚C to +125˚C |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| $\quad$ 'AC Devices | |
| $\quad V_{IN}$ from 30% to 70% of $V_{CC}$ | |
| $\quad V_{CC}$ @ 3.3V, 4.5V, 5.5V | 125 mV/ns |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| $\quad$ 'ACT Devices | |
| $\quad V_{IN}$ from 0.8V to 2.0V | |
| $\quad V_{CC}$ @ 4.5V, 5.5V | 125 mV/ns |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. Obviously the databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

## DC Electrical Characteristics

For 'AC Family Devices

| Symbol | Parameter | $V_{CC}$ (V) | 54AC $T_A =$ −55˚C to +125˚C Guaranteed Limits | Units | Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High Level Input Voltage | 3.0 | 2.1 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| | | 4.5 | 3.15 | | |
| | | 5.5 | 3.85 | | |
| $V_{IL}$ | Maximum Low Level Input Voltage | 3.0 | 0.9 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| | | 4.5 | 1.35 | | |
| | | 5.5 | 1.65 | | |
| $V_{OH}$ | Minimum High Level Output Voltage | 3.0 | 2.9 | V | $I_{OUT} = -50$ µA |
| | | 4.5 | 4.4 | | |
| | | 5.5 | 5.4 | | |
| | | 3.0 | 2.4 | V | (Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12$ mA |
| | | 4.5 | 3.7 | | $I_{OH} = -24$ mA |
| | | 5.5 | 4.7 | | $I_{OH} = -24$ mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 3.0 | 0.1 | V | $I_{OUT} = 50$ µA |
| | | 4.5 | 0.1 | | |
| | | 5.5 | 0.1 | | |
| | | 3.0 | 0.50 | V | (Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = 12$ mA |
| | | 4.5 | 0.50 | | $I_{OH} = 24$ mA |
| | | 5.5 | 0.50 | | $I_{OH} = 24$ mA |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | ±1.0 | µA | $V_I = V_{CC}$, GND |

**Note 2:** All outputs loaded; threshold on input associated with output under test.

## DC Electrical Characteristics
For 'AC Family Devices

| Symbol | Parameter | V$_{CC}$ (V) | 54AC T$_A$ = −55°C to +125°C Guaranteed Limits | Units | Conditions |
|---|---|---|---|---|---|
| | (Note 4) | | | | |
| I$_{OLD}$ | Minimum Dynamic | 5.5 | 50 | mA | V$_{OLD}$ = 1.65V Max |
| I$_{OHD}$ | Output Current | 5.5 | −50 | mA | V$_{OHD}$ = 3.85V Min |
| I$_{CC}$ | Maximum Quiescent Supply Current | 5.5 | 80.0 | µA | V$_{IN}$ = V$_{CC}$ or GND |
| I$_{OZT}$ | Maximum I/O Leakage Current | 5.5 | ±5.5 | µA | V$_I$(OE) = V$_{IL}$, V$_{IH}$ V$_I$ = V$_{CC}$, GND V$_O$ = V$_{CC}$, GND |

**Note 3:** All outputs loaded; threshold on input associated with output under test.

**Note 4:** Maximum test duration 20 ms, one output loaded at a time.

**Note 5:** I$_{IN}$ and I$_{CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V$_{CC}$.

I$_{CC}$ for 54AC @ 25°C is identical to 74AC @ 25°C.

## DC Electrical Characteristics
For 'ACT Family Devices

| Symbol | Parameter | V$_{CC}$ (V) | 54ACT T$_A$ = −55°C to +125°C Guaranteed Limits | Units | Conditions |
|---|---|---|---|---|---|
| V$_{IH}$ | Minimum High Level Input Voltage | 4.5 | 2.0 | V | V$_{OUT}$ = 0.1V |
| | | 5.5 | 2.0 | | or V$_{CC}$ − 0.1V |
| V$_{IL}$ | Maximum Low Level Input Voltage | 3.0 | 0.8 | | V$_{OUT}$ = 0.1V |
| | | 4.5 | 0.8 | | or V$_{CC}$ − 0.1V |
| V$_{OH}$ | Minimum High Level | 4.5 | 4.4 | V | I$_{OUT}$ = −50 µA |
| | | 5.5 | 5.4 | | |
| | | 4.5 | 3.70 | V | (Note 7) V$_{IN}$ = V$_{IL}$ or V$_{IH}$ I$_{OH}$ = −24 mA |
| | | 5.5 | 4.70 | | I$_{OH}$ = −24 mA |
| V$_{OL}$ | Maximum Low Level Output Voltage | 4.5 | 0.1 | V | I$_{OUT}$ = 50 µA |
| | | 5.5 | 0.1 | | |
| | | 4.5 | 0.50 | V | (Note 7) V$_{IN}$ = V$_{IL}$ or V$_{IH}$ I$_{OL}$ = 24 mA |
| | | 5.5 | 0.50 | | I$_{OL}$ = 24 mA |
| I$_{IN}$ | Maximum Input Leakage Current | 5.5 | ±1.0 | µA | V$_I$ = V$_{CC}$, GND |
| I$_{CCT}$ | Maximum I$_{CC}$/Input | 5.5 | 1.6 | mA | V$_I$ = V$_{CC}$ − 2.1V |
| | (Note 8) | | | | |
| I$_{OLD}$ | Minimum Dynamic | 5.5 | 50 | mA | V$_{OLD}$ = 1.65V Max |
| I$_{OHD}$ | Output Current | 5.5 | −50 | mA | V$_{OHD}$ = 3.85V Min |
| I$_{CC}$ | Maximum Quiescent Supply Current | 5.5 | 80.0 | µA | V$_{IN}$ = V$_{CC}$ or GND |
| I$_{OZT}$ | Maximum I/O Leakage Current | 5.5 | ±5.0 | µA | V$_I$(OE) = V$_{IL}$, V$_{IH}$ V$_I$ = V$_{CC}$, GND V$_O$ = V$_{CC}$, GND |

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# DC Electrical Characteristics (Continued)

**Note 6:** $I_{CC}$ limit for 54ACT @25˚C is identical to 74ACT @25˚C.

**Note 7:** All outputs loaded; thresholds on input associated with output under test.

**Note 8:** Maximum test duration 2.0 ms, one output loaded at a time.

## Capacitance

| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = 5.0V |
| $C_{PD}$ | Power Dissipation Capacitance | 170 | pF | $V_{CC}$ = 5.5V |

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) (Note 9) | 54AC $T_A$ = –55˚C to +125˚C $C_L$ = 50 pF Min | Max | Units | Fig. No. |
|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Input Frequency | 3.3 | 70 | | MHz | |
| | | 5.0 | 80 | | | |
| $t_{PLH}$ | Propagation Delay CP to $Q_0$ or $Q_7$ (Shift Left or Right) | 3.3 | 1.0 | 25.5 | | |
| | | 5.0 | 1.0 | 17.5 | ns | |
| $t_{PHL}$ | Propagation Delay CP to $Q_0$ or $Q_7$ (Shift Left or Right) | 3.3 | 1.0 | 26.5 | | |
| | | 5.0 | 1.0 | 18.0 | ns | |
| $t_{PLH}$ | Propagation Delay $\overline{CP}$ to $I/O_n$ | 3.3 | 1.0 | 24.5 | ns | |
| | | 5.0 | 1.0 | 17.0 | | |
| $t_{PHL}$ | Propagation Delay $\overline{CP}$ to $I/O_n$ | 3.3 | 1.0 | 26.5 | ns | |
| | | 5.0 | 1.0 | 18.5 | | |
| $t_{PHL}$ | Propagation Delay $\overline{MR}$ to $Q_0$ or $Q_7$ | 3.3 | 1.0 | 27.0 | ns | |
| | | 5.0 | 1.0 | 18.5 | | |
| $t_{PHL}$ | Propagation Delay $\overline{MR}$ to $I/O_n$ | 3.3 | 1.0 | 26.5 | ns | |
| | | 5.0 | 1.0 | 18.0 | | |
| $t_{PZH}$ | Output Enable Time $\overline{OE}$ to $I/O_n$ | 3.3 | 1.0 | 22.0 | ns | |
| | | 5.0 | 1.0 | 15.0 | | |
| $t_{PZL}$ | Output Enable Time $\overline{OE}$ to $I/O_n$ | 3.3 | 1.0 | 23.5 | ns | |
| | | 5.0 | 1.0 | 16.0 | | |
| $t_{PHZ}$ | Output Disable Time $\overline{OE}$ to $I/O_n$ | 3.3 | 1.0 | 22.5 | ns | |
| | | 5.0 | 1.0 | 17.0 | | |
| $t_{PLZ}$ | Output Disable Time $\overline{OE}$ to $I/O_n$ | 3.3 | 1.0 | 21.5 | ns | |
| | | 5.0 | 1.0 | 16.0 | | |

**Note 9:** Voltage Range 3.3 is 3.3V ±0.3V.

Voltage Range 5.0 is 5.0V ±0.5V.

## AC Operating Requirements

| Symbol | Parameter | $V_{CC}$ (V) (Note 10) | 54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF Guaranteed Minimum | Units | Fig. No. |
|---|---|---|---|---|---|
| $t_s$ | Setup Time, HIGH or LOW $S_0$ or $S_1$ to CP | 3.3 5.0 | 9.5 7.0 | ns | |
| $t_h$ | Hold Time, HIGH or LOW $S_0$ or $S_1$ to CP | 3.3 5.0 | 2.0 2.5 | ns | |
| $t_s$ | Setup Time, HIGH or LOW $I/O_n$ to CP | 3.3 5.0 | 6.0 4.0 | ns | |
| $t_h$ | Hold Time, HIGH or LOW $I/O_n$ to CP | 3.3 5.0 | 1.5 2.0 | ns | |
| $t_s$ | Setup Time, HIGH or LOW $DS_0$ or $DS_7$ to CP | 3.3 5.0 | 7.5 5.0 | ns | |
| $t_h$ | Hold Time, HIGH or LOW $DS_0$ or $DS_7$ to CP | 3.3 5.0 | 1.5 1.5 | ns | |
| $t_w$ | CP Pulse Width, LOW | 3.3 5.0 | 5.5 5.0 | ns | |
| $t_w$ | $\overline{MR}$ Pulse Width, LOW | 3.3 5.0 | 5.5 5.0 | ns | |
| $t_{rec}$ | Recovery Time $\overline{MR}$ to CP | 3.3 5.0 | 2.5 2.5 | ns | |

**Note 10:** Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) (Note 11) | 54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF | | Units | Fig. No. |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| $f_{max}$ | Maximum Input Frequency | 5.0 | 70 | | MHz | |
| $t_{PLH}$ | Propagation Delay CP to $Q_0$ or $Q_7$ (Shift Left or Right) | 5.0 | 1.0 | 15.5 | ns | |
| $t_{PHL}$ | Propagation Delay CP to $Q_0$ or $Q_7$ (Shift Left or Right) | 5.0 | 1.0 | 16.0 | ns | |
| $t_{PLH}$ | Propagation Delay CP to $I/O_n$ | 5.0 | 1.0 | 15.0 | ns | |
| $t_{PHL}$ | Propagation Delay CP to $I/O_n$ | 5.0 | 1.0 | 18.0 | ns | |
| $t_{PHL}$ | Propagation Delay $\overline{MR}$ to $Q_0$ or $Q_7$ | 5.0 | 1.0 | 18.0 | ns | |
| $t_{PHL}$ | Propagation Delay $\overline{MR}$ to $I/O_n$ | 5.0 | 1.0 | 17.5 | ns | |

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## AC Electrical Characteristics (Continued)

| Symbol | Parameter | $V_{CC}$ (V) (Note 11) | 54ACT $T_A = -55°C$ to +125°C $C_L = 50$ pF | | Units | Fig. No. |
|--------|-----------|----------------------|----------------------------------------------|------|-------|----------|
| | | | Min | Max | | |
| $t_{PZH}$ | Output Enable Time $\overline{OE}$ to I/O$_n$ | 5.0 | 1.0 | 14.0 | ns | |
| $t_{PZL}$ | Output Enable Time $\overline{OE}$ to I/O$_n$ | 5.0 | 1.0 | 14.5 | ns | |
| $t_{PHZ}$ | Output Disable Time $\overline{OE}$ to I/O$_n$ | 5.0 | 1.0 | 14.5 | ns | |
| $t_{PLZ}$ | Output Disable Time $\overline{OE}$ to I/O$_n$ | 5.0 | 1.0 | 14.0 | ns | |

**Note 11:** Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements

| Symbol | Parameter | $V_{CC}$ (V) (Note 12) | 54ACT $T_A = -55°C$ to +125°C $C_L = 50$ pF Guaranteed Minimum | Units | Fig. No. |
|--------|-----------|----------------------|-----------------------------------------------------------------|-------|----------|
| $t_s$ | Setup Time, HIGH or LOW $S_0$ or $S_1$ to CP | 5.0 | 6.5 | ns | |
| $t_h$ | Hold Time, HIGH or LOW $S_0$ or $S_1$ to CP | 5.0 | 1.5 | ns | |
| $t_s$ | Setup Time, HIGH or LOW I/O$_n$ to CP | 5.0 | 4.5 | ns | |
| $t_h$ | Hold Time, HIGH or LOW I/O$_n$ to CP | 5.0 | 1.5 | ns | |
| $t_s$ | Setup Time, HIGH or LOW $DS_0$ or $DS_7$ to CP | 5.0 | 5.5 | ns | |
| $t_h$ | Hold Time, HIGH or LOW $DS_0$ or $DS_7$ to CP | 5.0 | 1.5 | ns | |
| $t_w$ | CP Pulse Width HIGH or LOW | 5.0 | 5.0 | ns | |
| $t_w$ | $\overline{MR}$ Pulse Width, LOW | 5.0 | 5.0 | ns | |
| $t_{rec}$ | Recovery Time $\overline{MR}$ to CP | 5.0 | 1.5 | ns | |

**Note 12:** Voltage Range 5.0 is 5.0V ±0.5V.

# Physical Dimensions inches (millimeters) unless otherwise noted

$\frac{0.350 \pm 0.008}{(8.890 \pm 0.203)}$

$\frac{0.063 - 0.075}{(1.600 - 1.905)}$

**Top View**

DETAIL A

**Side View**

$\frac{0.200 \pm 0.005}{(5.080 \pm 0.127)}$ TYP

$45° \times \frac{0.015 \pm 0.010}{(0.381 \pm 0.254)}$

$\frac{0.015}{(0.381)}$ MIN TYP

$\frac{0.007 - 0.011}{(0.178 - 0.279)}$ R TYP

$\frac{0.022 - 0.028}{(0.559 - 0.711)}$ TYP

$\frac{0.077 - 0.093}{(1.959 - 2.362)}$

PIN #1 INDEX

$\frac{0.045 - 0.055}{(1.143 - 1.397)}$ TYP

$\frac{0.067 - 0.083}{(1.702 - 2.108)}$ TYP

$\frac{0.045 - 0.055}{(1.143 - 1.397)}$ TYP

$45° \times \frac{0.040 \pm 0.010}{(1.016 \pm 0.254)}$ 3 PLCS

**Bottom View**

$\frac{0.003}{(0.076)}$ MIN TYP

$\frac{0.015}{(0.381)}$ MAX TYP

$\frac{0.022}{(0.559)}$ MAX TYP

$\frac{0.006}{(0.152)}$ MIN TYP

**Detail A**
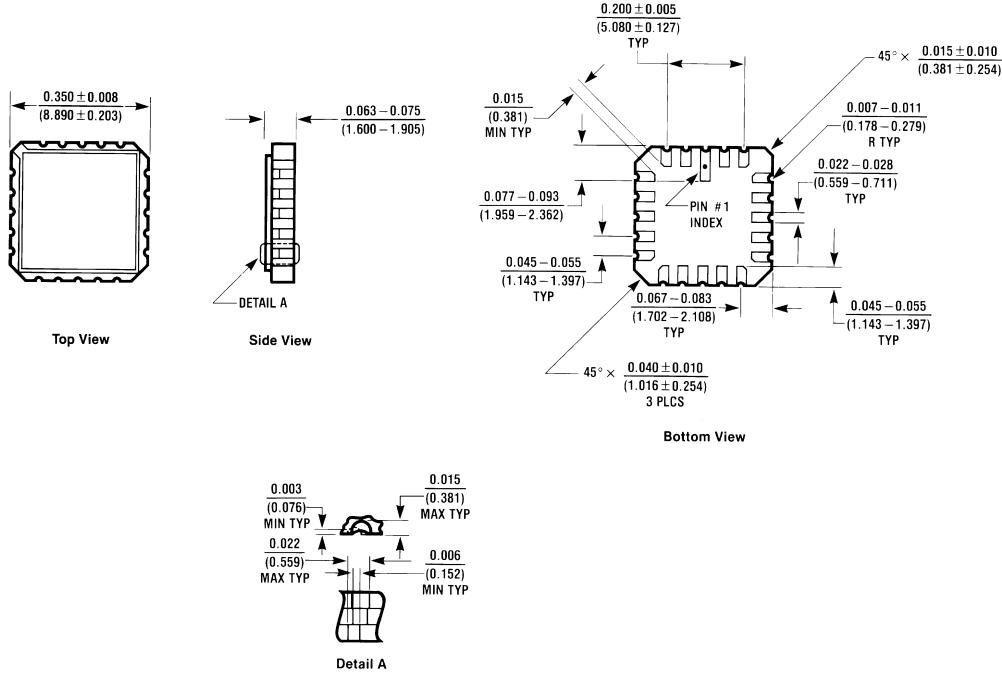
E20A (REV D)

**20 Terminal Ceramic Leadless Chip Carrier (LCC)**
**NS Package Number E20A**

$\frac{0.985}{(25.019)}$ MAX

$\frac{0.025}{(0.635)}$ RAD

20 19 18 17 16 15 14 13 12 11

$\frac{0.220 - 0.310}{(5.588 - 7.874)}$

1 2 3 4 5 6 7 8 9 10

$\frac{0.005 - 0.020}{(0.127 - 0.508)}$ RAD TYP

$\frac{0.037 \pm 0.005}{(0.940 \pm 0.127)}$

$\frac{0.180}{(4.572)}$ MAX

$\frac{0.290 - 0.320}{(7.366 - 8.128)}$

GLASS SEALANT

$\frac{0.005}{(0.127)}$ MIN

$\frac{0.055 \pm 0.005}{(1.397 \pm 0.127)}$

$\frac{0.020 - 0.060}{(0.508 - 1.524)}$

$\frac{0.200}{(5.080)}$ MAX

$95° \pm 5°$

$\frac{0.008 - 0.012}{(0.203 - 0.305)}$

$86°$ $94°$

$\frac{0.150}{(3.810)}$ MIN

$\frac{0.125 - 0.200}{(3.175 - 5.080)}$

$\frac{0.310 - 0.410}{(7.874 - 10.41)}$

$\frac{0.060}{(1.524)}$ MAX BOTH ENDS

$\frac{0.018 \pm 0.003}{(0.457 \pm 0.076)}$

$\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)}$

J20A (REV M)

**20 Lead Ceramic Dual-In-Line Package (J)**
**NS Package Number J20A**

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<br>

**54ACC299 • 54ACT299 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.090
0.060

0.040
0.030
TYP

0.540 MAX

0.050 ± 0.005
TYP

0.005 MIN TYP

20     11

0.370
0.250

0.285 MAX
GLASS

0.270
0.260

0.006
0.004
TYP

0.370
0.250

DETAIL A

PIN #1
IDENT

0.019
0.015 TYP

1     10

0.045 MAX
TYP

0.012
0.008

DETAIL A

W20A (REV E)

**20 Lead Ceramic FLATPAK**
**NS Package Number W20A**
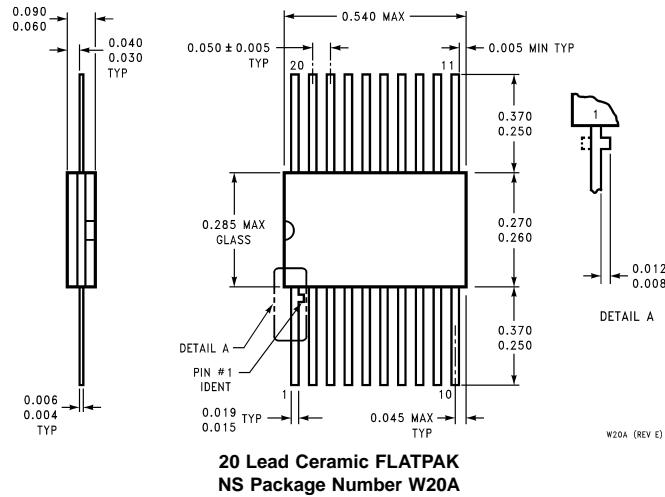
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