HA17384SPS/SRP, HA17384HPS/HRP, HA17385HPS/HRP

High Speed Current Mode PWM Control IC for Switching Power Supply

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Description

The HA17384S/H and HA17385H are PWM control switching regulator IC series suitable for highspeed, current-mode switching power supplies. With ICs from this series and a few external parts, a small, low cost flyback-transformer switching power supply can be constructed, which facilitates good line regulation by current mode control. Synchronous operation driven after an external signal can also be easily obtained which offers various applications such as a power supply for monitors small multi-output power supply.

The IC series are composed of circuits required for a switching regulator IC. That is a under-voltage lockout (UVL), a high precision reference voltage regulator (5.0 V ± 2%), a triangular wave oscillator for timing generation, a high-gain error amplifier, and as totem pole output driver circuit which directly drives the gate of power MOSFETs found in main switching devices. In addition, a pulse-by-pulse type, high-speed, current-detection comparator circuit with variable detection level is incorporated which is required for current mode control.

The HA17384SPS includes the above basic function circuits. In addition to these basic functions, the H Series incorporates thermal shut-down protection (TSD) and overvoltage protection (OVP) functions, for configuration of switching power supplies that meet the demand for high safety levels.

Between the HA17384 and HA17385, only the UVL threshold voltages differ as shown in the product lineup table.(See next page.)

This IC is pin compatible with the “3842 family” ICs made by other companies in the electronics industry. However, due to the characteristics of linear ICs, it is not possible to achieve ICs that offer full compatibility in every detail.

Therefore, when using one of these ICs to replace another manufacturer’s IC, it must be recognized that it has different electrical characteristics, and it is necessary to confirm that there is no problem with the power supply (mounting) set used.

Functions

- Under-voltage lockout system
- Reference voltage regulator of 5.0 V ± 2%
- Triangular wave (sawtooth) oscillator
- Error amplifier
- Totem pole output driver circuit (direct driving for power MOS FETs)
- Current-detection comparator circuit for current mode
- OVP function (over voltage protection) *1
- TSD function (thermal shut-down protection) *1
- Protect function by zener diode (between power input and GND)

Note: 1. H series only.

Features

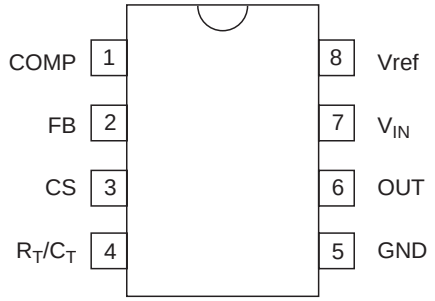
- High-safety UVL circuit is used (Both V_{IN} and Vref are monitored)
- High speed operation:
  - Current detection response time: 100 ns Typ
  - Maximum oscillation frequency: 500 kHz
- Low standby current: 170 µA Typ
- Wide range dead band time
  (Discharge current of timing capacitance is constant 8.4 mA Typ)
- Able to drive power MOSFET directly
  (Absolute maximum rating of output current is ±1 A peak)
- OVP function (over voltage protection) is included *1
  (Output stops when FB terminal voltage is 7.0 V Typ or higher)
- TSD function (thermal shut-down protection) is included *1
  (Output stops when the temperature is 160°C Typ or higher)
- Zener protection is included
  (Clamp voltage between V_{IN} and GND is 34 V Typ)
- Wide operating temperature range:
  - Operating temperature: –20°C to +105°C
  - Junction temperature: 150°C *2

Notes: 1. H series only.
2. S series only.

Product Lineup

Package		Additional Function		UVL Power Supply Threshold Voltage	
DILP8 (DP-8B)	SOP8 (FP-8DC)	TSD (Thermal shut-down protection)	OVP (Over voltage protection)	$V_{TH\ UVL}$ (V) Typ	$V_{TL\ UVL}$ (V) Typ
HA17384SPS	HA17384SRP	–	–	16.0	10.0
HA17384HPS	HA17384HRP				
HA17385HPS	HA17385HRP			8.4	7.6

Pin Arrangement



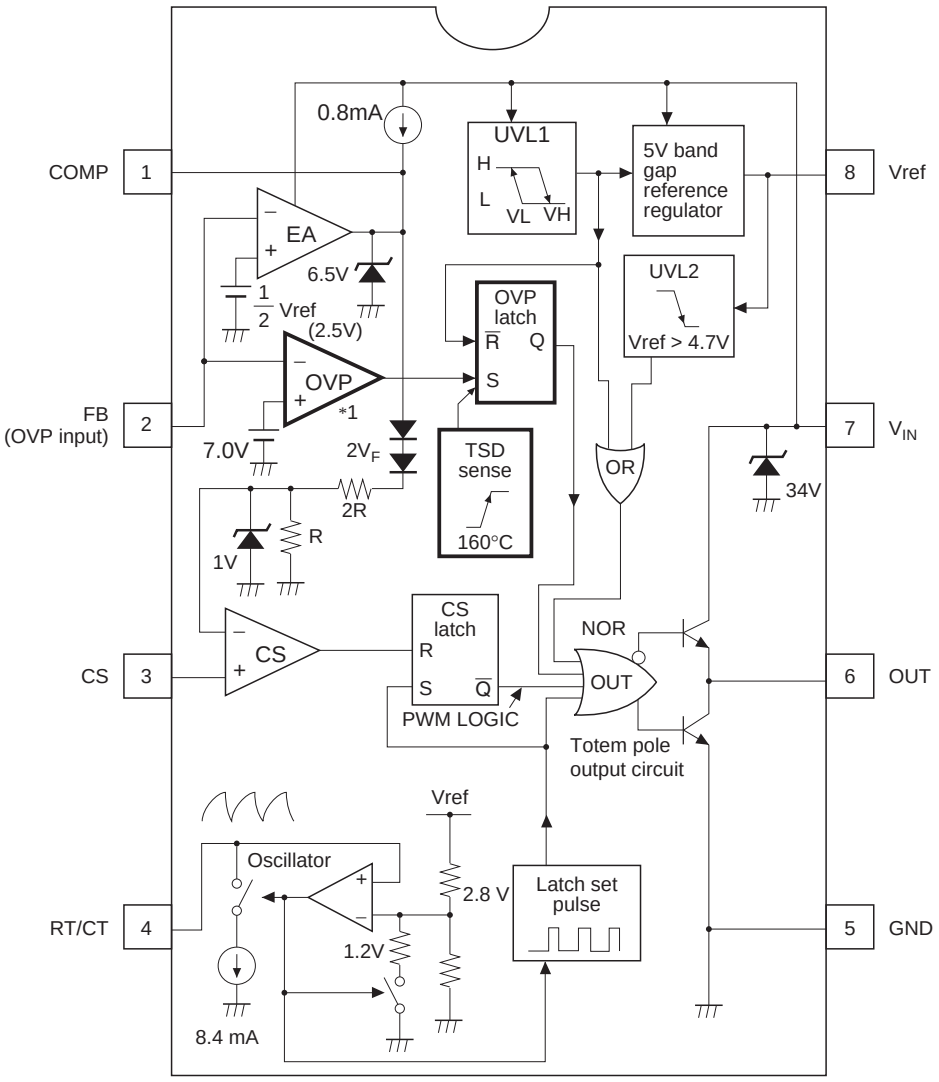
(Top view)

Pin Function

Pin No.	Symbol	Function	Note
1	COMP	Error amplifier output pin	
2	FB	Inverting input of error amp./OVP input pin	1
3	CS	Current sensing signal input pin	
4	R_T/C_T	Timing resistance, timing capacitance connect pin	
5	GND	Groung pin	
6	OUT	PWM Pulse output pin	
7	V_{IN}	Power supply voltage input pin	
8	Vref	Reference voltage 5V output pin	

Note: 1. Overvoltage protection (OVP) input is usable only for the HA17384H and HA17385H.

Block Diagram



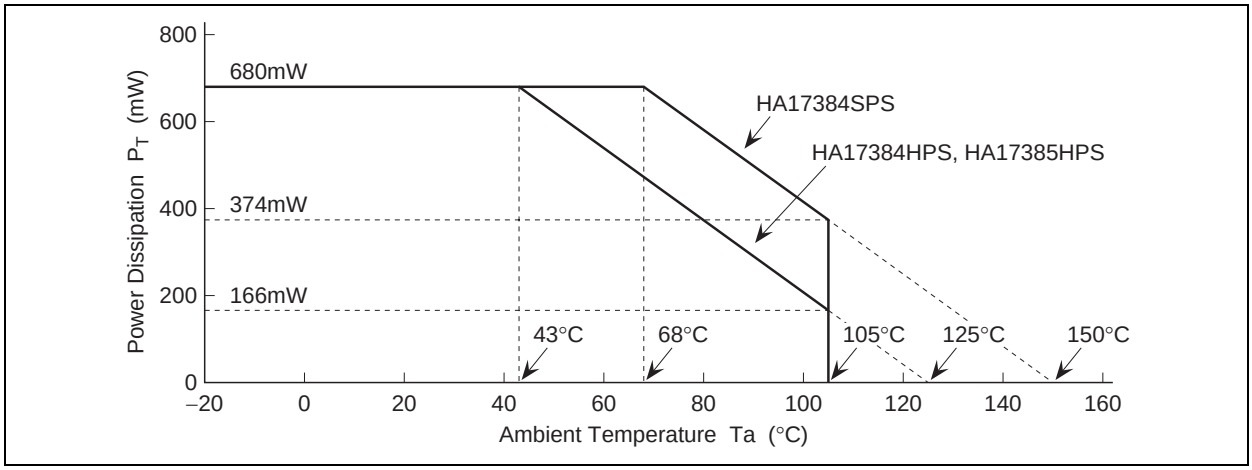
Note: 1. Blocks with bold line are not included in HA17384SPS/SRP.

Absolute Maximum Ratings

(Ta = 25°C)

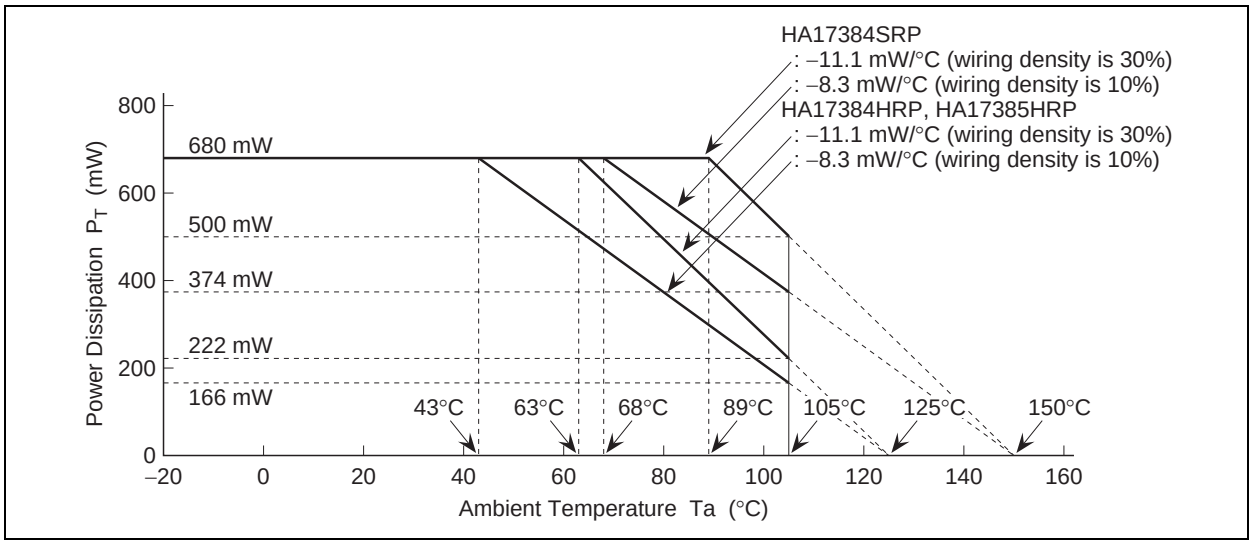
Item	Symbol	Rating	Unit	Note
Supply voltage	V_{IN}	30	V	
DC output current	I_O	±0.1	A	
Peak output current	$I_{O\ PEAK}$	±1.0	A	
Error amplifier input voltage	V_{FB}	–0.3 to V_{IN}	V	
COMP terminal input voltage	V_{COMP}	–0.3 to +7.5	V	
Error output sink current	I_{OEA}	10	mA	
Power dissipation	P_T	680	mW	1, 2
Operating temperature	Topr	–20 to +105	°C	
Junction temperature	Tj	125	°C	3
		150	°C	4
Storage temperature	Tstg	–55 to +125	°C	3
		–55 to +150	°C	4

Notes: 1. For the HA17384HPS and HA17385HPS,
This value applies up to Ta = 43°C; at temperatures above this, 8.3 mW/°C derating should be applied.
For the HA17384SPS,
This value applies up to Ta = 68°C; at temperatures above this, 8.3 mW/°C derating should be applied.



Absolute Maximum Ratings (cont.)

Notes: 2. This is the value when the device is mounted on a glass-epoxy substrate (40 mm × 40 mm × 1.6 mm). However,
For the HA17384HRP and HA17385HRP,
Derating should be performed with 8.3 mW/°C in the Ta ≥ 43°C range if the substrate wiring density is 10%.
Derating should be performed with 11.1 mW/°C in the Ta ≥ 63°C range if the substrate wiring density is 30%.
For the HA17384SRP,
Derating should be performed with 8.3 mW/°C in the Ta ≥ 68°C range if the substrate wiring density is 10%.
Derating should be performed with 11.1 mW/°C in the Ta ≥ 89°C range if the substrate wiring density is 10%.



3. Applies to the HA17384HPS/HRP and HA17385HPS/HRP.
4. Applies to the HA17384SPS/SRP.

Electrical Characteristics

(The condition is: Ta = 25°C, V_{IN} = 15 V, C_T = 3300 pF, R_T = 10 kΩ without notice)

- Reference Part

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Reference output voltage	Vref	4.9	5.0	5.1	V	Io = 1 mA	
Line regulation	Regline	–	20	50	mV	12 V ≤ V_{IN} ≤ 25 V	
Load regulation	Regload	–	10	25	mV	–1 mA ≥ Io ≥ –20 mA	
Output short current	Ios	–30	–100	–180	mA	Vref = 0V	
Temperature stability	ΔVref	–	80	–	ppm/°C	Io = –1 mA, –20°C ≤ Ta ≤ 105°C	1
Output noise voltage	V_N	–	100	–	μV	10 Hz ≤ fnoise ≤ 10 kHz	1

Note: 1. Reference value for design.

- Triangular Wave Oscillator Part

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Typical oscillating frequency	fosc Typ	47	52	57	kHz	C_T = 3300 pF, R_T = 10 kΩ	
Maximum oscillating frequency	fosc Max	500	–	–	kHz		
Supply voltage dependency of oscillating frequency	Δfosc 1	–	±0.5	±2.0	%	12 V ≤ V_{IN} ≤ 25 V	
Temperature dependency of oscillating frequency	Δfosc 2	–	±5.0	–	%	–20°C ≤ Ta ≤ 105°C	1
Discharge current of C_T	$Isink_{CT}$	7.5	8.4	9.3	mA	V_{CT} = 2.0 V	
Low level threshold voltage	V_{TLCT}	–	1.2	–	V		1
High level threshold voltage	V_{THCT}	–	2.8	–	V		1
Triangular wave amplitude	ΔV_{CT}	–	1.6	–	V	$\Delta V_{CT} = V_{THCT} - V_{TLCT}$	1

Note: 1. Reference value for design.

(The condition is: Ta = 25°C, V_{IN} = 15 V, C_T = 3300 pF, R_T = 10 kΩ without notice)

- Error Amplifire Part / OVP Part

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Non-inverting input voltage	V_{FB}	2.42	2.50	2.58	V	V_{COMP} = 2.5 V	
Input bias current	I_{IB}	–	–0.2	–2.0	μA	V_{FB} = 5.0 V	
Open loop voltage gain	A_{VOL}	65	90	–	dB	2.0 V ≤ V_O ≤ 4.0 V	
Unity gain bank width	BW	0.7	1.0	–	MHz		
Power supply voltage rejection ratio	PSRR	60	70	–	dB	12 V ≤ V_{IN} ≤ 25 V	
Output sink current	$I_{Osink\ EA}$	3.0	9.0	–	mA	V_{FB} = 2.7 V, V_{COMP} = 1.1 V	
Output source current	$I_{Osource\ EA}$	–0.5	–0.8	–	mA	V_{FB} = 2.3 V, V_{COMP} = 5.0 V	
High level output voltage	$V_{OH\ EA}$	5.5	6.5	7.5	V	V_{FB} = 2.3 V, R_L = 15 kΩ(GND)	
Low level output voltage	$V_{OL\ EA}$	–	0.7	1.1	V	V_{FB} = 2.7 V, R_L = 15 kΩ(Vref)	
OVP latch threshold voltage	V_{OVP}	6.0	7.0	8.0	V	Increase FB terminal voltage	1
OVP (FB) terminal input current	$I_{FB(OVP)}$	–	30	50	μA	V_{FB} = 8.0 V	1
OVP latch reset V_{IN} voltage	$V_{IN(OVP\ RES)}$	6.0	7.0	8.0	V	Decreasing V_{IN} after OVP latched	1

Note: 1. These values are not prescribe to the HA17384SPS/SRP because OVP function is not included.

Electrical Characteristics (cont.)

(The condition is: Ta = 25°C, V_{IN} = 15 V, C_T = 3300 pF, R_T = 10 kΩ without notice)

- Current Sensing Part

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Voltage gain	A_{VCS}	2.85	3.00	3.15	V/V	V_{FB} = 0 V	1
Maximum sensing voltage	Vth_{CS}	0.9	1.0	1.1	V		
Power supply voltage rejection ratio	PSRR	–	70	–	dB	12 V ≤ V_{IN} ≤ 25 V	2
Input bias current	I_{BCS}	–	–2	–10	µA	V_{CS} = 2 V	
Current sensing response time	tpd	50	100	150	ns	Time from when V_{CS} becomes 2 V to when output becomes "L" (2 V)	3

Notes: 1. The gain this case is the ratio of error amplifier output change to the current-sensing threshold voltage change.
2. Reference value for design.
3. Current sensing response time tpd is definded a shown in the figure 1.

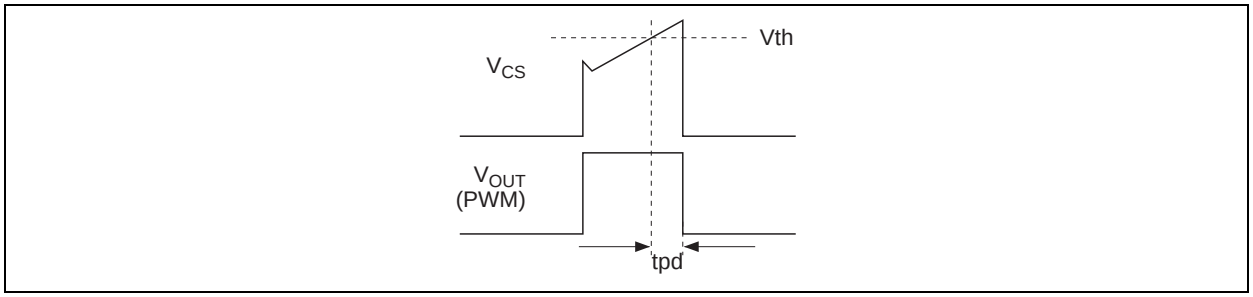


Figure 1 Definition of Current Sensing Response Time tpd

- PWM Output Part

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Output low voltage 1	V_{OL1}	–	0.7	1.5	V	Iosink = 20 mA	
Output low voltage 2	V_{OL2}	–	1.5	2.2	V	Iosink = 200 mA	1
Output high voltage 1	V_{OH1}	13.0	13.5	–	V	Iosource = –20 mA	
Output high voltage 2	V_{OH2}	12.0	13.3	–	V	Iosource = –200 mA	1
Output low voltage at standby mode	$V_{OL\ STB}$	–	0.8	1.1	V	V_{IN} = 5 V, Iosink = 1 mA	
Rise time	t_r	–	80	150	ns	C_L = 1000 pF	
Fall time	t_f	–	70	130	ns	C_L = 1000 pF	
Maximum ON duty	Du max	94	96	100	%		
Minimum ON duty	Du min	–	–	0	%		

Note: 1. Pulse application test

Electrical Characteristics (cont.)

(The condition is: Ta = 25°C, V_{IN} = 15 V, C_T = 3300 pF, R_T = 10 kΩ without notice)

- UVL Part

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Threshold voltage for high V_{IN} level	$V_{TH\ UVL}$	14.5	16.0	17.5	V	Turn-ON voltage when V_{IN} is rising	1
		7.6	8.4	9.2	V		2
Threshold voltage for low V_{IN} level	$V_{TL\ UVL}$	9.0	10.0	11.0	V	Minimum operating	1
		6.8	7.6	8.4	V	voltage after turn-ON	2
V_{IN} UVL hysteresis voltage	$V_{HYS\ UVL}$	5.0	6.0	7.0	V	$V_{HYS\ UVL} = V_{TH\ UVL} - V_{TL\ UVL}$	1
		0.6	0.8	1.0	V		2
Vref UVL threshold voltage	$V_{T\ Vref}$	4.3	4.7	Vref	V	Voltage is forced toVref terminal	

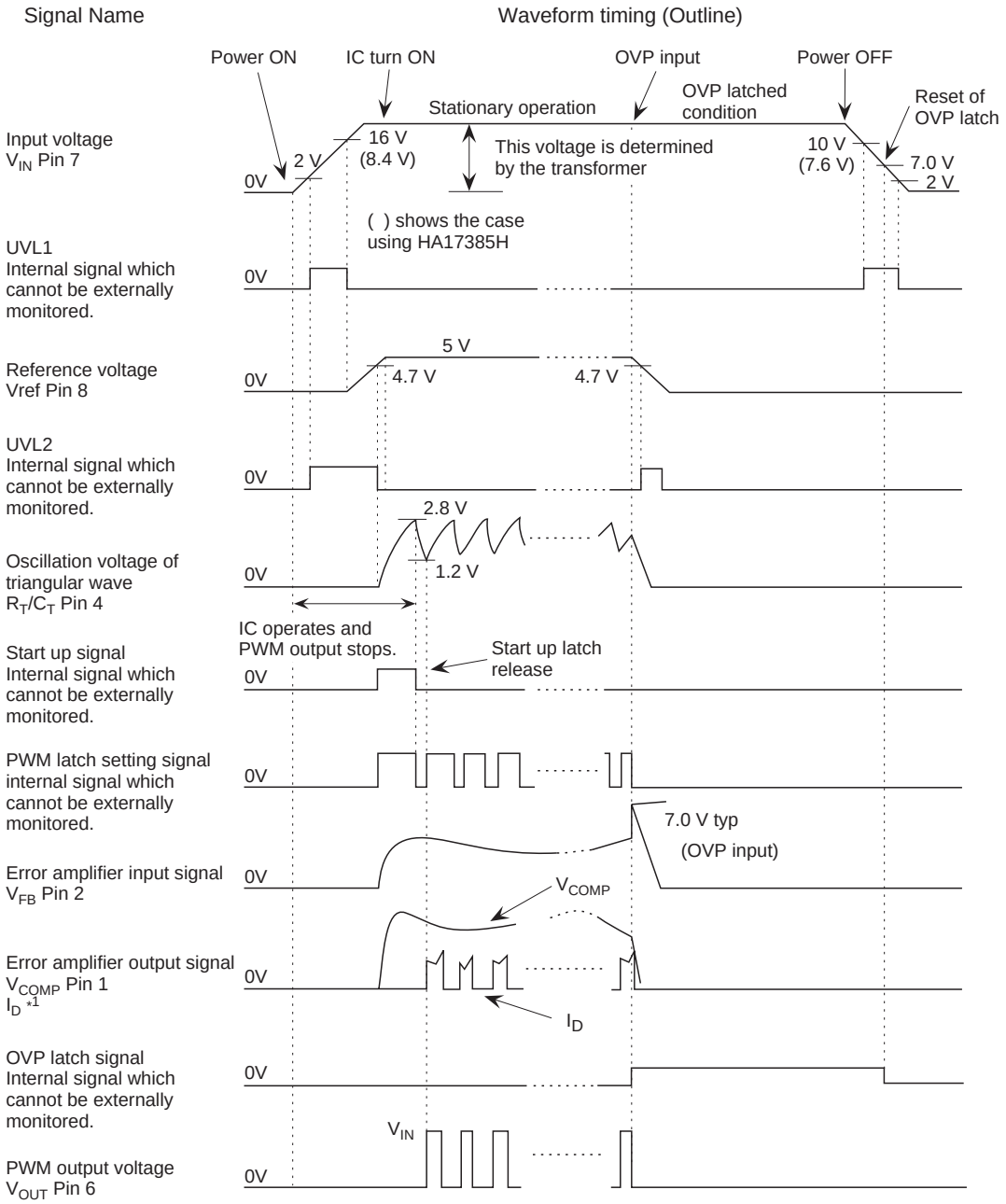
Notes: 1. For the HA17384S/H.
2. For the HA17385H.

- Total Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Operating current	I_{IN}	7.0	10.0	13.0	mA	C_L = 1000 pF, V_{FB} = V_{CS} = 0 V	
Standby current	I_{STBY}	120	170	230	µA	Current at start up	
Current of latch	I_{LATCH}	200	270	340	µA	V_{FB} = 0 V after V_{FB} = V_{OVP}	1, 2
Power supply zener voltage	V_{INZ}	31	34	37	V	I_{IN} + 2.5 mA	
Overheat protection starting temperature	Tj_{TSD}	–	160	–	°C		3, 4

Notes: 1. These values are not prescribe to the HA17384SPS/SRP because OVP function is not included.
2. V_{IN} = 8.5 V in case of the HA17384H.
3. These values are not prescribe to the HA17384SPS/SRP because TSD function is not included.
4. Reference value for design.

Timing Chart



Note: 1. I_D indicates the power MOSFET drain current; it is actually observed as voltage V_S generated by power MOSFET current detection source resistance R_S.
V_{COMP} indicates the error amp output voltage waveform. Current mode operation is performed so that a voltage 1/3 that of V_{COMP} is the current limiter level.

Operation (Description of Timing Chart)

From Power ON to Turn On

After the power is switched ON, the power supply terminal voltage (V_{IN}) of this IC rises by charging through bleeder resistor R_B. At this time, when the power voltage is in the range of 2 V to 16 V*[1]. The low-voltage, lock out UVL1 operates and accordingly the OUT voltage, that is, the gate voltage of the power MOS FET, is fixed at 1.3 V or a lower value, resulting in the power MOS FET remaining in the OFF state.

When the power supply voltage reaches 16 V, UVL1 of this IC is reset and the reference voltage (Vref) generating part turns ON. However, until Vref becomes 4.7 V, the low-voltage, lock out UVL2 operates to keep the OUT terminal voltage low. After Vref terminal voltage becomes 4.7 V or higher, OUT terminal outputs a PWM pulse.

Note: 1. The value is for the HA17384S/H.
The value is 8.4 V for the HA17385H.

Generation of Triangular Wave and PWM Pulse

After the output of the Vref, each blocks begins to operate. The triangular wave is generated on the R_T/C_T terminal. For PWM pulses, the triangular wave rise time is taken as the variable on-duty on-time. The triangular wave fall time is taken as the dead-band time. The initial rise of the triangular wave starts from 0 V, and to prevent a large on-duty at this time, the initial PWM pulse is masked and not output. PWM pulses are outputted after the second triangular wave. The above operation is enabled by the charge energy which is charged through the bleeder resistor R_B into the capacitor C_B of V_{IN}.

Stationary Operation

PWM pulses are outputted after the second wave of the triangular wave and stationary operation as the switching power supply starts.

By switching operation from ON/OFF to OFF/ON in the switching device (power MOS FET), the transformer converts the voltage. The power supply of IC V_{IN} is fed by the back-up winding of the transformer.

In the current mode of the IC, the current in the switcing device is always monitored by a source resistor R_{CS}. Then the current limiter level is varied according to the error voltage (COMP terminal voltage) for PWM control. One third of the error voltage level, which is divided by resistors “2R” and “R” in the IC, is used to sense the current (R = 25 kΩ).

Two diodes between the error output and the 2R-R circuit act only as a DC level shifter. Actually, these diodes are connected between the 2R-R circuit and GND, and, the current sensing comparator and GND, respectively. Therefore, these blocks operate 1.4 V higher than the GND level. Accordingly, the error of the current sensing level caused by the switching noise on the GND voltage level is eliminated. The zener diode of 1 V symbolically indicates that the maximum sensing voltage level of the CS terminal is 1 V.

Power OFF

At power OFF, the input voltage of the transformer gradually decreases and then V_{IN} of IC also decreases according to the input voltage. When V_{IN} becomes lower than 10 V*[2] or Vref becomes lower than 4.7 V, UVL1 (UVL2) operates again and the PWM pulse stops.

Note: 2. The value is for the HA17384S/H.
The value is 7.6 V for the HA17385H.

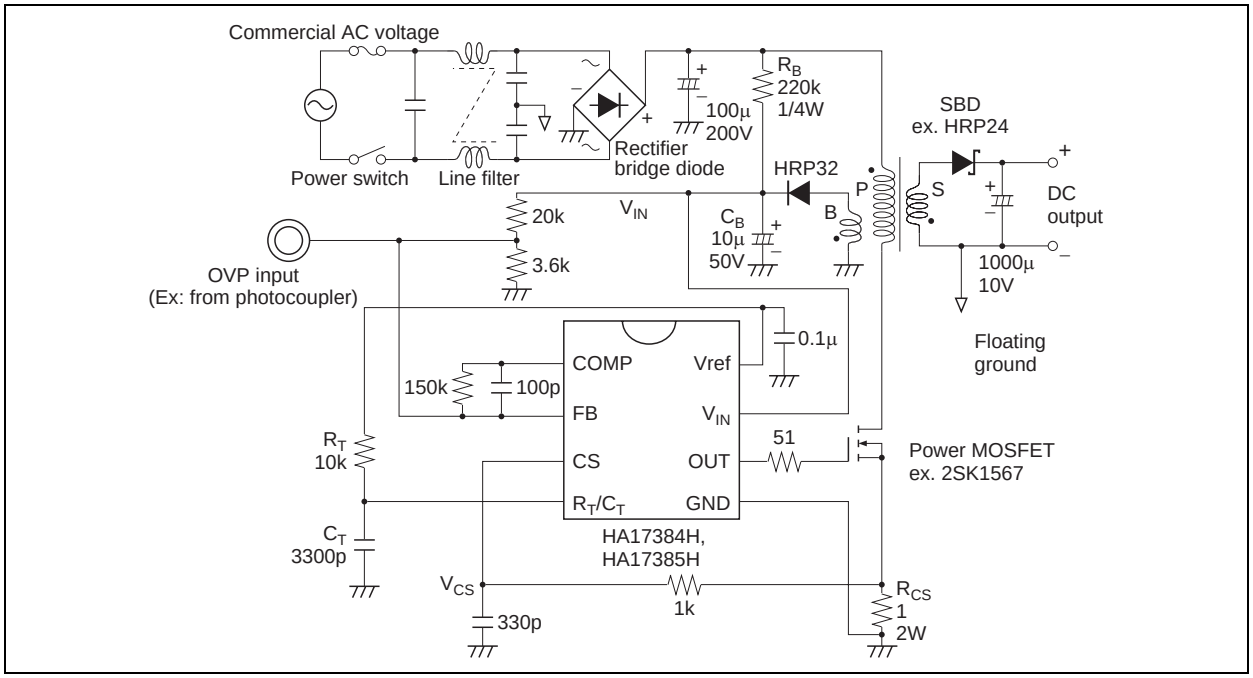


Figure 2 Mounting Circut Diagram for Operation Expression

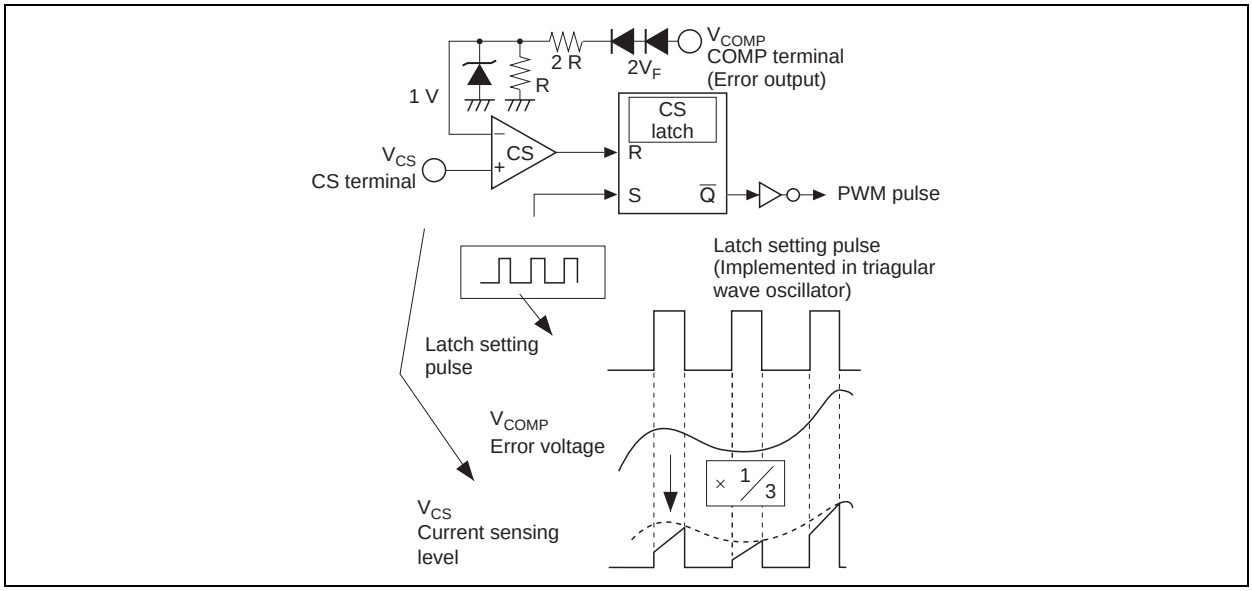


Figure 3 Operation Diagram of Current Sensing Part

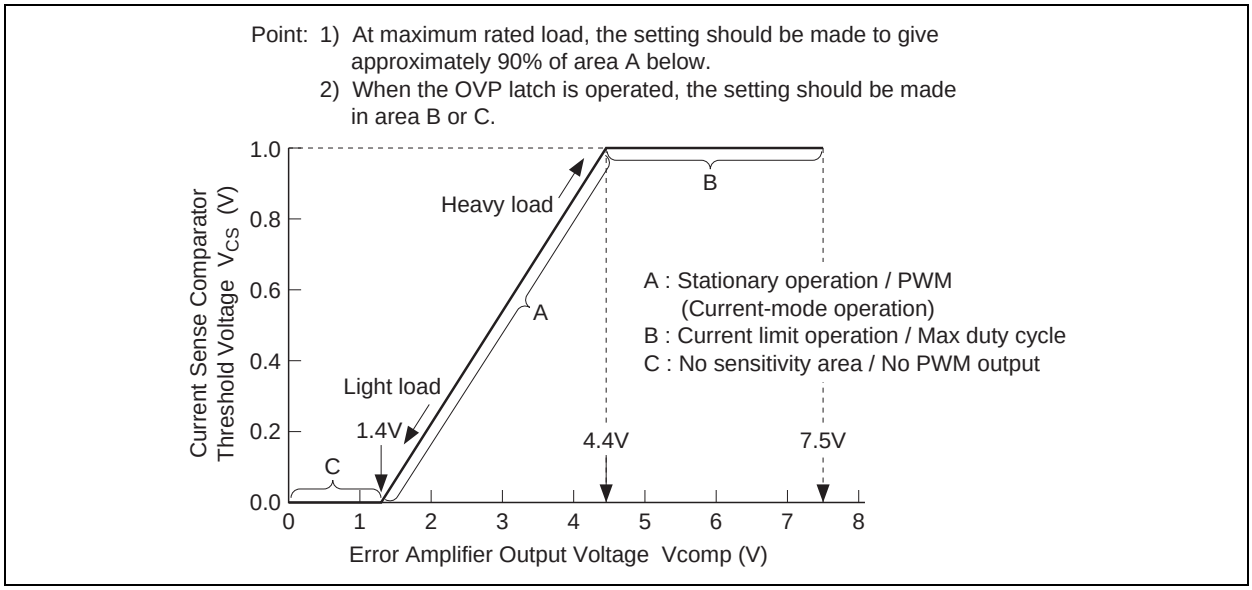


Figure 4 Current Sense Characteristics

Features and Theory of Current Mode Control

Features of Current Mode Control

- Switch element current detection is performed every cycle, giving a high feedback response speed.
- Operation with a constant transformer winding current gives a highly stable output voltage (with excellent line regulation characteristics, in particular).
- Suitable for flyback transformer use.
- External synchronous operation is easily achieved. (This feature, for example, is applicable to synchronization with a forizontal synchronizing signal of CRT monitor.)

Theory of Current Mode Control

In current mode control, a PWM pulse is generated not by comparing an error voltage with a triangular wave voltage in the voltage mode, but by changing the current limiter level in accordance with the error voltage (COMP terminal in this IC, that is,output of the error amplifier output) which is obtained by constantly monitoring the current of the switching device (power MOS FET) using source resistor R_{CS}.

One of the features of current mode control is that the current limited operates in all cycles of PWM as described by the above theory.

In voltage mode, only one feedback loop is made by an output voltage. In current mode, on the other hand, two loops are used. One is an output voltage loop and the other is a loop of the switching device current itself. The current of the switching device can be controlled switch high speed. In current mode control, the current in the transformer winding is kept constant, resulting in high stability. An important consequence is that the line regulation in terms of total characteristics is better than that in voltage mode.

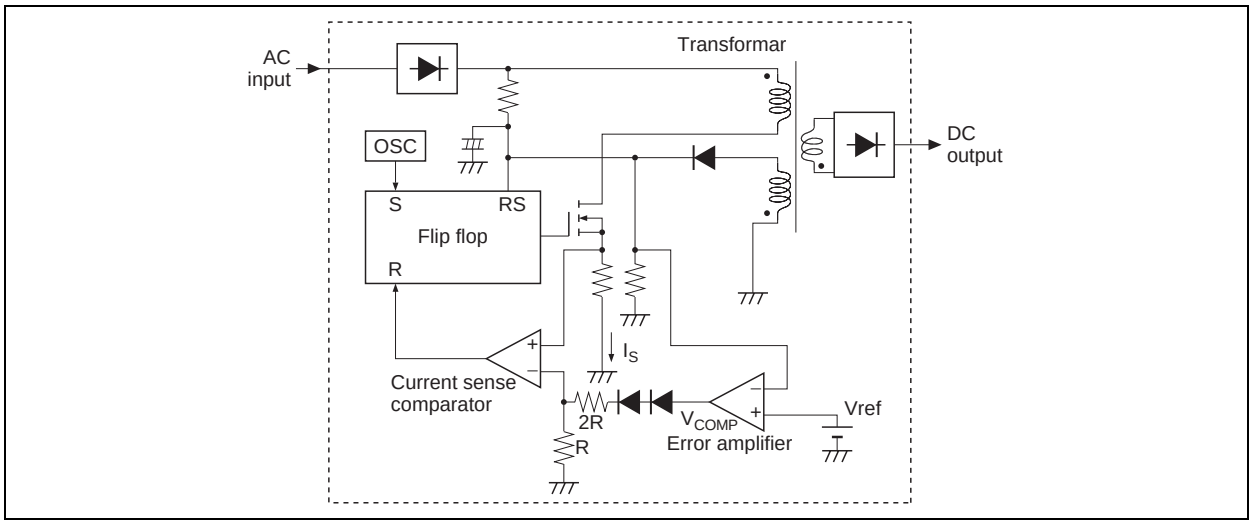
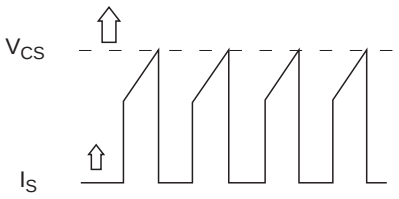
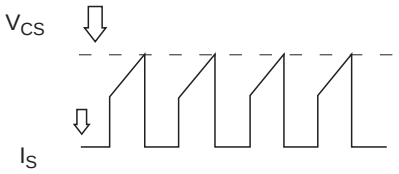


Figure 5 Block Diagram of Current Mode Switching Power Spply

A. Control in the case of heavy load



B. Control in the case of light load

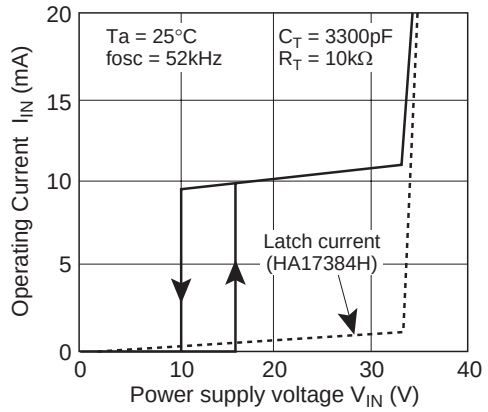


As the load becomes heavy and the DC output decreases, the current sensing level is raised as shown in A. above in order to increase the current in the switching device in each cycle. When the load decreases, inverse control is carried out as shown in B. above.

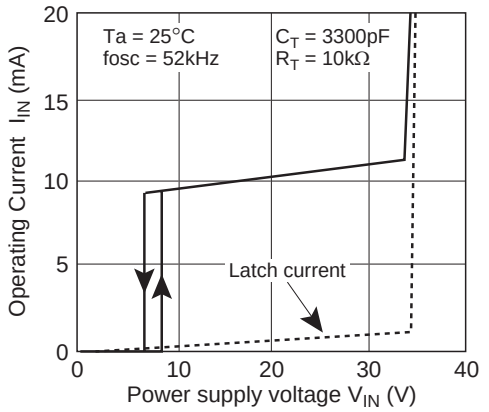
Figure 6 Primary Current Control of Transformer in Current Mode (Conceptual Diagram)

Main Characteristics

Supply Current vs. Supply Voltage (HA17384S/H)

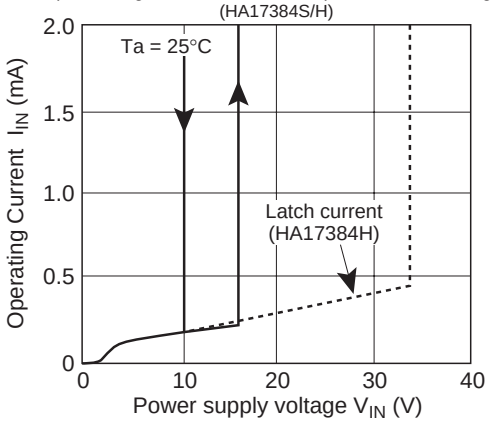


Supply Current vs. Supply Voltage (HA17385H)



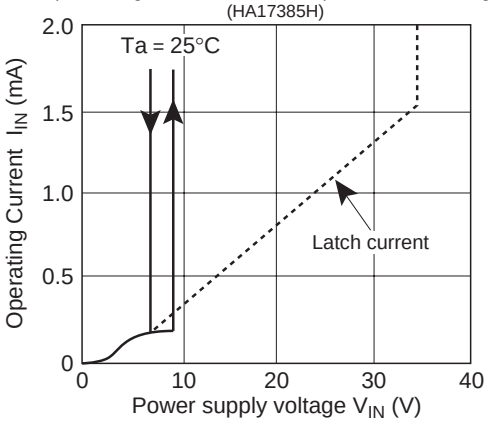
Standby Current/Latch Current vs. Supply Voltage

Exploded diagram of the small current part from the above figure (HA17384S/H)

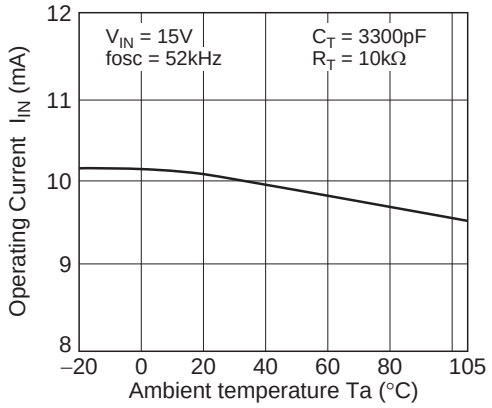


Standby Current/Latch Current vs. Supply Voltage

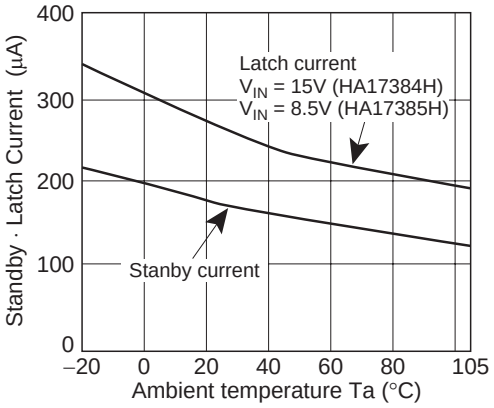
Exploded diagram of the small current part from the above figure (HA17385H)



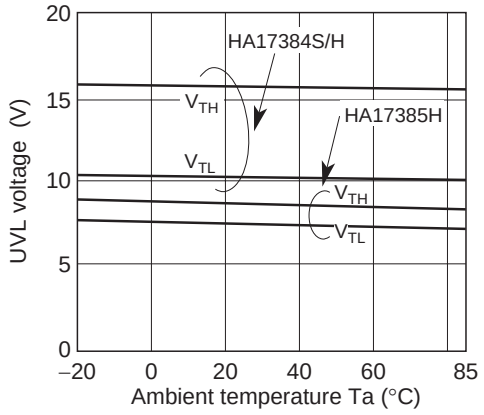
Operating Current vs. Ambient Temperature



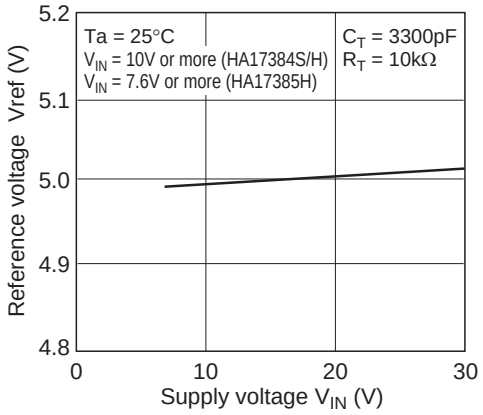
Standby Current/Latch Current vs. Ambient Temperature



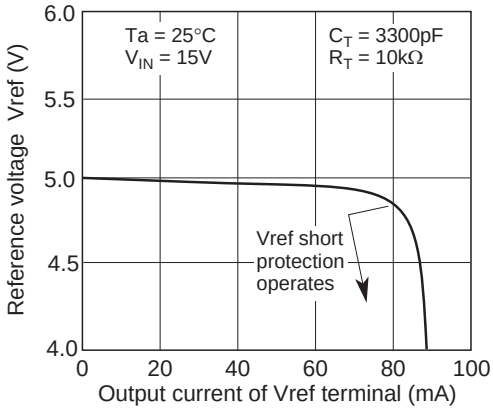
UVL Threshold Voltage vs. Ambient Temperature



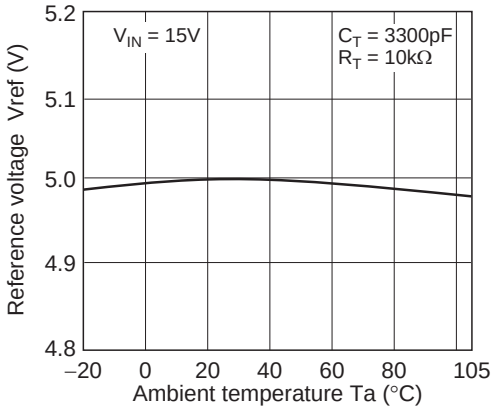
Line Regulation Characteristics of Reference Voltage



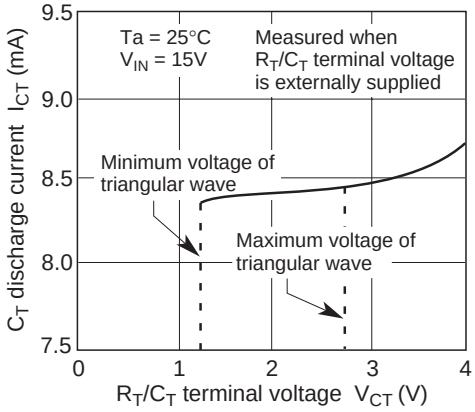
Load Regulation Characteristics of Reference Voltage



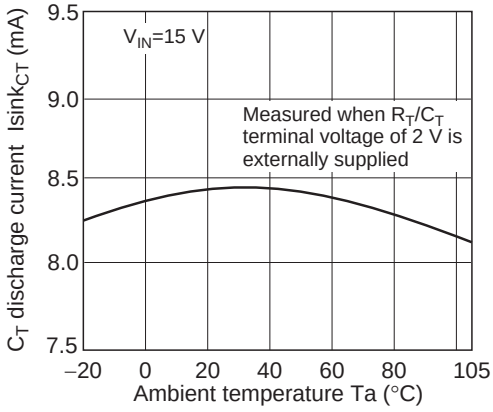
Reference Voltage vs. Ambient Temperature



C_T Discharge Current vs. R_T/C_T Terminal Voltage



C_T Discharge Current vs. Ambient Temperature



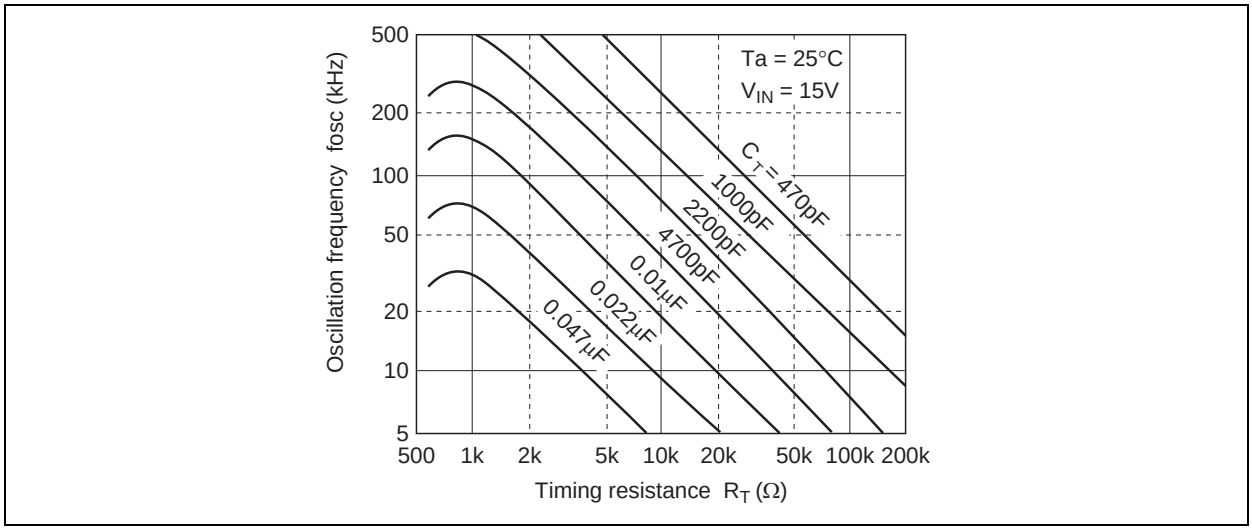


Figure 7 scillation Frequency vs. Timing Resistance

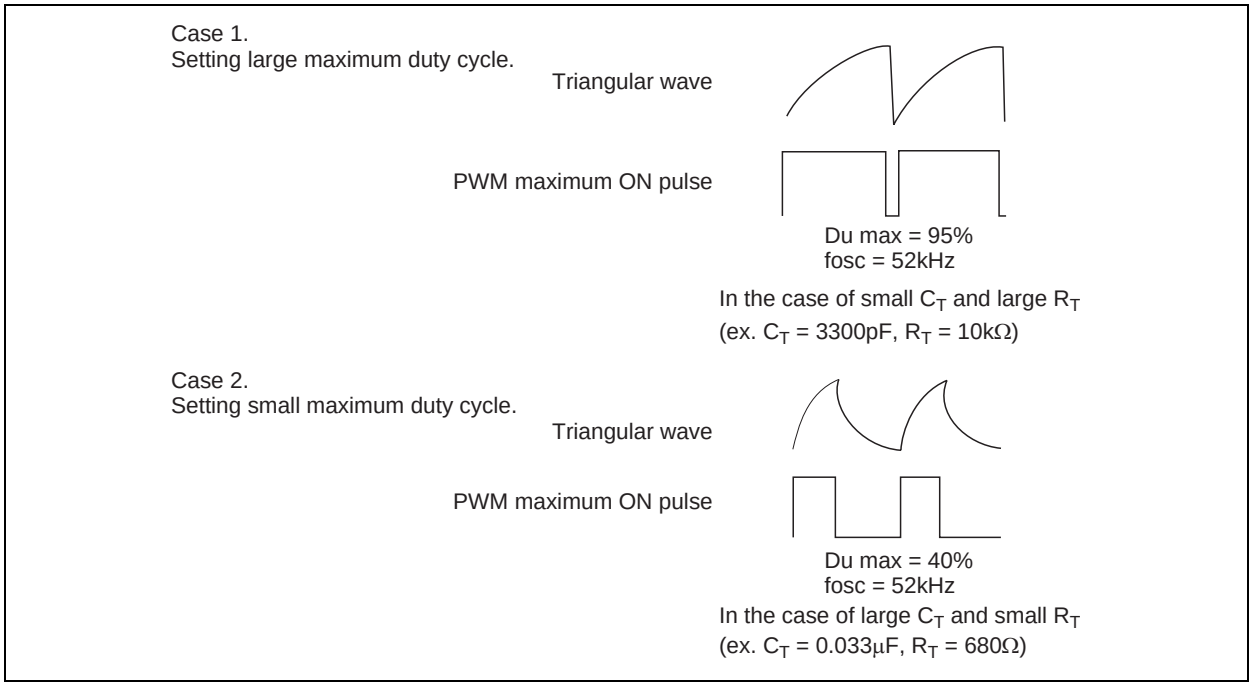
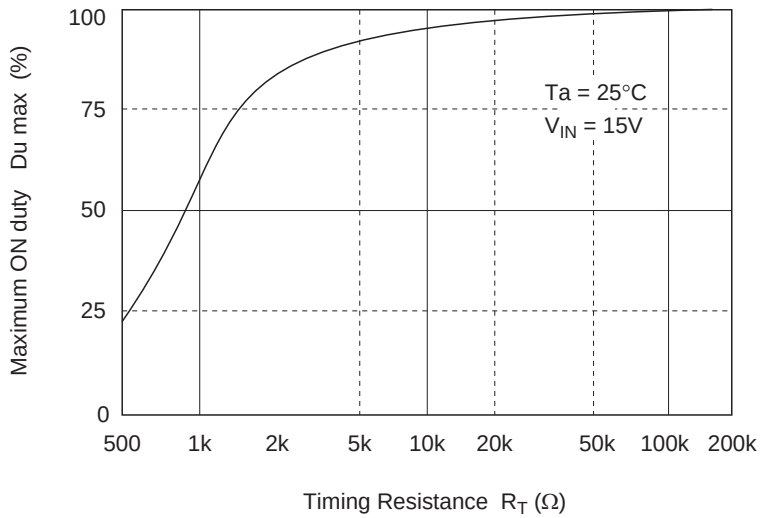


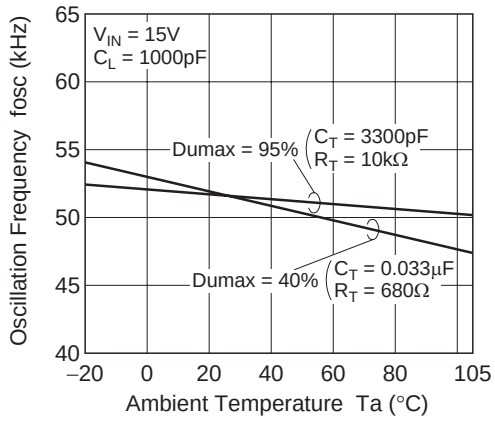
Figure 8 Relationship Between Triangular Wave and Maximum ON Duty of PWM Pulse



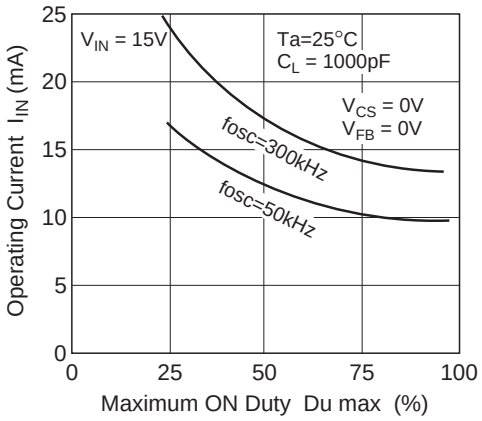
Note: In the oscillation system of this IC, a constant discharging current of 8.4mA flows the timing capacitor during triangular wave fall. Therefore, note that a small maximum ON duty (large dead band) leads to a large supply current. Refer to the equations of oscillation frequency and supply current for details.

Figure 9 PWM Pulse ON Duty vs. Timing Resistance

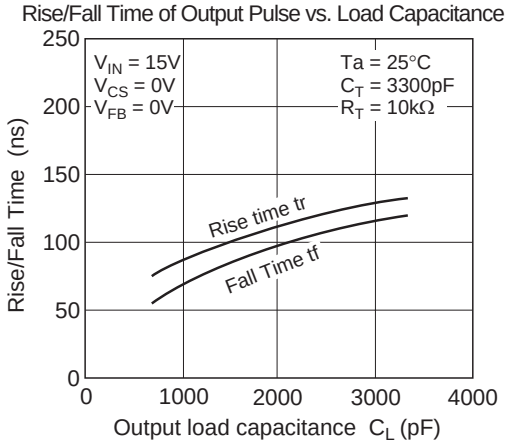
Oscillation Frequency vs. Ambient Temperature



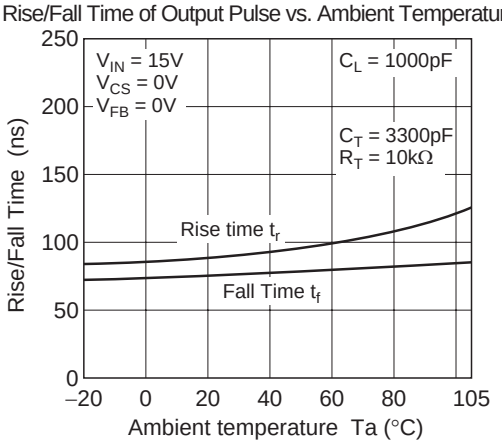
Operating Current vs. Maximum ON Duty



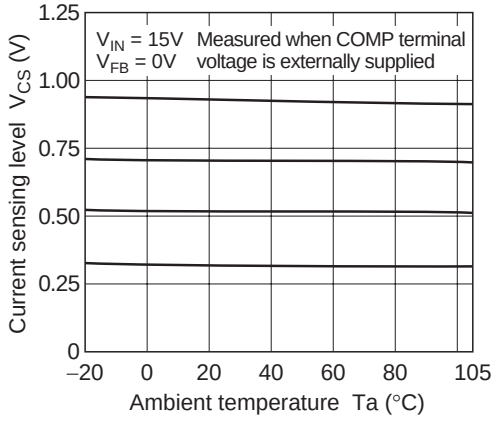
Rise/Fall Time of Output Pulse vs. Load Capacitance



Rise/Fall Time of Output Pulse vs. Ambient Temperature



Current Sensing Level vs. Ambient Temperature



Relationship Between Low Voltage Malfunction Protection and PWM Output

V_{IN} (UVL1)	L	H	H	L
Vref (UVL2)	L	L	H	H
PWM OUTPUT	L	L	Available to output	L
Condition description	Standby state	IC is in the ON state and output is fixed to LO.	Operation state	Standby state

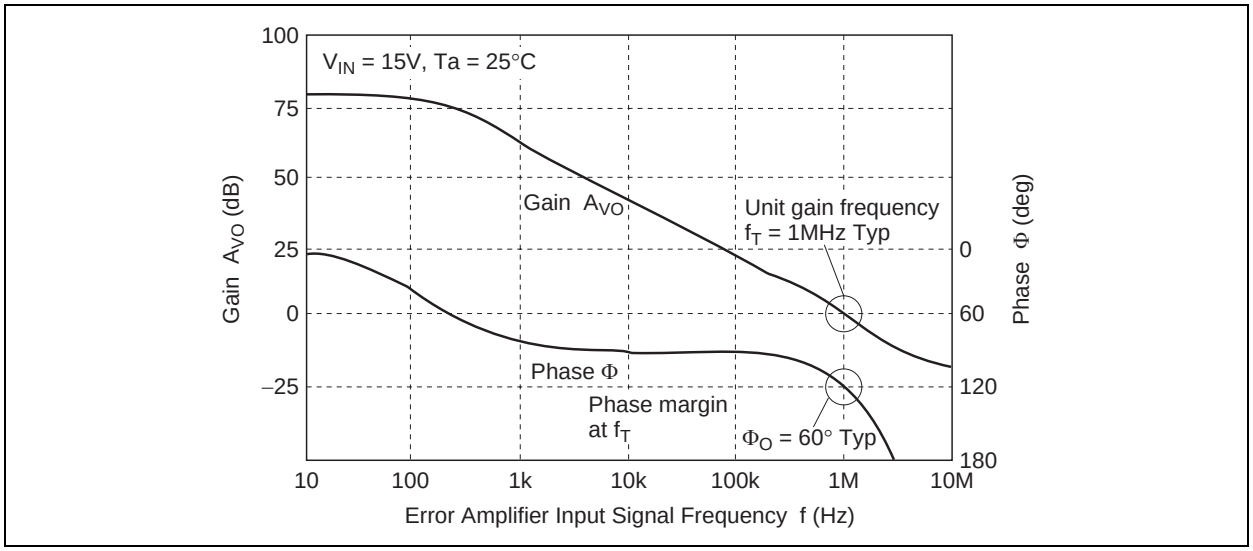


Figure 10 Open Loop Gain Characterisrics of Error Amplifier

● Calculation of operation parameters

1. Maximum ON duty Du max (Refer to the right figure.)

$$\text{Du max} = \frac{1}{1 + 1.78 \times \ln\left(1 + \frac{190\Omega}{R_T - 440\Omega}\right)}$$

2. Oscillation frequency fosc

$$\text{fosc} = \frac{1}{C_T \times R_T \times \left\{0.56 + \ln\left(1 + \frac{190\Omega}{R_T - 440\Omega}\right)\right\}}$$

From the above two equations, the following two equations are obtained.

3. Equalization to device R_T from Du max

$$R_T = \frac{190\Omega}{e^{0.56\,(1/\text{Du max} - 1)} - 1} + 440\Omega$$

(e = 2.71828.base of natural logarithm)

4. Equation to device C_T from fosc and R_T

$$C_T = 1.78 \times \frac{\text{Du max}}{\text{fosc} \times R_T}$$

5. Operating current I_{IN}

$I_{IN} = I_Q + \text{Isink}_{CT} \times (1 - \text{Du max}) + \text{Ciss} \times V_{IN} \times \text{fosc}$

providing that I_Q = 8.4mA Typ (Supply current when oscillation in IC stops.)
Ciss is the input gate capacitance of the power MOSFET which is connected and V_{IN} is the supply voltage of the IC.

Example 1: Calculation when R_T = 10kΩ and C_T = 3300pF
fosc = 52kHz, Du max = 95%, I_{IN} = 9.7mA

Example 2: Calculation for 50% of Du max and 200 kHz of fosc
R_T = 693Ω, C_T = 6360pF, I_{IN} = 12.5mA
However, Ciss = 1000pF, V_{IN} = 18V

Note that the actual value may differ from the calculated one because of the internal delay in operation and input characteristics of the POWER MOS FET. Check the value when mounting.
Additionally a small Dumax leads to a large supply current, even if the frequency is not changed, and start up may become difficult. In such a case, the following measure is recommended.

(1) For an AC/DC converter, a small bleeder resistance is required.
(2) The large capacitance between Vref and GND is required.
(3) Use a large Dumax with a triangular wave and raise the current limit of the switching device to around the maximum value (1.0V Typ).

The current limit is expressed as $\text{IDmax} = \frac{V_{THCS}}{R_{CS}}$

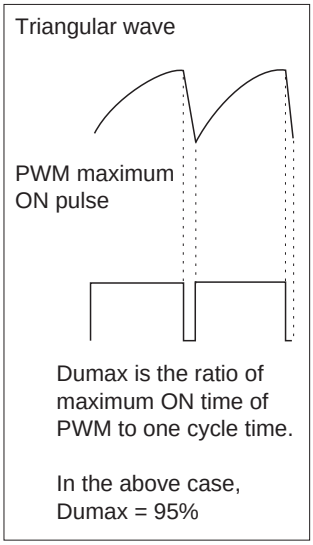
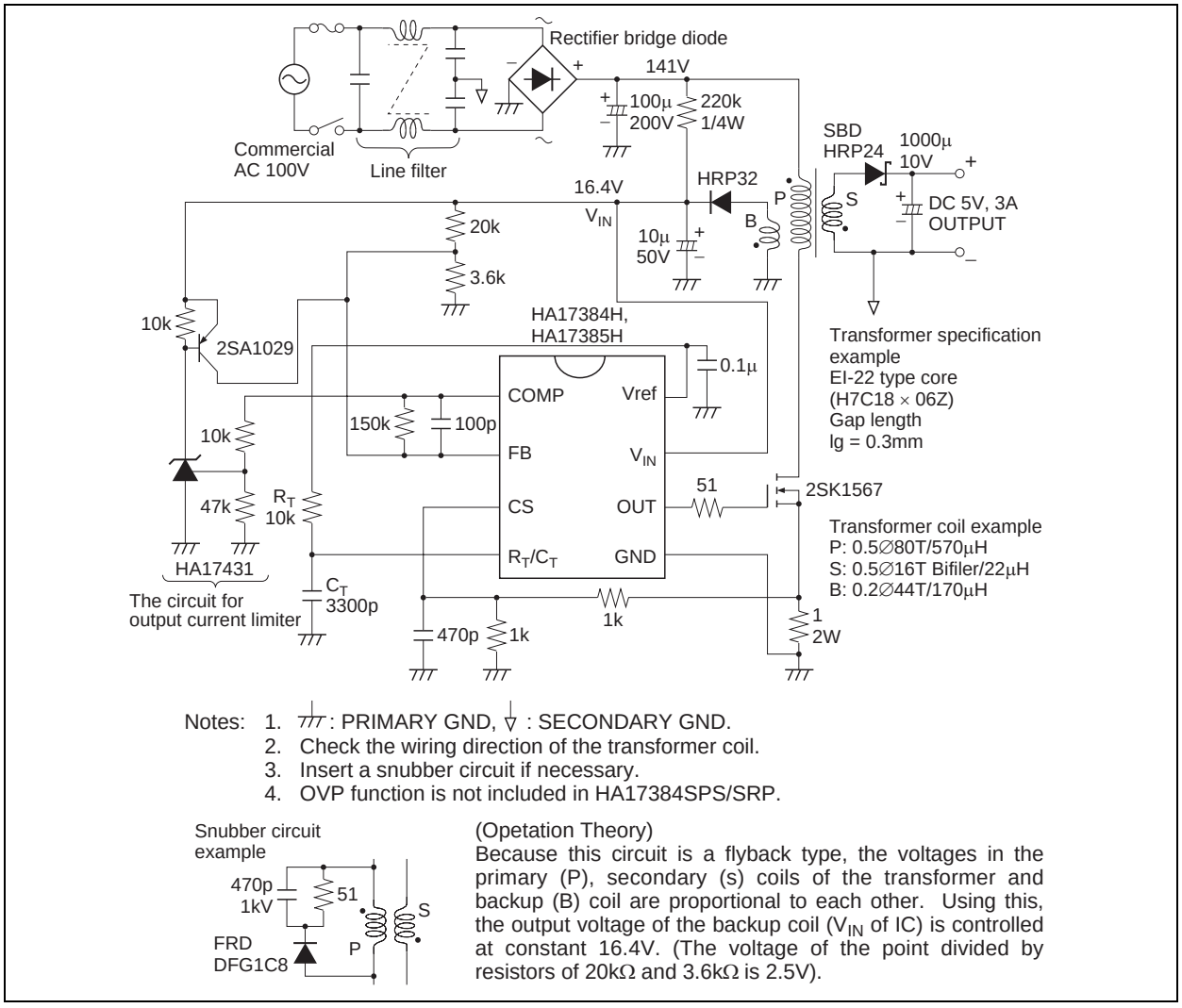


Figure 11 Calculation of Operation Parameters

Application Circuit Example (1)



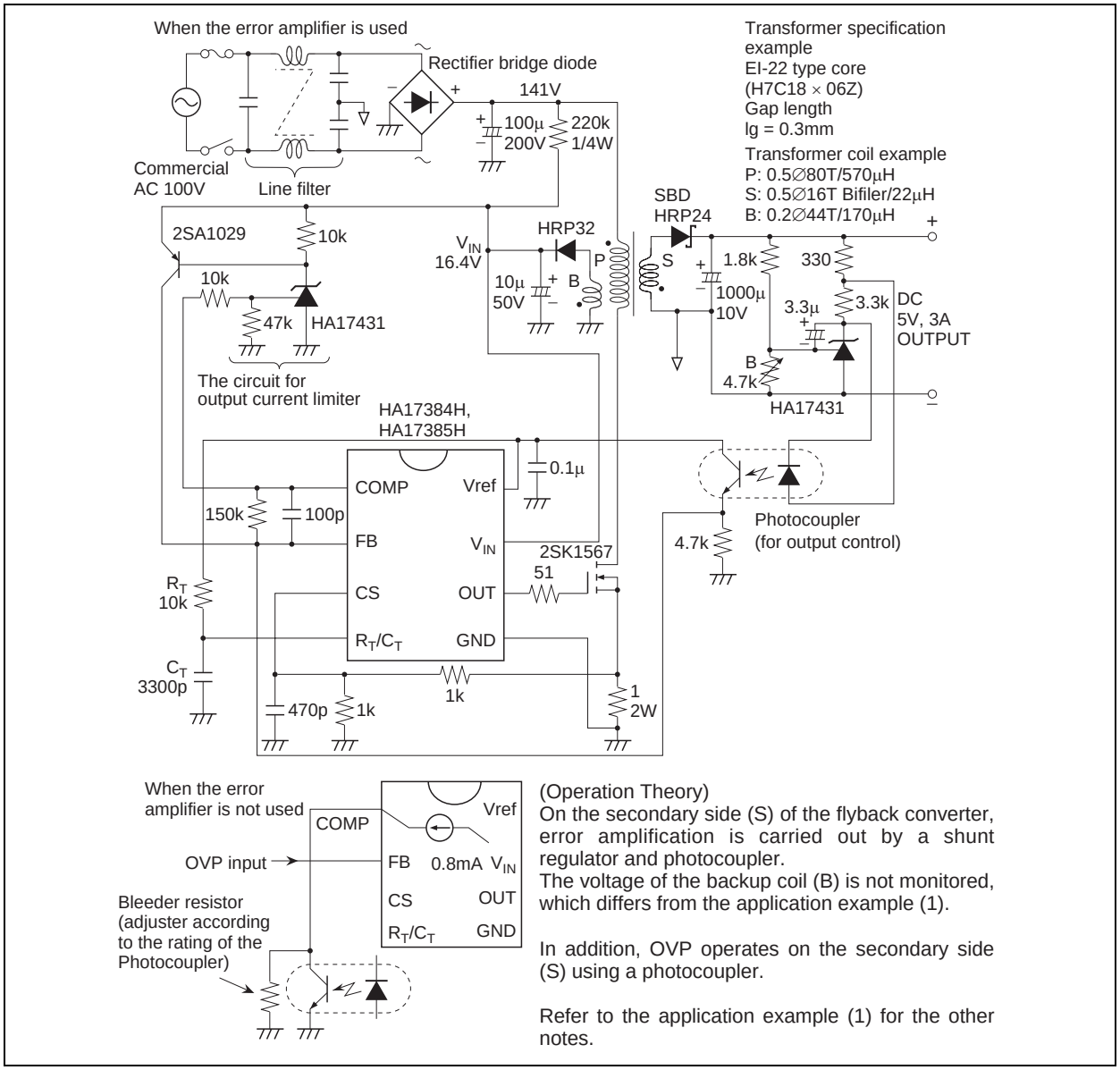
Notes: 1. ⏚: PRIMARY GND, ▽ : SECONDARY GND.
2. Check the wiring direction of the transformer coil.
3. Insert a snubber circuit if necessary.
4. OVP function is not included in HA17384SPS/SRP.

Snubber circuit
example

(Opetation Theory)
Because this circuit is a flyback type, the voltages in the primary (P), secondary (s) coils of the transformer and backup (B) coil are proportional to each other. Using this, the output voltage of the backup coil (V_{IN} of IC) is controlled at constant 16.4V. (The voltage of the point divided by resistors of 20kΩ and 3.6kΩ is 2.5V).

Figure 12 Primary Voltage Sensing Flyback Converter

Application Circuit Example (2)



(Operation Theory)
On the secondary side (S) of the flyback converter, error amplification is carried out by a shunt regulator and photocoupler.
The voltage of the backup coil (B) is not monitored, which differs from the application example (1).

In addition, OVP operates on the secondary side (S) using a photocoupler.

Refer to the application example (1) for the other notes.

Figure 13 Secondary Voltage Sensing Flyback Converter

Application Examples for Fuller Exploitation of Power Supply Functions

A number of application examples are briefly described below.

1. Soft start

   A soft start is a start method in which the PWM pulse width is gradually increased when the power supply is activated. This prevents the stress on the transformer and switch element caused by a rapid increase in the PWM pulse width, and also prevents overshoot when the secondary-side output voltage rises. The circuit diagram is shown in figure 14.

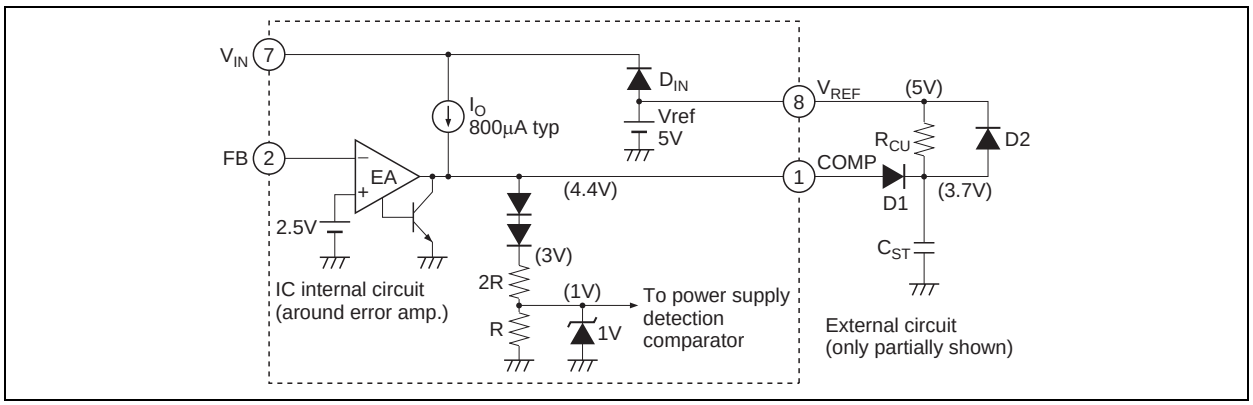


Figure 14 Circuit Diagram for Soft Start

Operation: In this circuit, error amp output source current I_O (800 µA typ.) gradually raises the switch element current detection level, using a voltage slope that charges soft start capacitance C_{ST}. When the voltage at each node is at the value shown in parentheses in the figure, the soft start ends. The soft start time is thus given by the following formula:

$$T_{ST} = (3.7\ V/800\ \mu A) \times C_{ST} \approx 4.62\ C_{ST}\ (ms)$$

(C_{ST} unit: µF)

External parts other than C_{ST} operate as follows:

— Diode D1 : Current detection level shift and current reverse-flow prevention.
— Diode D2 : Together with diode D_{IN} in the IC, C_{ST} charge drawing when power supply falls.
— Resistance R_{CU} : For C_{ST} charge-up at end of soft start. (Use a high resistance of the order of several hundred kΩ.)

Note: During a soft start, since PWM pulses are not output for a while after the IC starts operating, there is a lack of energy during this time, and intermittent mode may be entered. In this case, the capacitance between Vref and GND should be increased to around 4.7 µF to 10 µF.

Notice for Use

OVP Latch Block

- Case
  When DC power is applied directly as the power supply of the HA17384H, HA17385H, without using the transformer backup coil. Also, when high-frequency noise is superimposed on the V_{IN} pin.
- Problem
  The IC may not be turn on in the case of a circuit in which V_{IN} rises quickly (10 V/100 µs or faster), such as that shown in figure 15. Also, the OVP latch may operate even though the FB pin is normally at V_{OVP} or below after the IC is activated.
- Reason
  Because of the IC circuit configuration, the timer latch block operates first.
- Remedy (counter measure)
  Take remedial action such as configuring a time constant circuit (R_B, C_B) as shown in figure 16, to keep the V_{IN} rise speed below 10 V/100 µs. Also, if there is marked high-frequency noise on the V_{IN} pin, a noise cancellation capacitor (C_N) with the best possible high-frequency characteristics (such as a ceramic capacitor) should be inserted between the V_{IN} pin and GND, and close to the V_{IN} pin.

When configuring an IC power supply with an activation resistance and backup winding, such as an AC/DC converter, the rise of V_{IN} will normally be around 1 V/100 µs, and there is no risk of this problem occurring, but careful attention must be paid to high-frequency noise.

Also, this phenomenon is not occuring to the HA17384S, because OVP function is not built-in.

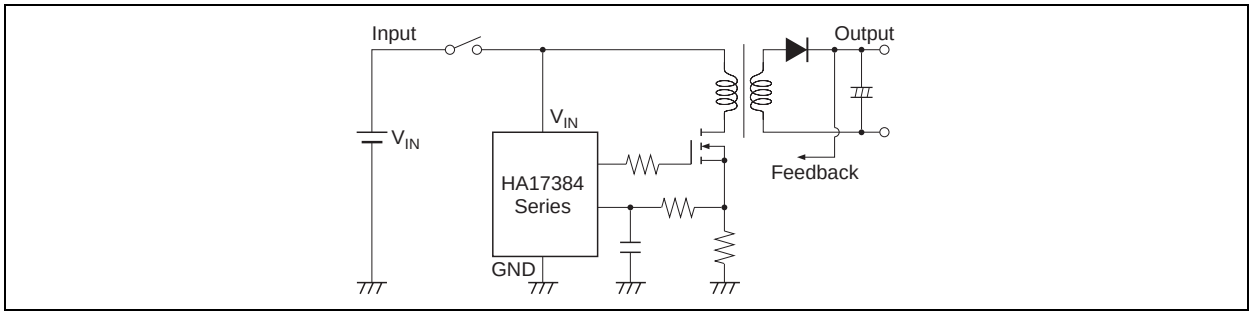


Figure 15 Example of Circuit with Fast V_{IN} Rise Time

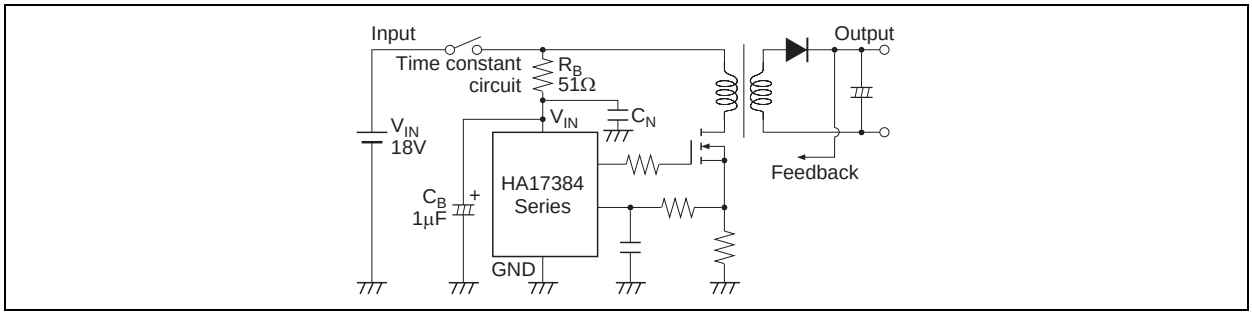


Figure 16 Sample Remedial Circuit

Externally Synchronized Operation

- Case
  When, with a power supply using the HA17384S/H or HA17385H, externally synchronized operation is performed by applying an external syncronous signal to the R_T/C_T pin (pin 4).
- Problem
  Synchronized operation may not be possible if the amplitude of the external syncronous signal is too large.
- Reason
  The R_T/C_T pin falls to a potential lower than the ground.
- Remedy (counter measure)
  In this case, clamping is necessary using a diode with as small a V_F value as possible, such as a schottky barrier diode, as shown in figure 17.

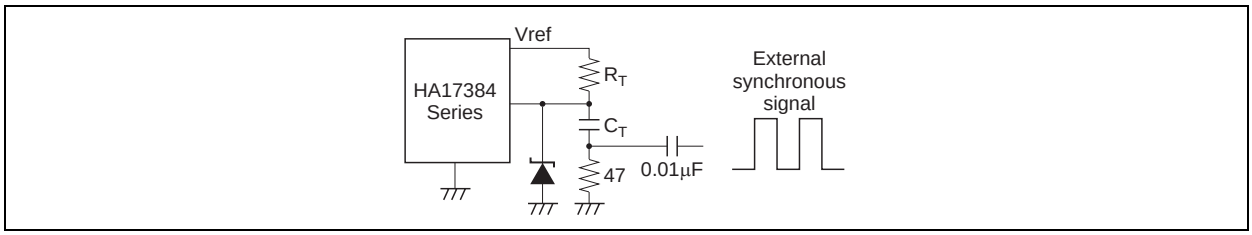
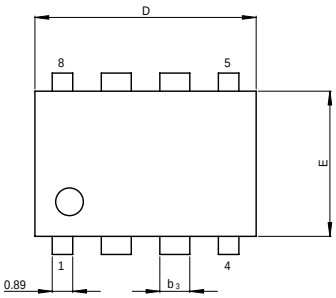
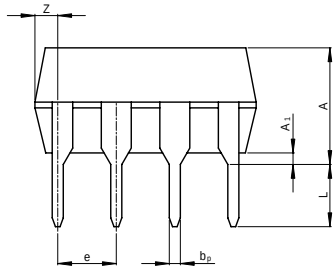


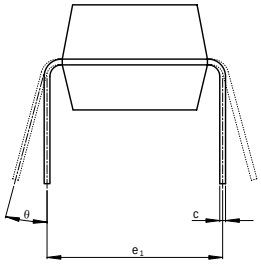
Figure 17 Sample Remedial Circuit

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP8-6.3x9.6-2.54	PRDP0008AF-A	DP-8B	0.51g

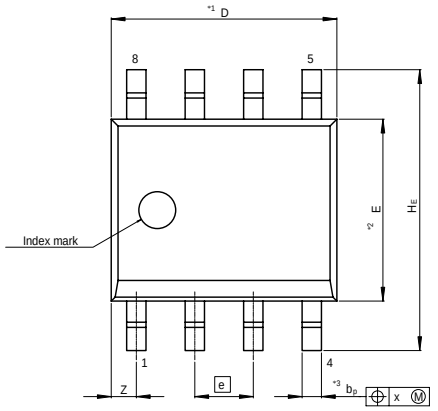


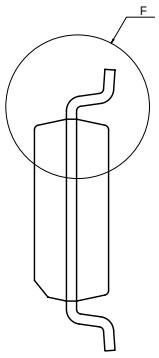




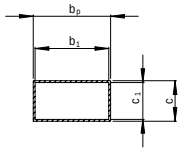
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e 1	——	7.62	——
D	——	9.6	10.6
E	——	6.3	7.4
A	——	——	5.06
A 1	0.5	——	——
b p	0.38	0.48	0.58
b 3	——	1.3	——
c	0.20	0.25	0.35
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	1.27
L	2.54	——	——

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-3.95x4.9-1.27	PRSP0008DD-B	FP-8DC	0.085g

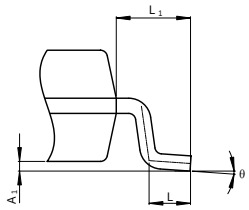




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	4.90	5.30
E	——	3.95	——
A 2	——	——	——
A 1	0.10	0.14	0.25
A	——	——	1.75
b p	0.34	0.42	0.50
b 1	——	0.40	——
c	0.19	0.22	0.25
c 1	——	0.20	——
θ	0°	——	8°
H E	5.80	6.10	6.20
e	——	1.27	——
x	——	——	0.25
y	——	——	0.10
Z	——	——	0.75
L	0.40	0.60	1.27
L 1	——	1.08	——

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