

## PCI EVALUATION BOARD FOR BCM1250

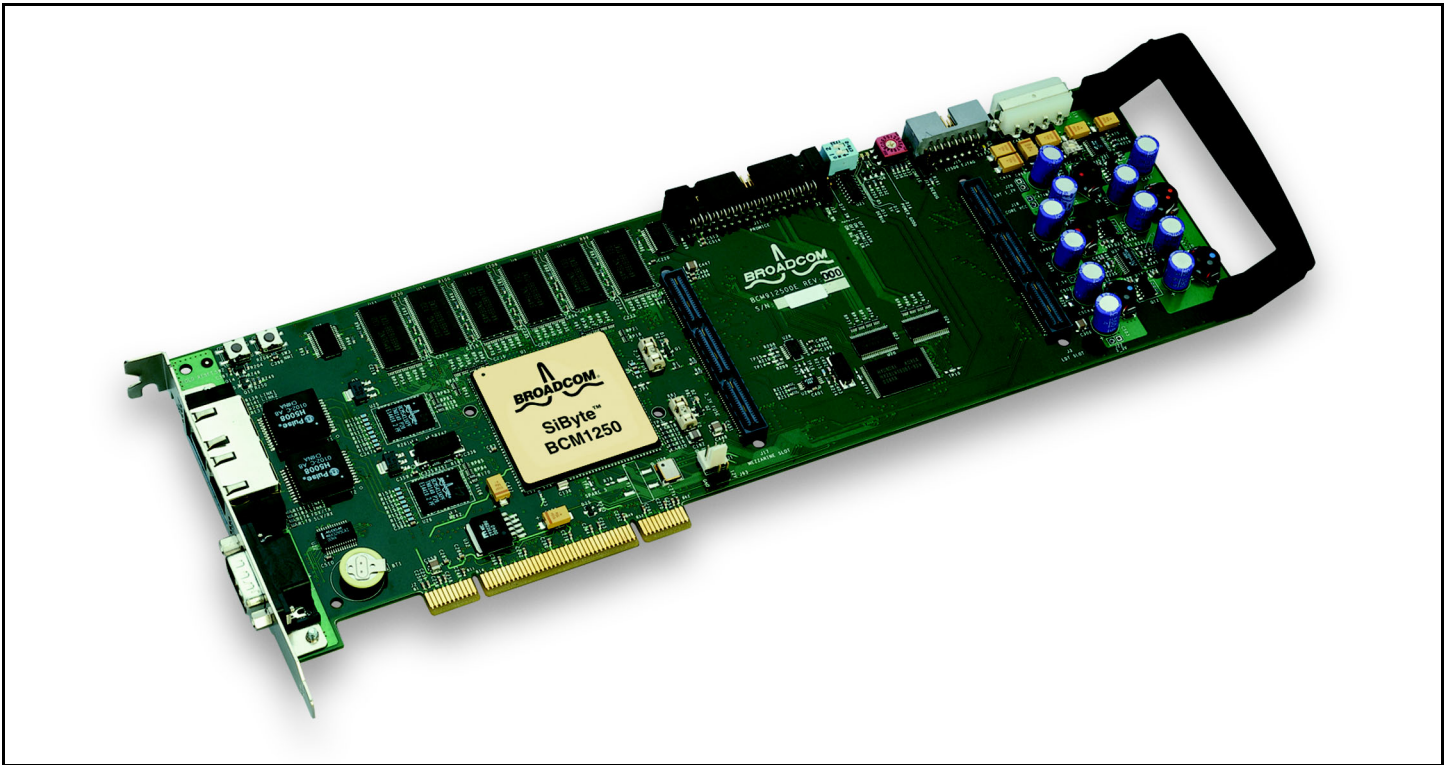
### FEATURES

- **BCM1250 System-on-a-Chip (SOC)**
  - Dual 64-bit MIPS processors running at current sampling speed
  - 32-KB instruction and 32-KB data cache
  - 512K L2 cache
- **Soldered-down 256-MB DDR SDRAM**
- **32-bit, 33/66-MHz, full-length PCI form factor**
  - Configured as PCI target device
  - Operable with 3.3V or 5V PCI interface
- **Two Gigabit Ethernet ports on I/O bracket**
  - 10/100/1000BASE-T on standard CAT 5 UTP cable
  - 802.3 compliant
  - Status LEDs showing link status and activity

### SUMMARY OF BENEFITS

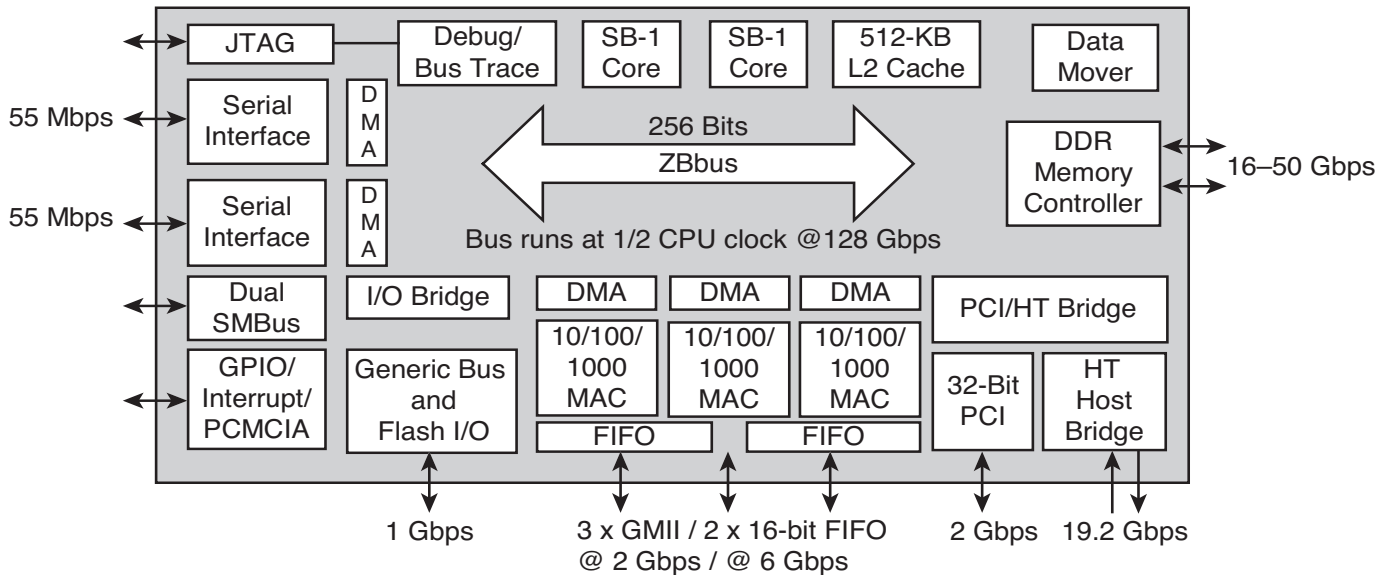
- **One serial port on I/O bracket**
  - Configured as a standard asynchronous UART with RS232 interface
- **One HyperTransport™ connector**
  - Supports HyperTransport™, SMBus, and generic bus signals
- **One Mezzanine socket**
  - Supports GMII, serial bus, generic bus and GPIO signals
- **Standard 4-pin disk drive power connector for stand-alone operation**
- **PROMICE connector for code testing and development**
- **EJTAG header for BCM1250 debug and test**
- **For additional information on the BCM1250 processor, refer to the BCM1250 product brief.**

### BCM91250E PCI Evaluation Board



# OVERVIEW

BCM1250 Block Diagram



## Product Overview

The **BCM91250E** is a full-length PCI evaluation board with the SiByte™ BCM1250 dual processor SOC. The board is designed for software development and for developing PCI applications which require high-performance processors. The **BCM91250E** can be plugged into a PCI slot in any PC, workstation, or server or can be used as a stand-alone device.

The **BCM91250E** comes with 256 MB of DDR SDRAM soldered down, two Gigabit Ethernet ports for network connectivity, a HyperTransport™ (formerly LDT) connector, and a Mezzanine socket for connection to daughter cards. Daughter cards can access HyperTransport, GMII, serial bus, SMBus, generic bus, and GPIO signals from the board by connecting to the appropriate sockets.

For more information on the BCM1250, refer to the BCM1250 product brief.

## Firmware

The **BCM91250E** board is provided with the Common Firmware Environment (CFE), which supports 32-bit and 64-bit operation. The CFE solution initializes the CPUs and the peripherals on the BCM1250, including the L2 cache, memory controller, Ethernet MACs, and UARTs. It also configures the HyperTransport fabric. CFE provides an environment for downloading and booting an Operating System using a disk, flash memory, the network, or the host as its boot device.

## Operating System Support

Two operating systems are provided for the BCM91250E:

- VxWorks® version 5.4 with 64-bit support for data. VxMPTM, a VxWorks kernel running independently on each core, is an available option. Developers need to use the Tornado® tools version 2.1 for 64-bit or VxMPTM support. The BSP for BCM91250E in source form is available initially only from Broadcom.
- Linux® version 2.4 running in 32-bit mode with full SMP support. Full source code is available from the MIPS-Linux repository (<http://oss.sgi.com/mips/downloads.html>), with full support by MontaVista ([www.mvista.com](http://www.mvista.com)).

## Development Tools

Broadcom supports the GNU toolchain. The toolchain is based on version 3.0 of the compiler, revision 2.11 of binutils and supports cross compilation from x86/Linux and SPARC/Solaris™ systems.

Broadcom has partnered with Corelis to provide debugging access through the BCM1250 EJTAG port. There are two EJTAG probe solutions:

- PICE-BCM1250 is a medium-performance probe that connects to the parallel port on a PC.
- NetICE-BCM1250 is a high-performance probe that connects over the Ethernet.

Corelis provides a powerful source-level GUI debugger that works with both probes. This is adapted for the BCM1250 and allows the registers of the internal peripherals to be examined easily.

In addition, Broadcom has enhanced the GNU debugger (GDB) to use the Corelis EJTAG probes and enable multi-CPU debugging.

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