



**ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ\text{C}$ )**

Supply Voltage	$V_{CC}$	-0.5 to +6.0	V
Input Voltage	$V_I$	-0.5 to $+V_{CC} + 0.3$	V
Output Current	$I_o$	-10	mA
Junction Temperature	$T_j$	+125	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +125	$^\circ\text{C}$

**RECOMMENDED OPERATING CONDITIONS**

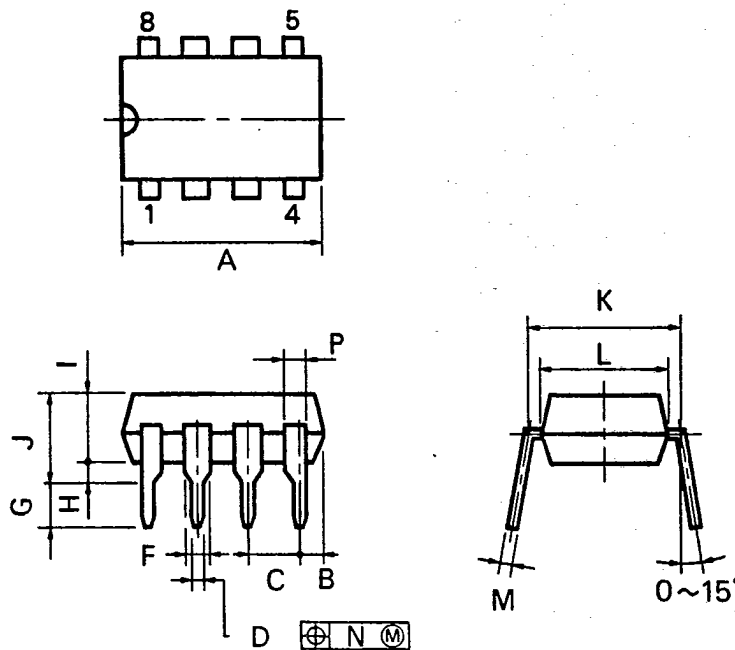
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Output Load Capacitance	$C_L$			30	pF
Ambient Temperature	$T_a$	-30		+75	$^\circ\text{C}$

**ELECTRIC CHARACTERISTICS ( $V_{CC} = 5.0 \pm 0.5\text{ V}$ ,  $T_a = -30$  to  $+75^\circ\text{C}$ )**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power Supply Current	$I_{CC}$		43	53.5	mA	$V_{CC}=5\text{V}$ , $T_a=25^\circ\text{C}$
Output Voltage	$V_O$	0.4	0.6	0.8	V <sub>p.p</sub>	OUT pin, $C_L = 5\text{ pF}$
High Level Input Voltage	$V_{IH}$	2.0			V	M <sub>1</sub> , M <sub>2</sub> pin
Low Level Input Voltage	$V_{IL}$			0.8	V	M <sub>1</sub> , M <sub>2</sub> pin
High Level Input Current	$I_{IH}$			150	$\mu\text{A}$	M <sub>1</sub> , M <sub>2</sub> pin, $V_I = V_{CC}$
Low Level Input Current	$I_{IL}$	50			$\mu\text{A}$	M <sub>1</sub> , M <sub>2</sub> pin, $V_I = 0$
Input Voltage	$V_{in}$	60		1500	mV <sub>p.p</sub>	IN pin
Operating Frequency	$f_{in}$	90		1000	MHz	$V_{in} = 60\text{ mV}_{p.p} \div 4, \div 8, \div 64$
		90		500	MHz	$V_{in} = 60\text{ mV}_{p.p} \div 2$
		90		1150	MHz	$V_{in} = 120\text{ mV}_{p.p} \div 4, \div 8, \div 64$

PACKAGE DIMENSIONS

8PIN PLASTIC DIP (300 mil)



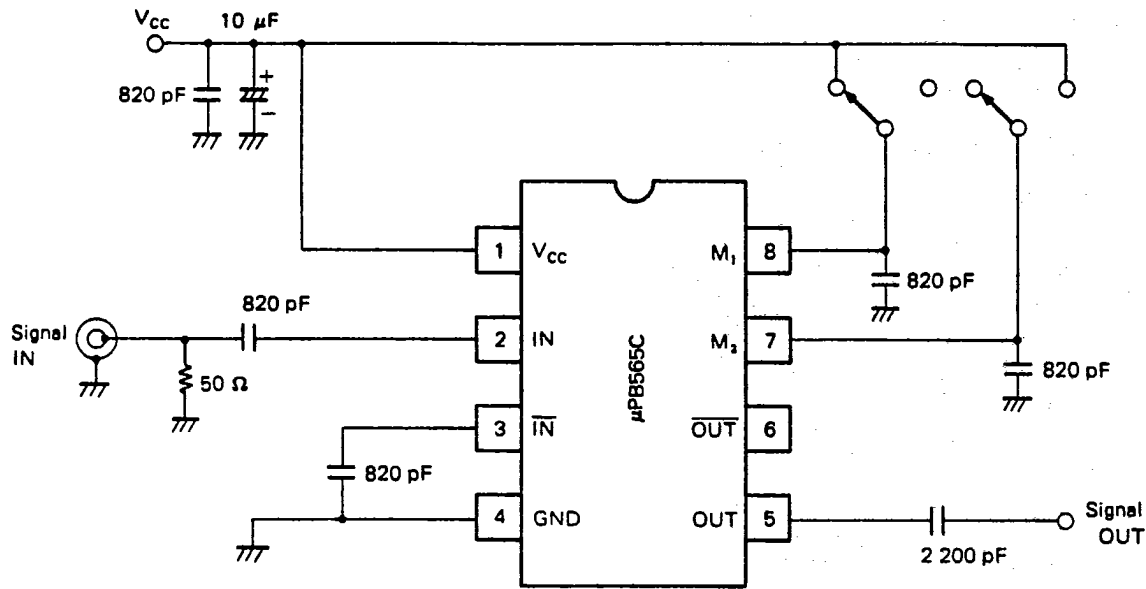
P8C-100-300A

NOTES

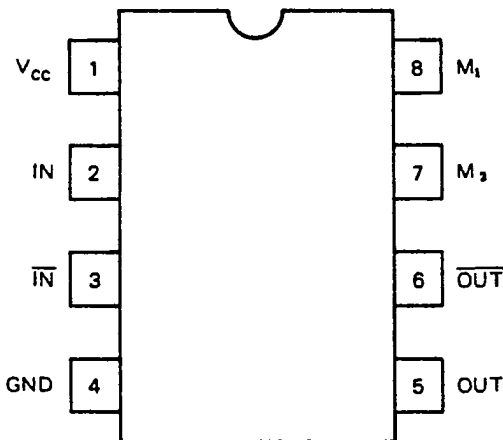
- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	10.16 MAX.	0.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 <sup>+0.10</sup>	0.020 <sup>+0.004</sup> / <sub>-0.005</sub>
F	1.4 MIN.	0.055 MIN.
G	2.9 <sup>+0.3</sup>	0.114
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	0.25 <sup>+0.10</sup> / <sub>-0.08</sub>	0.010 <sup>+0.004</sup> / <sub>-0.005</sub>
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.

TEST CIRCUIT



CONNECTION DIAGRAM (Top View)



- 1. V<sub>cc</sub> : Power Supply Pin (+5V)
- 2. IN : Signal Input Pin (Positive Logic)
- 3.  $\overline{IN}$  : Signal Input Pin (Negative Logic)
- 4. GND : GND Pin
- 5. OUT : Output Pin (Positive Logic)
- 6.  $\overline{OUT}$  : Output Pin (Negative Logic)
- 7. M<sub>2</sub> : Division Ratio Control
- 8. M<sub>1</sub> : Division Ratio Control

DIVISION RATIO CONTROL

M <sub>1</sub>	M <sub>2</sub>	Division Ratio
H	L	÷2
L	H	÷4
H	H	÷8
L	L	÷64

H : V<sub>cc</sub>  
L : OPEN

EXCLUSIVE AGENT FOR NEC Corporation RF & MICROWAVE SEMICONDUCTOR PRODUCTS—U.S. & CANADA

CALIFORNIA EASTERN LABORATORIES, INC. • Headquarters • 3260 Jay Street • Santa Clara, CA 95054 • (408) 988-3500 • Telex 34-6393/FAX (408) 988-0279