

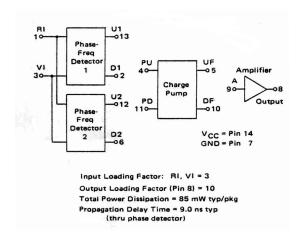
ML4344_4044 Phase Frequency Detector

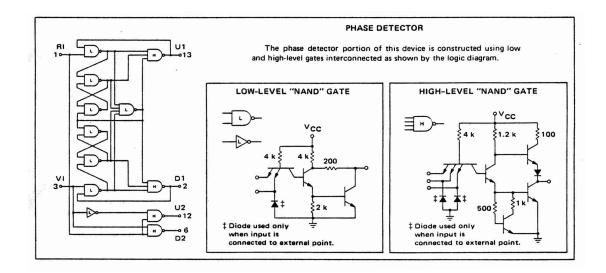
This device contains two digital phase detectors and a charge pump circuit which converts MTTL inputs to a dc voltage level for use in frequency discrimination and phase—locked—loop applications.

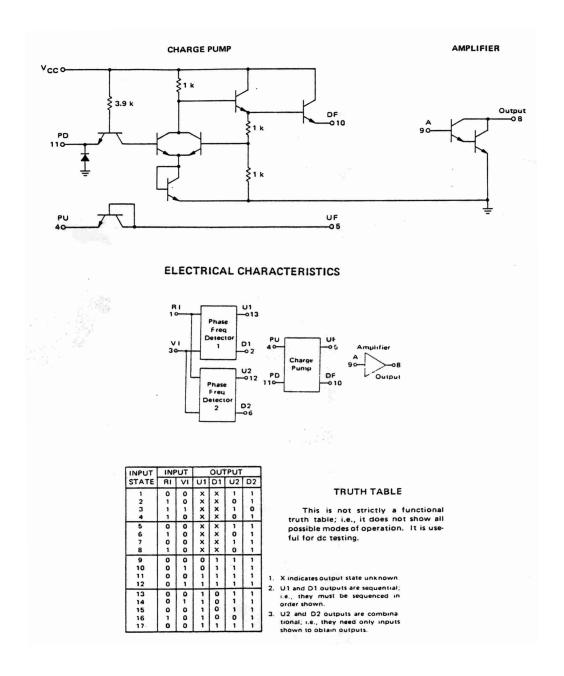
The two phase detectors have common inputs. Phase—frequency detector 1 is locked in (indicated by both outputs high) when the negative transitions of the variable input (V1) and reference input (R1) are equal in frequency and phase. If the variable input is lower in frequency or lags in phase, the U1 (up) output goes low; conversely the D1 (down) output goes low when the variable input is higher in frequency or leads the reference input in phase. It is important to note that the duty cycles of the variable input and the reference input are not important since negative transitions control system operation.

Phase detector 2, on the other hand, is locked in when the variable input phase lags the reference phase th 90° (indicated by the U2 and D2 outputs alternately going low with equal pulse widths). If the variable input phase lags by more than 90°, U2 will remain low longer than D2, and conversely, if the variable input phase lags the reference phase by less than 90°, D2 remains low longer. In this phase detector the variable input and the reference must have 50% duty cycles.

The charge pump accepts the phase detector outputs (U1 or U2 applied to PU, and D1 or D2 applied to PD) and converts them to fixed amplitude positive and negative pulses at the UF and DT outputs respectively. These pulses are applied to a lag-lead active filter, which incorporates external components, as well as the amplifier provided in the MC4344/4044 circuit. The filter provides a dc voltage proportional to the phase error.







																	TEST CURRENT/VOLTAGE VALUES														Г
															Test	-	IOH1 10H2 1 In 1D 1A VIL VIH VF VR VRN VOUL VCC VCCL V										T	1			
														Tem	-55°C			-1.0	i _{sn}							H Vou			5 5	1	
													M6434	4	+25°C		-16	-1.0	10				18						5.5		
														- 1	+125°C		-16	-10								15			55	1	
													ME40	. 1	0°C +25°C		-16 -16		10									4 /5		1	
													MENU	" 1	+75°C			-1.0										4 75			
		Pm				+25°C +125°C				oc MC		Test L		5°C	_		T	ST CU	RREN	T/VO	LTAC	E AP	PLIED	TO PI	NS LIS	TED BE	LOW:				
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r or war o Current	"	3		-48		-4.8 -1.6		-4.8 -1.G		-4.8		-4.8		-4.8	1	-			-	-		15	- 1			1	1 :				
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	-	11	-	40		40		40	-	40	-	40	-	40	1	ŀ	٠		-					_	11 -	+	+	-	14		_
Breakdown Voltage	BVin	3			55	-			-		55	. 0	-	-	Vdc	1			3							-	1:	-	14	-	1
Ciamp Voitage	V _D	11	-		-	-15	-		-	-	+	-15	-	-	Vdc	1		-	11	1	-		-	+		+	-	14		-	-
Output (Note 1)	-0	3		_		-15			-		-	-15	-	-	Vuc	-			-	3		-		+	+-	1	-	14	-		-
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		12	2.4	-	24		24	-	25	-	2.5	-	25	-	Vdc	-	12	-	-		-	1,3	1	+	+	+	1	14	-	-	-
	VOL	6		04		04		04		04	1	04		04	Vele	6				-			1.3	T	1			14			Г
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		-			-	-	-	-	-	-	-	-		-	Vdc	-	-		-	-	-	1.3	-	-		-	-	14	-	-	-
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	VOH	13	2.4	1	2.4	-	2.4	1	2.5	-	2.5	-	2.5	1	Vac	-	13	-	-	-	-	1,3		-	1	-	-	14	-	-	
	VOH	2	2.4	7	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc Vdc	-	13	-	-	1	-	1	3			1	-	14	:	1	
	VOL	2	-	0.4		04	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	2	-	-	-	-	-	1.3	- 1			-	-	14	-	-	
	VOH	13	2.4	0.4	2.4	0.4	2.4	0.4	2.5	0.4	2.5	0.4	2.5	0.4	Vdc	2	13	-	-	-	-	1,3	-	-	+-	-	-	14	-	-	H
	VOH	13	2.4	-	24	-	2.4		2.5	-	2.5	-	2.5	-	Voc	-	13	-	-	-	-	1	3 .	-		-	-	14	-	-	
	VOL	13	2.4	-	24	1	2.4	-	2.5 2.5	-	2.5	-	2.5 2.5	-	Vdc Vdc	2	13	-	-	-	-	1.3	: :			13	1	14	-	1	
	VOL	2	24	-	2.4	-	24	-	2.5	-	2.5	1	2.5	-	Vac	2	13		-	-	-	3	1 1			1:	1	14	-		
	VOH	2	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vac	-	2	- 1	-	-1	-	1,3	- -			-	-	14	-	-	7
Short-Circuit Current	isc	13	-20	-65	-20	-65	-20	-65	2.5	-65	-20	-65	-20	-65	Vdc mAdc	-	13	-	-	-	-	3	1 -	+	-	-	-	14	-	14	2.
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		12	7	1	1	7	*	1	4	Ť	Y	7	1	1	1	-	-	- 1	-	-	-	3	1 -			-	1				7.
Leakage Current	OLK	6	-	250	-	250	-	250	-	250	-	250	-	250	"Ack	-	-	-	-	2	-	1,3	1 :		-	1	14	-	-	:	7
		12	-		E	,			-		-		-		1	-	-	- 1	-	-	-	1,3			-	-		- 1	-	-	-
Collector-E mitter	VCE	5	-	-	0.5	-	-	-	-	-	0.5	-	-	-	Vac	-	-	- 1	5	-	-	-		1	-	-	-	-	-	-	4.
Output Vortage	VEH	10	1.5	-	1.5	-	15	-	1.5	-	1.5	-	15	-	Vac	-	-	10	-	-	-	17	-	+	-	1.		14	-	-	7
Output Current	10	8	10	-	1.0	- 1	10	-	10		10	-	10	-	mAdc	-	-	-	-	-	9	-		1.	-	-	-	-	8		7
Leasage Current	OLK	8	-	120	-	120	:	120 5 0	-	120	-	120	T.	120	µAdc µAdc	-	-	- 1	-	-	-	- 1		1	1 10	1:	1	-	8	2	7.5
Power Requirements (Total Device)					1														1	T				T	T						Т
Power Supply Drain	IPD	14	-	40	-	40	-	40	~	40	-	40		40	mAge	-	-	-	-	-	-	-			-	-	14	-	-	-	7
osa 1. The outputs of tr input states accor	e device m	will be I	ested t	y sequ	ericing	throug	n the i	ndicate	rd					CL -		cc	Lirari	o chang		er we	nlv vo	utace									

APPLICATIONS INFORMATION

FIGURE 1 - PHASE-LOCKED, FREQUENCY SYNTHESIZER LOOP

Figure 1 shows the ME4344/4044 in a phase-locked loop with the following features:

- 1. Zero phase error between the reference frequency and the output of the divide-by-N feedback, achieved because phasefrequency detector 1 locks negative edges in the system;
- 2. Adjustable channel spacing, achieved by changing the pre-
- Outstable chainies spacing, achieved by changing the prescaling factor (÷ P) when generating the reference frequency;
 Digitally programmed tuning of the output, in multiples of the reference frequency, accomplished by changing N in the divide-by-N chain in the feedback loop.

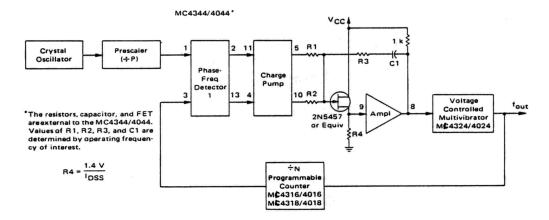
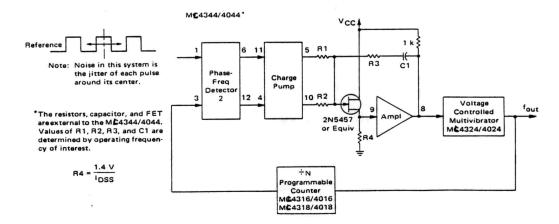


Figure 2 shows phase detector 2 of the MC4344/4044, which operates as a correlation detector, used in a phase-locked loop. There are two differences between this system and that shown in Figure 1. First, the VCM output, when locked in, lags the reference by 90°. Second, since the correlation detector integrates the product of its two inputs over each cycle, it can handle signals in a high-noise environment. This loop is sensitive to harmonics, therefore care must be taken to limit the frequency range of the VCM.

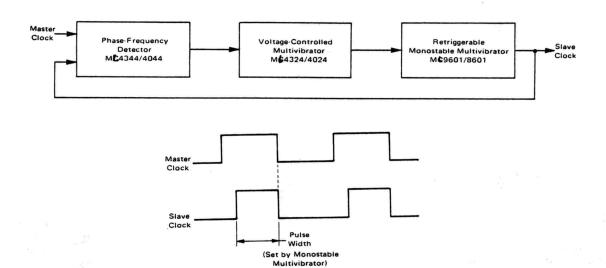
FIGURE 2 - PHASE-LOCKED, CORRELATION DETECTOR LOOP



APPLICATIONS INFORMATION (continued)

FIGURE 3 – SLAVE CLOCK PULSE GENERATOR Figure 3 depicts the M£4344/4044 in a system used to generate a slave clock pulse with its negative edge locked to the negative edge of the master clock, but with adjustable pulse width. The pulse width of the slave clock pulse is controlled only by the monostable multivibrator, which is triggered from the negative edge of an input pulse.

The slave clock application is useful when the clock from a master computer must be slaved to that of a satellite.



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