SPDT SWITCH GaAs MMIC

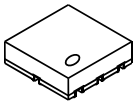
■ GENERAL DESCRIPTION

NJG1635AHB6 is a GaAs SPDT switch IC suited for mobile handset, WiBro and WiMAX devices. This switch features high power handling, low insertion loss, high isolation.

This switch includes logic decoder function, and can be operated by single bit control signal from 1.3V of logical high voltage. In addition, this switch includes ESD protection circuits.

The ultra-small & ultra-thin USB8-B6 package is adopted.

■ PACKAGE OUTLINE



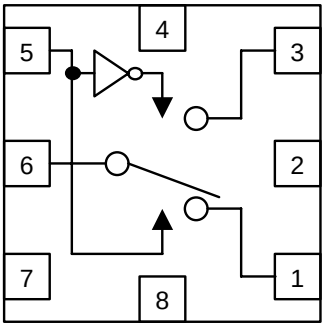
NJG1635AHB6

■ FEATURES

● Single bit low voltage control	+1.3V~+4.5V
● Operation supply voltage	+2.5~+4.5V
● Low insertion loss	0.30dB typ. @f=0.9GHz, P_{IN}=30dBm, V_{DD}=2.7V
	0.35dB typ. @f=1.9GHz, P_{IN}=30dBm, V_{DD}=2.7V
	0.40dB typ. @f=2.7GHz, P_{IN}=30dBm, V_{DD}=2.7V
● High isolation	35dB typ. @f=0.9/1.9GHz, P_{IN}=30dBm, V_{DD}=2.7V
	33dB typ. @f=2.7GHz, P_{IN}=30dBm, V_{DD}=2.7V
● High power handling	$P_{-0.1dB}$=32dBm min. @f=2.7GHz, V_{DD}=2.7V
● ESD protection circuit	
● Small & thin package	USB8-B6 (Package size: 1.5 x 1.5 x 0.55mm)

■ PIN CONFIGURATION

USB8-B6 Type
(Top view)



Pin connection
1. P1
2. GND
3. P2
4. GND
5. VCTL
6. PC
7. VDD
8. GND

■ TRUTH TABLE

Control Voltage: "H"=$V_{CTL\ (H)}$, "L"=$V_{CTL\ (L)}$

VCTL	PATH
H	P1-PC
L	P2-PC

NOTE: Please note that any information on this datasheet will be subject to change.

■ ABSOLUTE MAXIMUM RATINGS

(T_a=+25°C, Z_s=Z_l=50Ω))

PARAMETER	SYMBOL	CONDITIONS	CONDITIONS	UNITS
RF Input Power	P_{IN}	V_{DD}=2.7V, V_{CTL}=0/1.8V	35	dBm
Supply Voltage	V_{DD}	VDD terminal	5.0	V
Control Voltage	V_{CTL}	VCTL terminal	5.0	V
Power Dissipation	P_D	on PCB board	160	mW
Operating Temp.	T_{opr}		-40~+95	°C
Storage Temp.	T_{stg}		-55~+150	°C

■ ELECTRICAL CHARACTERISTICS

(General conditions: V_{DD}=2.7V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, Z_S=Z_l=50Ω, T_a=+25°C, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage	V_{DD}		2.5	2.7	4.5	V
Operating Current	I_{DD}	P_{IN}=30dBm	-	25	50	μA
Control Voltage (LOW)	$V_{CTL(L)}$		0	-	0.4	V
Control Voltage (HIGH)	$V_{CTL(H)}$		1.3	1.8	4.5	V
Control Current	I_{CTL}		-	5	10	μA
Insertion Loss 1	LOSS1	f=0.9GHz, P_{IN}=30dBm	-	0.30	0.45	dB
Insertion Loss 2	LOSS2	f=1.9GHz, P_{IN}=30dBm	-	0.35	0.50	dB
Insertion Loss 3	LOSS3	f=2.7GHz, P_{IN}=30dBm	-	0.40	0.60	dB
Isolation 1	ISL1	f=0.9GHz, P_{IN}=30dBm	32	35	-	dB
Isolation 2	ISL2	f=1.9GHz, P_{IN}=30dBm	30	35	-	dB
Isolation 3	ISL3	f=2.7GHz, P_{IN}=30dBm	25	33	-	dB
Input Power at 0.1dB Compression	$P_{-0.1dB}$	f=2.7GHz	32	-	-	dBm
2nd Harmonics 1	$2f_o$(1)	f=0.9GHz, P_{IN}=26dBm	-	-75	-65	dBc
2nd Harmonics 2	$2f_o$(2)	f=1.9GHz, P_{IN}=26dBm	-	-75	-65	dBc
3rd Harmonics 1	$3f_o$(1)	f=0.9GHz, P_{IN}=26dBm	-	-80	-65	dBc
3rd Harmonics 2	$3f_o$(2)	f=1.9GHz, P_{IN}=26dBm	-	-80	-65	dBc
Input 3rd Order Intercept Point 1	IIP3(1)	f=0.9GHz+0.901GHz P_{IN}=25dBm each	58	64	-	dBm
Input 3rd Order Intercept Point 2	IIP3(2)	f=1.9GHz+1.901GHz P_{IN}=25dBm each	58	62	-	dBm
VSWR (PC, P1, P2)	VSWR	f=2.7GHz, ON State	-	1.2	1.4	
Switching time	T_{SW}	PC-P1, PC-P2 port switching time	-	2	5	μs

The input 3rd order intercept point is defined as following equation, IIP3 = (3 x Pout – IM3)/2 + LOSS

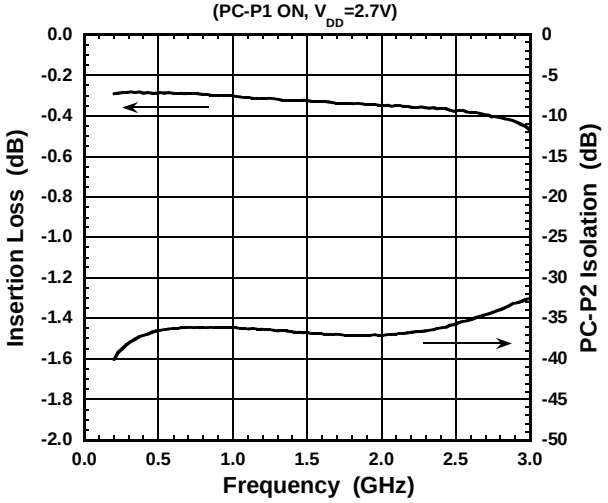
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	P1	This port is connected to PC port by control voltage of +1.3~4.5V($V_{CTL(H)}$) to 5th pin. An external capacitor is required to block the DC bias voltage of internal circuit.
2	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
3	P2	This port is connected to PC port by control voltage of +0.0~0.4V($V_{CTL(L)}$) to 5th pin. An external capacitor is required to block the DC bias voltage of internal circuit.
4	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
5	VCTL	Control port. This terminal is set to +1.3V~4.5V of logical high level for ON state between PC and P1 RF ports, and set to +0.0~0.4V of logical low level for ON state between PC and P2 RF ports.
6	PC	Common RF port. This PC port is connected to P1 or P2 by logical control voltage of VCTL. In order to block DC bias voltage of internal circuit, an external capacitor is required.
7	VDD	A supply voltage terminal (+2.5~+4.5V). Please place a bypass capacitor between this and GND for avoiding RF noise from outside.
8	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.

■ **ELECTRICAL CHARACTERISTICS** (with Application circuit, Loss of external circuit are excluded)

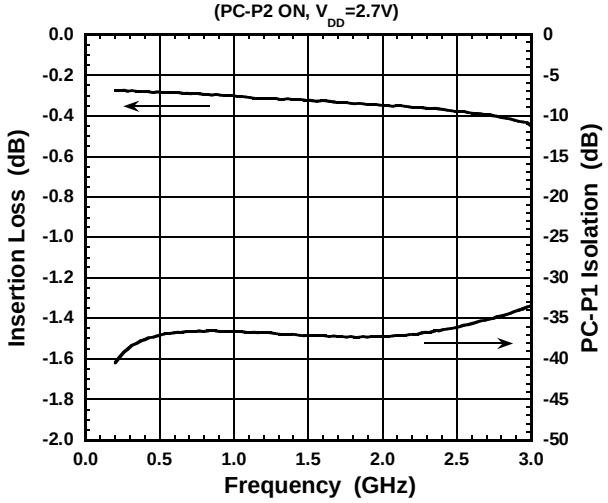
Loss, Isolation vs Frequency

(PC-P1 ON, V_{DD}=2.7V)



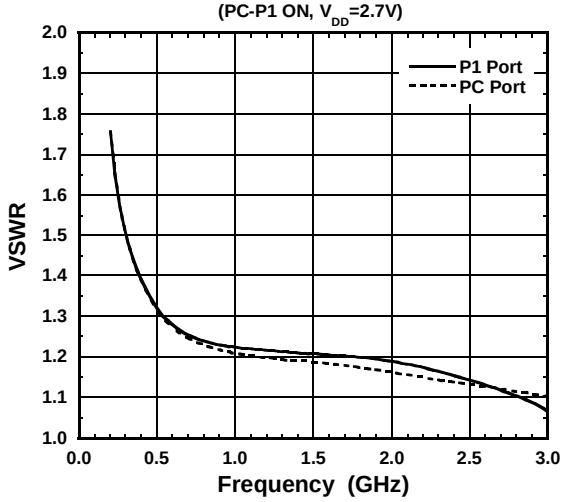
Loss, Isolation vs Frequency

(PC-P2 ON, V_{DD}=2.7V)



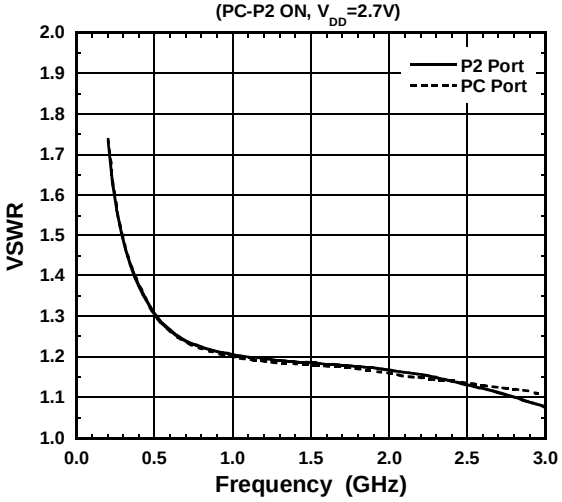
VSWR vs Frequency

(PC-P1 ON, V_{DD}=2.7V)



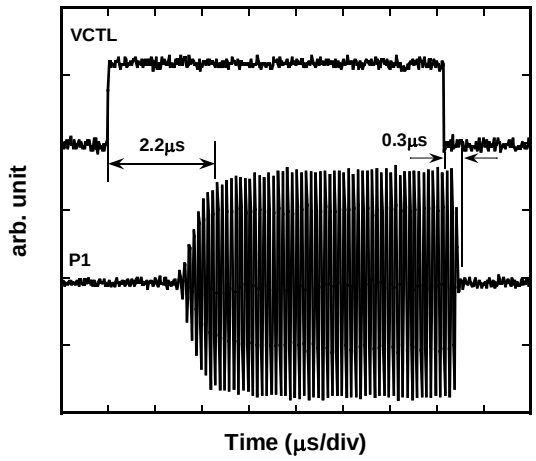
VSWR vs Frequency

(PC-P2 ON, V_{DD}=2.7V)



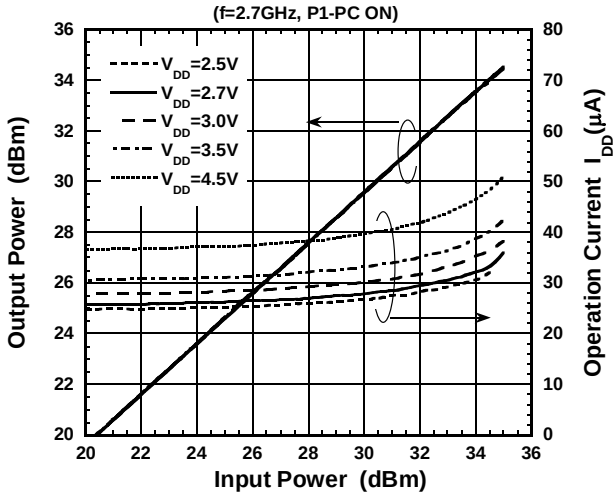
Switching Time

(V_{DD}=2.7V, VCTL=0/1.8V)

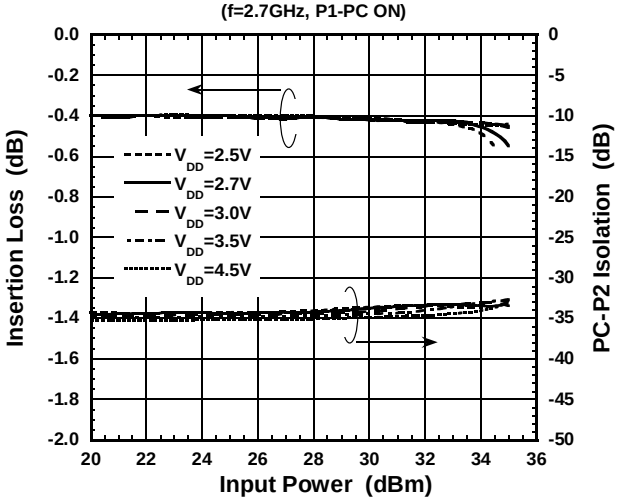


■ **ELECTRICAL CHARACTERISTICS** (with Application circuit, Loss of external circuit are excluded)

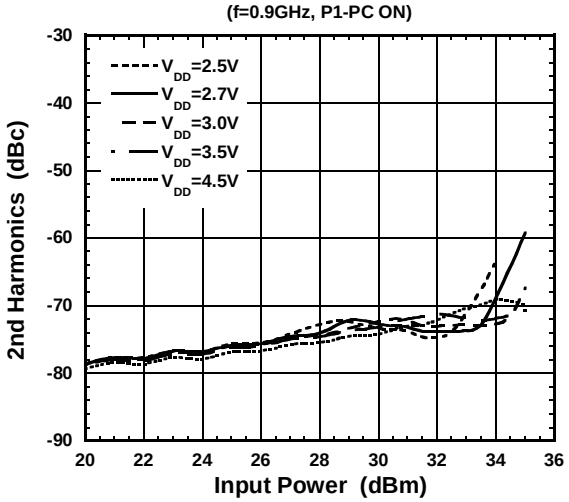
Output Power, I_{DD} vs Input Power



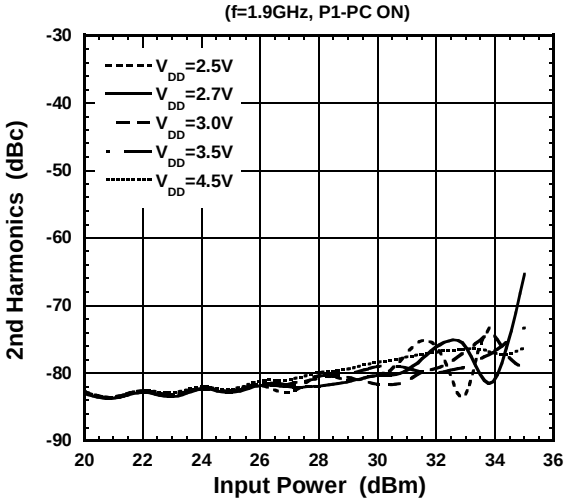
Loss, ISL vs Input Power



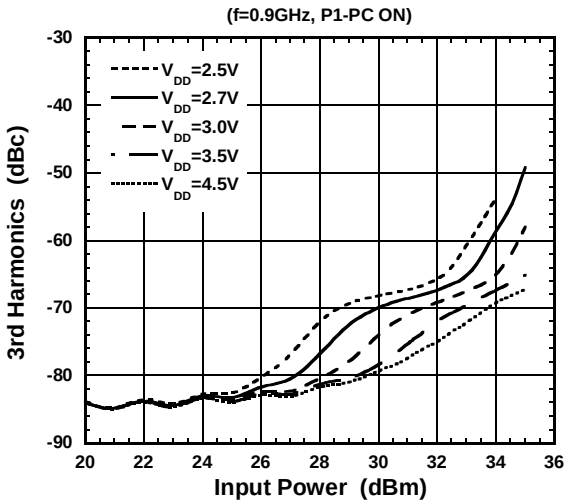
2nd Harmonics vs Input Power



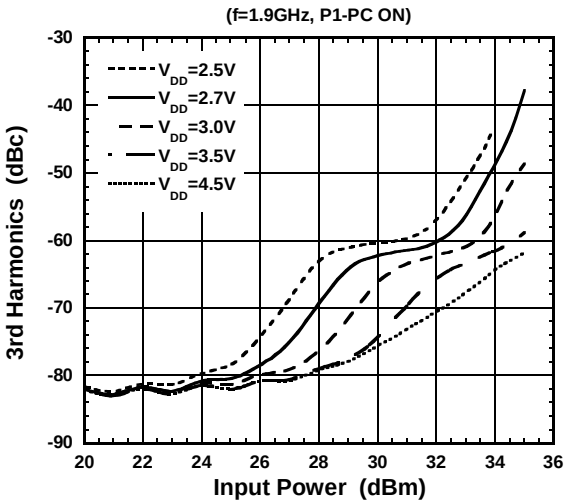
2nd Harmonics vs Input Power



3rd Harmonics vs Input Power



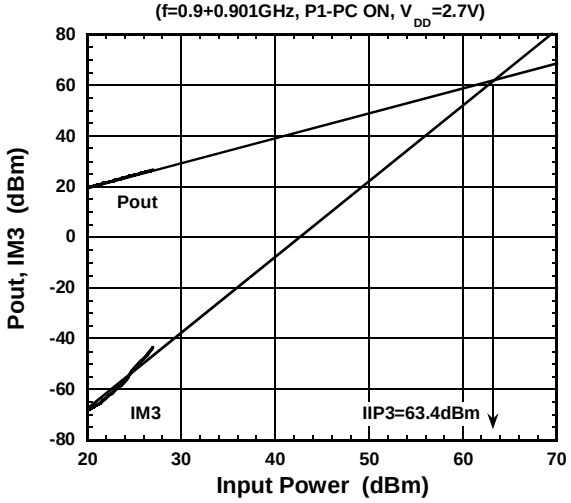
3rd Harmonics vs Input Power



■ **ELECTRICAL CHARACTERISTICS** (with Application circuit, Loss of external circuit are excluded)

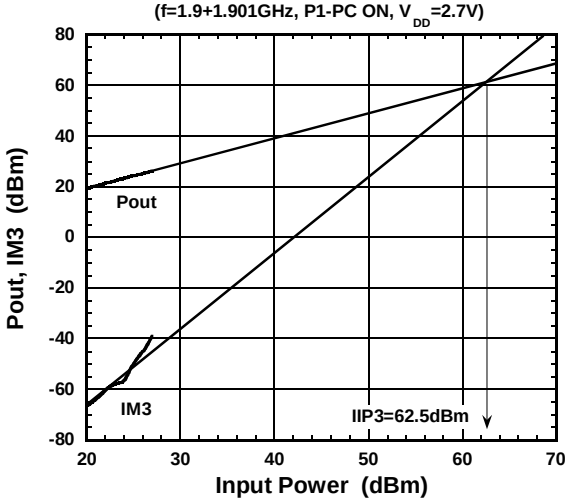
Pout, IM3 vs Input Power

(f=0.9+0.901GHz, P1-PC ON, V_{DD}=2.7V)



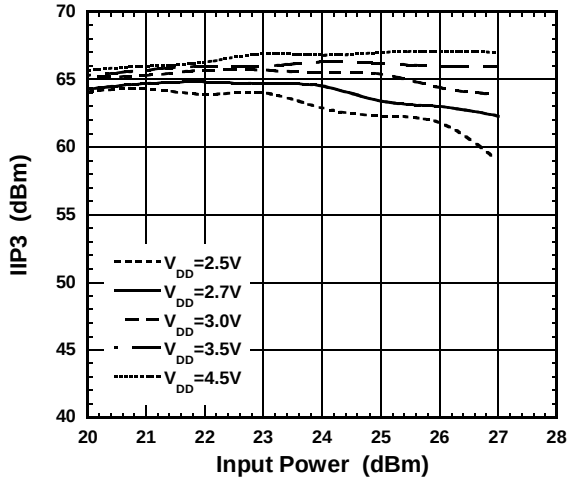
Pout, IM3 vs Input Power

(f=1.9+1.901GHz, P1-PC ON, V_{DD}=2.7V)



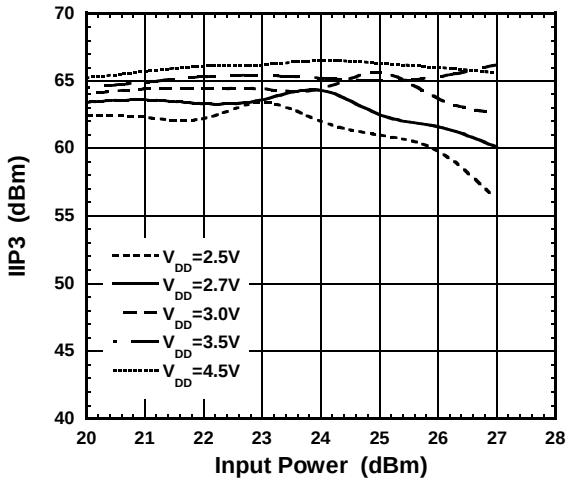
IIP3 vs Input Power

(f=0.9+0.901GHz, P1-PC ON)



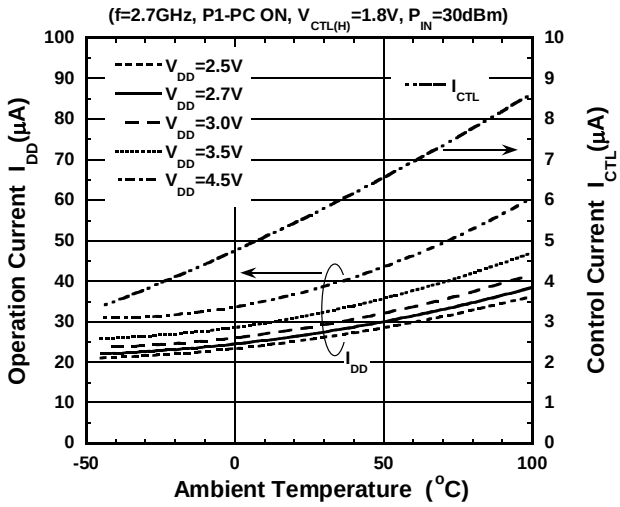
IIP3 vs Input Power

(f=1.9+1.901GHz, P1-PC ON)

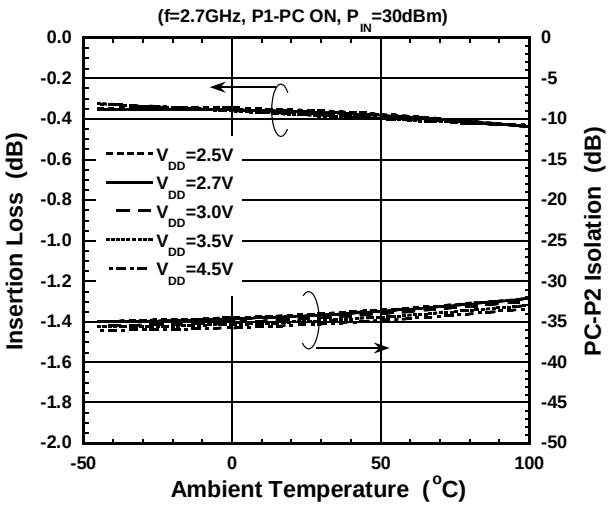


■ **ELECTRICAL CHARACTERISTICS** (with Application circuit, Loss of external circuit are excluded)

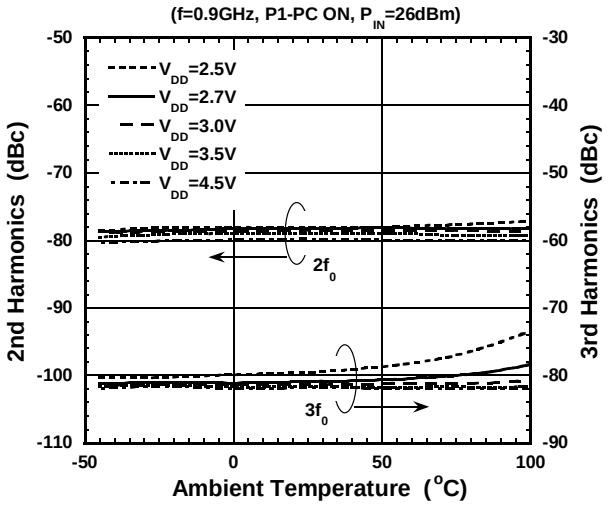
I_{DD}, I_{CTL} vs Ambient Temperature



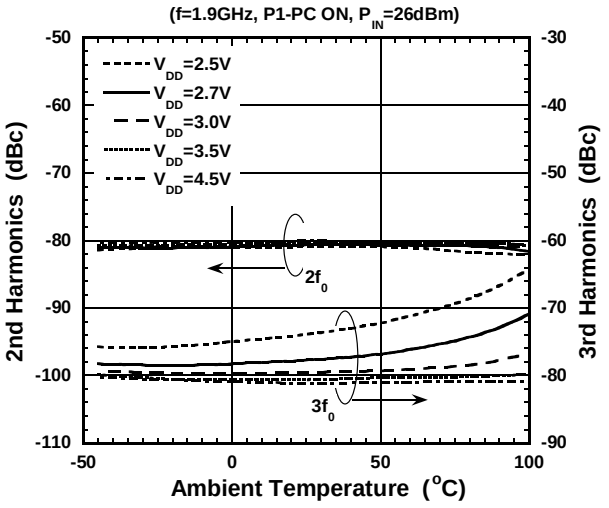
Loss, ISL vs Ambient Temperature



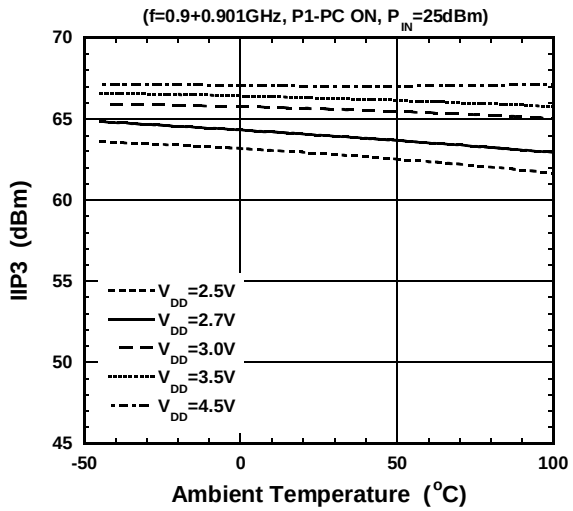
Harmonics vs Ambient Temperature



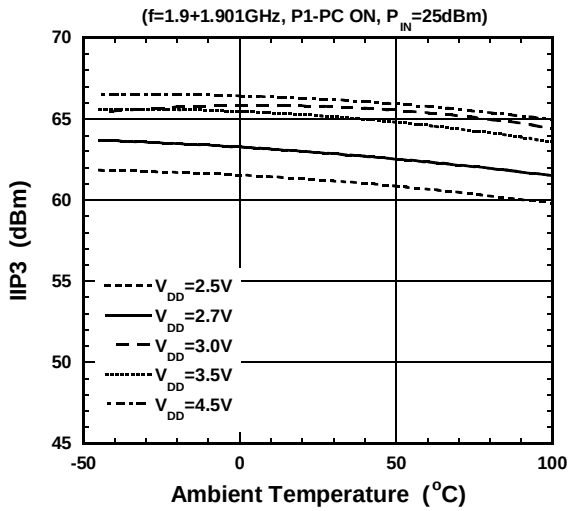
Harmonics vs Ambient Temperature



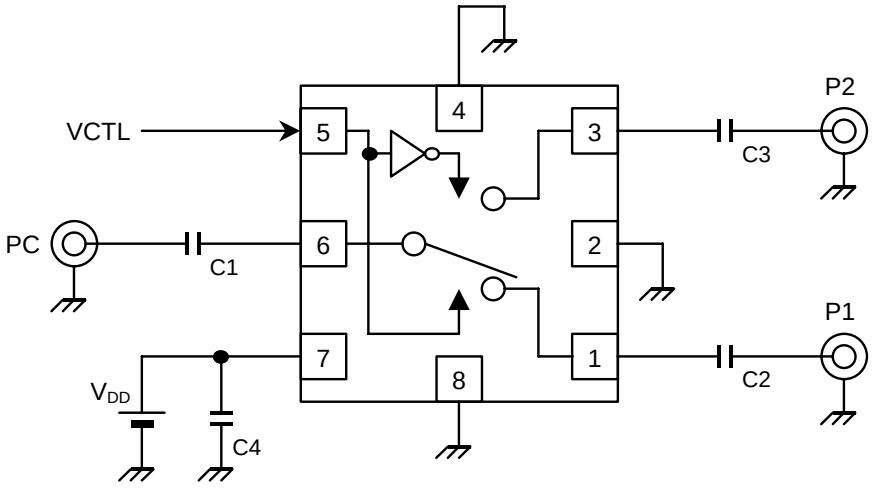
IIP3 vs Ambient Temperature



IIP3 vs Ambient Temperature



■ APPLICATION CIRCUIT

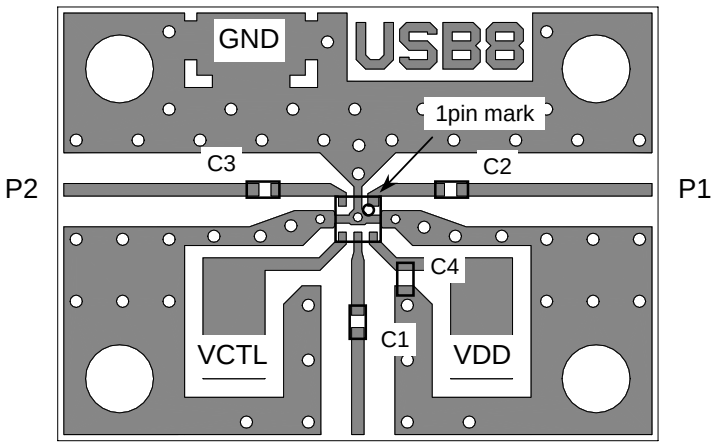


PARTS LIST

PART ID	Value	COMMENT
C1~C3	56pF	MURATA (GRM15)
C4	1000pF	

■ TEST PCB LAYOUT

(TOP VIEW)



PCB SIZE=19.4x14.0mm
PCB: FR-4, t=0.2mm
CAPACITOR: size 1005
STLIPLINE=0.4mm

Losses of PCB, capacitors and connectors

Frequency (GHz)	Loss (dB)
0.9	0.21
1.9	0.30
2.7	0.38

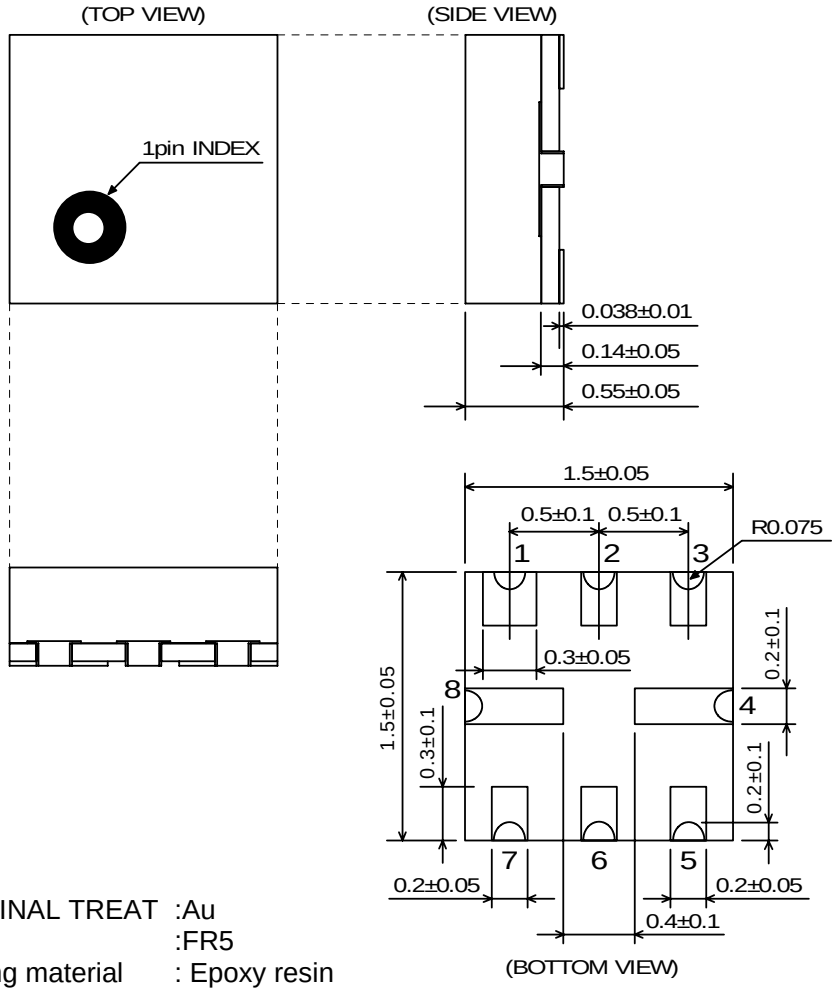
PRECAUTIONS

[1]The DC blocking capacitors have to be placed at RF terminal of P1, P2 and PC. Please choose appropriate capacitance values to the application frequency.

[2]To reduce strip line influence on RF characteristics, please locate bypass capacitors(C4) as close as possible to each terminal.

[3]For good isolation, the GND terminal (2nd pin) must be connected to the ground plane of substrate, and through-holes for GND should be placed near by the pin connection.

■ PACKAGE OUTLINE (USB8-B6)



TERMINAL TREAT	:Au
PCB	:FR5
Molding material	: Epoxy resin
UNIT	:mm
WEIGHT	:4mg

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.