

SPDT SWITCH GaAs MMIC

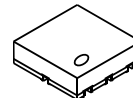
■ GENERAL DESCRIPTION

NJG1649HB6 is a GaAs SPDT switch IC suited for W-LAN, Bluetooth and sub-microwave applications.

This device can operate a single bit control signal from +1.3V.

The ultra-small & ultra-thin USB8-B6 package is adopted.

■ PACKAGE OUTLINE



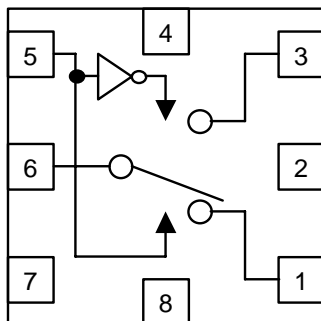
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■ FEATURES

- Single bit control +1.3V min.
- Low voltage operation +2.5~+4.5V
- Low insertion loss
 - 0.35dB typ. @f=1.0GHz, P_{IN}=23dBm, V_{DD}=2.7V
 - 0.40dB typ. @f=2.0GHz, P_{IN}=23dBm, V_{DD}=2.7V
 - 0.45dB typ. @f=2.5GHz, P_{IN}=23dBm, V_{DD}=2.7V
- Input power at 0.2dB compression point 30dBm typ. @f=2.5GHz, V_{DD}=2.7V
- High isolation
 - 27dB typ. @f=1.0GHz, P_{IN}=23dBm, V_{DD}=2.7V
 - 22dB typ. @f=2.0GHz, P_{IN}=23dBm, V_{DD}=2.7V
 - 20dB typ. @f=2.5GHz, P_{IN}=23dBm, V_{DD}=2.7V
- Small & thin package USB8-B6 (Package size: 1.5x1.5x0.55mm)

■ PIN CONFIGURATION

USB8-B6 Type
(TOP VIEW)



Pin connection

- 1. P1
- 2. GND
- 3. P2
- 4. GND
- 5. VCTL
- 6. PC
- 7. VDD
- 8. GND

■ TRUTH TABLE

Control Voltage: "H"=V_{CTL(H)}, "L"=V_{CTL(L)}

VCTL	PATH
H	P1-PC
L	P2-PC

NOTE: The information on this datasheet is subject to change without notice.

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■ ABSOLUTE MAXIMUM RATINGS

($T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$)

PARAMETER	SYMBOL	CONDITIONS	CONDITIONS	UNITS
RF input power	P_{IN}	$V_{DD}=2.7\text{V}$, $V_{CTL}=0\text{V}/1.8\text{V}$	32	dBm
Supply voltage	V_{DD}	VDD terminal	5.0	V
Control voltage	V_{CTL}	VCTL terminal	5.0	V
Power dissipation	P_D	On PCB board	160	mW
Operating temp.	T_{opr}		-40~+85	$^{\circ}\text{C}$
Storage temp.	T_{stg}		-55~+150	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS

(General conditions: $T_a=+25^{\circ}\text{C}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, $Z_s=Z_l=50\Omega$ with application circuit)

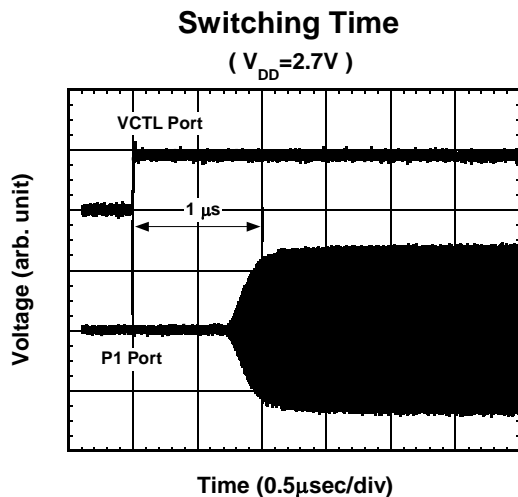
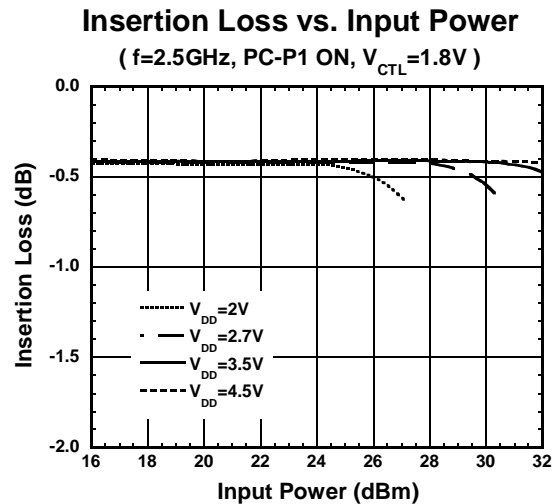
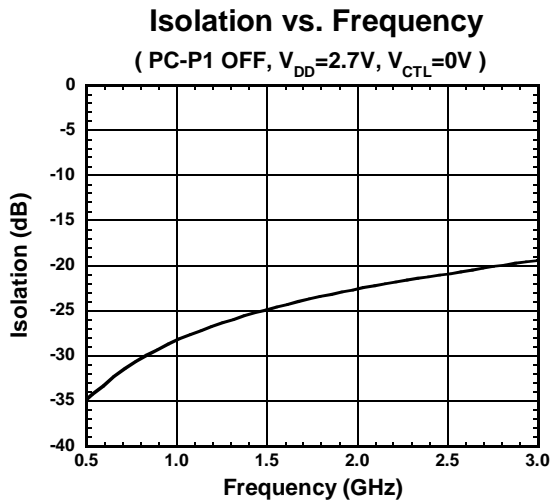
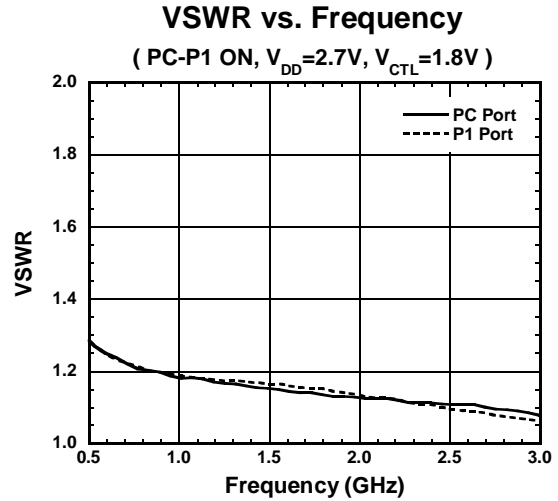
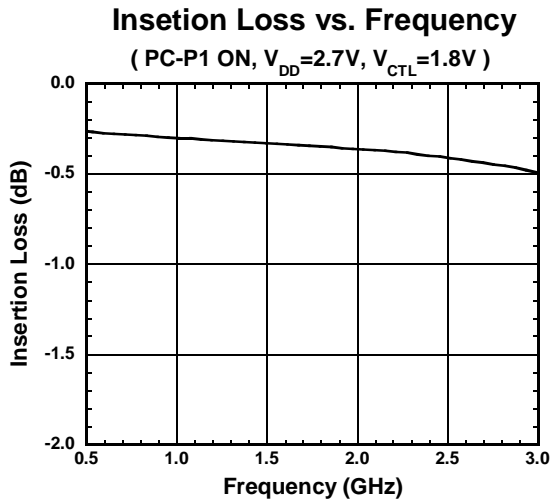
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltage	V_{DD}		2.5	2.7	4.5	V
Operating current	I_{DD}	$f=2.5\text{GHz}$, $P_{IN}=23\text{dBm}$	-	20	40	μA
Control voltage (LOW)	$V_{CTL(L)}$		0	-	0.4	V
Control voltage (HIGH)	$V_{CTL(H)}$		1.3	1.8	4.5	V
Control current	I_{CTL}		-	3	10	μA
Insertion loss 1	LOSS1	$f=1.0\text{GHz}$, $P_{IN}=23\text{dBm}$	-	0.35	0.50	dB
Insertion loss 2	LOSS2	$f=2.0\text{GHz}$, $P_{IN}=23\text{dBm}$	-	0.40	0.55	dB
Insertion loss 3	LOSS3	$f=2.5\text{GHz}$, $P_{IN}=23\text{dBm}$	-	0.45	0.60	dB
Isolation 1	ISL1	$f=1.0\text{GHz}$, $P_{IN}=23\text{dBm}$	24	27	-	dB
Isolation 2	ISL2	$f=2.0\text{GHz}$, $P_{IN}=23\text{dBm}$	19	22	-	dB
Isolation 3	ISL3	$f=2.5\text{GHz}$, $P_{IN}=23\text{dBm}$	17	20	-	dB
Input power at 0.2dB compression point	$P_{-0.2\text{dB}}$	$f=2.5\text{GHz}$	28	30	-	dBm
VSWR	VSWR	$f=0.1\sim 2.5\text{GHz}$, ON State	-	1.1	1.3	
Switching time	T_{SW}		-	1	5	μs

■ TERMINAL INFORMATION

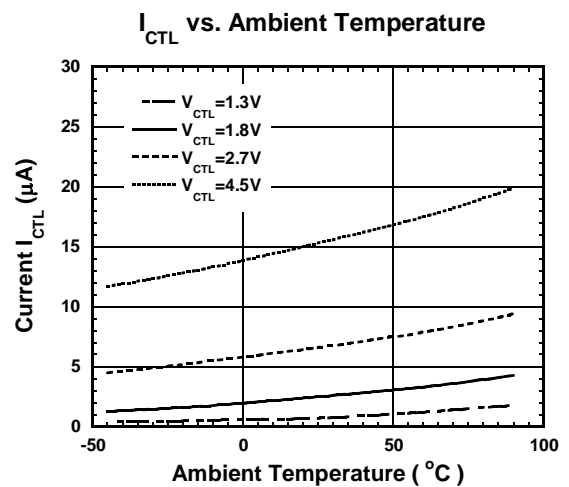
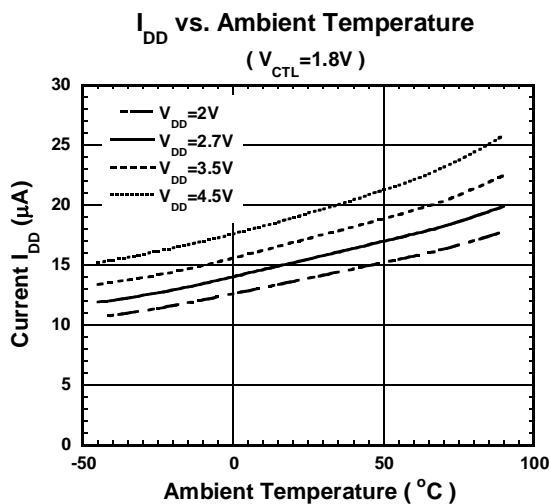
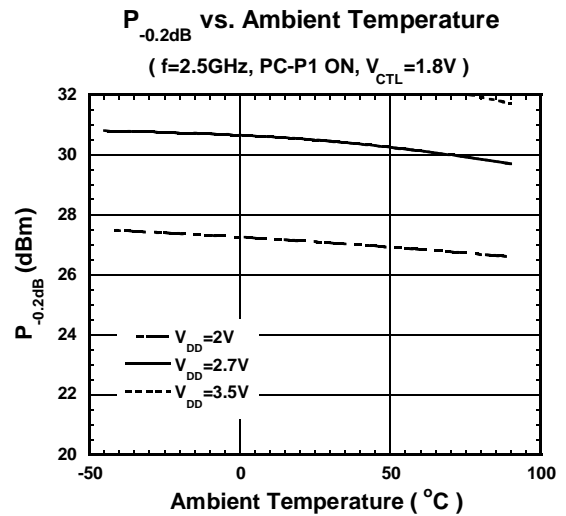
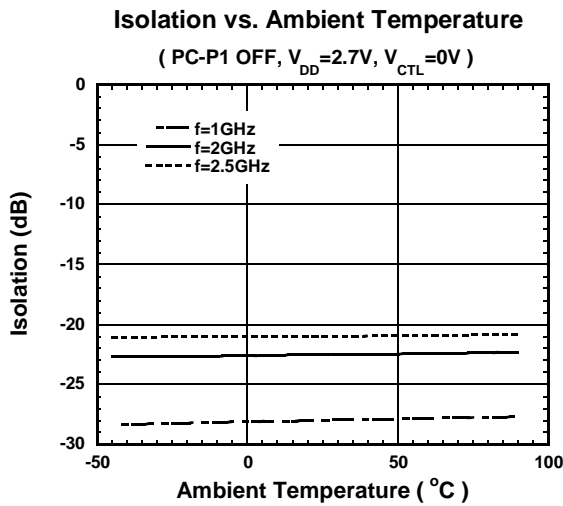
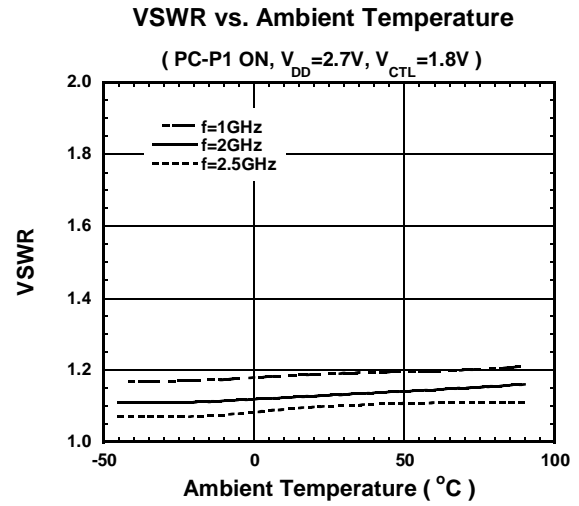
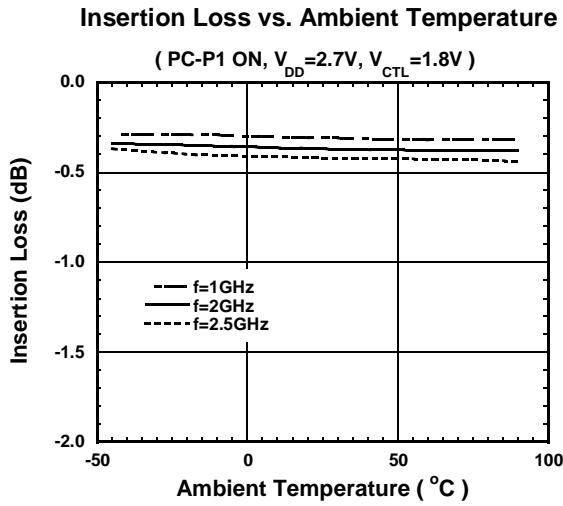
No.	SYMBOL	DESCRIPTION
1	P1	RF port. This port is connected to PC port by control voltage of +1.3~4.5V($V_{CTL(H)}$) at 5th pin. In order to block DC bias voltage of internal circuit, an external capacitor is required.
2	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
3	P2	RF port. This port is connected to PC port by control voltage of +0.0~0.4V($V_{CTL(L)}$) at 5th pin. In order to block DC bias voltage of internal circuit, an external capacitor is required.
4	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
5	VCTL	Control port. This terminal is set to +1.3V~4.5V of logical high level for ON state between PC and P1 RF ports, and set to +0.0~0.4V of logical low level for ON state between PC and P2 RF ports.
6	PC	Common RF port. This PC port is connected to P1 or P2 by logical control voltage of VCTL. In order to block DC bias voltage of internal circuit, an external capacitor is required.
7	VDD	A supply voltage terminal (+2.5~+4.5V). Please place a bypass capacitor between this and GND for avoiding RF noise from outside.
8	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.

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■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

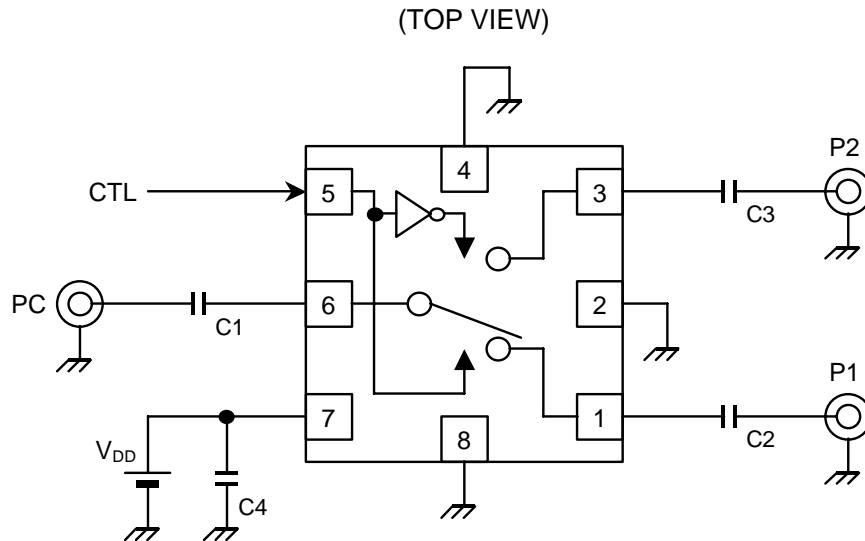


■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)



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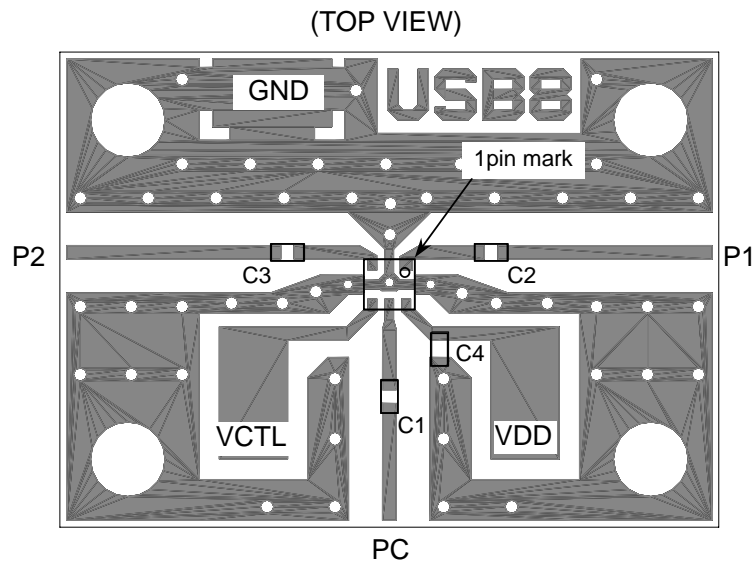
APPLICATION CIRCUIT



PARTS LIST

Parts ID	Value	Notes
C1, C2, C3	56pF	Murata (GRM15)
C4	1000pF	

TEST PCB LAYOUT



PCB SIZE=19.4x14.0mm
PBC: FR-4, t=0.2mm
CAPACITOR: size 1005
STLIPLINE=0.4mm

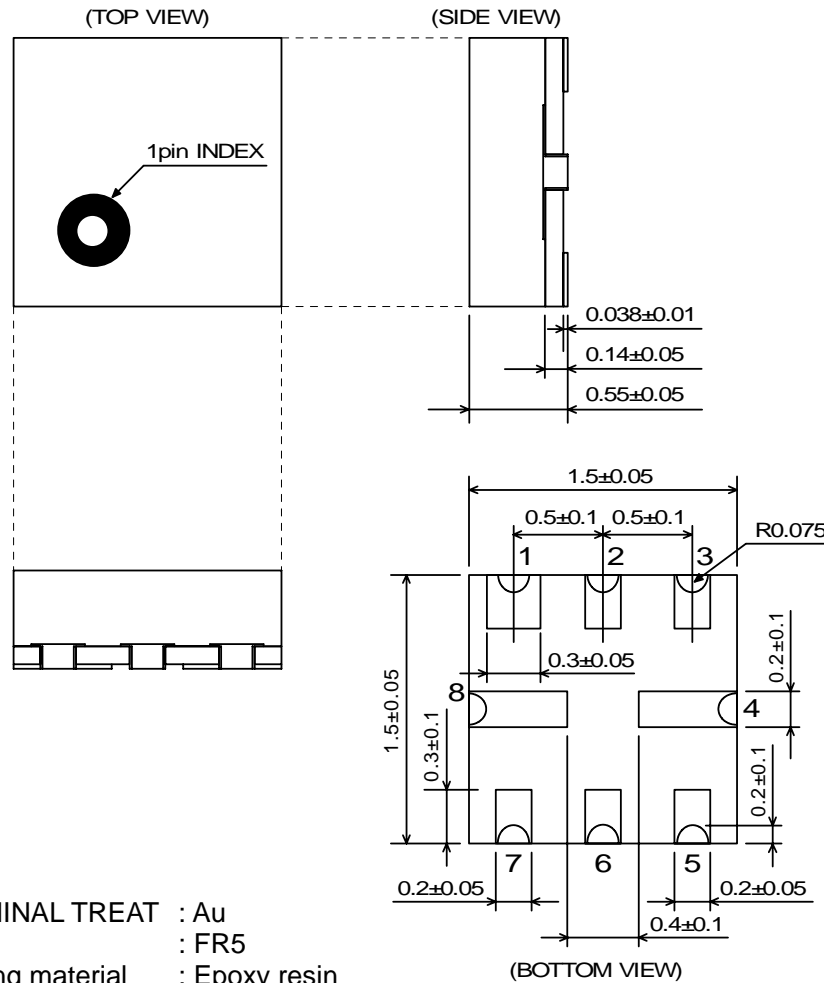
Losses of PCB, capacitors and connectors

Frequency (GHz)	Loss (dB)
1.0	0.21
2.0	0.31
2.5	0.36

PRECAUTIONS

- [1]The DC blocking capacitors have to be placed at RF terminal of P1, P2 and PC. Please choose appropriate capacitance values to the application frequency.
- [2]For avoiding the degradation of RF performance, please place bypass capacitor(C4) as close as possible to each terminal.
- [3]For good isolation, the GND terminal must be connected with the ground plane of substrate, and through-holes for GND should be placed near by the IC.

■ PACKAGE OUTLINE (USB8-B6)



TERMINAL TREAT : Au
 PCB : FR5
 Molding material : Epoxy resin
 UNIT : mm
 WEIGHT : 4mg

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.