

# **SP3T SWITCH GaAs MMIC**

#### **■** GENERAL DESCRIPTION

NJG1650HB6 is a SP3T switch IC featured low insertion loss, high isolation and small size package.

This switch is suitable for W-LAN, Bluetooth, and sub-microwave applications.

A small and thin package of USB8-B6 is adopted.

#### **■ PACKAGE OUTLINE**



NJG1650HB6

#### **■ FEATURES**

Control voltage range

Low insertion loss

High isolation

• Input power at 0.2dB compression point

Low current consumption

Small & thin package

+2.0~+5.0V

0.38dB typ. @f=1.0GHz,  $P_{IN}$ =23dBm,  $V_{CTL(H)}$ =2.7V 0.42dB typ. @f=2.0GHz,  $P_{IN}$ =23dBm,  $V_{CTL(H)}$ =2.7V 0.45dB typ. @f=2.5GHz.  $P_{IN}$ =23dBm,  $V_{CTL(H)}$ =2.7V 21dB typ. @f=2.5GHz,  $P_{IN}$ =23dBm,  $V_{CTL(H)}$ =2.7V

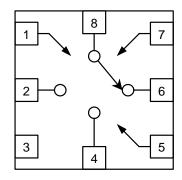
28dBm typ. @f=2.5GHz, V<sub>CTL(H)</sub>=2.7V

 $5\mu$ A typ. @ V<sub>CTL(H)</sub>=2.7V

USB8-B6 (package Size: 1.5 x 1.5 x 0.55mm typ.)

#### **■ PIN CONFIGURATION**

# USB8-B6 Type (Top view)



#### Pin connection

- 1. VCTL3
- 2. P3
- 3. GND
- 4. P2
- 5. VCTL2
- 6. P1
- 7. VCTL1
- 8. PC

#### **■ TRUTH TABLE**

"H"=V<sub>CTL</sub>(H), "L"=V<sub>CTL</sub>(L)

· · · · · · · · · · · · · · · · · · ·					
VCTL1	VCTL2	VCTL3	PATH		
Н	L	L	PC-P1		
L	Н	L	PC-P2		
L	L	Н	PC-P3		

NOTE: The information on this datasheet is subject to change without notice.

# **NJG1650HB6**

### ■ ABSOLUTE MAXIMUM RATINGS

 $(T_a=+25^{\circ}C, Z_s=Z_l=50\Omega)$ 

PARAMETERS	SYMBOL	CONDITIONS	RATINGS	UNITS
Input Power $P_{IN}$ $V_{CTL}(H)=2.7V$		V <sub>CTL</sub> (H)=2.7V	30	dBm
Control Voltage	$V_{CTL}$		6.0	V
Power Dissipation	$P_{D}$	On PCB Board	150	mW
Operating Temp.	$T_{opr}$		-40~+85	°C
Storage Temp.	$T_{stg}$		-55~+150	°C

# ■ ELECTRICAL CHARACTERISTICS

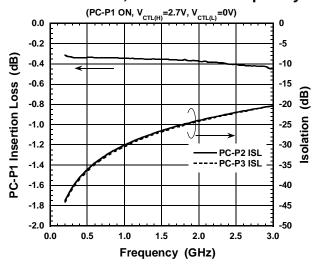
$(V_{CTL(L)}=0V, V_{CTL(H)}=2.7V, Z_S=Z_I=50\Omega, T_a=+25^{\circ}C, with application circles (V_{CTL(L)}=0V, V_{CTL(H)}=2.7V, Z_S=Z_I=50\Omega, Z_S$						
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Control voltage(LOW)	V <sub>CTL</sub> (L)		-0.2	-	+0.2	V
Control voltage (HIGH)	V <sub>CTL</sub> (H)		2.0	2.7	5.0	V
Control current	I <sub>CTL</sub>		-	5	10	μΑ
Insertion Loss 1	LOSS1	f=1.0GHz, P <sub>IN</sub> =23dBm	-	0.38	0.55	dB
Insertion Loss 2	LOSS2	f=2.0GHz, P <sub>IN</sub> =23dBm	-	0.42	0.60	dB
Insertion Loss 3	LOSS3	f=2.5GHz, P <sub>IN</sub> =23dBm	-	0.45	0.60	dB
Isolation 1	ISL1	f=1.0GHz, P <sub>IN</sub> =23dBm	27	29	-	dB
Isolation 2	ISL2	f=2.0GHz, P <sub>IN</sub> =23dBm	21	23	-	dB
Isolation 3	ISL3	f=2.5GHz, P <sub>IN</sub> =23dBm	19	21	-	dB
Input power at 0.2dB compression point	P <sub>-0.2dB</sub>	f=2.5GHz	25	28	-	dBm
VSWR (PC, P1, P2, P3)	VSWR	f=2.5GHz, On state	-	1.1	1.3	
Switching time	T <sub>SW</sub>	50% CTL to 10/90% RF	-	150	500	ns

# **■ TERMINAL INFORMATION**

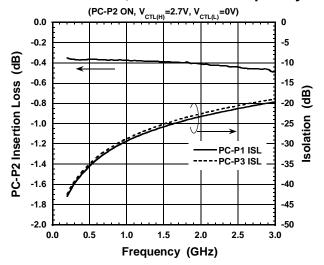
No.	SYMBOL	DESCRIPTION	
1	VCTL3	Control port. This port is set to $V_{\text{CTL(H)}}$ (+2.0~+5.0V) or $V_{\text{CTL(L)}}$ (-0.2~+0.2V). For good RF performance, please place a bypass capacitor between this port and GND, close to this port. Please choose optimum capacitance value from 10pF to 1000pF because this capacitor influences a switching time.	
2	P3	RF port. This port is connected to PC port by control voltage of $V_{\text{CTL}(H)}$ at 1st pin, $V_{\text{CTL}(L)}$ at 5th and 7th pins. In order to block DC bias voltage of internal circuit, an external capacitor is required.	
3	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.	
4	P2	RF port. This port is connected to PC port by control voltage of $V_{\text{CTL(H)}}$ at 5th pin, $V_{\text{CTL(L)}}$ at 1st and 7th pins. In order to block DC bias voltage of internal circuit, an external capacitor is required.	
5	VCTL2	Control port. This port is set to $V_{\text{CTL(H)}}$ (+2.0~+5.0V) or $V_{\text{CTL(L)}}$ (-0.2~+0.2V). For good RF performance, please place a bypass capacitor between this port and GND, close to this port. Please choose optimum capacitance value from 10pF to 1000pF because this capacitor influences a switching time.	
6	P1	RF port. This port is connected to PC port by control voltage of $V_{\text{CTL(H)}}$ at 7th pin, $V_{\text{CTL(L)}}$ at 1st and 5th pins. In order to block DC bias voltage of internal circuit, an external capacitor is required.	
7	VCTL1	Control port. This port is set to $V_{\text{CTL(H)}}$ (+2.0~+5.0V) or $V_{\text{CTL(L)}}$ (-0.2~+0.2V). For good RF performance, please place a bypass capacitor between this port and GND, close to this port. Please choose optimum capacitance value from 10pF to 1000pF because this capacitor influences a switching time.	
8	PC	Common RF port. This PC port is connected with either of P1, P2 and P3 by logical control voltage of VCTL1 to 3. In order to block DC bias voltage of internal circuit, an external capacitor is required.	

■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

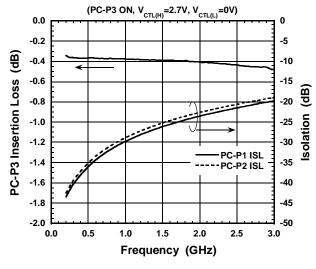
# Insertion Loss, Isolation vs Frequency



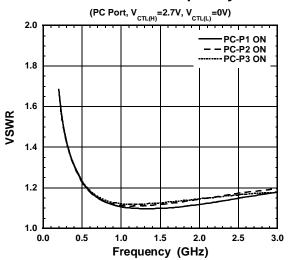
# Insertion Loss, Isolation vs Frequency



# Insertion Loss, Isolation vs Frequency

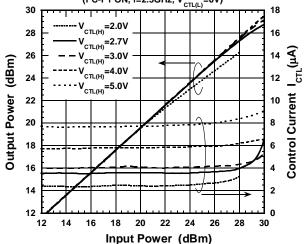


# VSWR vs Frequency

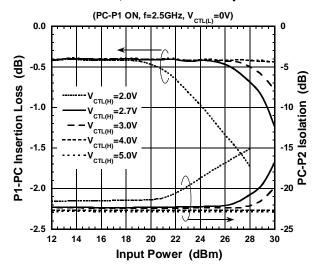


■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

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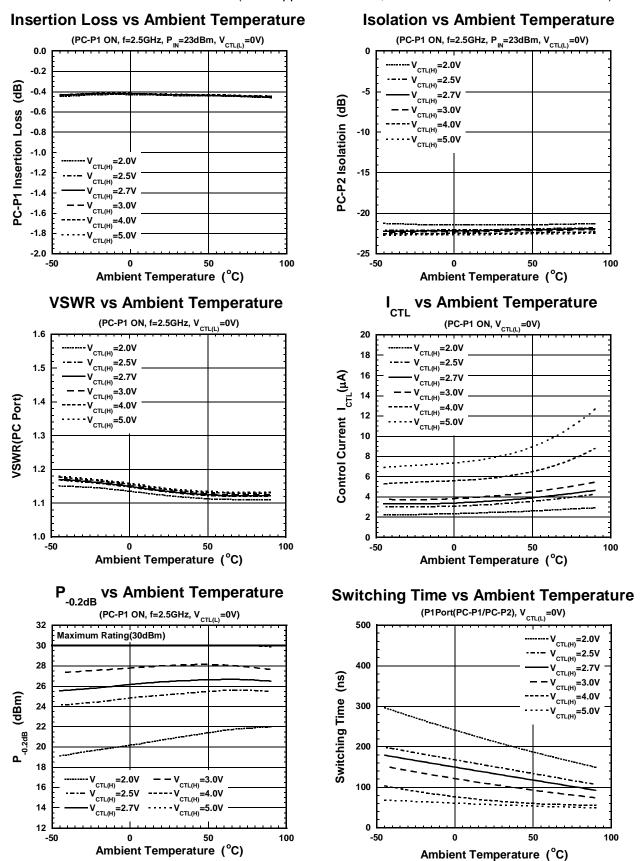


# Insertion Loss, Isolation vs Input Power

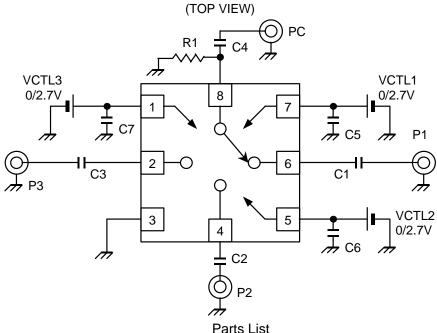


# Switching Time (PC-P1/P2, V<sub>CTL</sub>=2.7/0V) VCTL1 136ns 142ns Time (100ns/div)

■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

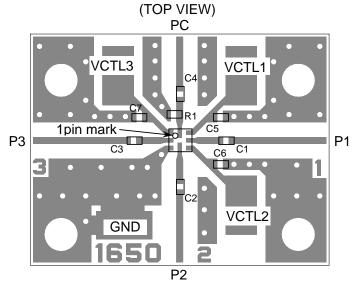


### **■ APPLICATION CIRCUIT**



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Parts number	Value	Notes
C1~C4	56pF	GRM15 MURATA
C5~C7	10pF	GRIVITS WORATA
R1	560k ohm	-

#### **■ TEST PCB LAYOUT**



PCB SIZE=19.4x14.0mm

PCB: FR-4, t=0.2mm

CAPACITOR: size 1005

Stlipline =0.4mm

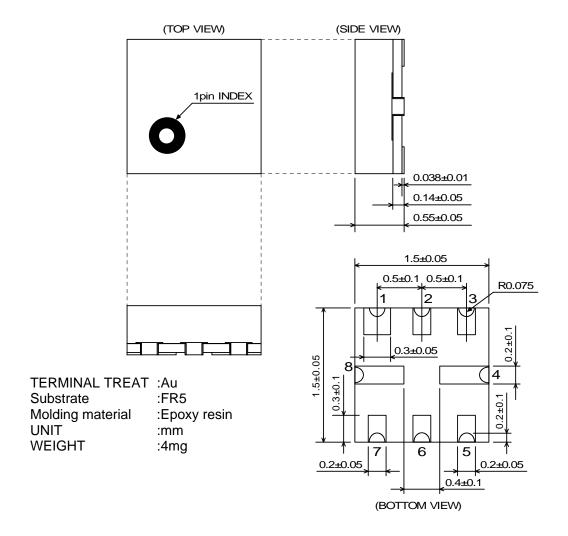
Losses of PCB, Connector and capacitors

Freq.(GHz)	Loss (dB)
1.0	0.21
2.0	0.30
2.5	0.35

#### **PRECAUTIONS**

- [1] The DC blocking capacitors have to be placed at RF terminal of P1, P2, P3 and PC.
- [2] To reduce stripline influence on RF characteristics, please locate bypass capacitors (C5~C7) close to each terminal.
- [3] For good isolation, the GND terminal must be connected with the ground plane of substrate, and through-holes for GND should be placed near by the IC.

# **■PACKAGE OUTLINE** (USB8-B6)



#### Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

#### [CAUTION]

The specifications on this databook are only given for information , without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.