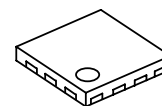


SP5T SWITCH GaAs MMIC

■ GENERAL DESCRIPTION

The NJG1667MD7 is a GaAs SP5T switch featured low insertion loss, high isolation and small size package, and suited for mobile terminal applications. The NJG1667MD7 switches a path between common RF port and five RF ports by three bit control signal from 1.3V of logical high voltage. In addition, this switch includes ESD protection circuits for good ESD tolerance. The NJG1667MD7 is available in a very small, lead-free, halogen-free, 1.6mm x 1.6mm x 0.397 mm, 14-pin EQFN14-D7 package.

■ PACKAGE OUTLINE



NJG1667MD7

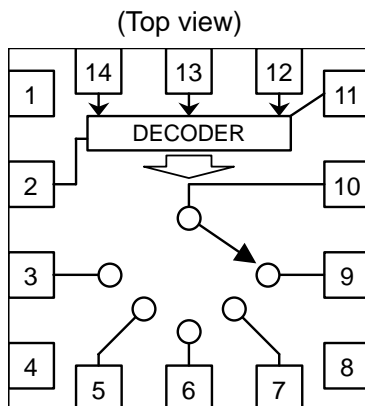
■ FEATURES

- Low control voltage
- Low operating voltage
- Low insertion loss

- High ESD tolerance
- Small and thin package
- Lead -free and halogen-free

$V_{CTL(H)} = +1.3V$ min
 $V_{DD} = +2.0 \sim +4.5V$
 0.40 dB typ. @f=1.0GHz, $P_{IN}=23dBm$
 0.50 dB typ. @f=2.0GHz, $P_{IN}=23dBm$
 0.60 dB typ. @f=2.5GHz, $P_{IN}=23dBm$
 On-chip ESD protection circuit
 EQFN14-D7 (package size: 1.6mm x 1.6mm x 0.397mm typ.)

■ PIN CONFIGURATION



Pin connection

- | | |
|--------|----------|
| 1. GND | 8. GND |
| 2. VDD | 9. P1 |
| 3. P5 | 10. PC |
| 4. GND | 11. GND |
| 5. P4 | 12. CTL3 |
| 6. P3 | 13. CTL2 |
| 7. P2 | 14. CTL1 |

■ TRUTH TABLE

PATH	CTL1	CTL2	CTL3
PC-P1	L	H	H
PC-P2	L	L	H
PC-P3	L	L	L
PC-P4	L	H	L
PC-P5	H	X	X

"H"... $V_{CTL(H)}$, "L"... $V_{CTL(L)}$, "X"...Do not care.

NOTE: The information on this datasheet is subject to change without notice

NJG1667MD7

■ ABSOLUTE MAXIMUM RATINGS

($T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF input power	P_{IN}	$V_{DD}=2.7\text{V}$, $V_{CTL}=0\text{V} / 1.8\text{V}$	30	dBm
Supply voltage	V_{DD}	VDD terminal	5.0	V
Control voltage	V_{CTL}	CTL1~3 terminals	5.0	V
Power dissipation	P_D	Four-layer FR4 PCB with through-hole (JESD51-5), $T_j=150^{\circ}\text{C}$	1300	mW
Operating temp.	T_{opr}		-40~+85	$^{\circ}\text{C}$
Storage temp.	T_{stg}		-55~+150	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS (DC)

(General conditions: $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, $Z_s=Z_l=50\Omega$, $T_a=+25^{\circ}\text{C}$, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltage	V_{DD}		2.0	2.7	4.5	V
Operating current	I_{DD}	$f=2.0\text{GHz}$, $P_{IN}=23\text{dBm}$		45	100	μA
Control voltage (LOW)	$V_{CTL(L)}$		0	-	0.4	V
Control voltage (HIGH)	$V_{CTL(H)}$		1.3	1.8	4.5	V
Control Current	I_{CTL}		-	5	10	μA

■ ELECTRICAL CHARACTERISTICS (RF)

(General conditions: $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, $Z_s=Z_l=50\Omega$, $T_a=+25^{\circ}\text{C}$, with application circuit)

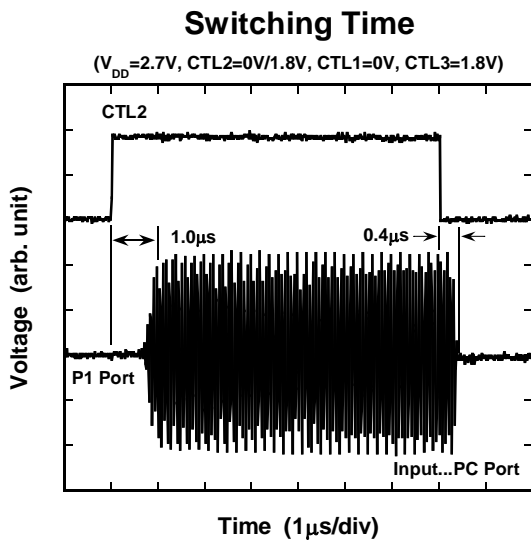
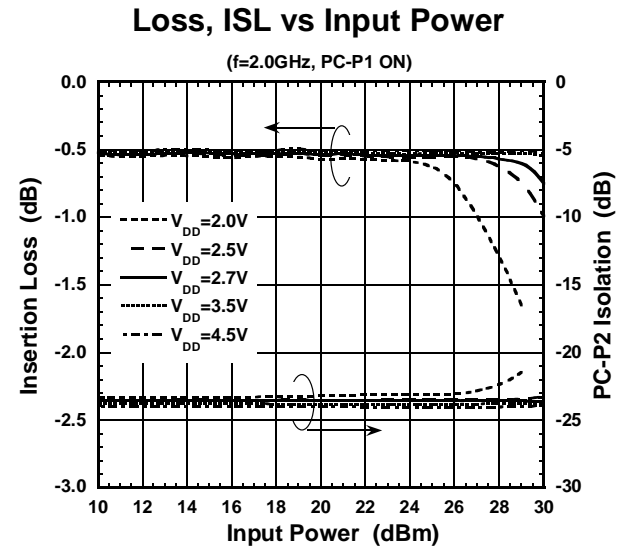
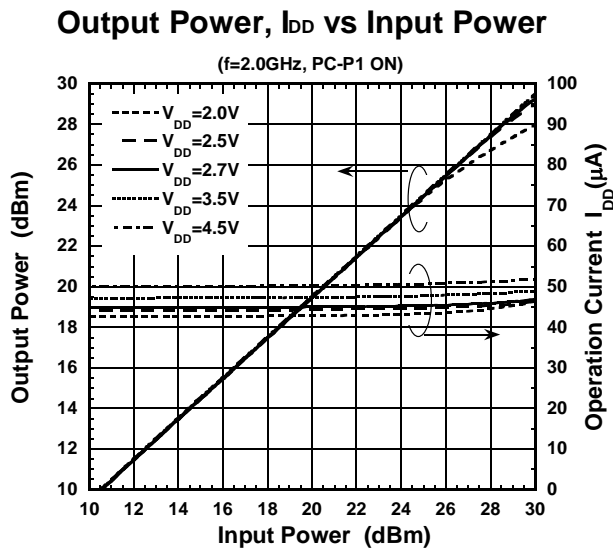
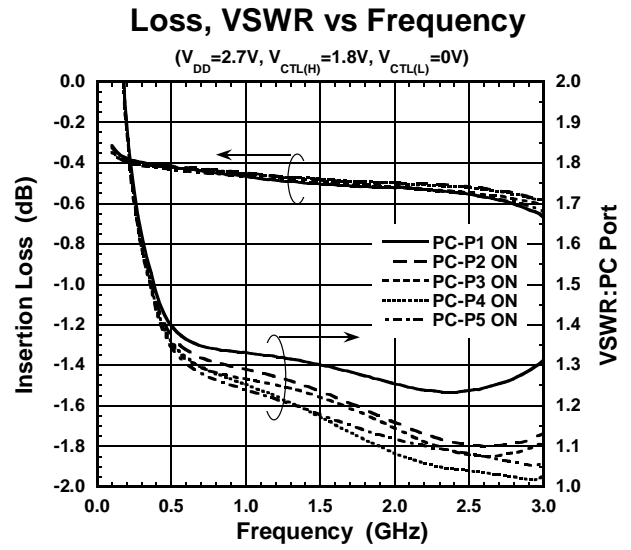
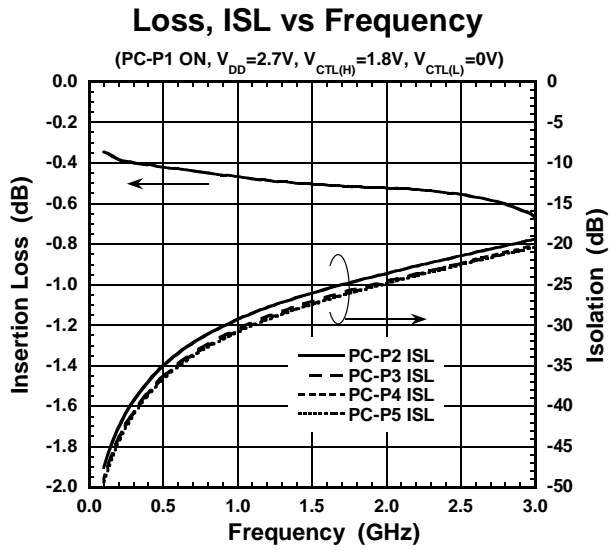
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss1	LOSS1	$f=1.0\text{GHz}$, $P_{IN}=23\text{dBm}$	-	0.40	0.60	dB
Insertion Loss2	LOSS2	$f=2.0\text{GHz}$, $P_{IN}=23\text{dBm}$	-	0.50	0.70	dB
Insertion Loss3	LOSS3	$f=2.5\text{GHz}$, $P_{IN}=23\text{dBm}$	-	0.60	0.80	dB
Isolation1	ISL1	$f=1.0\text{GHz}$, $P_{IN}=23\text{dBm}$	25	29	-	dB
Isolation2	ISL2	$f=2.0\text{GHz}$, $P_{IN}=23\text{dBm}$	20	23	-	dB
Isolation3	ISL3	$f=2.5\text{GHz}$, $P_{IN}=23\text{dBm}$	18	21	-	dB
Input Power at 0.2dB Compression Point	$P_{-0.2\text{dB}}$	$f=2.0\text{GHz}$	26	29	-	dBm
VSWR	VSWR	$f=2.0\text{GHz}$, ON state		1.2	1.5	
Switching Time	T_{SW}	50% CTL to 10%/90% RF		1	5	μs

■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	GND	Ground terminal. Connect to the PCB ground plane.
2	VDD	Power supply input. This terminal should be connected to GND via a bypass capacitor.
3	P5	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
4	GND	Ground terminal. Connect to the PCB ground plane.
5	P4	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
6	P3	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
7	P2	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
8	GND	Ground terminal. Connect to the PCB ground plane.
9	P1	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
10	PC	Common RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
11	GND	Ground terminal. Connect to the PCB ground plane.
12	CTL3	Control port. "High level" is DC +1.3V~4.5V, "Low level" is DC 0~+0.4V.
13	CTL2	Control port. "High level" is DC +1.3V~4.5V, "Low level" is DC 0~+0.4V.
14	CTL1	Control port. "High level" is DC +1.3V~4.5V, "Low level" is DC 0~+0.4V.

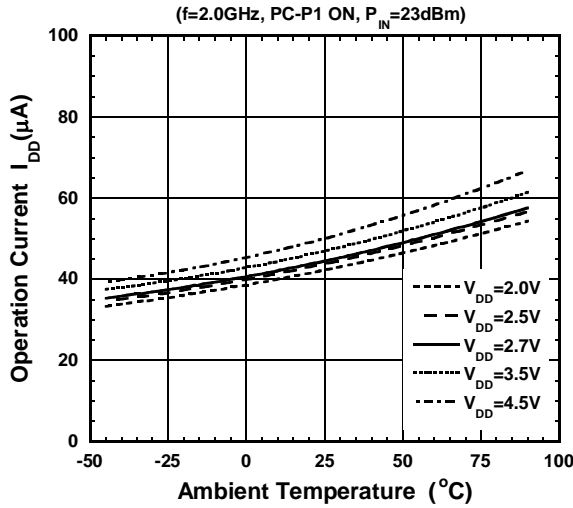
NJG1667MD7

■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

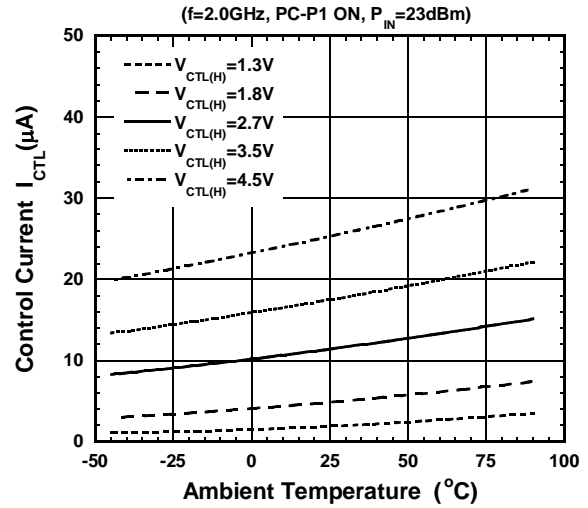


ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

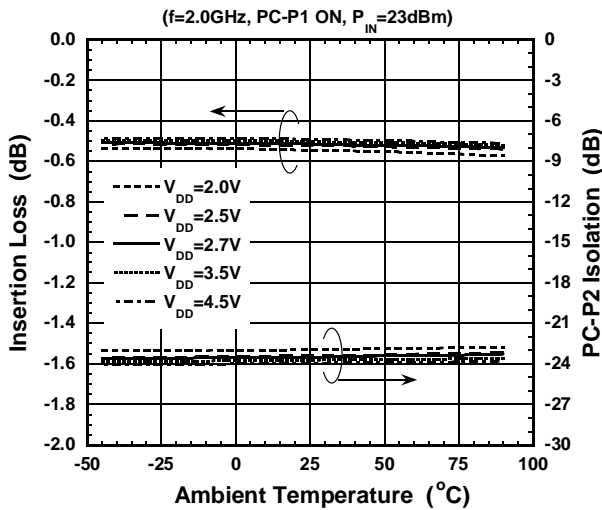
Operation Current vs Temperature



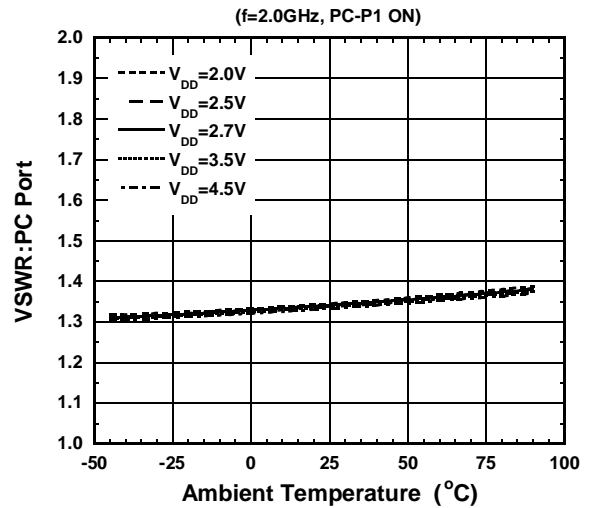
Control Current vs Temperature



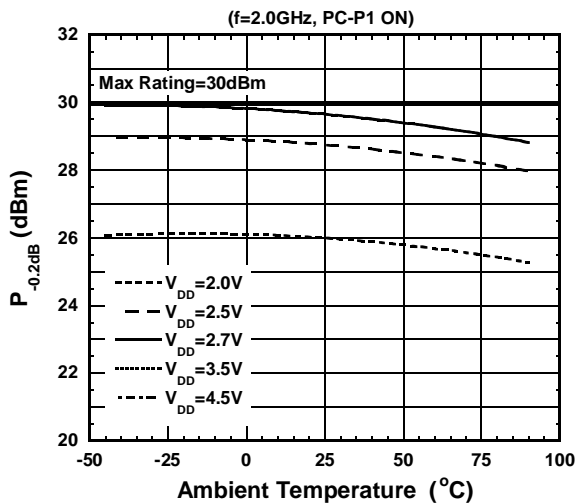
LOSS, ISL vs Temperature



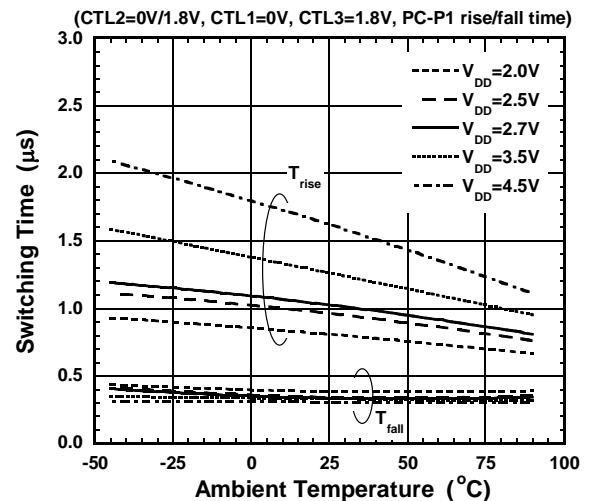
VSWR vs Temperature



P_{-0.2dB} vs Temperature

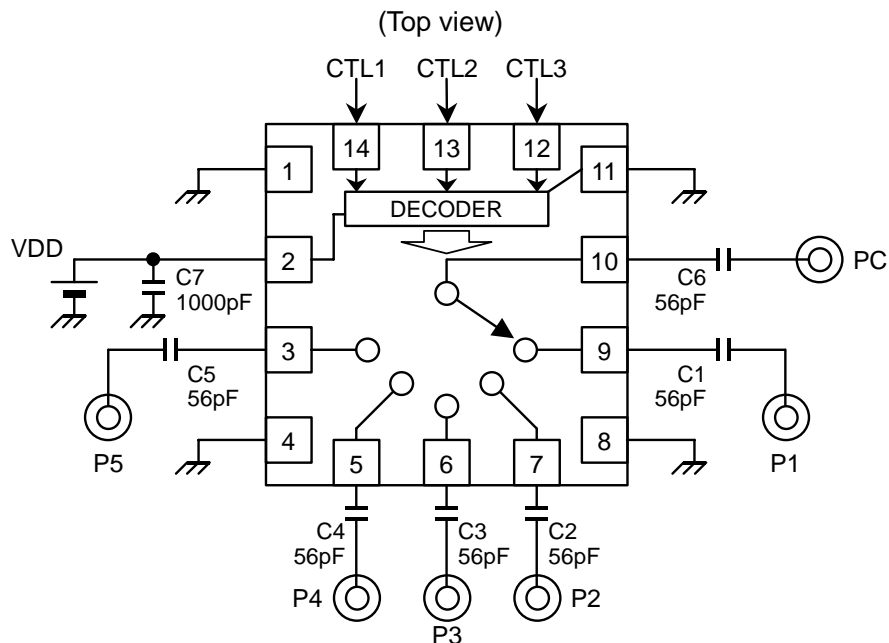


Switching Time vs Temperature



NJG1667MD7

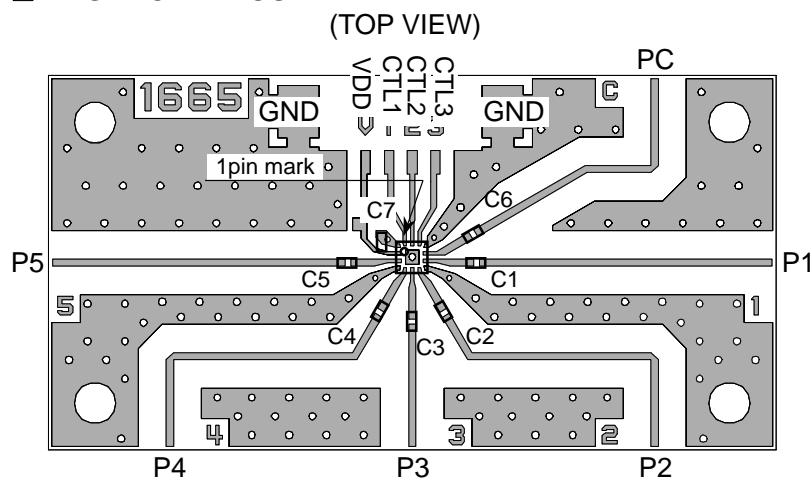
APPLICATION CIRCUIT



PARTS LIST

Part ID	Value	Notes
C1~C6	56pF	MURATA MFG (GRM15)
C7	1000pF	

TEST PCB LAYOUT



PCB SIZE=39.0 x 20.0mm
 PCB: FR-4, t=0.2mm
 CAPACITOR: size 1005
 STRIP LINE WIDTH=0.4mm

Losses of PCB and Connectors

Freq. (GHz)	Loss (dB)		
	PC-P1 PC-P5	PC-P2 PC-P4	PC-P3
1.0	0.41	0.43	0.36
2.0	0.62	0.65	0.52
2.5	0.74	0.79	0.61

PRECAUTIONS

- [1] The DC blocking capacitors should be placed at RF terminal of P1, P2, P3, P4, P5 and PC. Please choose appropriate capacitance values to the application frequency.
- [2] The bypass capacitor (C7) should be placed as close as possible to VDD terminal.
- [3] For good RF performance, all GND terminals are should be connected to PCB ground plane.

