

## 450MHz Band LNA GaAs MMIC

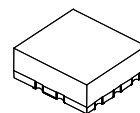
### GENERAL DESCRIPTION

NJG1128HB6 is a LNA IC designed for 450MHz band CDMA cellular phone. This IC has the function which bypasses LNA, and high gain mode or low gain mode can be chosen.

High IIP3 and a low noise are achieved at the High gain mode. And low current consumption can be achieved at the low gain mode because LNA enters the state of the standby.

A small and thin package of USB8 is adopted.

### PACKAGE OUTLINE

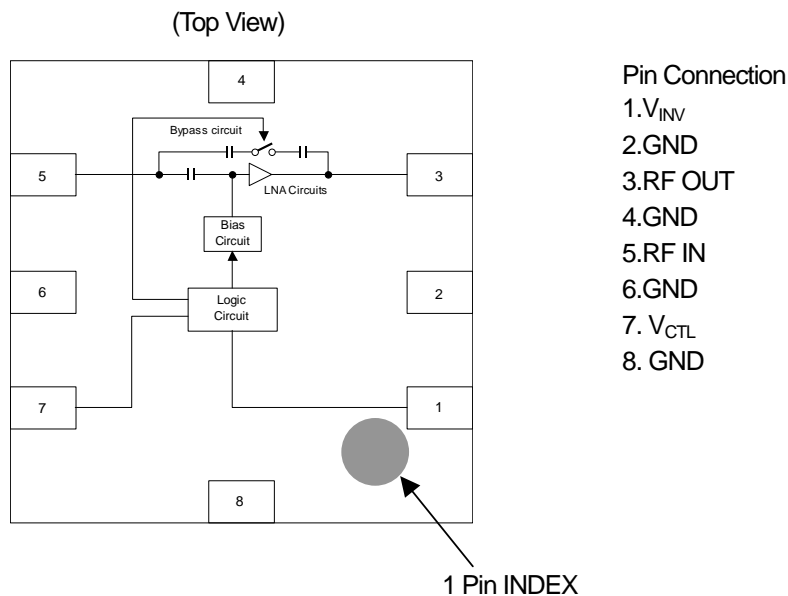


NJG1128HB6

### FEATURES

- Low voltage operation +2.8V typ.
- Low control voltage operation +1.85V typ.
  
- [LNA High Gain Mode]
- High Input IP3 +11.0dBm typ. @ f=460-470MHz
- Low noise figure 1.4dB typ. @ f=460-470MHz
  
- [LNA Low Gain Mode]
- Low current consumption 15uA typ.
- High Input IP3 +21.0dBm typ. @ f=460-470MHz
  
- Small & thin package USB8-B6 (Package size: 1.5mm x1.5mm x 0.55mm typ.)

### PIN CONFIGURATION



Note: Specifications and description listed in this catalog are subject to change without prior notice.

# NJG1128HB6

## ■ABSOLUTE MAXIMUM RATINGS

( $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ )

PARAMETERS	SYMBOL	CONDITIONS	RATINGS	UNITS
Supply voltage	$V_{DD}$		5.0	V
Inverter supply voltage	$V_{INV}$		5.0	V
Control voltage	$V_{CTL}$		5.0	V
Input power	$P_{in}$		+15	dBm
Power dissipation	$P_D$	on PCB board, at $T_{jmax}=150^{\circ}\text{C}$	160	mW
Operating temperature	$T_{opr}$		-40~+85	$^{\circ}\text{C}$
Storage temperature	$T_{stg}$		-55~+150	$^{\circ}\text{C}$

## ■ELECTRICAL CHARACTERISTICS 1 (DC CHARACTERISTICS)

(General Conditions:  $V_{DD}=V_{INV}=2.8\text{V}$ ,  $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ )

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating voltage	$V_{DD}$		2.65	2.80	2.95	V
Inverter supply voltage	$V_{INV}$		2.65	2.80	2.95	V
Control voltage (High)	$V_{CTL(H)}$		1.80	1.85	$V_{DD}+0.3$	V
Control voltage (Low)	$V_{CTL(L)}$		-0.3	0	0.3	V
Operating current1 (LNA High Gain Mode)	$I_{DD1}$	RF OFF, $V_{CTL}=1.85\text{V}$	-	10.0	16.0	mA
Operating current2 (LNA Low Gain Mode)	$I_{DD2}$	RFOFF, $V_{CTL}=0\text{V}$	-	1	5	$\mu\text{A}$
Inverter current1 (LNA High Gain Mode)	$I_{INV1}$	RF OFF, $V_{CTL}=1.85\text{V}$	-	150	240	$\mu\text{A}$
Inverter current2 (LNA Low Gain Mode)	$I_{INV2}$	RF OFF, $V_{CTL}=0\text{V}$	-	15	40	$\mu\text{A}$
Control current	$I_{CTL}$	RF OFF, $V_{CTL}=1.85\text{V}$	-	5	15	$\mu\text{A}$

## ■ELECTRICAL CHARACTERISTICS 2 (LNA High Gain Mode)

(General Conditions:  $V_{DD}=V_{INV}=2.8V$ ,  $V_{CTL}=1.85V$ ,  $f_{RF}=460-470MHz$ ,  $T_a=+25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$ )

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain1	Gain1		13.5	15.0	17.0	dB
Noise figure1	NF1	Exclude PCB & connector losses	-	1.4	1.8	dB
1dB gain compression output power1	P-1dB_1		+4.0	+9.0	-	dBm
3rd order Input Intercept Point1	IIP3_1	$f1=f_{RF}$ , $f2=f_{RF}+100kHz$ , $P_{in}=-25dBm$	+8.0	+11.0	-	dBm
RF IN VSWR1	VSWR <sub>i_1</sub>		-	1.5	2.0	
RF OUT VSWR1	VSWR <sub>o_1</sub>		-	2.3	2.7	

## ■ELECTRICAL CHARACTERISTICS 3 (LNA Low Gain Mode)

(General Conditions:  $V_{DD}=V_{INV}=2.8V$ ,  $V_{CTL}=0V$ ,  $f_{RF}=460-470MHz$ ,  $T_a=+25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$ )

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain2	Gain2		-5.0	-3.0	0	dB
Noise figure2	NF2	Exclude PCB & connector losses	-	3.0	4.5	dB
1dB gain compression output power2	P-1dB_2		+1.0	+8.0	-	dBm
3rd order Input Intercept Point2	IIP3_2	$f1=f_{RF}$ , $f2=f_{RF}+100kHz$ , $P_{in}=-12dBm$	+15.0	+21.0	-	dBm
RF IN VSWR2	VSWR <sub>i_2</sub>		-	2.3	2.7	
RF OUT VSWR2	VSWR <sub>o_2</sub>		-	1.5	2.0	

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## ■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	VINV	Supply voltage terminal for internal logic circuit (inverter).
2	GND	Ground terminal.
3	RFOUT	RF signal comes out from this terminal, and goes through an external matching circuit connected to this. Inductor L3 as shown in the application circuit is a part of an external matching circuit, and also provide DC power to LNA. Capacitor C3 as shown in the application circuit is a bypass capacitor.
4	GND	Ground terminal.
5	RFIN	RF input terminal. The RF signal is input through external matching circuit connected to this terminal. A DC blocking capacitor is not required.
6	GND	Ground terminal.
7	VCTL	Control port. A logic control signal is required to select High or Low gain mode of LNA. This terminal is set to more than +1.8V of logical high level for High gain mode of LNA, and set to -0.3~+0.3V of logical low level for Low gain mode.
8	GND	Ground terminal.

### CAUTION

- 1) Ground terminal (No.2, 4, 6, 8) should be connected to the ground plane as close as possible for excellent RF performance, because distance to GND makes parasitic inductance.

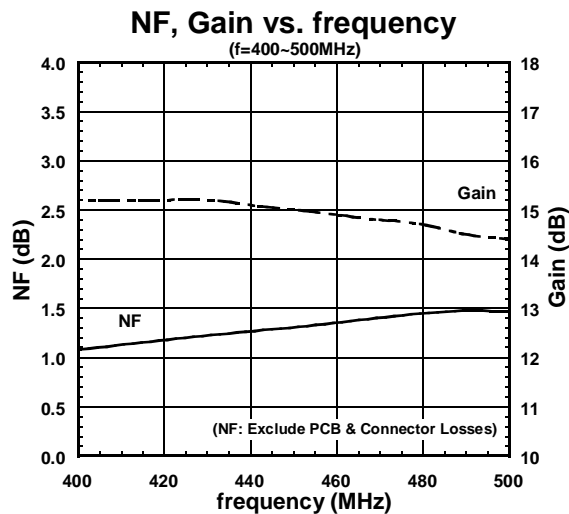
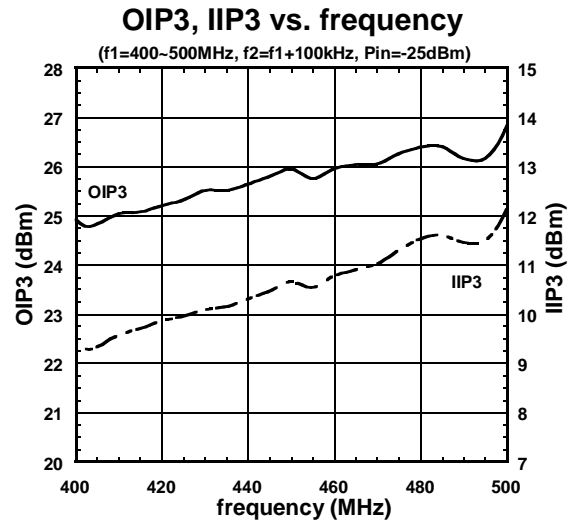
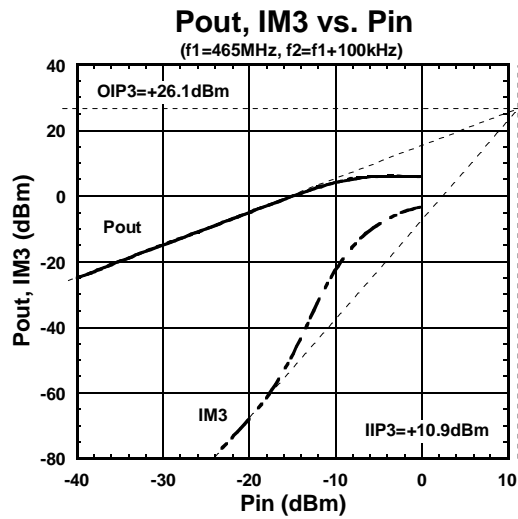
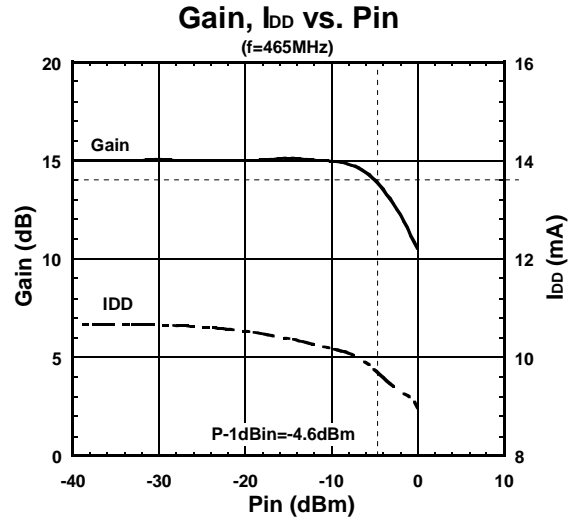
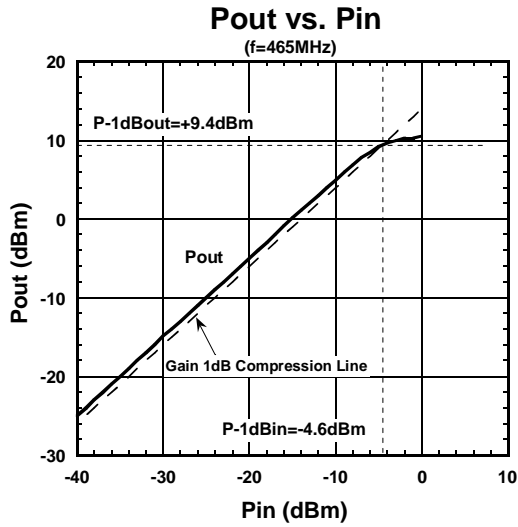
## ■ TRUTH TABLE

"H"= $V_{CTL}(H)$ , "L"= $V_{CTL}(L)$

$V_{CTL}$	Gain Mode	LNA
L	Low	bypass
H	High	pass

## ELECTRICAL CHARACTERISTICS (LNA High Gain Mode)

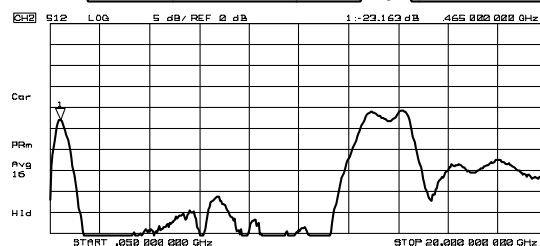
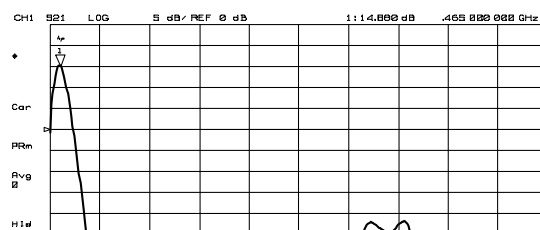
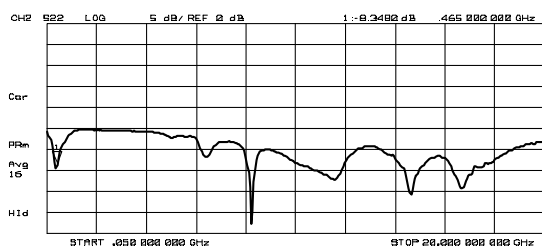
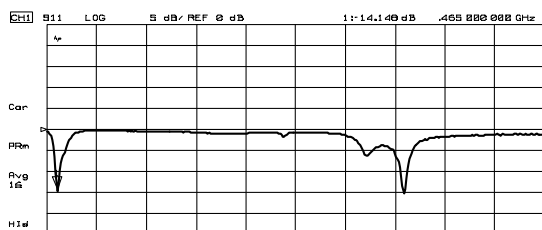
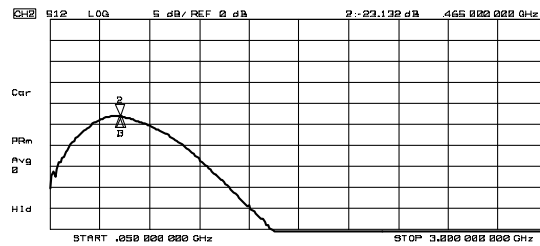
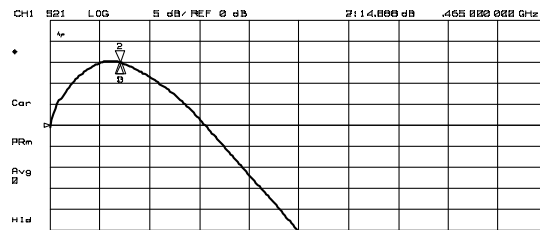
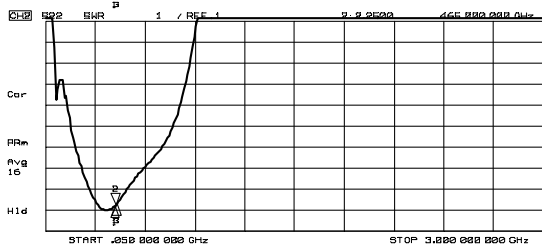
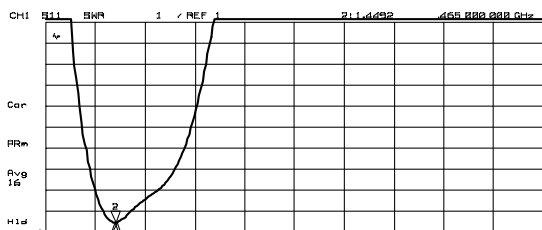
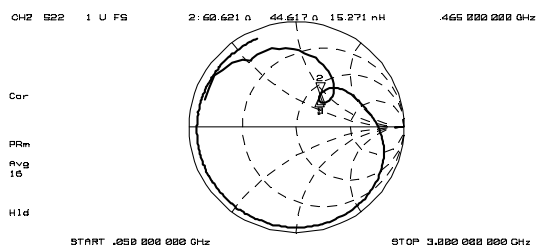
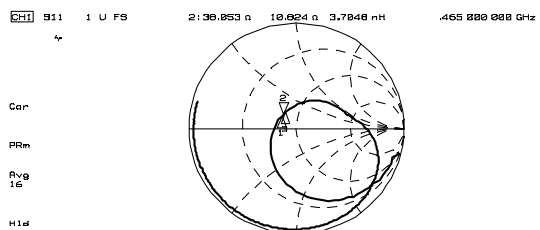
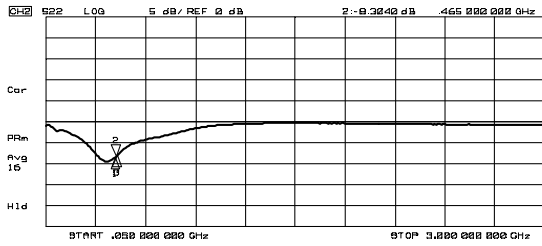
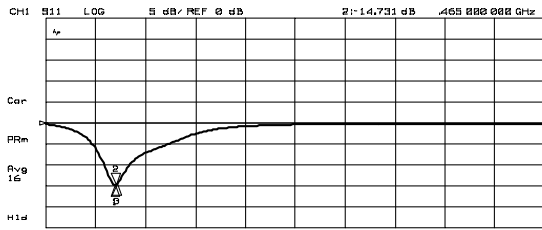
(General Conditions:  $T_a=+25^\circ\text{C}$ ,  $V_{DD}=V_{INV}=2.8\text{V}$ ,  $V_{CTL}=1.85\text{V}$ ,  $Z_S=Z_L=50\Omega$ )



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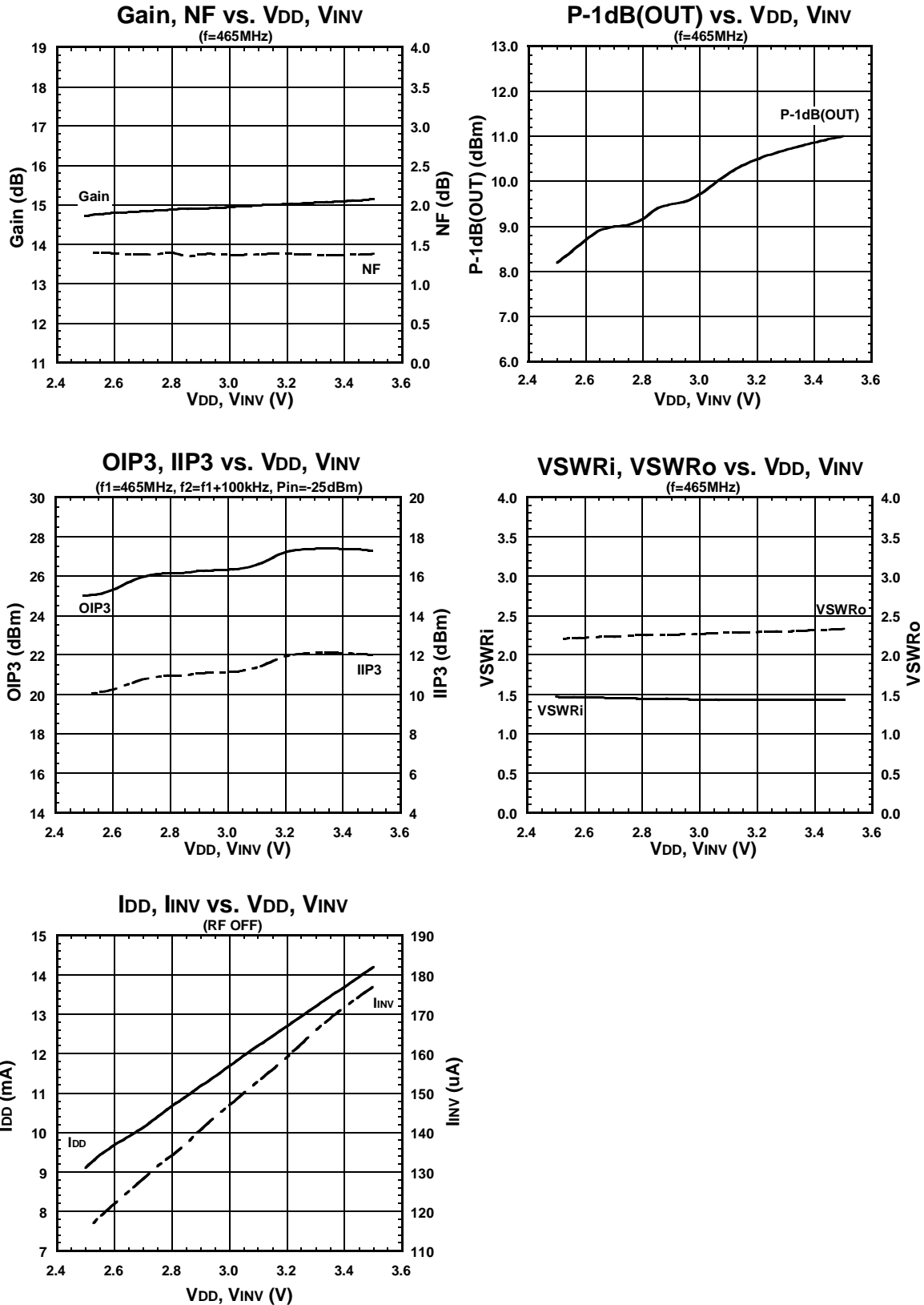
## ELECTRICAL CHARACTERISTICS (LNA High Gain Mode)

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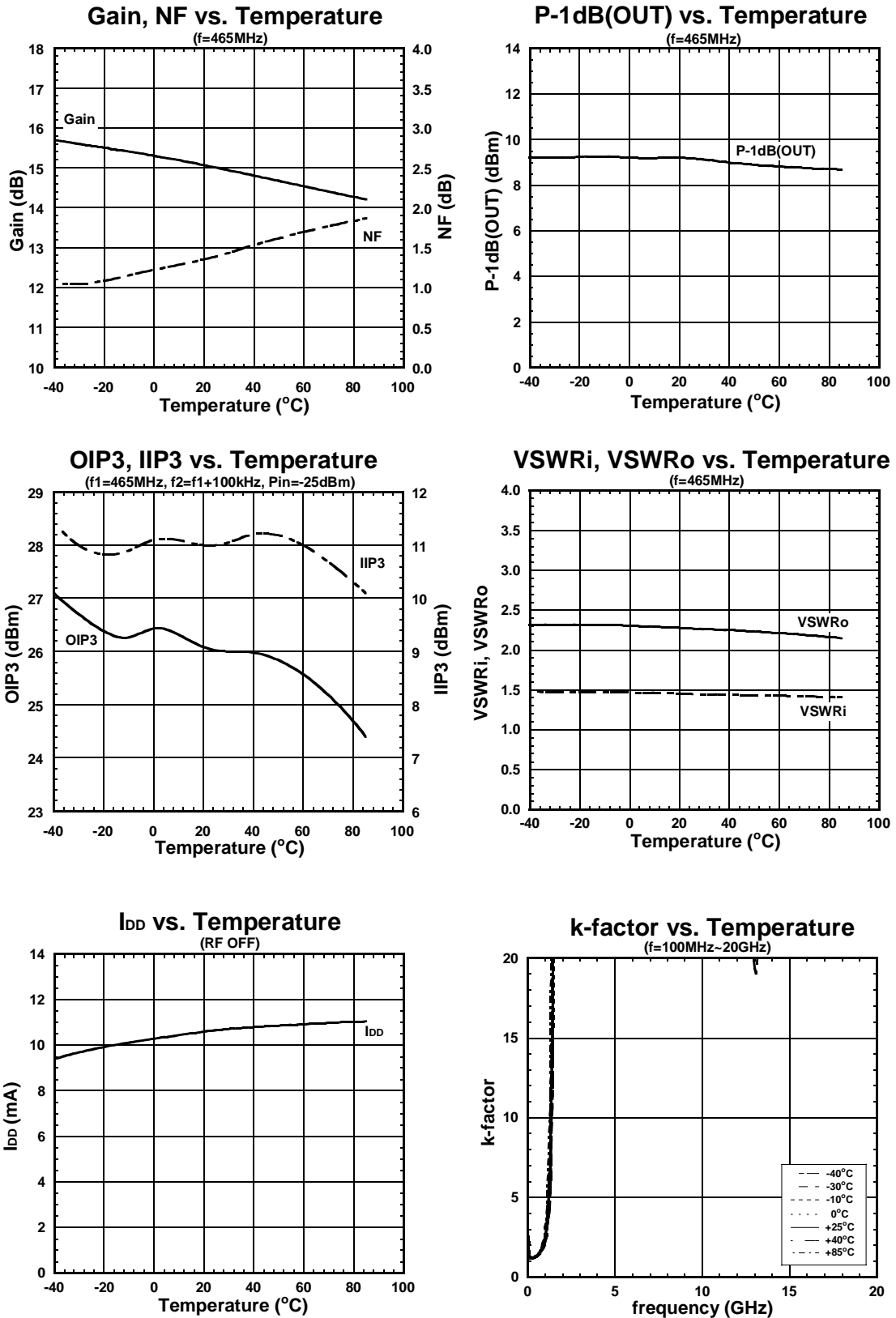
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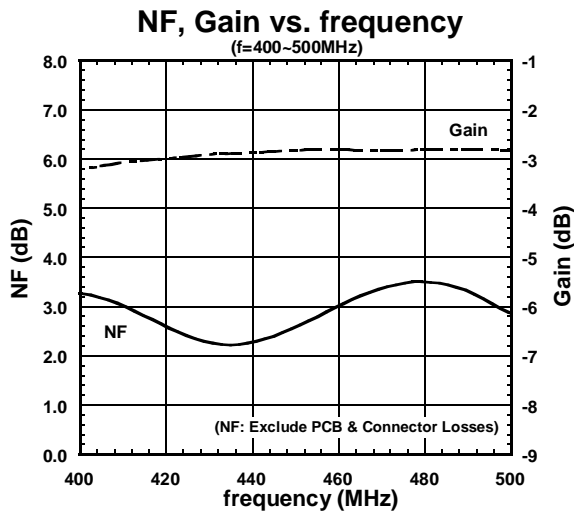
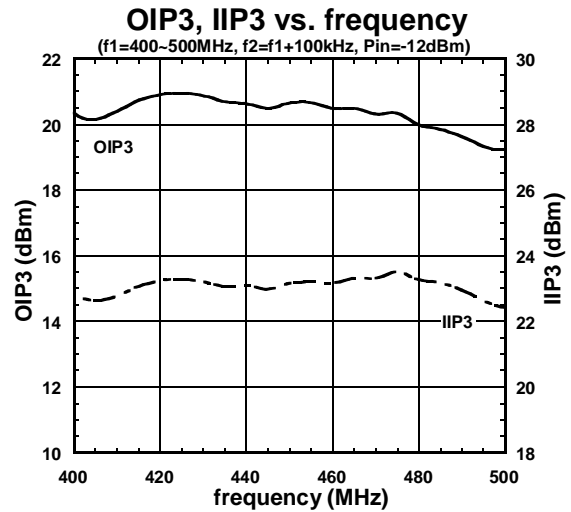
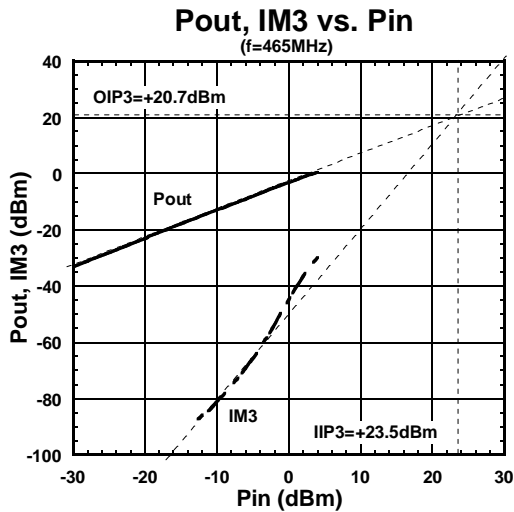
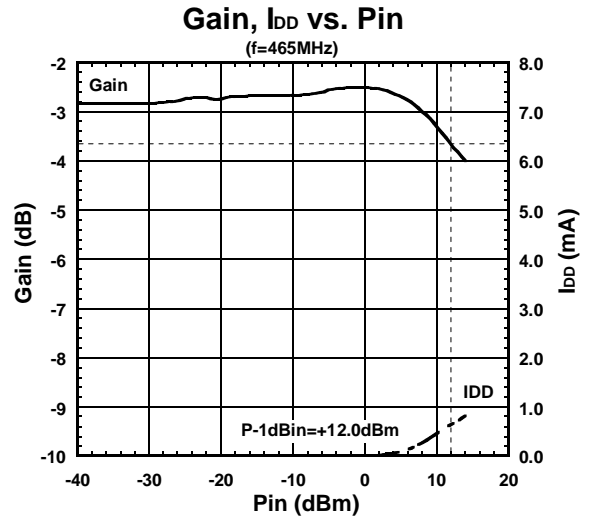
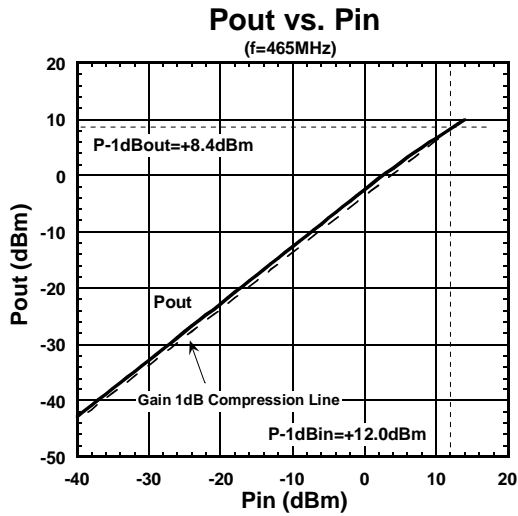
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## ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode)

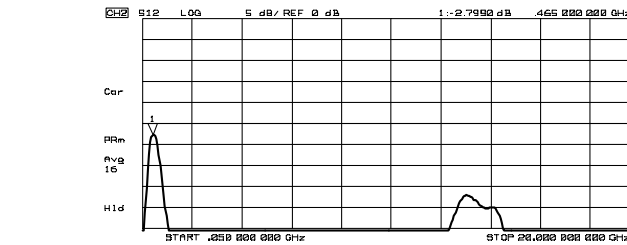
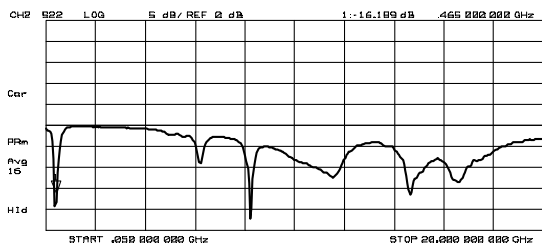
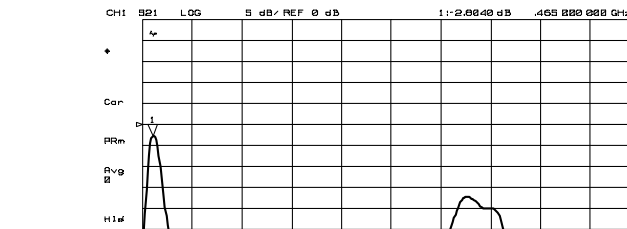
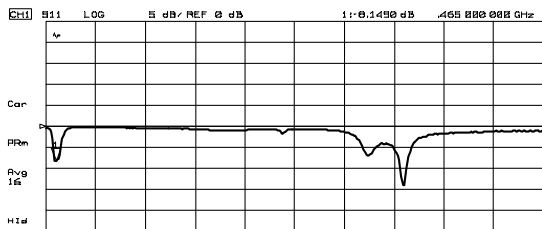
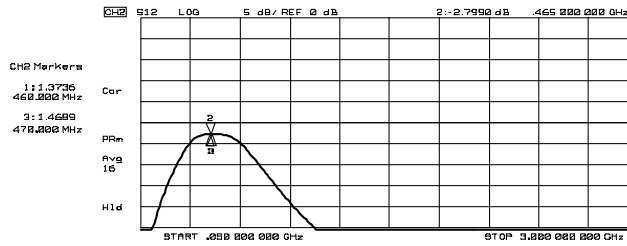
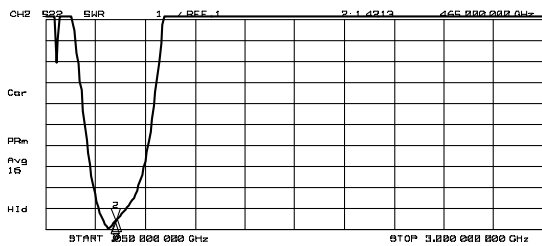
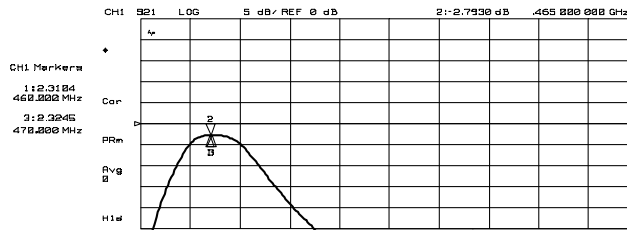
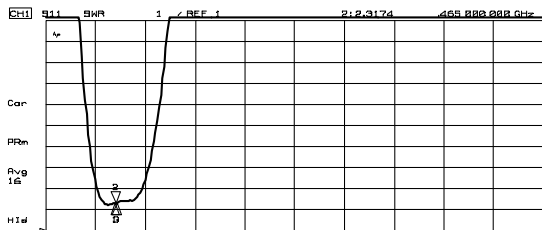
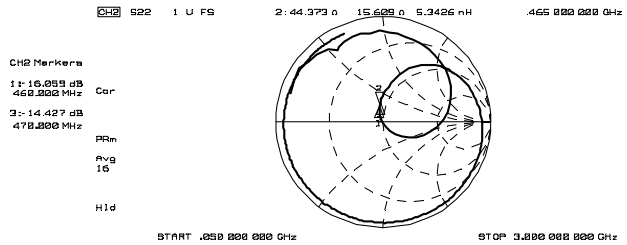
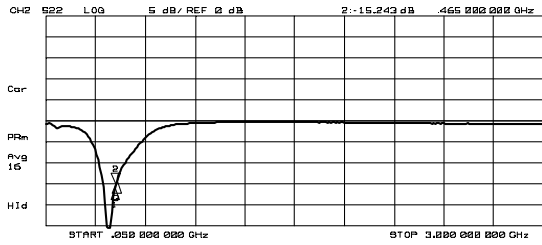
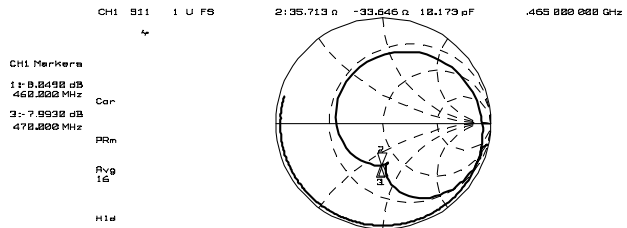
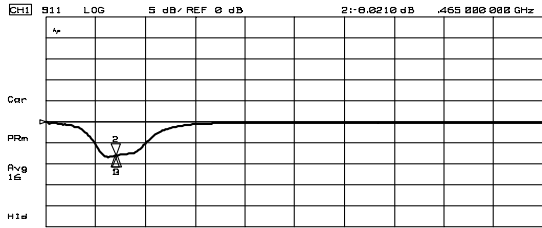
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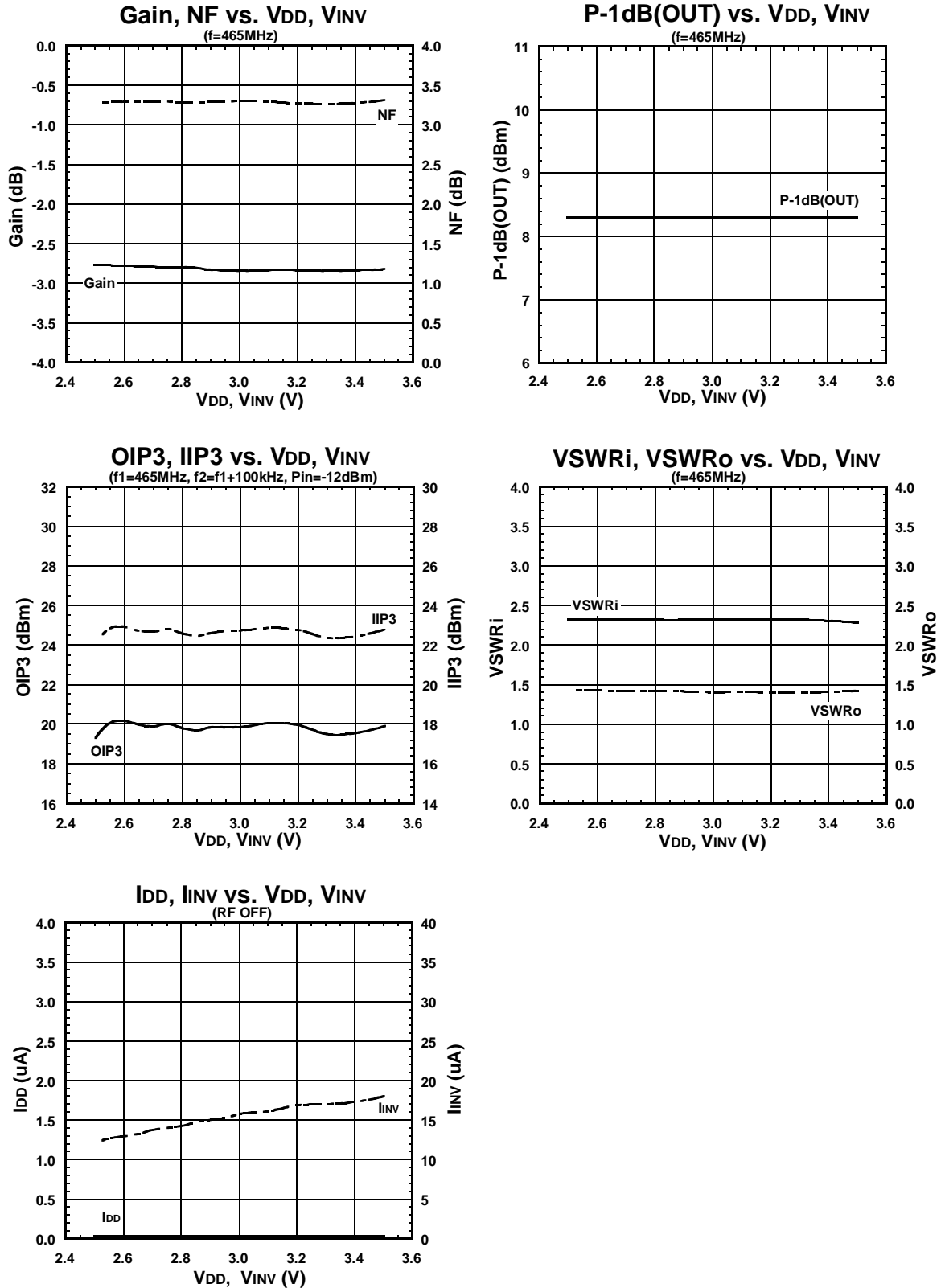
## ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode)

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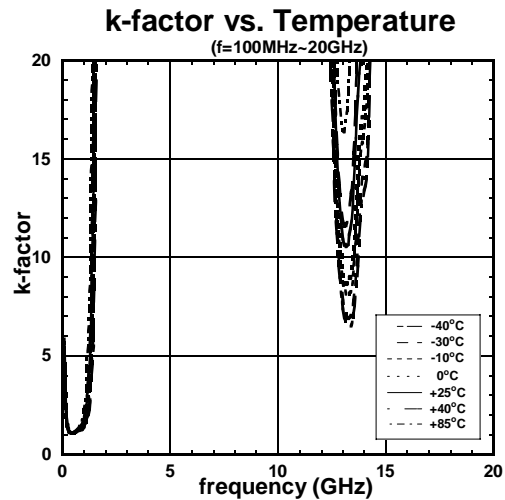
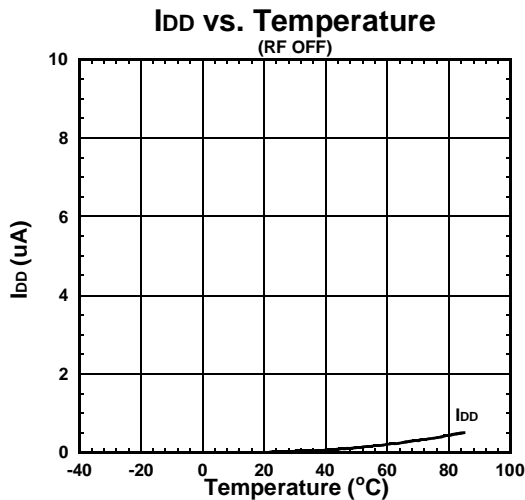
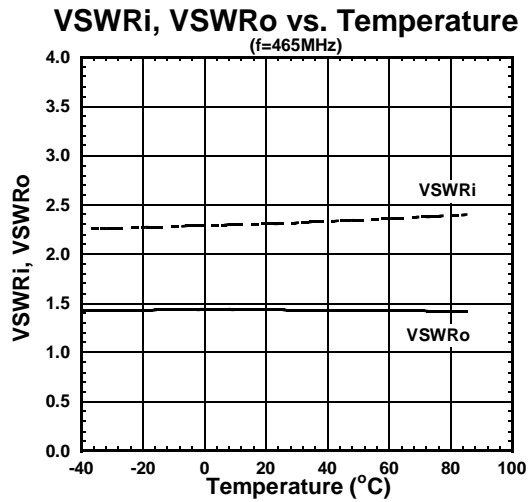
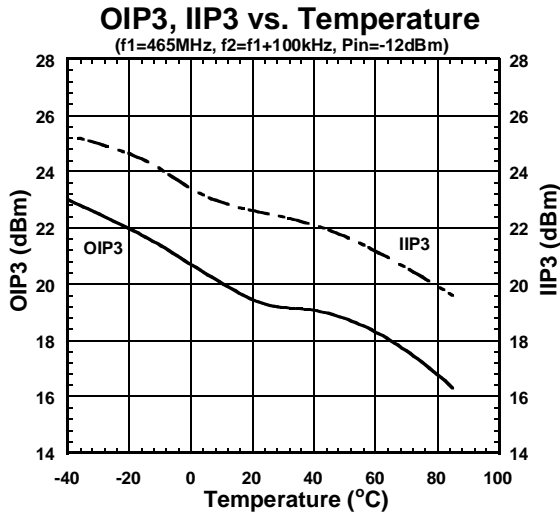
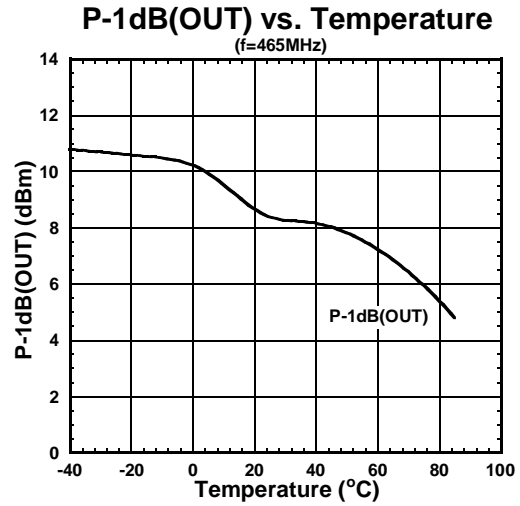
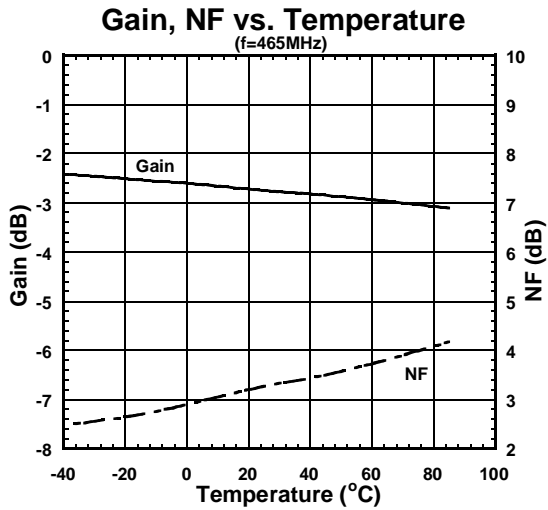
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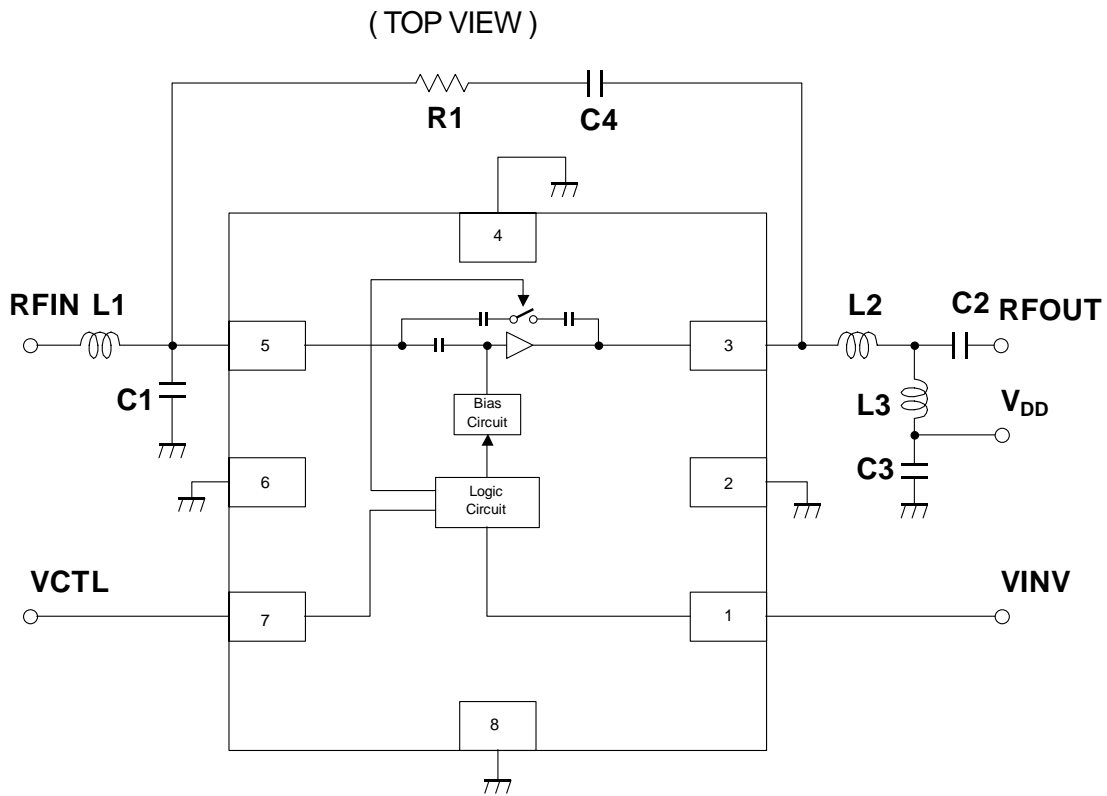
# NJG1128HB6

## ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode)

(General Conditions:  $T_a=+25^\circ\text{C}$ ,  $V_{DD}=V_{INV}=2.8\text{V}$ ,  $V_{CTL}=0\text{V}$ ,  $Z_s=Z_l=50\Omega$ )



## APPLICATION CIRCUIT

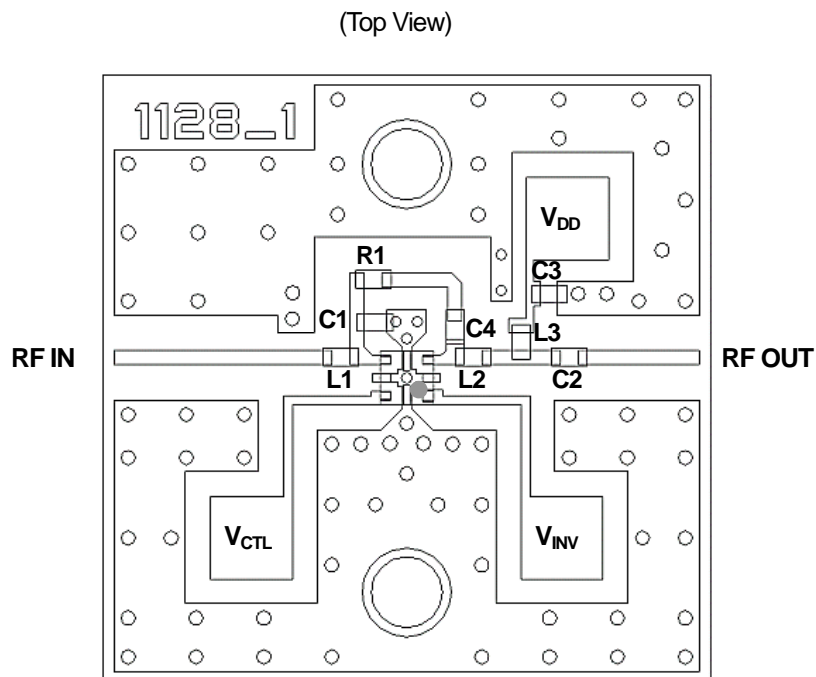


### Parts List

PART ID	CONSTANTS	COMMENT
L1	27nH	MURATA (LQW15A)
L2	33nH	TAIYO-YUDEN (HK1005)
L3	33nH	TAIYO-YUDEN (HK1005)
C1	0.75pF	MURATA (GRM15)
C2	1000pF	MURATA (GRM15)
C3	1000pF	MURATA (GRM15)
C4	2pF	MURATA (GRM15)
R1	2.7kΩ	1005size

# NJG1128HB6

## TEST PCB LAYOUT



PCB(FR-4),t=0.2mm

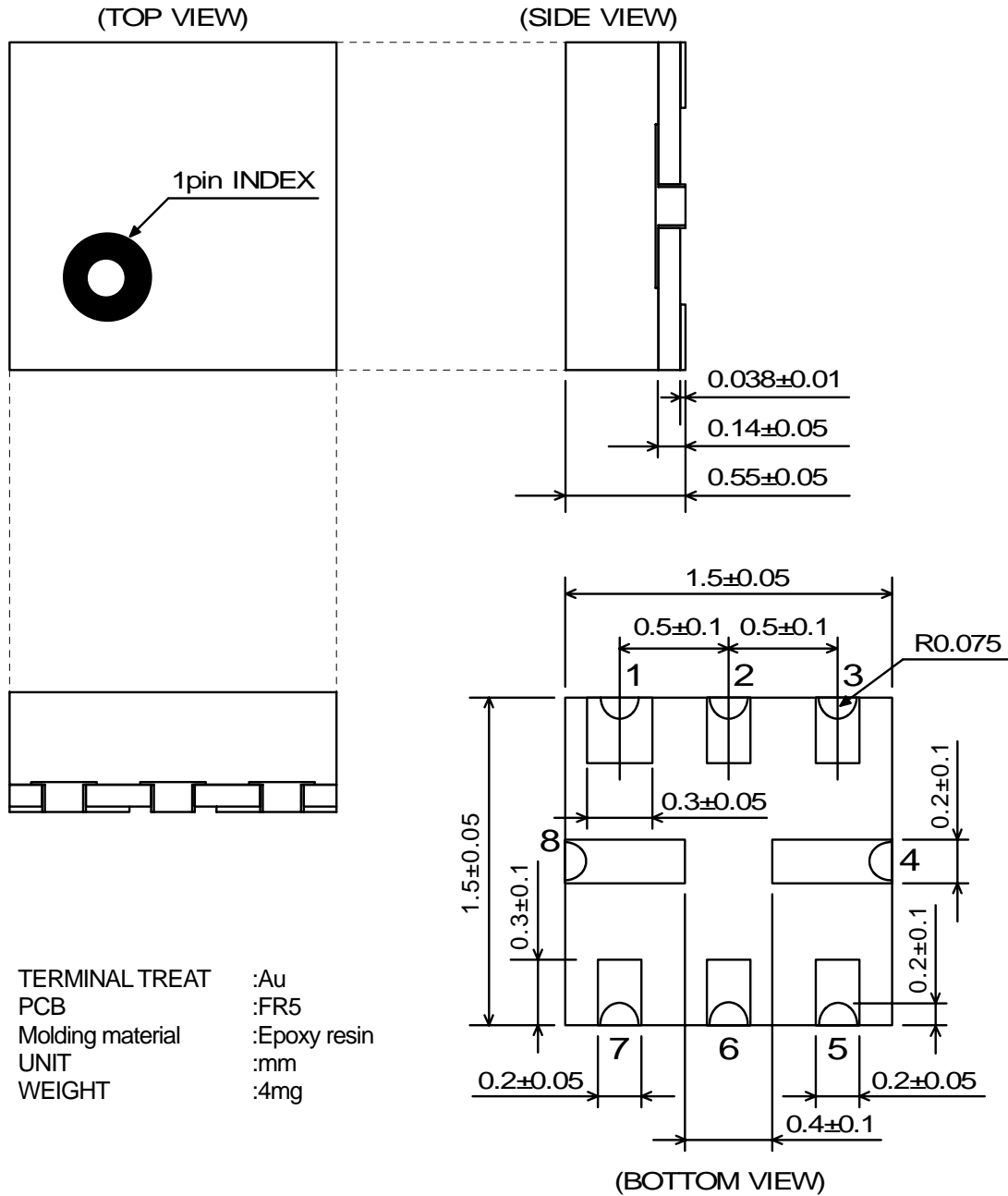
MICROSTRIP LINE WIDTH=0.4mm( $Z_0=50\Omega$ )

PCB SIZE : 17.0 X 17.0mm

### PRECAUTIONS

- [1] C1 and L1 form the input matching circuit. They should be placed close to RFIN terminal (5<sup>th</sup> pin).
- [2] L2 and L3 form the output matching circuit. They should be placed close to RFOUT terminal (3<sup>rd</sup> pin).
- [3] R1 and C4 form the negative feedback circuit. The pattern between RFOUT terminal (3<sup>rd</sup> pin) and RFIN terminal (5<sup>th</sup> pin) should be designed as short as possible for good performance.
- [4] C2 is a DC-blocking capacitor.
- [5] C3 is a bypass capacitor, it should be placed close to L3.
- [6] Ground terminals(2<sup>nd</sup>, 4<sup>th</sup>, 6<sup>th</sup> and 8<sup>th</sup> pin) should be connected to ground plane as close as possible for good performance.

## PACKAGE OUTLINE (USB8-B6)



### Cautions on using this product

- This product contains Gallium-Arsenide (GaAs) which is a harmful material.
- Do NOT eat or put into mouth.
  - Do NOT dispose in fire or break up this product.
  - Do NOT chemically make gas or powder with this product.
  - To waste this product, please obey the relating law of your country.

### [CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.