SPDT SWITCH GaAs MMIC

■GENERAL DESCRIPTION

NJG1533KB2 is a SPDT switch IC featured low insertion loss, medium handling power and high isolation.

This device is suitable for switching of Tx/Rx signals at sub-microwave applications.

This switch exhibits wide frequency range from 50MHz to 3.0GHz at low operating voltage of 2.5V, and is operated up to 25dBm at 3.0V operating voltage.

The ultra small & ultra thin FLP6 package is applied.

Reversed logic version of this device is NJG1523KB2.

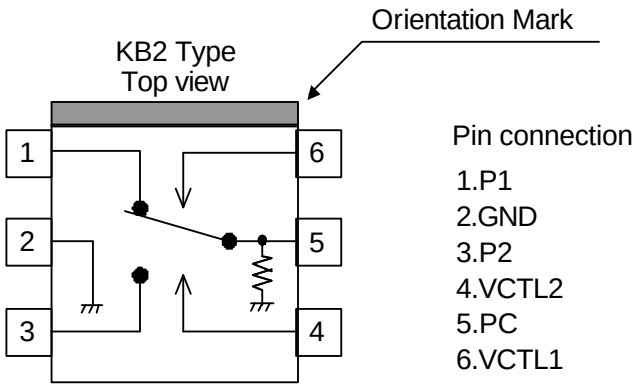
■PACKAGE OUTLINE

NJG1533KB2

■FEATURES

●Single low voltage control	+2.5~+6.5V	
●Low insertion loss	0.4dB	typ. @f=1GHz, P_{IN}=23dBm
	0.5dB	typ. @f=2GHz, P_{IN}=23dBm
●High isolation	29dB	typ. @f=2GHz, P_{IN}=23dBm
●Handling power	25dBm	max. @f=2GHz, V_{CTL}=3.0V
●Low current consumption	8uA	typ. @f=0.05~2.5GHz, P_{IN}=23dBm
●Ultra small & ultra thin package	FLP6-B2 (Package size: 2.0x2.1x0.75mm)	

■PIN CONFIGURATION



Pin connection

1.P1
2.GND
3.P2
4.VCTL2
5.PC
6.VCTL1

■TRUTH TABLE

"H"=$V_{CTL\ (H)}$, "L"=$V_{CTL\ (L)}$

V_{CTL1}	H	L	L	H
V_{CTL2}	L	H	L	H
PC – P1	OFF	ON	Insertion loss=17dB P1 return Loss=2dB	Insertion loss=18dB P1 return Loss=2dB
PC – P2	ON	OFF	Insertion loss=17dB P2 return Loss=2dB	Insertion loss=18dB P2 return Loss=2dB

Note: Reversed logic version of this device is NJG1523KB2.
The values of insertion losses and return losses are the typical values at 2GHz.

■ABSOLUTE MAXIMUM RATINGS

(T_a=25°C)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
Input Power	P_{in}	$V_{CTL\ (L)}$=0V, $V_{CTL\ (H)}$=2.7V	32	dBm
Control Voltage	V_{CTL}	$V_{CTL\ (H)}$-$V_{CTL\ (L)}$	7.5	V
Power Dissipation	P_D		450	mW
Operating Temp.	T_{opr}		-30~+85	°C
Storage Temp.	T_{stg}		-55~+125	°C

■ELECTRICAL CHARACTERISTICS

($V_{CTL\ (L)}$=0V, $V_{CTL\ (H)}$=2.7V, Z_S=Z_l=50Ω, T_a=25°C)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating voltage (LOW)	$V_{CTL\ (L)}$		-0.2	0	0.2	V
Operating voltage (HIGH)	$V_{CTL\ (H)}$		2.5	2.7	6.5	V
Control current	I_{CTL}	f=2.0GHz, P_{IN}=23dBm	-	8	14	uA
Insertion loss 1	LOSS1	f=1GHz, P_{IN}=23dBm	-	0.4	0.7	dB
Insertion loss 2	LOSS2	f=2GHz, P_{IN}=23dBm	-	0.5	0.8	dB
Isolation 1 (PC-P1, PC-P2, P1-P2)	ISL1	f=1GHz, P_{IN}=23dBm	27	29	-	dB
Isolation 2 (PC-P1, PC-P2, P1-P2)	ISL2	f=2GHz, P_{IN}=23dBm	26	29	-	dB
Maximum input power 1*	$P_{in}1$	$V_{CTL\ (H)}$=2.7V, f=2GHz	-	-	24.0	dBm
Maximum input power 2*	$P_{in}2$	$V_{CTL\ (H)}$=3.0V, f=2GHz	-	-	25.0	dBm
Maximum input power 3*	$P_{in}3$	$V_{CTL\ (H)}$=6.5V, f=2GHz	-	-	34.5	dBm
Pin at 1dB compression point	P_{-1dB}	f=2.0GHz	28	30.5	-	dBm
VSWR (PC, P1, P2)	VSWR	f=0.05~2.2GHz, ON State	-	1.4	1.6	
Switching time	T_{SW}	f_{in}=0.05~2.5GHz	-	20	-	ns

* Maximum input power: This value is defined as maximum input power of linear operating region or damage free operating region

■TERMINAL INFORMATION

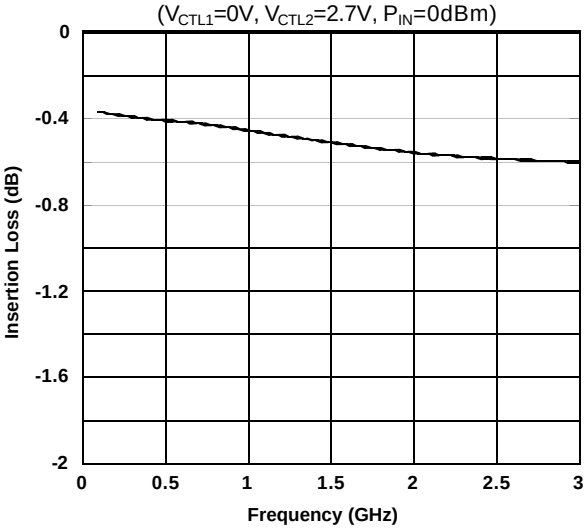
No.	SYMBOL	DESCRIPTION
1	P1	RF port. This port is connected with PC port by controlling 4th pin ($V_{CTL(H)}$) to 2.5~6.5V and 6th pin($V_{CTL(L)}$) to -0.2~+0.2V. An external capacitor is required to block the DC bias voltage of internal circuit. (50~100MHz: 0.01uF, 0.1~0.5GHz: 1000pF, 0.5~2.5GHz: 56pF)
2	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
3	P2	RF port. This port is connected with PC port by controlling 6th pin ($V_{CTL\ (H)}$) to 2.5~6.5V and 4th pin($V_{CTL(L)}$) to -0.2~+0.2V. An external capacitor is required to block the DC bias voltage of internal circuit. (50~100MHz: 0.01uF, 0.1~0.5GHz: 1000pF, 0.5~2.5GHz: 56pF)
4	VCTL2	Control port 2. The voltage of this port controls PC to P1 state. The 'ON' and 'OFF' state is toggled by controlling voltage of this terminal such as high-state (2.5~6.5V) or low-state (-0.2~+0.2V). The voltage of 6th pin have to be set to opposite state. The bypass capacitor has to be chosen to reduce switching time delay from 10pF~1000pF range.
5	PC	Common RF port. In order to block the DC bias voltage of internal circuit, an external capacitor is required. (50~100MHz:0.01uF, 0.1~0.5GHz: 1000pF, 0.5~2.5GHz: 56pF)
6	VCTL1	Control port 1. The voltage of this port controls PC to P2 state. The 'ON' and 'OFF' state is toggled by controlling voltage of this terminal such as high-state (2.5~6.5V) or low-state (-0.2~+0.2V). The voltage of 4th pin have to be set to opposite state. The bypass capacitor has to be chosen to reduce switching time delay from 10pF~1000pF range.

■ELECTRICAL CHARACTERISTICS

(f=0.1~3.0GHz, with Application circuit, Losses of external circuit are excluded)

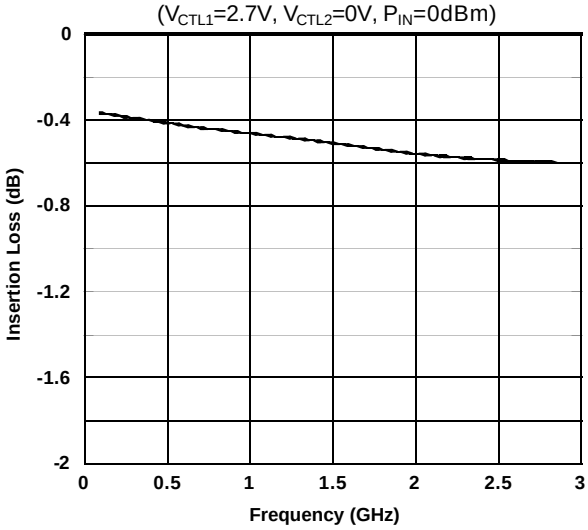
PC-P1 Insertion Loss vs. Frequency

(V_{CTL1}=0V, V_{CTL2}=2.7V, P_{IN}=0dBm)



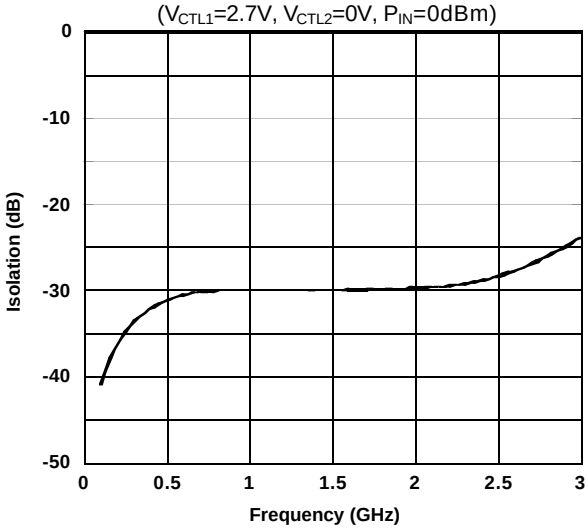
PC-P2 Insertion Loss vs. Frequency

(V_{CTL1}=2.7V, V_{CTL2}=0V, P_{IN}=0dBm)



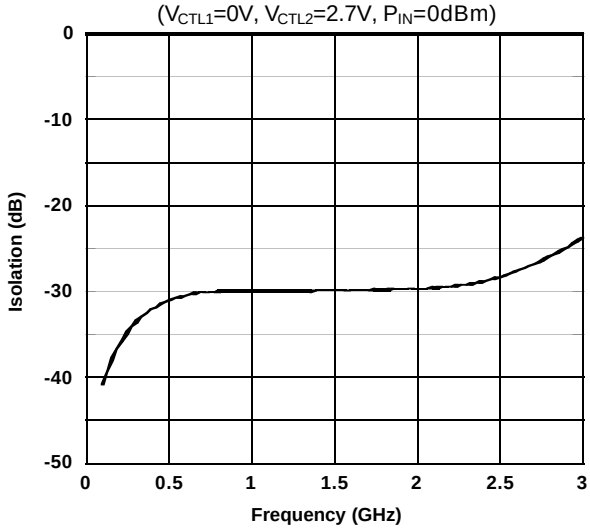
PC-P1 Isolation vs. Frequency

(V_{CTL1}=2.7V, V_{CTL2}=0V, P_{IN}=0dBm)



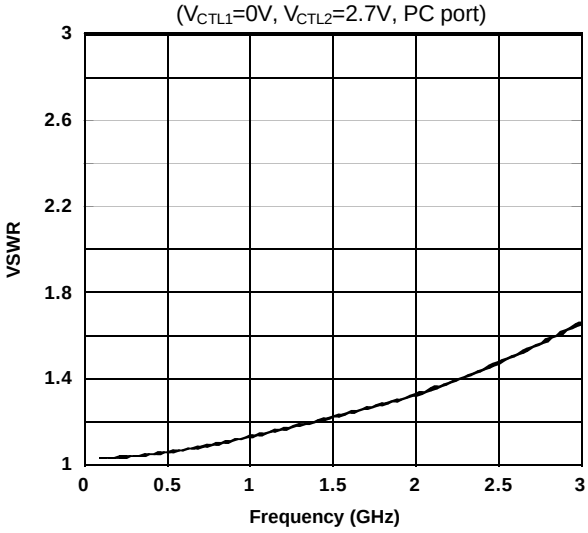
PC-P2 Isolation vs. Frequency

(V_{CTL1}=0V, V_{CTL2}=2.7V, P_{IN}=0dBm)



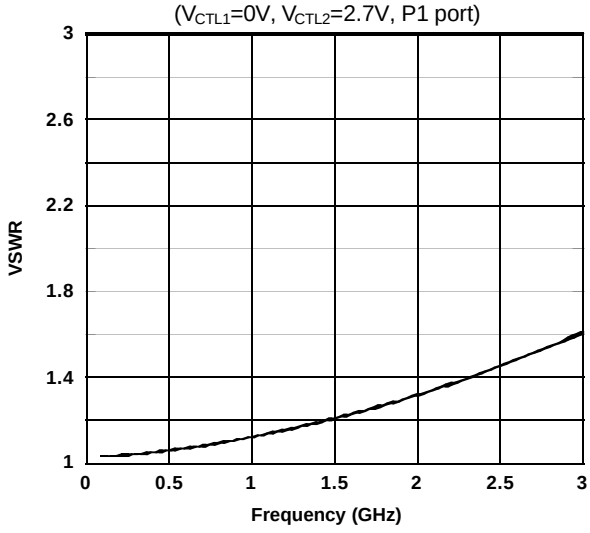
PC-P1 VSWR vs. Frequency

(V_{CTL1}=0V, V_{CTL2}=2.7V, PC port)



P1-PC VSWR vs. Frequency

(V_{CTL1}=0V, V_{CTL2}=2.7V, P1 port)

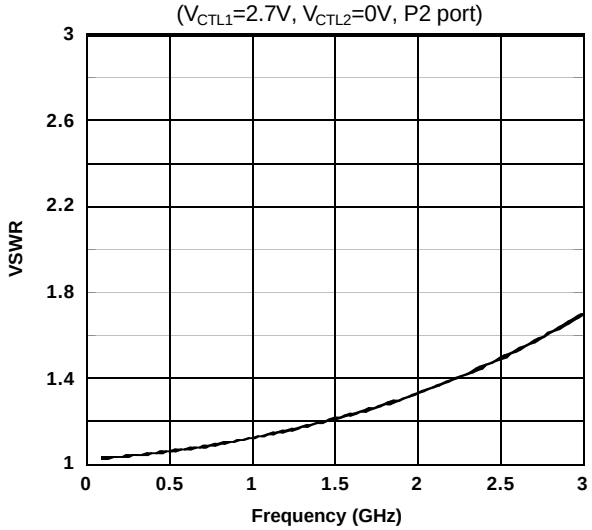


■ELECTRICAL CHARACTERISTICS

(with application circuit, without DC Blocking Capacitor, Losses of external circuit are excluded)

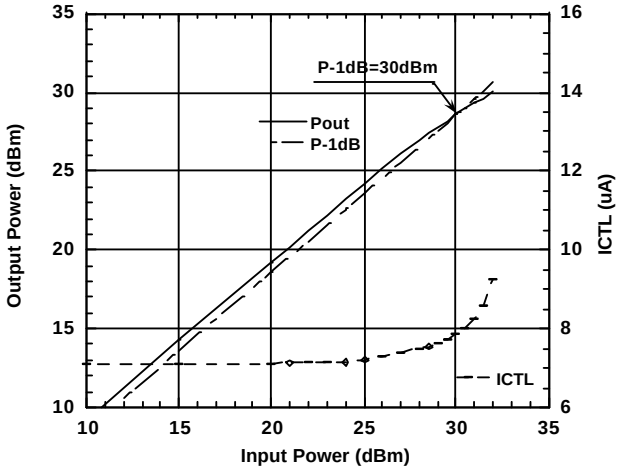
P2-PC VSWR vs. Frequency

(V_{CTL1}=2.7V, V_{CTL2}=0V, P2 port)



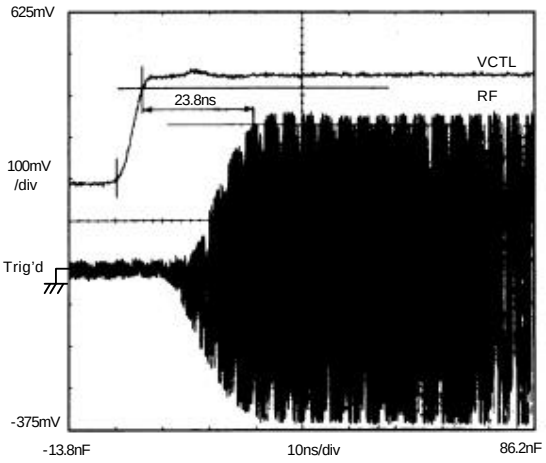
Input Power vs. Output Power,

($V_{CTL(L)}$=0V, $V_{CTL(H)}$=2.7V)



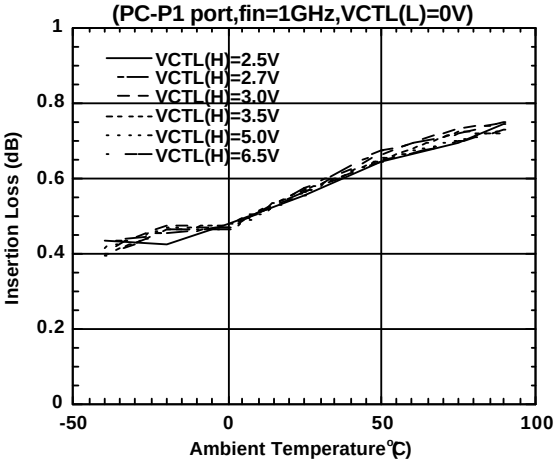
Switching Speed

($V_{CTL\ (L)}$=0V, $V_{CTL\ (H)}$=2.7V)



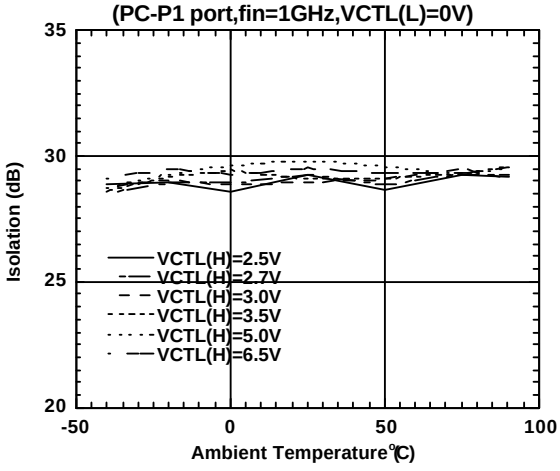
Insertion Loss vs. Ambient Temperature

(PC-P1 port,fin=1GHz,VCTL(L)=0V)



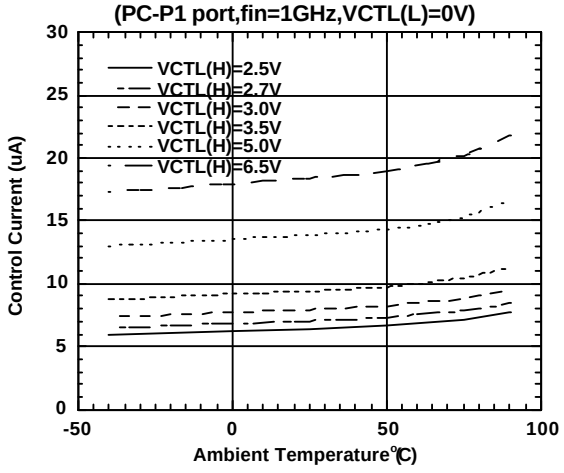
Isolation vs. Ambient Temperature

(PC-P1 port,fin=1GHz,VCTL(L)=0V)



ICTL vs. Ambient Temperature

(PC-P1 port,fin=1GHz,VCTL(L)=0V)

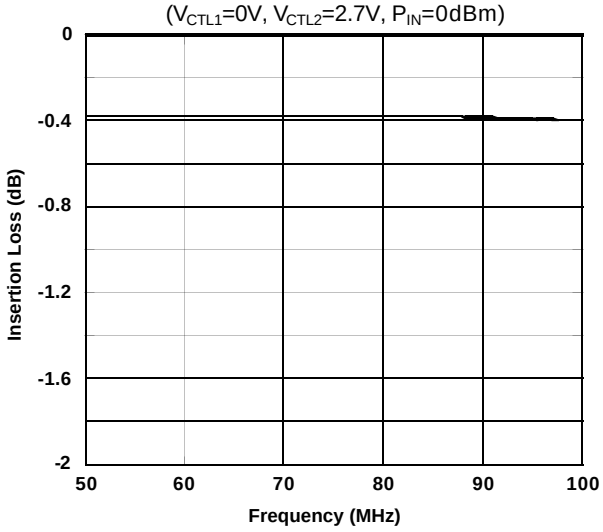


■ELECTRICAL CHARACTERISTICS

(f=50~100MHz, with Application circuit (Parts list 1), Losses of PCB, connector and DC blocking capacitor are included)

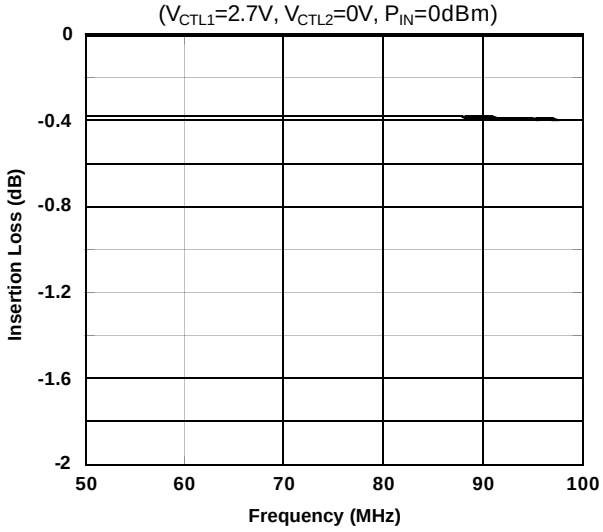
PC-P1 Insertion Loss vs. Frequency

(V_{CTL1}=0V, V_{CTL2}=2.7V, P_{IN}=0dBm)



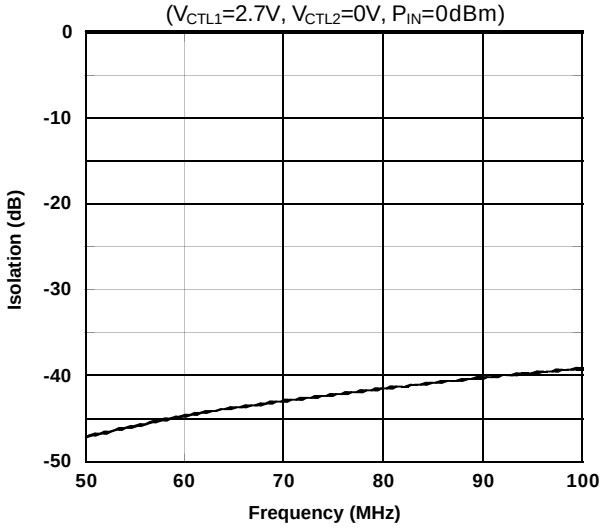
PC-P2 Insertion Loss vs. Frequency

(V_{CTL1}=2.7V, V_{CTL2}=0V, P_{IN}=0dBm)



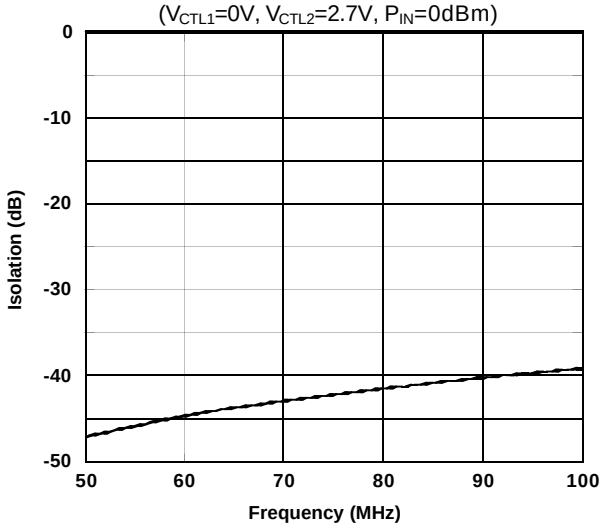
PC-P1 Isolation vs. Frequency

(V_{CTL1}=2.7V, V_{CTL2}=0V, P_{IN}=0dBm)



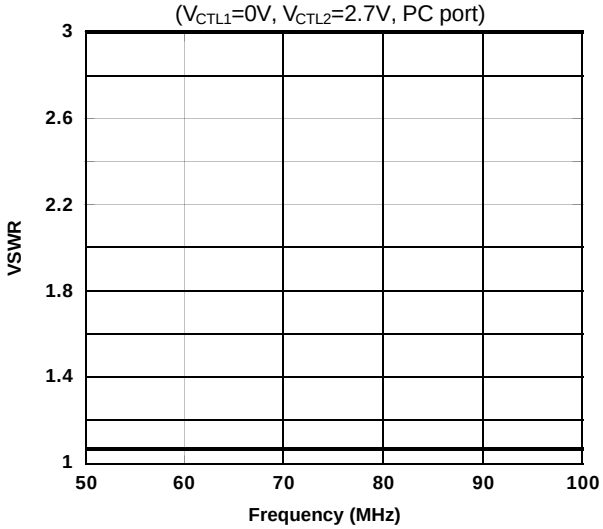
PC-P2 Isolation vs. Frequency

(V_{CTL1}=0V, V_{CTL2}=2.7V, P_{IN}=0dBm)



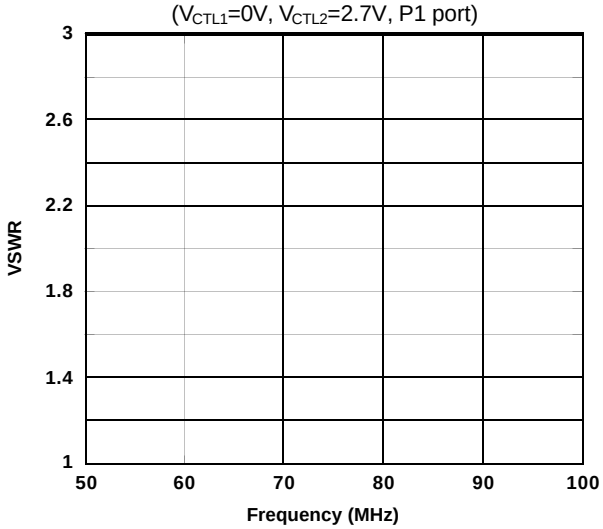
PC-P1 VSWR vs. Frequency

(V_{CTL1}=0V, V_{CTL2}=2.7V, PC port)



P1-PC,P2-PC VSWR vs. Frequency

(V_{CTL1}=0V, V_{CTL2}=2.7V, P1 port)

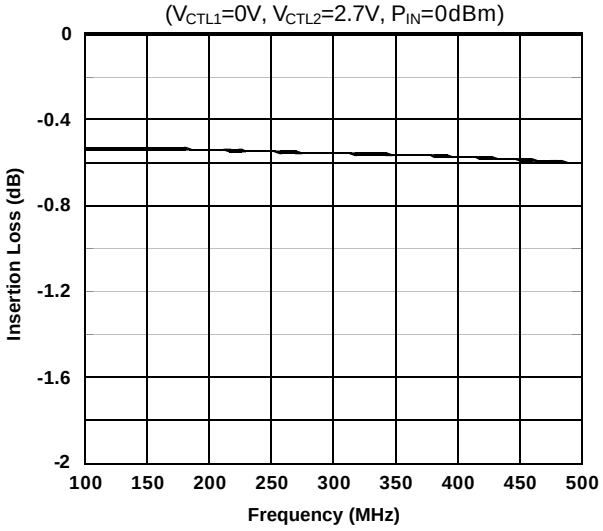


■ELECTRICAL CHARACTERISTICS

(f=100~500MHz, with Application circuit (Parts list 2), Losses of PCB, connector and DC blocking capacitor are included)

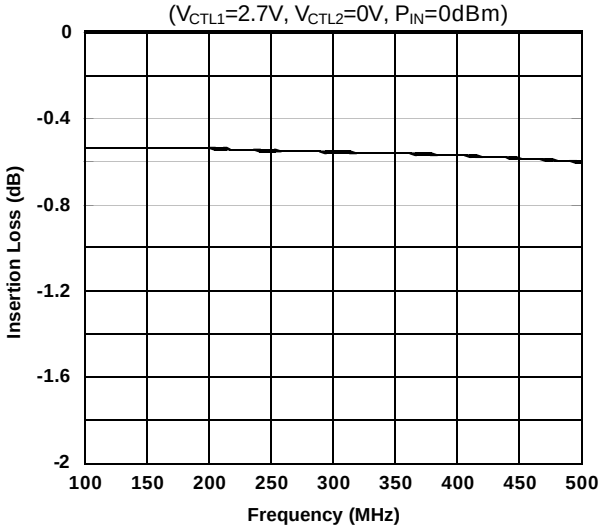
PC-P1 Insertion Loss vs. Frequency

(V_{CTL1}=0V, V_{CTL2}=2.7V, P_{IN}=0dBm)



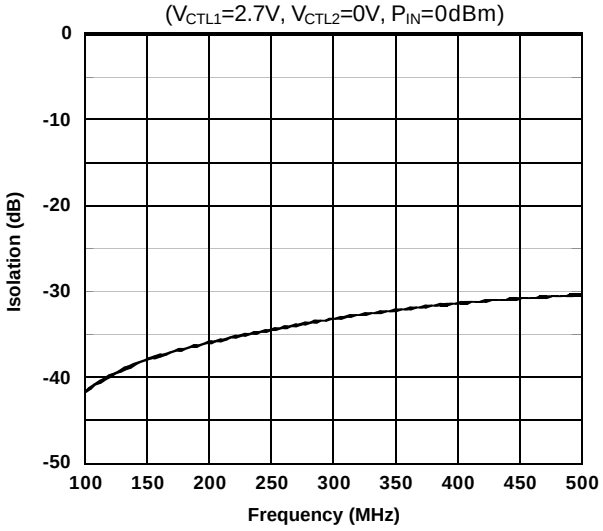
PC-P2 Insertion Loss vs. Frequency

(V_{CTL1}=2.7V, V_{CTL2}=0V, P_{IN}=0dBm)



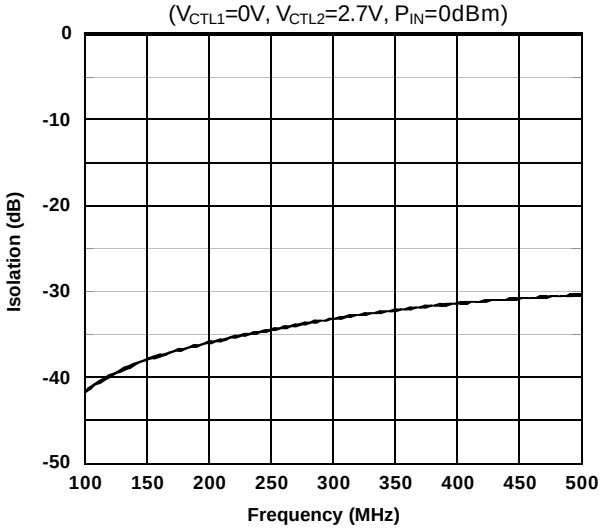
PC-P1 Isolation vs. Frequency

(V_{CTL1}=2.7V, V_{CTL2}=0V, P_{IN}=0dBm)



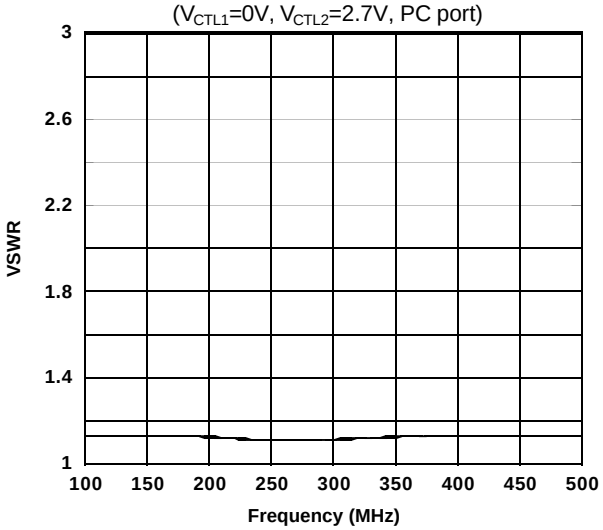
PC-P2 Isolation vs. Frequency

(V_{CTL1}=0V, V_{CTL2}=2.7V, P_{IN}=0dBm)



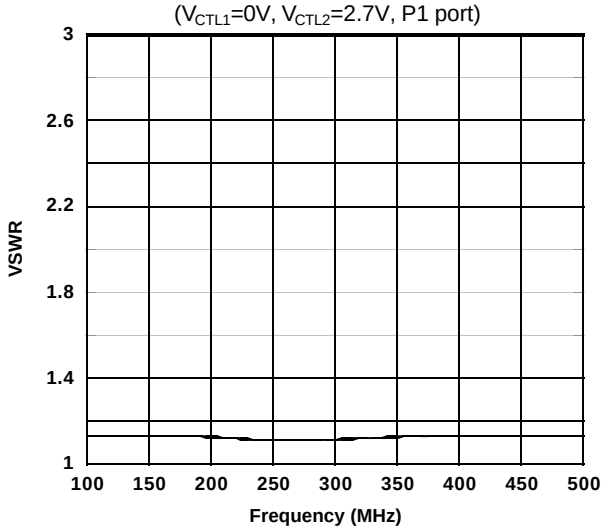
PC-P1 VSWR vs. Frequency

(V_{CTL1}=0V, V_{CTL2}=2.7V, PC port)



PC-P1,P2-PC VSWR vs. Frequency

(V_{CTL1}=0V, V_{CTL2}=2.7V, P1 port)

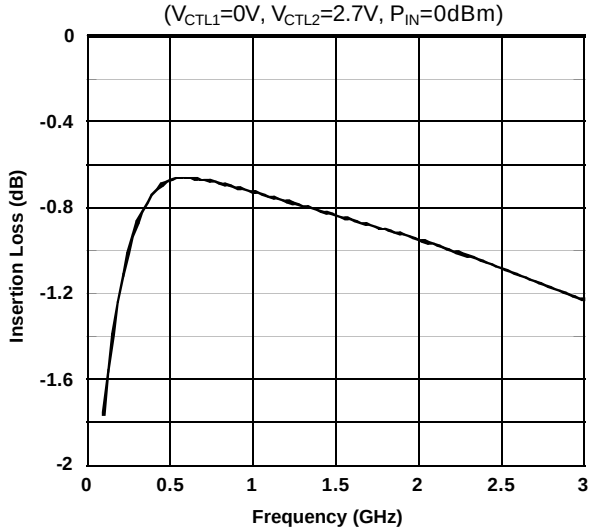


■ELECTRICAL CHARACTERISTICS

(f=0.1~3.0GHz, with Application circuit (Parts list 3), Losses of PCB, connector and DC blocking capacitor are included)

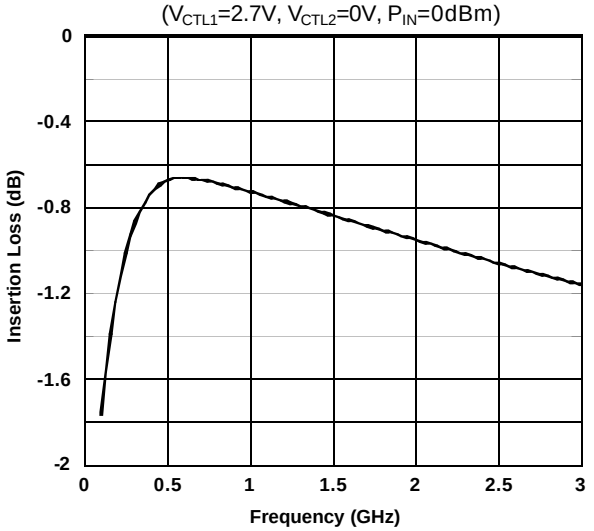
PC-P1 Insertion Loss vs. Frequency

(V_{CTL1}=0V, V_{CTL2}=2.7V, P_{IN}=0dBm)



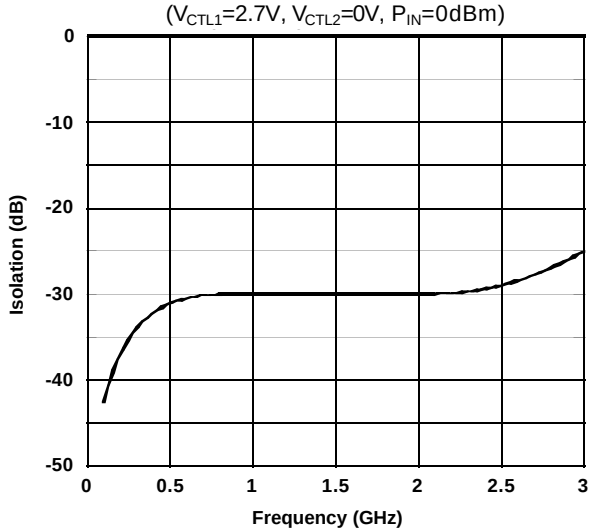
PC-P2 Insertion Loss vs. Frequency

(V_{CTL1}=2.7V, V_{CTL2}=0V, P_{IN}=0dBm)



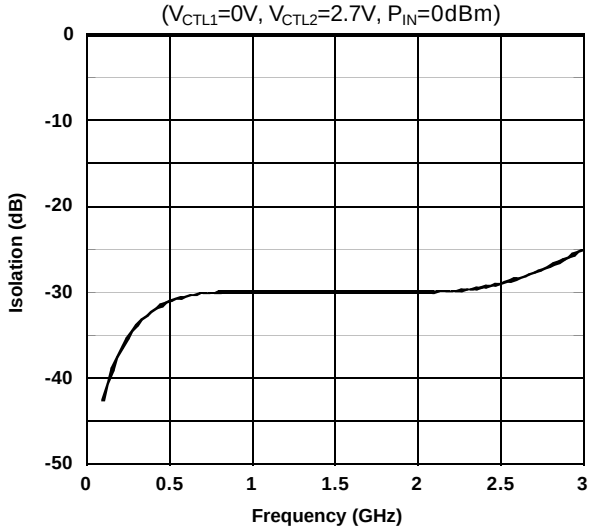
PC-P1 Isolation vs. Frequency

(V_{CTL1}=2.7V, V_{CTL2}=0V, P_{IN}=0dBm)



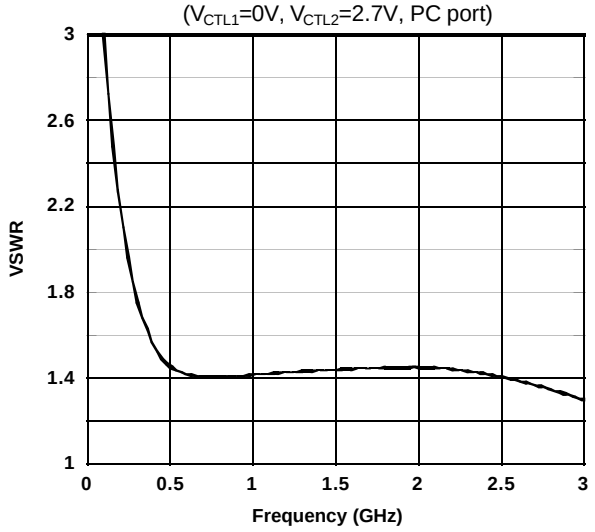
PC-P2 Isolation vs. Frequency

(V_{CTL1}=0V, V_{CTL2}=2.7V, P_{IN}=0dBm)



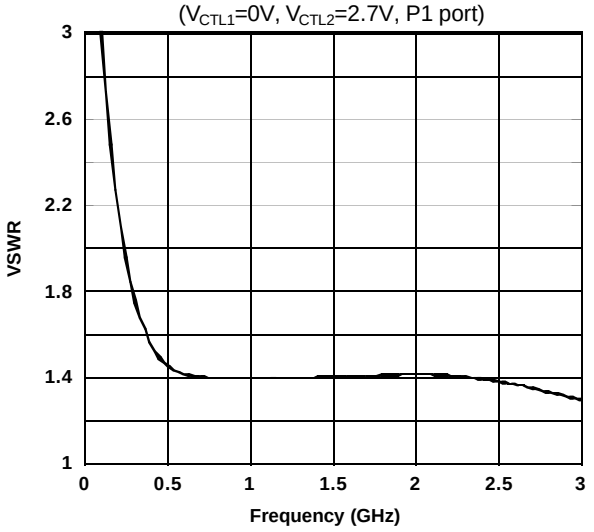
PC-P1 VSWR vs. Frequency

(V_{CTL1}=0V, V_{CTL2}=2.7V, PC port)



P1-PC,P2-PC VSWR vs. Frequency

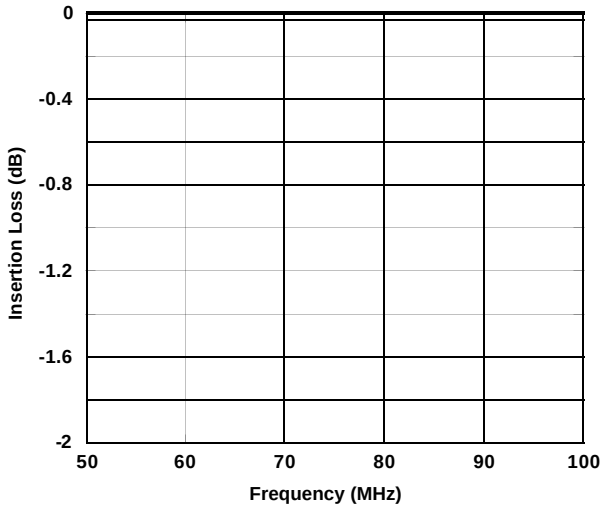
(V_{CTL1}=0V, V_{CTL2}=2.7V, P1 port)



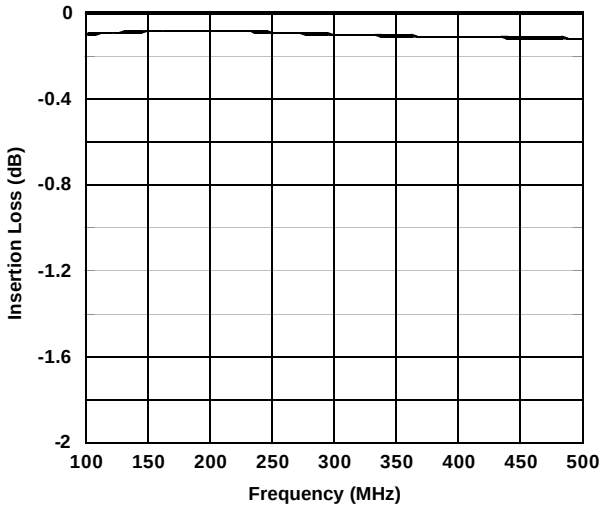
■ELECTRICAL CHARACTERISTICS

(Losses of PCB, connector and DC blocking capacitor at each frequency.)

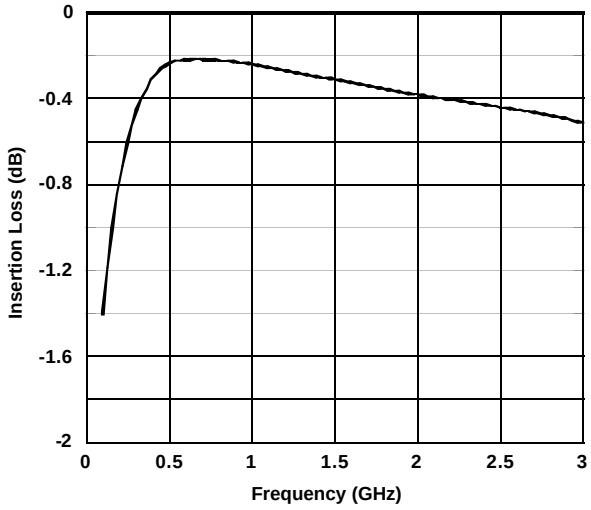
PCB Through Loss vs. Frequency
(Frequency:50MHz-100MHz)



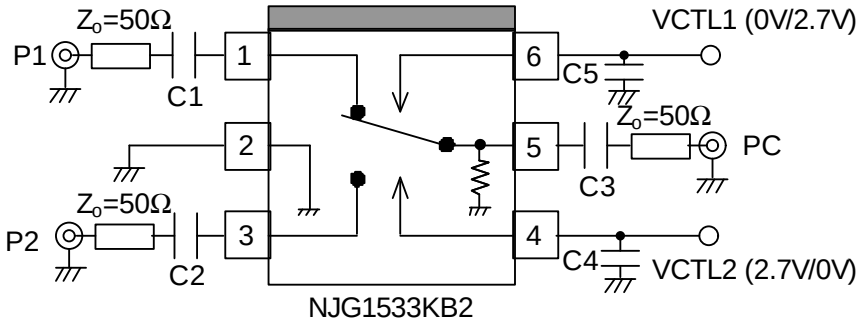
PCB Through Loss vs. Frequency
(Frequency:100MHz-500MHz)



PCB Through Loss vs. Frequency
(Frequency:100MHz-3GHz)



■APPLICATION CIRCUIT

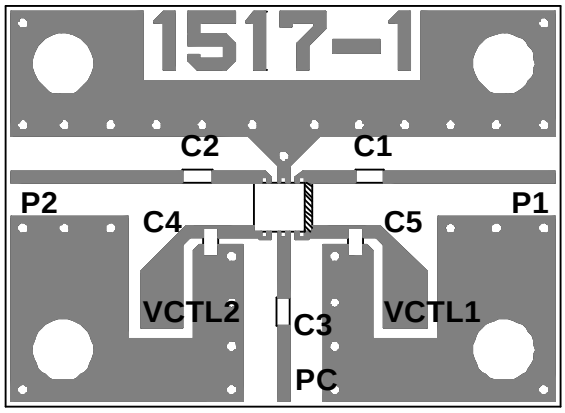


Parts List

Parts number	List 1	List 2	List 3	Notes
	50~100MHz	0.1~0.5GHz	0.5~2.5GHz	
C1~C3	0.01uF	1000pF	56pF	GRM36 MURATA
C4, C5	10pF	10pF	10pF	GRM36 MURATA

■RECOMMENDED PCB DESIGN

(TOP VIEW)



PCB SIZE=19.4x14.0mm
PCB: FR-4, t=0.2mm
CAPACITOR: size 1005
STRIPLINE WIDTH=0.4mm

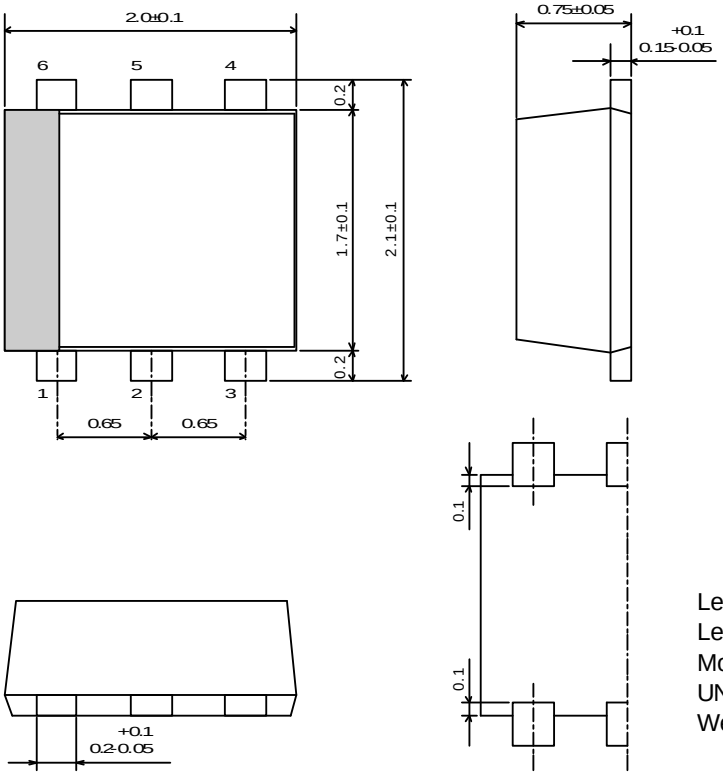
PRECAUTIONS

[1] The DC blocking capacitors have to be placed at RF terminal of P1, P2 and PC. Please choose appropriate capacitance values to the application frequency.

[2]To reduce stlipline influence on RF characteristics, please locate bypass capacitors (C4, C5) close to each terminals.

[3]For good isolation, the GND terminal (2^{nd} pin) must be placed possibly close to ground plane of substrate, and through holes for GND should be placed near by the pin connection.

■ PACKAGE OUTLINE (FLP6-B2)



Lead material	: Copper
Lead surface finish	: Solder plating
Molding material	: Epoxy resin
UNIT	: mm
Weight	: 6.5mg

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.