CV221-2A

1.9 – 2.7 GHz Dual-Branch Downconverter

Product Features

- High dynamic range downconverter with integrated LO and IF amplifiers
- Dual channels for diversity
- +28 dBm Input IP3
- +11.5 dBm Input P1dB
- RF: 1900 – 2700 MHz
- IF: 65 – 300 MHz
- +5V Single supply operation
- RoHS-compliant / Pb-free 6x6mm 28-pin QFN package
- Low-side LO configuration

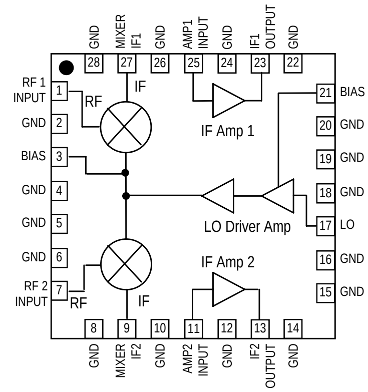
Product Description

The CV221-2A is a dual-channel high-linearity down-converter designed to meet the demanding performance, functionality, and cost goals of current and next generation mobile infrastructure basestations and repeaters. It provides high dynamic range performance in a low profile RoHS-compliant/lead-free surface-mount leadless package that measures 6 x 6 mm square.

It is ideally suited for high dynamic range receiver front ends using diversity receive channels. Functionality includes frequency conversion and IF amplification, while an integrated LO driver amplifier powers the passive mixer. The MCM is implemented with reliable and mature GaAs MESFET and InGaP HBT technology.

Typical applications include frequency downconversion used in 3G W-CDMA and WiMax basestation transceiver or repeater applications.

Functional Diagram



Specifications (1)

Parameters	Units	Min	Typ	Max	Min	Typ	Max	Comments
RF Frequency Range	MHz		1900 – 2400			2500 – 2700		
LO Frequency Range	MHz		1600 – 2335			2200 – 2565		
IF Frequency Range	MHz		65 – 300			135 – 300		See note 2
% Bandwidth around IF center frequency	%		±7.5			±12		See note 3
IF Test Frequency	MHz		240			155		
SSB Conversion Gain	dB	6.5	9.2	10.5	5.4	8.4	9.9	Temp = 25 °C
Gain Drift over Temp (-40 to 85 °C)	dB		±0.6			±0.6		Referenced to +25 °C
Input IP3	dBm	+24	+28		+17	+22		See note 4
Input 1 dB Compression Point	dBm		+11.5			+8.0		See note 4
Noise Figure	dB		11			13		See note 5
LO Input Drive Level	dBm	-2.5	0	+2.5	-2.5	0	+2.5	
LO-RF Isolation	dB		12			9		P_{LO} = 0 dBm
LO-IF Isolation	dB		26			26		P_{LO} = 0 dBm
RF-IF Isolation	dB		25			25		
Branch-Branch Isolation	dB		45			40		
Return Loss: RF Port	dB		14			12		
Return Loss: LO Port	dB		14			14		
Return Loss: IF Port	dB		13			10		
Operating Supply Voltage	V		+5			+5		
Supply Current	mA		315	330		315	330	See note 6
Thermal Resistance	°C / W			34			34	
Junction Temperature	°C			160			160	See note 6

1. Specifications when using the application specific circuit (shown on page 3) with a low side LO = 0 dBm and IF = 240 MHz in a downconverting application at 25 °C.
2. IF matching components affect the center IF frequency. Proper component values for other IF center frequencies than shown can be provided by emailing to applications.engineering@wj.com.
3. The IF bandwidth of the converter is defined as 15% around any center frequency in its operating IF frequency range. The bandwidth is determined with external components. Specifications are valid around the total ±7.5% bandwidth. ie. with a center frequency of 240 MHz, the specifications are valid from 240 ± 18 MHz.
4. Assumes the supply voltage = +5 V. IIP3 is measured with Δf = 1 MHz with RFin = -5 dBm / tone.
5. Assumes LO injection noise is filtered at the thermal noise floor, -174 dBm/Hz, at the RF, IF, and Image frequencies.
6. The R1 resistor can be modified for the CV221-2A to draw less current. Changing it from 13 to 18Ω is expected to have the converter draw 17mA less current so that the converter will draw about 300mA typically under LO drive, while degrading the IIP3 performance by 0.5 dB.

Absolute Maximum Rating

Parameter	Rating
Operating Case Temperature	-40 to +85 °C
Storage Temperature	-55 to +150 °C
DC Voltage	+5.5 V
Junction Temperature	+220 °C

Operation of this device above any of these parameters may cause permanent damage.

Ordering Information

Part No.	Description
CV221-2AF	1.9-2.7GHz Dual-Branch Downconverter (lead-free/RoHS-compliant 6x6mm QFN package)
CV221-2APCB240	Fully Assembled Eval. Board, IF = 240MHz

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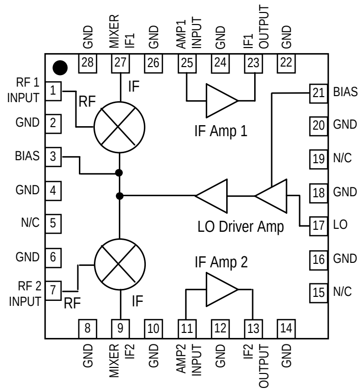
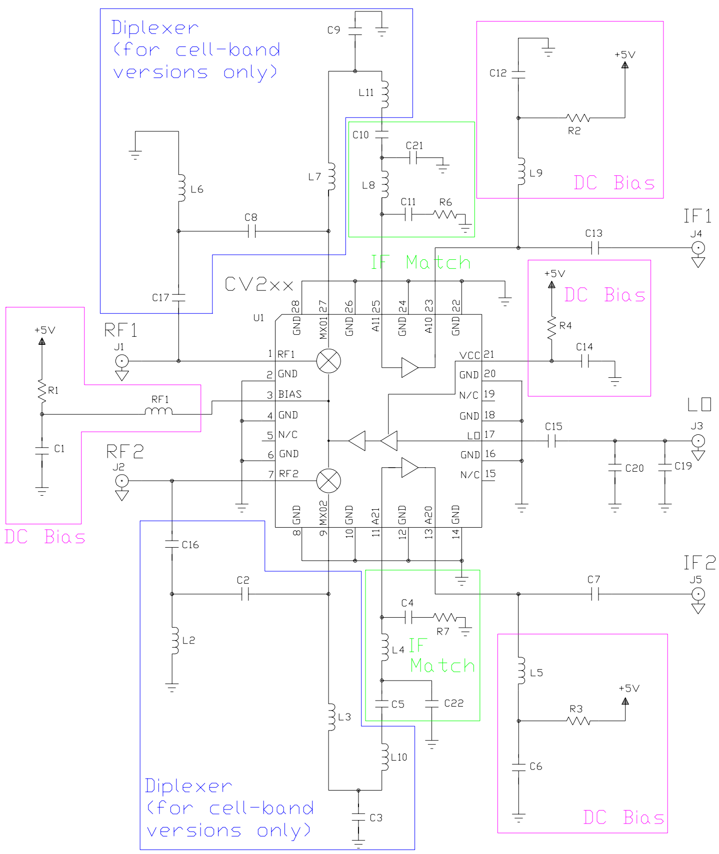
Device Architecture / Application Circuit Information



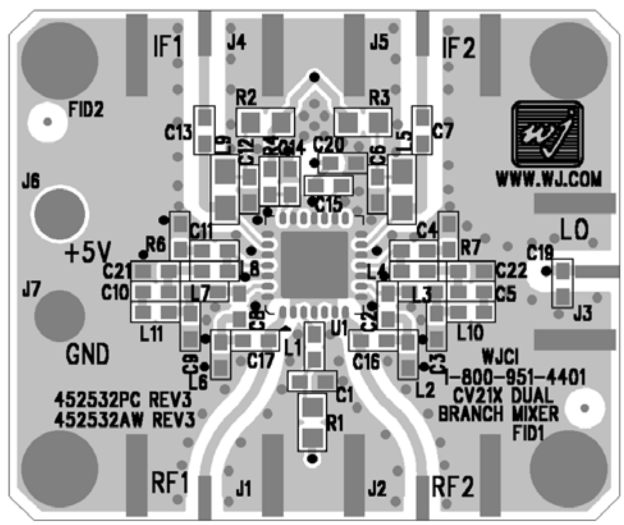
Typical 2.1 GHz Downconverter Performance Chain Analysis (Each Branch)

Stage	Gain (dB)	Input P1dB (dBm)	Input IP3 (dBm)	NF (dB)	Current (mA)	Cumulative Performance			
						Gain (dB)	Input P1dB (dBm)	Input IP3 (dBm)	NF (dB)
LO Amp / MMIC Mixer	-8.4	20	33	9	115	-8.4	20	33	9
IF Amplifier	17.6	1	21	2.2	100	9.2	9	27.8	11
CV221-2A	**Cumulative Performance**				**315***	**9.2**	**9**	**27.8**	**11**

* The 2nd branch includes another mixer and IF amplifier, which increases the total current consumption of the MCM to be 315 mA.



Printed Circuit Board Material:
.014" FR-4, 4 layers, .062" total thickness



CV221-2A: The application circuit can be broken up into three main functions as denoted in the colored dotted areas above: RF/IF diplexing (blue), IF amplifier matching (green), and dc biasing (purple). There are various placeholders for chip components in the circuit schematic so that a common PCB can be used for all WJ dual-branch converters.

External Diplexer: This is only used with the cellular-band CV products. The mixer performs the diplexing internally for the CV221-2A; therefore the components shown in the diplexer section should be not be loaded except for L3, L10, L7, and L11, which should contain a 0 Ω jumper.

IF Amplifier Matching: The IF amplifier requires matching elements to optimize the performance of the amplifier to the desired IF center frequency. Since IF bandwidths are typically on the order of 5 to 10%, a simple two element matching network, in the form of either a high-pass or low-pass filter structure, is sufficient to match the MMIC IF amplifier over these narrow bandwidths. Proper component values for other IF center frequencies can be provided by emailing to applications.engineering@wj.com.

DC Biasing: DC bias must be provided for the LO and IF amplifiers in the converter. R1 sets the operating current for the last stage of the LO amplifier and is chosen to optimize the mixer LO drive level. Proper RF chokes and bypass capacitors are chosen for proper amplifier biasing at the intended frequency of operation. The "+5 V" dc bias should be supplied directly from a voltage regulator.

WiMax Operation: There is no change to the application circuit for operation in the 2.5 to 2.7 GHz band.

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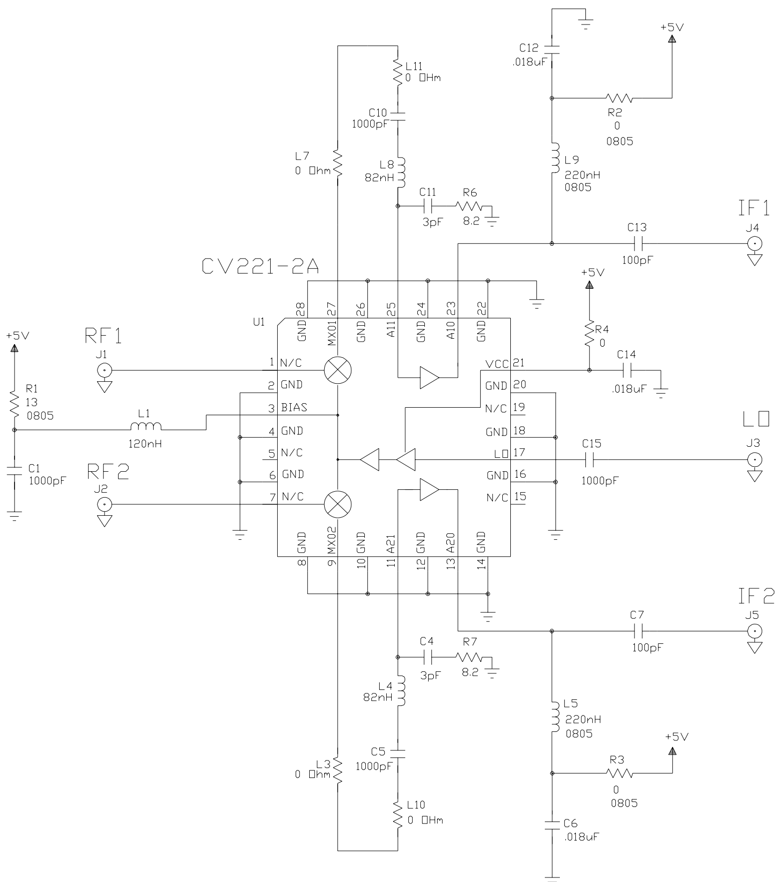
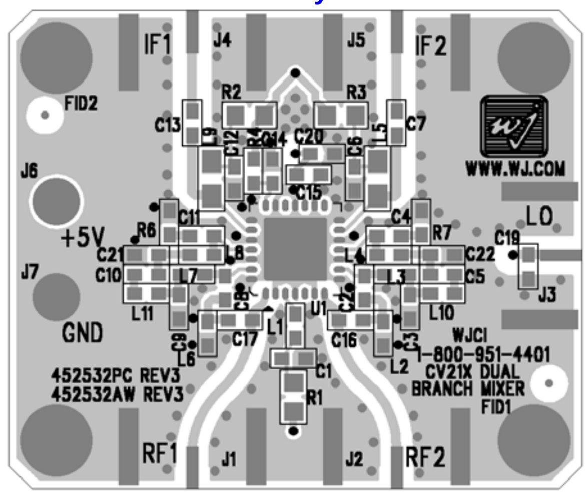
Application Circuit: IF = 240 MHz (CV221-2APCB240)

RF = 1900 – 2700 MHz, IF = 240 MHz



PCB Layout



Circuit Board Material: .014" FR-4, 4 layers, .062" total thickness

Bill of Materials

Ref. Desig.	Component	Size
R1 (1)	13 Ω chip resistor	0805
R2, R3, R4, L3, L7 L10, L11	0 Ω chip resistor	0603
R6, R7	8.2 Ω chip resistor	0603
C1, C5, C10, C15	1000 pF chip capacitor	0603
C4, C11 (2)	3 pF chip capacitor	0603
C6, C12, C14	.018 µF chip capacitor	0603
C7, C13	100 pF chip capacitor	0603
L1	120 nH chip inductor	0603
L4, L8 (2)	82 nH chip inductor	0603
L5, L9	220 nH chip inductor	0805
C2, C3, C8, C9, C16 C17, C19, C20, C21 C22, L2, L6	Shown on silkscreen, but not used in actual circuit.	
U1	CV221-2A WJ Converter	QFN

Notes:

1. The R1 resistor can be modified for the CV221-2A to draw less current. Changing it from 13 to 18Ω is expected to have the converter draw 17mA less current so that the converter will draw about 300mA typically under LO drive, while degrading the IIP3 performance by 0.5 dB.
2. The values shown above have the IF tuned at 240 MHz and will affect the optimal performance of the converter. For other frequencies, these components need to be modified as follows:

IF Amplifier Matching

Ref. Desig.	50	70	75	100	120	130	140	155	180	240
C4, C11	18 pF	15 pF	15 pF	8.2 pF	8.2 pF	6.8pF	5.6 pF	5.6 pF	3.9pF	3.0 pF
L4, L8	390 nH	220 nH	220 nH	180 nH	150 nH	150nH	150 nH	120 nH	110 nH	82 nH

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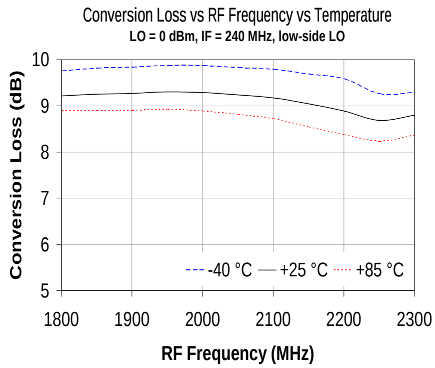
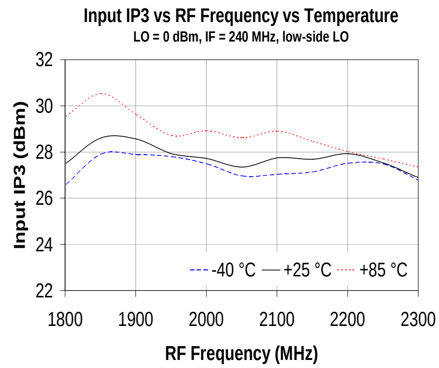
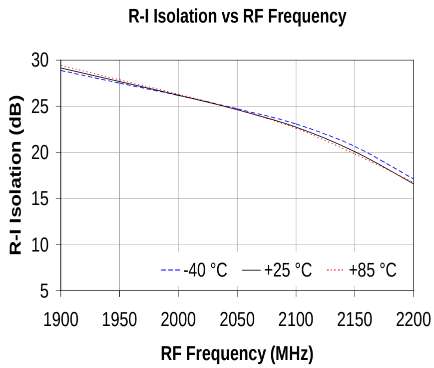
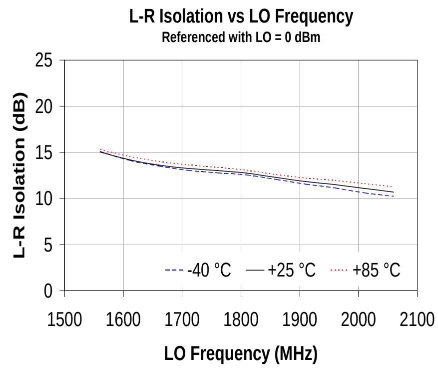
Typical Downconversion Performance Plots

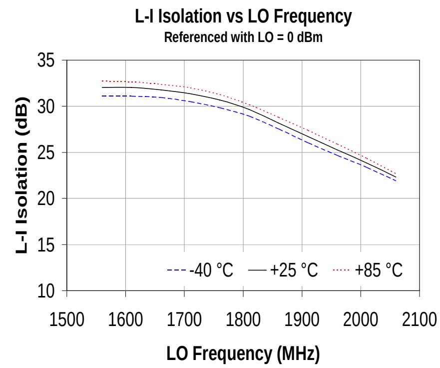
Performance using the circuitry on the CV221-2APCB240 Evaluation Board

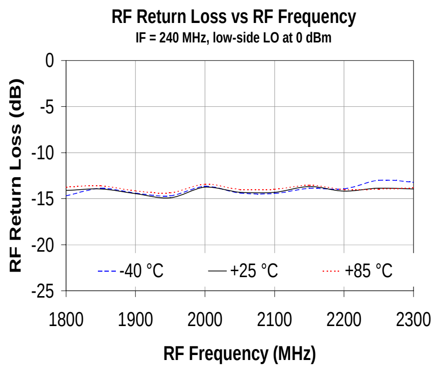


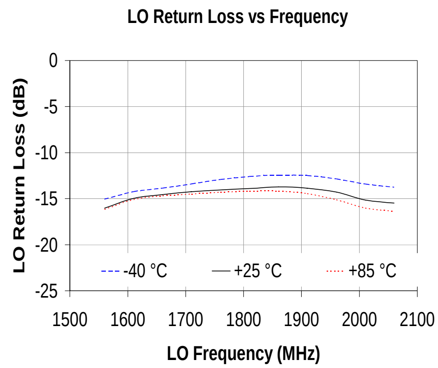


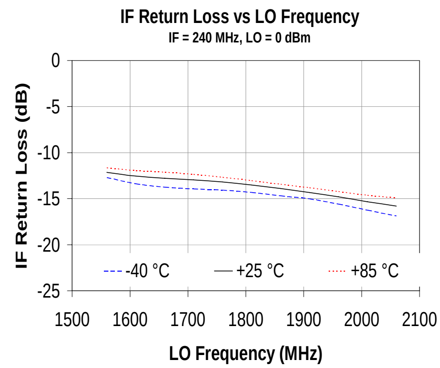


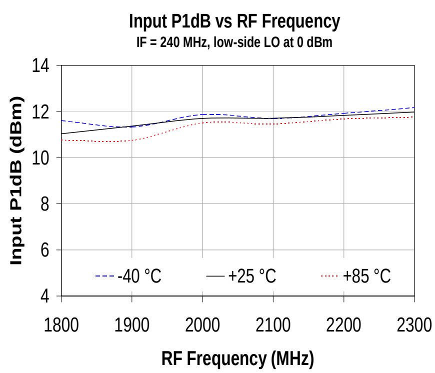


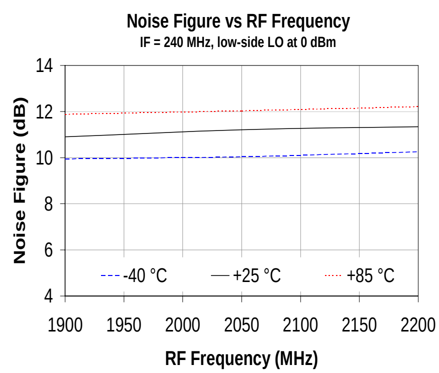












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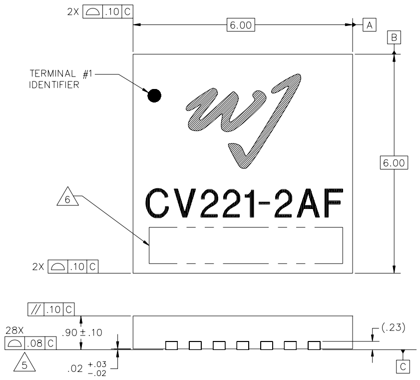
CV221-2AF Mechanical Information

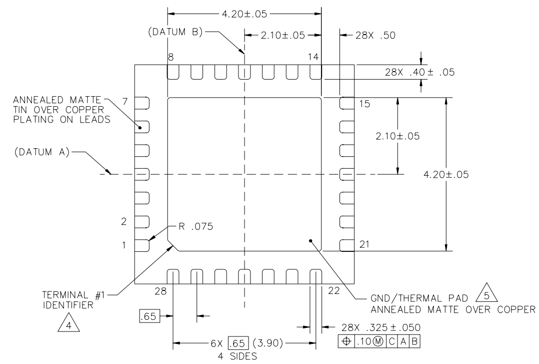
This package is lead-free/RoHS-compliant. The plating material on the pins is annealed matte tin over copper. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes.

Outline Drawing

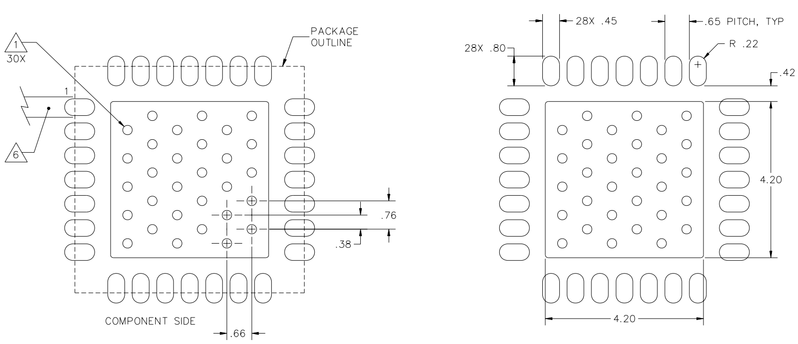


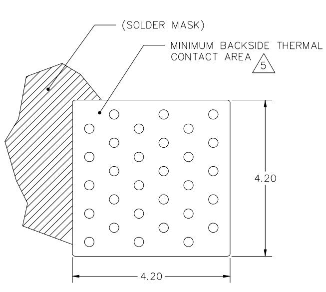
NOTES:

1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-220, ISSUE E (VARIATION VJJC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95-1 SPP-012.
5. COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
6. ALPHA-NUMERIC LOT CODE.



Mounting Configuration / Land Pattern





NOTES:

1. GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCE OF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL, PLATED THRU DIAMETER OF .25mm (.010").
2. ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
3. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL.
4. ADD MOUNTING SCREWS NEAR THE PART TO FASTEN THE BOARD TO A HEATSINK. ENSURE THAT THE GROUND/THERMAL VIA REGION CONTACTS THE HEATSINK.
5. DO NOT PUT SOLDER MASK ON THE BACK SIDE OF THE PC BOARD IN THE REGION WHERE THE BOARD CONTACTS THE HEATSINK.
6. RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.
7. USE 1 OZ. COPPER MINIMUM.
8. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

Product Marking

The component will be lasermarked with a “CV221-2AF” product label with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part will be located on the website in the “Application Notes” section.

ESD / MSL Information

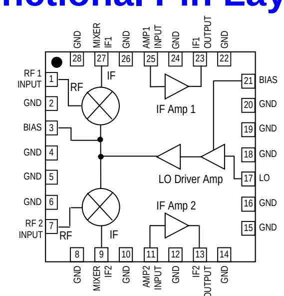
Caution! ESD sensitive device.

ESD Rating: Class 1B
Value: Passes /500V to <1000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class III
Value: Passes /500V to <1000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 2 at +260 °C convection reflow
Standard: JEDEC Standard J-STD-020

Functional Pin Layout



Pin	Function	Pin	Function
1	Ch. 1 Mixer RF Input	15	N/C or GND
3	LO Amp Bias	17	LO input
5	N/C or GND	19	N/C or GND
7	Ch. 2 Mixer RF Input	21	+5 V
9	Ch. 2 Mixer IF Output	23	Ch. 1 IF Amp Output / Bias
11	Ch. 2 IF Amp Input	25	Ch. 1 IF Amp Input
13	Ch. 2 IF Amp Output / Bias	27	Ch. 1 Mixer IF Output

The even numbered pins are hard grounded to the backside paddle internally. They can be grounded or not connected. The backside paddle is required to be grounded.

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