ML5012 – 12 Bit SAR A/D Converter

◆ Features

- 4-pins Serial control interface CS, DIN, DOUT, SCK
- Operates with 3.3V or analog adjusted voltage reference
- Differential Input Programmable Gain Amplifier (PGA) : 0 ~40.25dB
- Channel selectable
- Differential & Single End input mode
- 0V to VDD input range with single 2.2V to 5.0V power supply
- 4 MOSFET switch for external loads on/off
- MCU programmalbe AD clock frequency from 1M to 7.8Khz and AD startup time.
- Successive AD conversion mode

◆ Applications

- General Metering Application

◆ Key Specification

Resolution	12 Bits
Total Unadjusted Error	+/- 6 LSB
Single Voltage Supply	2.2V ~ 5.0V
A/D Conversion Time	15 ADCLK
Comparison Time	15 ADCLK
MOSFET Current	5mA

◆Ordering Information

Item	Package	Shipping
ML5012	Dice Form	

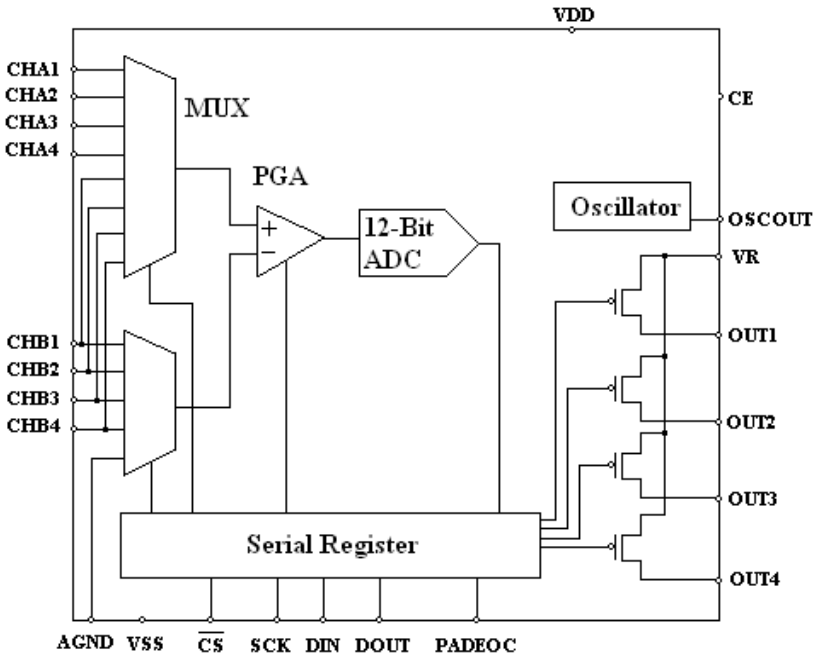
◆ General Description

The ML5012 is CMOS 12-bit SAR A/D converter, Differential Input Programmable Gain Amplifier and four MOSFET ON/OFF switches. A 4-pin serial control interface is easy to communicate with MCU.

◆ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Supply Voltage	VDD	-0.3 ~ 5.5	V
Input Voltage at any pin	VIN	-0.3 ~ VDD + 0.3	V
Output Voltage	VIO	VSS-0.3 ~ VIN+0.3	V
Operation Ambient Temperature	Topr	-20 ~ +70	°C
Storage Temperature	Tstg	-40 ~ +90	°C

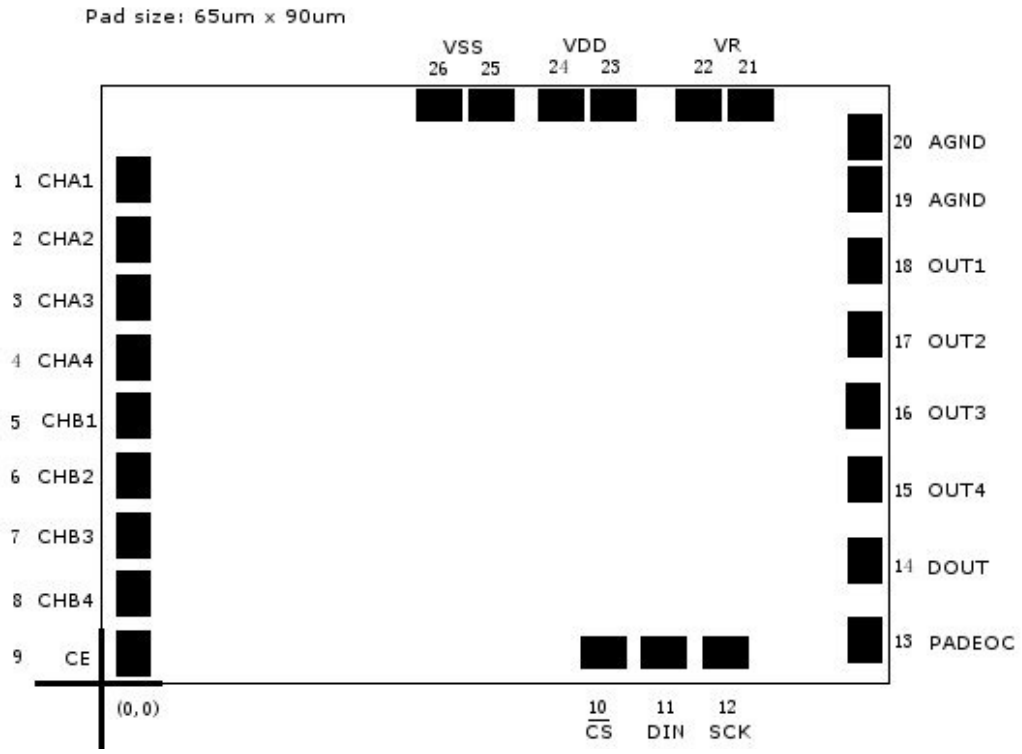
◆ Block Diagram



◆ Pin Function

Pin Name	I/O	Description
VDD	P	Positive power supply
VR	P	Reference voltage for analog input signal
CE	I	Chip enable control signal
PADEOC	O	A pulse signal of EOC (End of conversion)
OUT1 ~ 4	O	MOSFET ON/OFF Switch Output
$\overline{CS}$	I	Chip Select for serial interface
SCK	I	Clock for serial interface
DIN	I	Data input for serial interface
DOUT	O	Data output for serial interface, tri-state output
VSS	P	Negative supply voltage
CHA1 ~ CHA4	I	Analog input channels for positive differential input of PGA
CHB1 ~ CHB4	I	Analog input channels for positive/negative differential input of PGA
AGND	P	Analog GND

◆ Bonding Diagram



◆ Pin Function

	Pin	(x,y)	Description		Pin	(x,y)	Description
1	CHA1	(85,1110)	Analog input channel	14	DOUT	(1660,290)	Data output
2	CHA2	(85,980)	Analog input channel	15	OUT4	(1660,465)	MOSFET Switch
3	CHA3	(85,855)	Analog input channel	16	OUT3	(1660,620)	MOSFET Switch
4	CHA4	(85,725)	Analog input channel	17	OUT2	(1660,780)	MOSFET Switch
5	CHB1	(85,600)	Analog input channel	18	OUT1	(1660,935)	MOSFET Switch
6	CHB2	(85,470)	Analog input channel	19	AGND	(1660,1090)	Analog GND
7	CHB3	(85,345)	Analog input channel	20	AGND	(1660,1200)	Analog GND
8	CHB4	(85,215)	Analog input channel	21	VR	(1415,1270)	Reference voltage
9	CE	(85,85)	Chip Enable	22	VR	(1300,1270)	Reference voltage
10	$\overline{CS}$	(1095,85)	Chip Select	23	VDD	(1115,1270)	Positive supply voltage
11	DIN	(1225,85)	Data input for serial interface	24	VDD	(1000,1270)	Positive supply voltage
12	SCK	(1355,85)	Clock for serial interface	25	VSS	(855,1270)	Negative supply voltage
13	PADEOC	(1660,115)	End of conversion	26	VSS	(740,1270)	Negative supply voltage

◆ Allowable Operating Conditions

Ta = 0 °C to 70 °C unless otherwise specified

Parameter	Symbol	Conditions	Ta=25°C			Units
			Min	Typ	Max	
Supply Voltage	VDD		2.2		5.5	V
Analog Input Voltage	Vin		0		5.5	V
Oscillator Frequency	Fosc			100		kHz

◆ Electrical Characteristics

1. A/D Converter & PGA Digital Levels and DC Specification

VDD = 3.0V, VR = 3.0V DC, Ta = 25 °C unless otherwise specified

Parameter	Symbol	Conditions	Ta=25°C			Units
			Min	Typ	Max	
Operating current	Ivdd			0.60	0.70	mA
	Isb	VDD = 2.0V ~ 3.3V, A/D inactive			1	uA
	Ivr	AD active		0.05		mA
		OSC. Active, A/D inactive		0.15		mA
OFF Channel Leakage Current	Ioff(+)	Analog Multiplexer VDD = 3.0V, VIN = 3.0V		0		uA
	Ioff(-)	Analog Multiplexer VDD = 3.0V, VIN = 0V		0		uA
PGA Input Offset	Voff	VDD = 3.0V, VCHA = VCHB = 1.5V Differential Input Mode	-5		5	mV

2. Digital Levels and DC Specification

VDD = 3.0V, VR = 3.0V DC, Ta = 25 °C unless otherwise specified

Parameter	Symbol	Conditions	Ta=25°C			Units
			Min	Typ	Max	
Logical "1" Input Voltage	Vih		2.2		3.0	V
Logical "0" Input Voltage	Vil		0		0.7	V
Logical "1" Output Voltage	Voh	Ioh = 1mA	2.2			V
Logical "0" Output Voltage	Vol	Iol = -1mA			0.7	V

3. A/D Converter and Comparator Timing Specification

VDD = 3.0V, VR = 3.0V DC, Ta = 25°C unless otherwise specified

Parameter	Symbol	Conditions	Ta=25°C			Units
			Min	Typ	Max	
A/D Conversion Time	Tadc	Fosc = 100KHz		150		us
Comparator Conversion Time	Tcomp	Fosc = 100KHz		150		us

4. A/D Conversion Specification

VDD = 3.0V, VR = 3.0V DC, Ta = 25°C unless otherwise specified

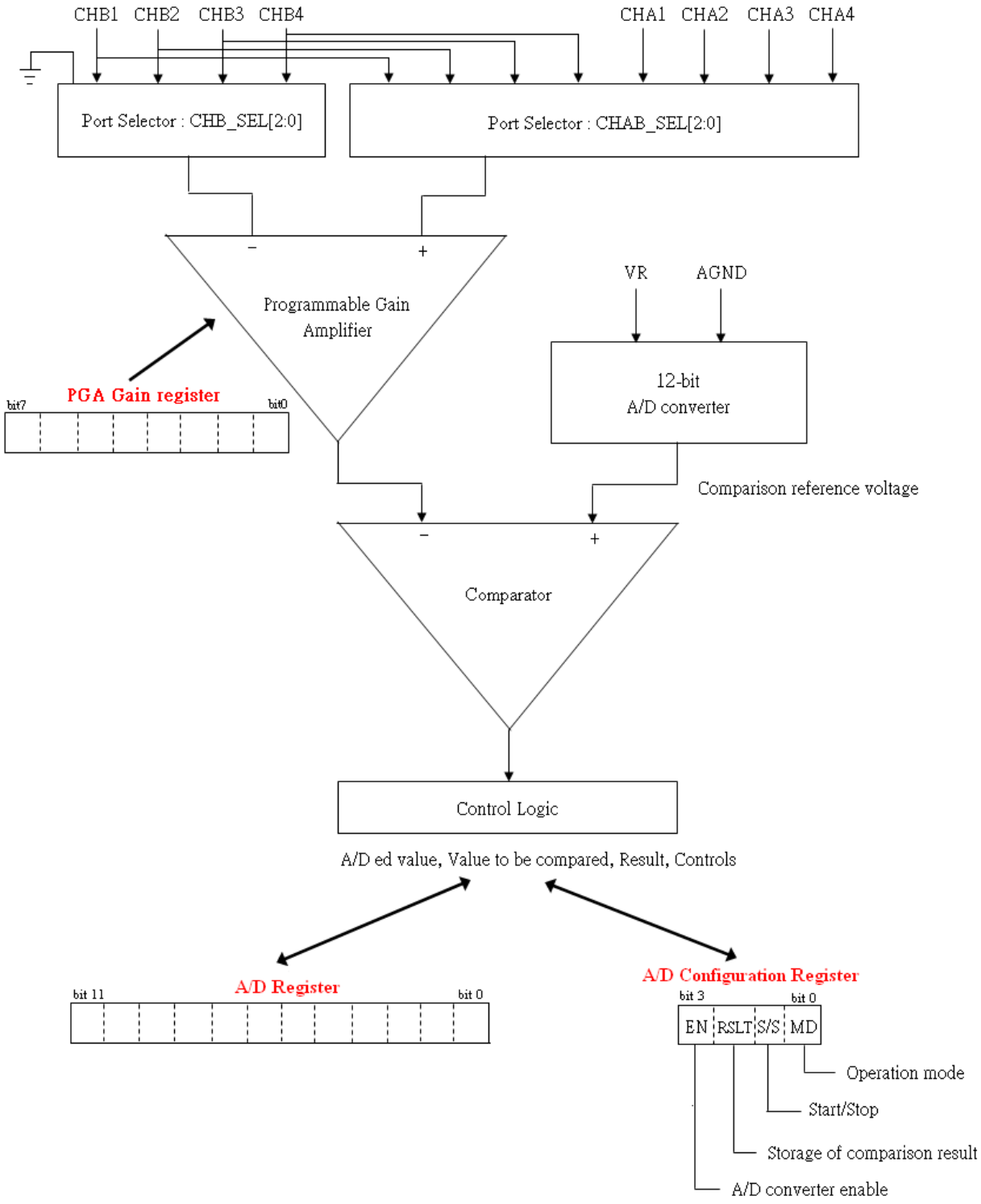
Parameter	Symbol	Conditions	Ta=25°C			Units
			Min	Typ	Max	
Resolution	Res	PGA Gain = 0dB		10		bit
A/D Error	Err	PGA Gain = 0dB, Fosc = 2MHz, VDD = VR = 3.3V		+/- 4	+/- 6	LSB

5. MOSFET Switch Specification

VDD = 3.0V, VR = 3.0V DC, Ta = 25°C unless otherwise specified

Parameter	Symbol	Conditions	Ta=25°C			Units
			Min	Typ	Max	
High Output Voltage	Voh	VR = 3.0V, Ioh = -5mA		2.9		V

◆ Block Diagram of PGA and A/D Converter



◆ Function Description

1. Serial Interface Command

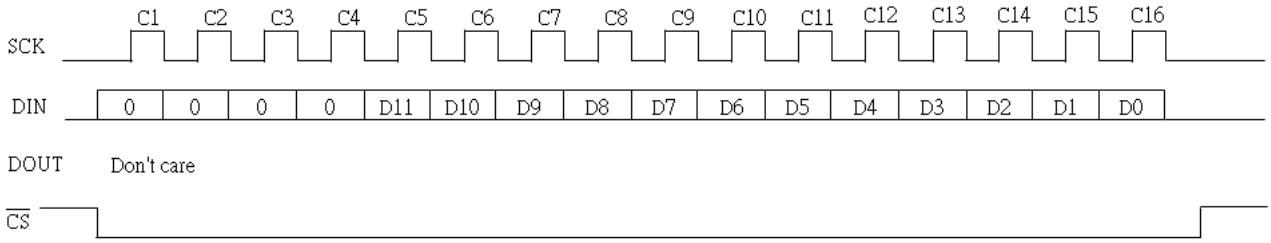
There are 5 commands for serial interface, STCH, PGA_AC, WR_AD, WR_OSC, RR_AC and RR_AD as shown the below Command Code map.

Command Code Map

R/W	Command Code				Interface Command	Function Description
	C1	C2	C3	C4		
W	0	0	0	0	WR_STCH	STCH register. Enable Oscillator for A/D, Select PGA input channel, Enable MOSFET and Select A/D range
W	0	0	0	1	WR_PGA_AC	Set PGA Gain & write A/D configuration
W	0	0	1	0	WR_AD	Write data to A/D register
W	0	0	1	1	WR_SYS	SYS register. Set AD conversion frequency, ADC startup time, Successive AD mode, Reference voltage to AGND or (VR-AGND)/2
R	1	0	0	0	RR_STCH	Read STCH register value
R	1	0	0	1	RR_PGA_AC	Read PGA gain & A/D configuration
R	1	0	1	0	RR_AD	Read data from A/D register
R	1	0	1	1	RR_SYS	Read SYS register value

1-1. WR_STCH Command. Select PGA input channel (CHAB_SEL & CHB_SEL), enable oscillator (ENOSC) for A/D, AD Range Selection (AD_Range) and MOSFET Enable control (M1_EN, M2_EN, M3_EN & M4_EN).

The following diagram shows the timing of sending WR_STCH command.



The DIN data in C1~C4 cycle is WR_STCH command code.

The DIN data in C5 cycle is Oscillator Enable bit, D11 = ENOSC.

The DIN data in C6 cycle is AD Range Selection bit, D10 = AD_Range

The DIN data in C7~C9 cycle is Channel AB selection, D[9:7] = CHAB_SEL[2:0].

The DIN data in C10~C12 cycle is Channel B selection, D[6:4] = CHB_SEL[2:0].

The DIN data in C13 cycle is MOSFET 1 Enable, D3= M1_EN.

The DIN data in C14 cycle is MOSFET 2 Enable, D2= M2_EN.

The DIN data in C15 cycle is MOSFET 3 Enable, D1= M3_EN.

The DIN data in C16 cycle is MOSFET 4 Enable, D0= M4_EN.

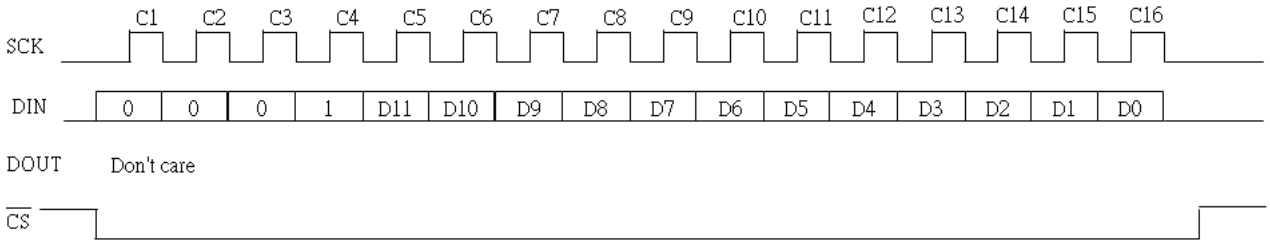
STCH Register Operations Table

Function	Control												Operations
	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Oscillator Enable	0												RC Oscillator Disable
(ENOSC)	1												RC Oscillator Enable
AD Range Select		0											AD Range : 0 ~ 4,095
(AD_Range)		1											AD Range : -2,047 ~ 2,047
Channel AB Select CHAB_SEL[2:0]			0	0	0								CHAB = CHA1
			0	0	1								CHAB = CHA2
			0	1	0								CHAB = CHA3
			0	1	1								CHAB = CHA4
			1	0	0								CHAB = CHB1
			1	0	1								CHAB = CHB2
			1	1	0								CHAB = CHB3
			1	1	1								CHAB = CHB4
Channel B Select CHB_SEL[2:0]						0	0	0					CHB = CHB1
						0	0	1					CHB = CHB2
						0	1	0					CHB = CHB3
						0	1	1					CHB = CHB4
						1	x	x					CHB = AGND
MOSFET 1 Enable									0				MOSFET 1 Disable
(M1_EN)									1				MOSFET 1 Enable
MOSFET 2 Enable										0			MOSFET 2 Disable
(M2_EN)										1			MOSFET 2 Enable
MOSFET 3 Enable											0		MOSFET 3 Disable
(M3_EN)											1		MOSFET 3 Enable
MOSFET 4 Enable												0	MOSFET 4 Disable
(M4_EN)												1	MOSFET 4 Enable

Note : 'x' = don't care

1-2. WR_PGA_AC Command. Write data into PGA Gain Register & Set A/D configuration register

The following diagram shows the timing diagram of writing data into PGA Gain Register & setting A/D configuration register.



The DIN data in C1~C4 cycle is PGA_AC Gain command code.

The DIN data in C5 cycle is A/D converter enable bit, D11 = EN.

The DIN data in C6 cycle is Storage of comparison result bit, D10 = RSLT.

The DIN data in C7 cycle is Start/Stop bit of A/D converter, D9 = S/S.

The DIN data in C8 cycle is Operation Mode bit of A/D converter, D8 = MD.

The DIN data in C9~C16 cycles are setting the PGA Gain for PGA Gain Register, D[7:0] = PGA[7:0].

A/D Converter Configuration Register Table

Function	Control				Operations
	D11	D10	D9	D8	
A/D Converter Enable (EN)	0				A/D Converter Disable
	1				A/D Converter Enable
Storage of comparison result (RSLT)		0			Input voltage * PGA Gain < internal reference voltage
		1			Input voltage * PGA Gain > internal reference voltage
Start/Stop of A/D Converter (S/S)			0		Stop A/D Conversion or comparison operation
			1		Start A/D Conversion or comparison operation
Operation Mode of A/D Converter (MD)				0	A/D Conversion Mode
				1	Comparison Mode

PGA Gain Register Table

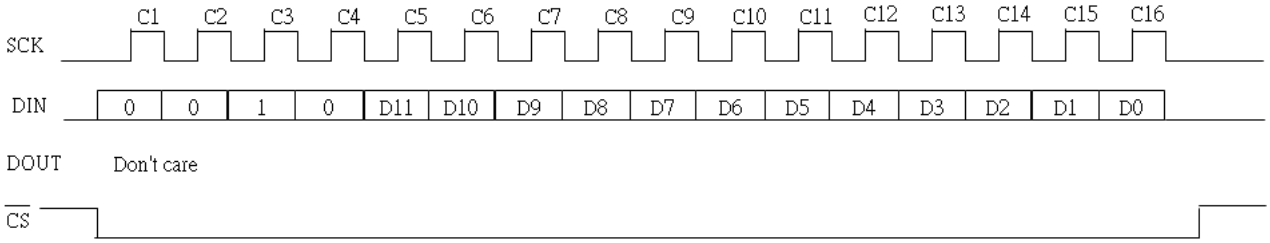
Function	Control								Gain Code		PGA Gain factor
	D7	D6	D5	D4	D3	D2	D1	D0	Decimal	HEX	
PGA Gain	0	0	0	0	0	0	0	0	0	0	1
	0	0	0	0	0	0	0	1	1	1	1.4
	0	0	0	0	0	0	1	0	2	2	1.8
	0	0	0	0	0	0	1	1	3	3	2.2
	0	0	0	0	0	1	0	0	4	4	2.6
	…….								….	….	
	0	0	0	0	0	1	1	1	7	7	3.8
	0	0	0	0	1	0	0	0	8	8	4.2
	0	0	0	0	1	0	0	1	9	9	4.6
	…….								….	….	
	0	0	0	0	1	1	1	1	15	F	7
	0	0	0	1	0	0	0	0	16	10	7.4
	0	0	0	1	0	0	0	1	17	11	7.8
	…….								….	….	
	0	0	0	1	1	1	1	1	31	1F	13.4
	0	0	1	0	0	0	0	0	32	20	13.8
	0	0	1	0	0	0	0	1	33	21	14.2
	…….								….	….	
	0	0	1	1	1	1	1	1	63	3F	26.2
	0	1	0	0	0	0	0	0	64	40	26.6
	0	1	0	0	0	0	0	1	65	41	27
	…….								….	….	
	0	1	1	1	1	1	1	1	127	7F	51.8
	1	0	0	0	0	0	0	0	128	80	52.2
	1	0	0	0	0	0	0	1	129	81	52.6
	…….								….	….	
	1	1	1	1	1	1	1	0	254	FE	102.6
	1	1	1	1	1	1	1	1	255	FF	103

*Note: PGA Gain = 1 + "Gain Code" * 0.4*

*Eg. If "Gain Code" = 100, PGA Gain = 1 + 0.4*100 = 41.*

1-3. WR_AD Command. Write data into A/D Register

The following diagram shows the timing diagram of writing data into A/D Register.

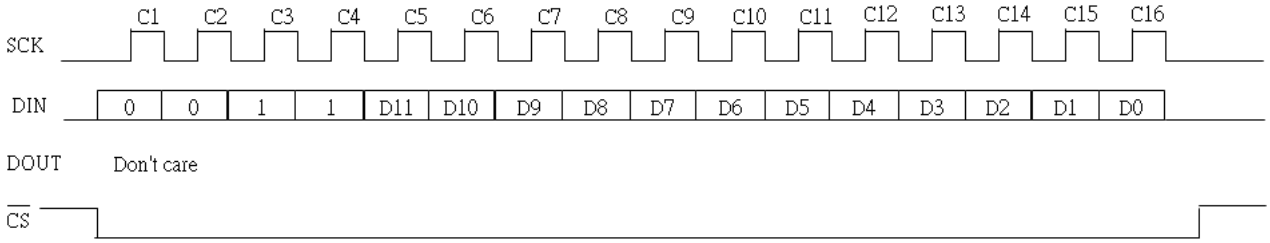


The DIN data in C1~C4 cycle is WR_AD command code.

The DIN data in C5~C16 cycles are input data for A/D Register, D[11:0] = A/D[11:0].

1-4. WR_SYS Command. Set AD conversion clock frequency, AD startup time, Successive AD conversion mode, PGA Reference voltage to AGND or (VR-AGND)/2

The following diagram shows the timing diagram of writing data to control the AD conversion frequency.



The DIN data in C1~C4 cycle is WR_SYS command code.

The DIN data in C5~C7 cycles are output data of ADC Clock, D[11:9] = AD_Clock[2:0].

The DIN data in C8~C9 cycles are output data of Start time, D[8:7] = STA_OPT[1:0].

The DIN data in C10~C13 are reserved.

The DIN data in C14 is Successive AD mode enable, D[2] = SMODE.

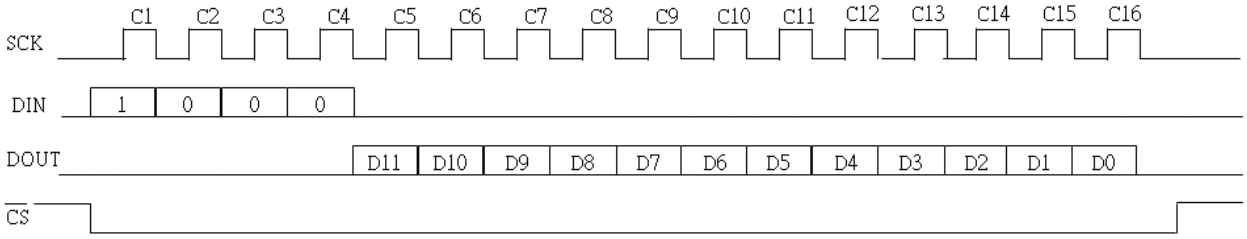
The DIN data in C15 is Reference AGND connection enable, D[1] = VGND_EN.

The DIN data in C16 is Reference (VR-AGND)/2 connection enable, D[0] = VMID_EN.

Function	Control								Operations
	D11	D10	D9	D8	D7	D2	D1	D0	
Set AD Clock Frequency (AD_Clock[2:0])	0	0	0						AD Clock Frequency = 1MHz
	0	0	1						AD Clock Frequency = 500kHz (default)
	0	1	0						AD Clock Frequency = 250kHz
	0	1	1						AD Clock Frequency = 125kHz
	1	0	0						AD Clock Frequency = 62.5kHz
	1	0	1						AD Clock Frequency = 31.25kHz
	1	1	0						AD Clock Frequency = 15.625kHz
	1	1	1						AD Clock Frequency = 7.8125kHz
Set AD Converter Startup Time (STA_OPT[1:0])				0	0				Startup Time = 1000us (default)
				0	1				Startup Time = 800us
				1	0				Startup Time = 600us
				1	1				Startup Time = 400us
Set Successive AD Conversion Mode (SMODE)						0			Successive AD conversion mode disable
						1			Successive AD conversion mode enable
Enable PGA reference connect to VMIN (VMIN_EN)							0		PGA Reference connect to AGND
							1		PGA Reference connect to VMIN
Reserved								-	
								-	

1-5 RR_STCH Command. Read STCH register value

The following diagram shows the timing diagram of reading data from the STCH register.



The DIN data in C1~C4 cycle is RR_STCH command code.

The DOUT data in C5 cycle is RC oscillator enable bit, D11 = ENOSC.

The DOUT data in C6 cycle is AD Range Select, D10 = AD_RANGE.

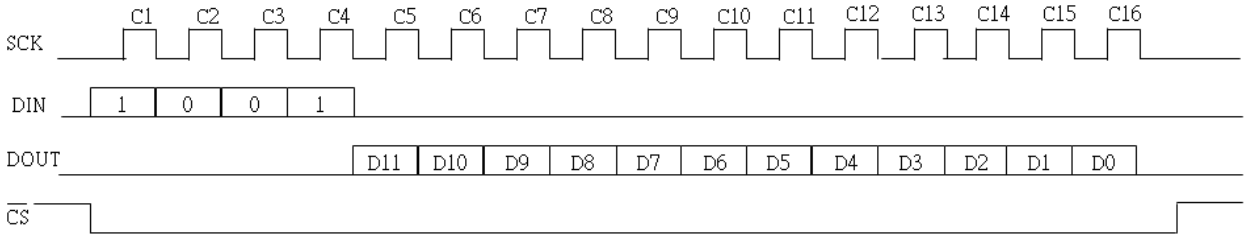
The DOUT data in C7~C9 cycle is Channel AB select, D9 – D7 = CHAB_SEL[2:0].

The DOUT data in C10~C12 cycle is Channel B select, D6 – D4 = CHB_SEL[2:0].

The DOUT data in C13~C16 cycles are MOSFET enable, D3 = M1_ENB, D2 = M2_ENB, D1 = M3_ENB, D0 = M4_ENB.

1-6 RR_PGA_AC Command. Read data from A/D Configuration Register

The following diagram shows the timing diagram of read data from A/D Configuration Register.



The DIN data in C1~C4 cycle is RR_AC command code.

The DIN data in C5 cycle is A/D converter enable bit, D11 = EN.

The DIN data in C6 cycle is Storage of comparison result bit, D10 = RSLT.

The DIN data in C7 cycle is Start/Stop bit of A/D converter, D9 = S/S.

The DIN data in C8 cycle is Operation Mode bit of A/D converter, D8 = MD.

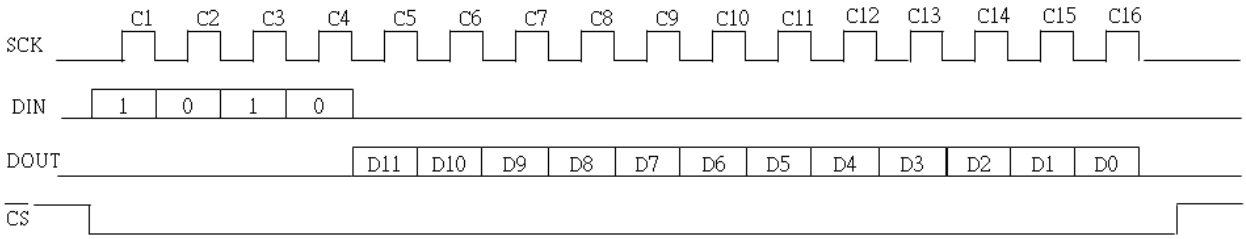
The DIN data in C9~C16 cycles are PGA gain setting, D[7:0] = PGA[7:0].

A/D Converter Configuration Register Table

Function	Control				Operations
	D11	D10	D9	D8	
A/D Converter Enable (EN)	0				A/D Converter Disable
	1				A/D Converter Enable
Storage of comparison result (RSLT)		0			Input voltage * PGA Gain < internal reference voltage
		1			Input voltage * PGA Gain > internal reference voltage
Start/Stop of A/D Converter (S/S)			0		Stop A/D Conversion or comparison operation
			1		Start A/D Conversion or comparison operation
Operation Mode of A/D Converter (MD)				0	A/D Conversion Mode
				1	Comparison Mode

1-7 RR_AD Command. Read data from A/D Register.

The following diagram shows the timing diagram of read data from A/D Register.

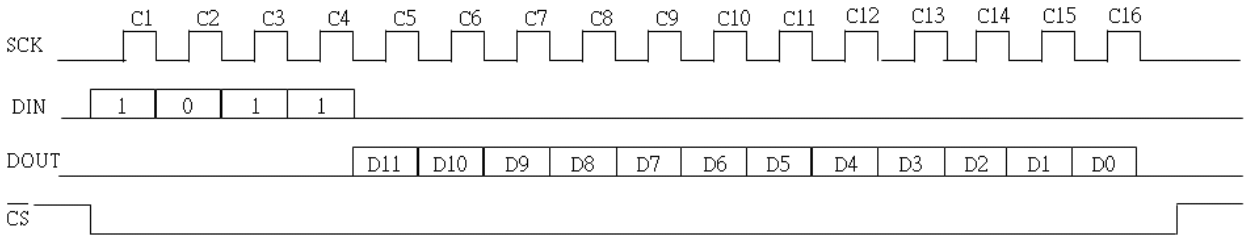


The DIN data in C1~C4 cycle is RR_AD command code.

The DOUT data in C5~C16 cycles are output data from A/D Register, D[11:0] = A/D[11:0].

1-8 RR_SYS Command. Read data from SYS Register.

The following diagram shows the timing diagram of read data from A/D Register.



The DIN data in C1~C4 cycle is RR_SYS command code.

The DOUT data in C5~C7 cycles are output data of ADC Clock, D[11:9] = AD_Clock[2:0].

The DOUT data in C8~C9 cycles are output data of Start time, D[8:7] = STA_OPT[1:0].

The DOUT data in C10~C13 are reserved.

The DOUT data in C14 is Successive AD mode enable, D[2] = SMODE.

The DOUT data in C15 is Reference AGND connection enable, D[1] = VGND_EN.

The DOUT data in C16 is Reference (VR-AGND)/2 connection enable, D[0] = VMID_EN.

2. Chip Enable and Chip Reset

The CE input pin is an input for chip enabled controlled and chip reset controlled. When CE=0, the chip will enter reset condition. In this time, all functions stops operating and the DOUT pin becomes tri-state output, and PADEOC becomes low output. For reducing the power consumption, it is recommended to reset CE pin as 0 when ADC function is inactive.

When CE=1, the chip will wake up from reset condition. All functions have ready to operate and the DOUT pin becomes output data. The chip will get into waiting state to receive the command from serial interface.

Since no power on reset circuitry is built in this chip, it is necessary to set CE pin to 0 after power on state to initiate this chip.

3. PGA OFFSET Initialization

After system power up, ML5012 will initialize the PGA Offset register automatically.

4. System register control

The AD_Clock controls the AD conversion clock frequency; slower clock can save power, but longer conversion time. The STA_OPT, is the startup time option, the shorter the startup time, the sooner will get the result, but the AD result may not be stable.

SMODE is the successive AD conversion mode, when enabled, the ADC will not be automatically disabled after each AD conversion, otherwise, the ADC will be disabled after each AD conversion to save power, when enabled, and the STA_OPT will not have effect after the first conversion, as the ADC is always enabled.

VGND_EN, "VREF = AGND" and VMID_EN, "VREF = (VR-AGND)/2" are selecting the VREF voltage to the PGA, from the below output voltage equation of the PGA.

$$PGA\_OUT = (V_{CHA} - V_{CHB}) \times PGA\_GAIN + VREF$$

Then the PGA_OUT will input to the ADC directly.

When selecting the AD_Range, it's actually selecting the reference zero point. For AD_Range is 0 – 4096, the reference zero point is AGND, when AD_Range is -2047~+2046, the reference zero point is (VR-AGND)/2, so users can select your target AD_Range based on the above calculation.

If AD_Range = 0

$$AD\_OUT = \frac{4096}{VR - AGND} \times [(V_{CHA} - V_{CHB}) \times PGA\_GAIN + VREF]$$

If AD_Range = 1

$$AD\_OUT = \frac{4096}{VR - AGND} \times [(V_{CHA} - V_{CHB}) \times PGA\_GAIN + VREF] - 2048$$

5. A/D conversion mode

The A/D conversion mode converts the analog voltage on the A/D pin into the digital value. The input analog voltage is successively compared with weighted voltages from the capacitor array. Digitized conversion data (12-bit) are stored into 12 bits A/D register A/D[11:0].

The time required for the converter to complete conversion is as follows:

Conversion duration = Oscillator clock period x 15

Example:

(a). 150us (oscillator clock at 100KHz)

(b). 75us (oscillator clock at 200kHz)

Caution:

While in the A/D conversion mode, do not use A/D register A/D[11:0] to store other data.

5-1. Selecting PGA input channel AB & B, PGA Gain & A/D enable control

Executing STCH command to enable Oscillator and then select one of PGA input channel AB (ie. CHA1~4 or CHB1~4) & input channel B (ie. CHB1~4 or AGND) for differential or single end analog input.

- Setting of Oscillator enable pins

  Before using A/D conversion, ENOSC bit must be set to 1 to start-up the oscillator in order to provide the clock for A/D conversion mode.

  It is recommended to turn off the oscillator when A/D conversion mode is completed in order to reduce the power consumption.

- Setting of AD Output Range

Setting of AD Output Range	Output Range
AD_Range = 0	0 ~ 4,095
AD_Range = 1	-2,047 ~ 2,047

Please refer to Section 3-4 for more details.

- Setting of PGA input channel A and B

Case 1 : Differential Analog Input

CHAB_SEL[2:0]			Channel AB	CHB_SEL[2:0]			Channel B
Bit 2	Bit 1	Bit 0		Bit 2	Bit 1	Bit 0	
0	0	0	CHA1	0	0	0	CHB1
0	0	1	CHA2	0	0	1	CHB2
0	1	0	CHA3	0	1	0	CHB3
0	1	1	CHA4	0	1	1	CHB4

Case 2 : Single End Analog Input

CHAB_SEL[2:0]			Channel AB	CHB_SEL[2:0]			Channel B
Bit 2	Bit 1	Bit 0		Bit 2	Bit 1	Bit 0	
0	0	0	CHA1	1	0	0	AGND
0	0	1	CHA2				
0	1	0	CHA3				
0	1	1	CHA4				
1	0	0	CHB1				
1	0	1	CHB2				
1	1	0	CHB3				
1	1	1	CHB4				

- Setting of PGA Gain

  Executing PGA_AC command to set PGA Gain from 0dB to 40.25dB. Please refer to section 1-2 for more details.

5-2. Starting A/D conversion

A/D conversion starts according to the bit setting of the A/D configuration register. All settings specified by the contents of the A/D configuration register which shall set at the same time when A/D conversion starts. Execute PGA_AC command and delivers the desired value into A/D configuration register. Please refer to section 1-2. for the execution of PGA_AC command.

- Setting to start A/D conversion

Setting of A/D configuration register	Operation
EN, S/S = 1	Start of A/D conversion
MD = 0	Set operation mode to A/D conversion

When setting A/D configuration register for A/D conversion start, the bits of A/D configuration register other than bits shown in the table above can be any value. These bits will not affect A/D conversion. In contrast, do not modify contents of the A/D configuration register, the AD Output range and PGA gain value while the A/D converter is running.

5-3. Indication of end of A/D conversion

At the end of A/D conversion the bit S/S and bit EN are cleared. Monitoring one of these bits detects the end of A/D conversion. There is an external pin (PADEOC) to indicate the end of conversion. When the conversion is completed, an "H" pulse signal will be outputted to this pin.

5-4. Storing digitized data

The digital equivalent of analog input voltage (A/Ded data) consisting of 12 bits is stored into A/D register : A/D[11:0].

- A/Ded data stored in A/D register : A/D[11:0]

- Input voltage and A/Ded data at AD_Range = 0 (ie. A/D data = 0 ~ 4,095)
  Input voltage = A/D[11:0] / 4,096 *VR (V) / PGA gain
  Note: A/Ded data (unsigned 12 bits) = Converts into decimal value

- Input voltage and A/Ded data at AD_Range = 1 (ie. A/D data = -2,047 ~ 2,047)

  A/Ded data is a 12 bits signed data which A/D[11] shows the sign of A/Ded data as follow :

  Case 1 : If A/D[11] = 0,

  Input voltage = **+** A/D[10:0] / 2048 *VR (V) / PGA gain

  Case 2 : If A/D[11] = 1,

  Input voltage = **-** A/D[10:0] / 2048 *VR (V) / PGA gain

  Note: A/Ded data (signed 12 bits) = Converts into decimal value

  Executing RR_AD command could read out the contents of A/D register to DOUT pin. Please refer to section 1-5. for the operation of RR_AD command.

6. Comparison mode

The comparison mode compares the level of analog voltage coming from channel AB and B with internal voltage set by the A/D configuration register, storing the result into the bit RSLT of A/D configuration register.

The time required for the converter to complete conversion is as follows:

Conversion duration = Oscillator clock period x 15

Example:

(a). 150us (oscillator clock at 100KHz)

(b). 75us (oscillator clock at 200kHz)

6-1. Selecting PGA channel AB & B input pin, PGA Gain & A/D enable control

Executing STCH command to enable Oscillator and then select one of PGA input channel AB & B for differential analog input or single end input.

- Setting of Oscillator enable pins

  Before using A/D conversion, ENOSC bit must be set to 1 to start-up the oscillator in order to provide the clock for A/D conversion mode.

  It is recommended to turn off the oscillator when A/D conversion mode is completed in order to reduce the power consumption.

- Setting of AD Output Range

Setting of AD Output Range	Output Range
AD_Range = 0	0 ~ 4,095
AD_Range = 1	-2,047 ~ 2,047

Please refer to Section 4-2 for more details.

- Setting of PGA input channel A and B

Case 1 : Differential Analog Input

CHAB_SEL[2:0]			Channel AB	CHB_SEL[2:0]			Channel B
Bit 2	Bit 1	Bit 0		Bit 2	Bit 1	Bit 0	
0	0	0	CHA1	0	0	0	CHB1
0	0	1	CHA2	0	0	1	CHB2
0	1	0	CHA3	0	1	0	CHB3
0	1	1	CHA4	0	1	1	CHB4

Case 2 : Single End Analog Input

CHAB_SEL[2:0]			Channel AB	CHB_SEL[2:0]			Channel B
Bit 2	Bit 1	Bit 0		Bit 2	Bit 1	Bit 0	
0	0	0	CHA1	1	0	0	AGND
0	0	1	CHA2				
0	1	0	CHA3				
0	1	1	CHA4				
1	0	0	CHB1				
1	0	1	CHB2				
1	1	0	CHB3				
1	1	1	CHB4				

- Setting of PGA Gain

  Executing PGA Gain command to set PGA Gain from 0dB to 40.8dB. Please refer to section 1-2 for more details.

6-2. Setting internal comparison voltage

The internal voltage data to be compared with the analog A/D input is stored into the A/D register A/D[11:0], the same location as for storing A/Ded data. The same register are used for storing A/Ded data and internal voltage data.

Executing WR_AD command to deliver the internal voltage data and store the data into A/D register.

- Internal reference voltage data stored in A/D register: A/D[11:0]

- Internal reference voltage at AD Output Range = 0 (A/D Data : 0 ~ 4,095)
  Comparison reference voltage = A/D[11:0] / 4096 * VR (V)
  Note: A/D Register value (unsigned 12 bits) = Convert register value into decimal number

- Internal reference voltage at AD Output Range = 1 (A/D Data : -2,047 ~ 2,047)
  Register value is a 12 bits signed data which A/D[11] shows the sign of A/D Register value as follow :

  Case 1 : If A/D[11] = 0,
  Comparison reference voltage = + A/D[10:0] / 2048 *VR (V)

  Case 2 : If A/D[11] = 1,
  Comparison reference voltage = - A/D[10:0] / 2048 *VR (V)

  Note: A/D Register value (signed 12 bits) = Convert register value into decimal number.

6-3. Starting comparison

The comparison starts when the bit S/S of A/D configuration register is set. The operation mode should be set upon starting of the comparison. All A/D configuration register settings are made at the same time.

- Setting to start comparison

Setting of A/D configuration register	Operation
EN, S/S = 1	Start of A/D conversion
MD = 1	Set operation mode to Comparison mode

Settings of bits other than those necessary to start comparison will not affect the comparison operation. Please do not modify A/D configuration register, AD output range and PGA gain value while the A/D converter is running.

6-4. Indication of end of comparison

At the end of A/D conversion the bit S/S and bit EN are cleared. Monitoring one of these bits detects the end of comparison.

There is an external pin (PADEOC) to indicate the end of conversion. When the conversion is completed, an "H" pulse signal will be outputted to this pin.

6-5. Storing comparison result

The result of comparison sets the bit RSLT of A/D configuration register to either '1' or '0' depending on the level of the input voltages as shown below.

RSLT	Result
RSLT=0	Input voltage * PGA Gain < internal reference voltage
RSLT=1	Input voltage * PGA Gain > internal reference voltage

When the input voltage * PGA Gain is equal to the internal reference voltage, the level of bit RSLT is undefined.

7. Setting MOSFET enable

When CE pin set to 1, all of the MOSFETs are disable. Executing STCH command to enable the MOSFET accordingly. Each of these MOSFETs could be enabled or disable individually.

M1_EN	M2_EN	M3_EN	M4_EN	MOSFET
0	0	0	0	All MOSFETs turn off
1	0	0	0	MOSFET 1 turn on
0	1	0	0	MOSFET 2 turn on
0	0	1	0	MOSFET 3 turn on
0	0	0	1	MOSFET 4 turn on
1	1	1	1	All MOSFETs turn on

8. Summary of A/D Converter operations

Typical operation procedure of A/D converter is summarized as below The bit represented by [X] is user settable.

8-1. General procedure of using A/D conversion mode

The procedure below is to use the A/D converter in the A/D conversion mode. Steps below are to convert the analog voltage between input channel CHA1 and CHB1 in differential input mode to digital value at PGA gain = 0dB with A/D Output Range from -2,047 to 2,047, and VREF = (VR – AGND)/2

	Operation	Setting
1	Start-up oscillator	ENOSC = 1
2	Set A/D Output Range : -2,047 to 2,047	AD_Range = 1
3	Set VREF = (VR – AGND)/2	VMID_EN = 1
4	Select differential analog input CHA1 and CHB1	CHAB_SEL[2:0] = '000' and CHB_SEL[2:0] = '000'
5	Set PGA Gain = 0 dB	PGA_Gain Register = '0000 0000'
6	Specify operation mode and start A/D converter	A/D Configuration Register = '1010'

This procedure starts the A/D converter. When A/D conversion time has elapsed, the A/D converter stops and stores the result in A/D register A/D[11:0]. End of the operation can be verified by reading bits S/S or EN that should be '0'.

8-2. General procedure of using comparison mode

This procedure below is to compare the analog voltage from the analog voltage between CHA2 and AGND in single end input mode at PGA Gain = 20.48dB with internal reference digital value at A/D output range from 0 to 4,095, and VREF = AGND

	Operation	Setting
1	Start-up oscillator	ENOSC = 1
2	Set A/D Output Range : 0 to 4,095	AD_Range = 0
3	Set VREF = AGND	VGND = 1
3	Select single end analog input CHA2 and AGND	CHAB_SEL[2:0] = '001' and CHB_SEL[2:0] = '100'
4	Set PGA Gain = 20.48 dB	PGA_Gain Register = '1000 0000'
5	Store 12 bits of comparison data at A/D register	A/D[11:0] = 'XXXX XXXX XXXX'
6	Specify operation mode and start A/D converter	A/D Configuration Register ='1011'

This procedure starts the A/D converter. When the conversion time has elapsed, the converter stops and stores the result of comparison into bit RSLT of A/D configuration register as follow:

RSLT = '1' when the analog input is higher than the reference voltage

RSLT = '0' when the analog input is lower than the reference voltage

Typical Application Circuit