CV111-1

PCS/DCS-band High Linearity Downconverter

The Communications Edge ™

Product Information

Product Features

- High dynamic range downconverter with integrated LO, IF, & RF amps
- RF: 1710 – 2000 MHz
- IF: 65 – 250 MHz
- +38 dBm Output IP3
- +21 dBm Output P1dB
- 5.3 dB Noise Figure
- Single supply operation (+5 V)
- 6x6 mm 28-pin QFN package
- Low-side LO configuration
- Common footprint with other PCS/UMTS/cellular versions

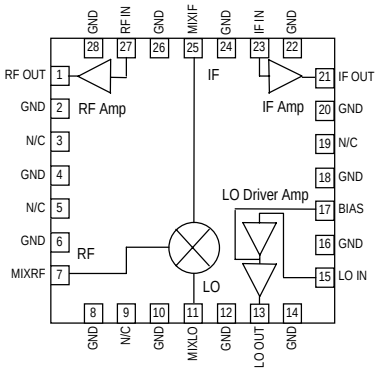
Product Description

The CV111-1 is a high linearity downconverter designed to meet the demanding issues for performance, functionality, and cost goals of current and next generation mobile infrastructure basestations. It provides high dynamic range performance in a low profile surface-mount leadless package that measures 6 x 6 mm square.

Functionality includes RF amplification, frequency conversion and IF amplification, while an integrated LO driver amplifier powers the passive mixer. The MCM is implemented with reliable and mature GaAs MESFET and InGaP HBT technology.

Typical applications include frequency down conversion, modulation and demodulation for receivers used in CDMA/GSM/TDMA, CDMA2000, W-CDMA, GPRS, and EDGE 2.5G mobile infrastructure technologies for PCS / DCS frequency bands.

Functional Diagram



Specifications[1]

Parameters	Units	Minimum	Typical	Maximum	Comments
RF Frequency Range	MHz	1710		2000	
LO Frequency Range	MHz	1460		1935	
IF Center Frequency Range	MHz	65	240	250	See note 2
% Bandwidth around IF center frequency	%		±7.5		See note 2
SSB Conversion Gain	dB		21		Temp = 25° C
Gain Drift over Temp (-40° C to 85° C)	dB		±1.5		Referenced to +25° C
Output IP3	dBm		+38		See note 3
Output IP2	dBm		+48		See note 3
Output 1dB Compression Point	dBm		+21		
Noise Figure	dB		5.3		See note 4
LO Input Drive Level	dBm	-2.5	0	+2.5	
LO-RF Isolation	dB		45		P_{LO} = 0 dBm
LO-IF Isolation	dB		35		P_{LO} = 0 dBm
Return Loss: RF Port	dB		14		
Return Loss: LO Port	dB		14		
Return Loss: IF Port	dB		11		
Operating Supply Voltage	V	+4.9	+5	+5.1	
Supply Current	mA	290	360	480	
FIT Rating	failures/1E9 hrs			72.1	@ 70° C ambient, 90% confidence
Junction Temperature	°C			160	See note 5

1. Specifications when using the application specific circuit (shown on page 3) with a low side LO = 0 dBm in a downconverting application over the operating case temperature range.
2. The IF bandwidth of the converter is defined as 15% around any center frequency in its operating IF frequency range. The bandwidth is determined with external components. Specifications are valid around the total ±7.5% bandwidth. ie. with a center frequency of 240 MHz, the specifications are valid from 240 ± 18 MHz.
3. Assumes the supply voltage = +5 V. OIP3 is measured with Δf = 1 MHz with IF_{out} = 5 dBm / tone.
4. Assumes LO injection noise is filtered at the thermal noise floor, -174 dBm/Hz, at the RF, IF, and Image frequencies.
5. The maximum junction temperature ensures a minimum MTBF rating of 1 million hours of usage.

Absolute Maximum Rating

Parameters	Rating
Operating Case Temperature	-40° to +85° C
Storage Temperature	-55° to +125° C
DC Voltage	+6 V
Junction Temperature	+220 °C
RF Input (continuous)	+2 dBm

Operation of this device above any of these parameters may cause permanent damage.

Ordering Information

Part No.	Description
CV111-1	PCS/DCS-band High Linearity Downconverter
CV111-1PCB240RX	Fully-Assembled Application Board, RF = 1850 – 1910 MHz, IF = 240 MHz
CV111-1PCB240TX	Fully-Assembled Application Board, RF = 1930 – 1990 MHz, IF = 240 MHz

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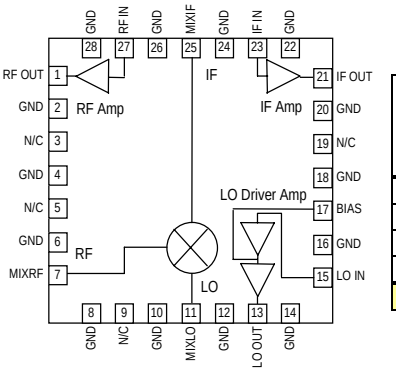
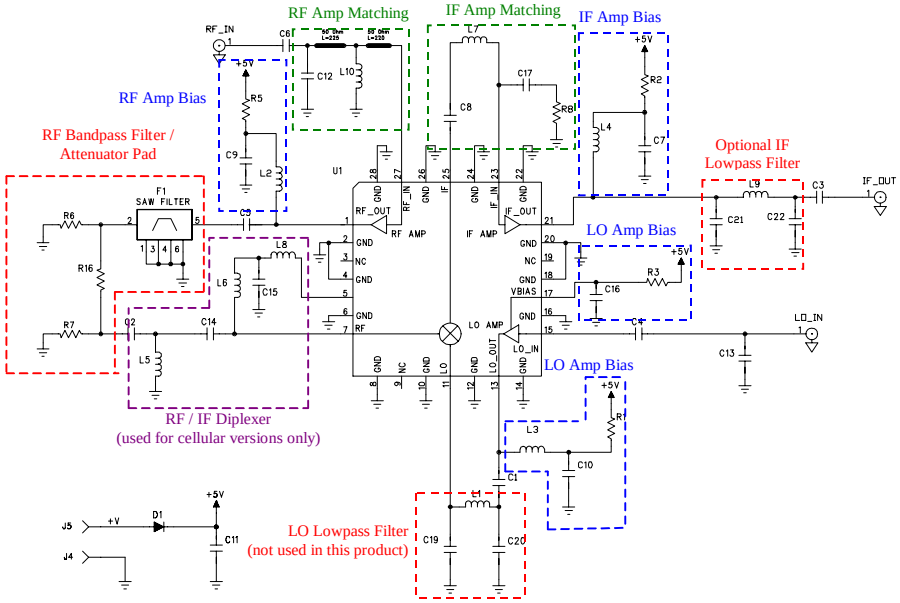
Specifications and information are subject to change without notice

Device Architecture / Application Circuit Information

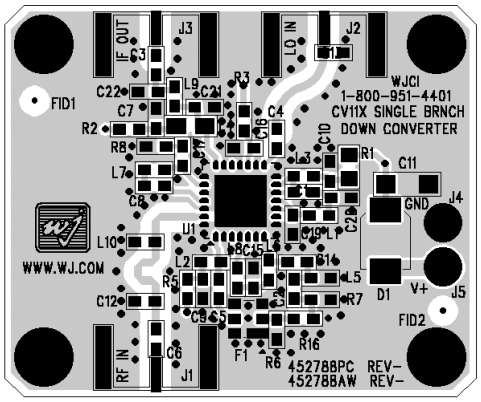


Typical Downconverter Performance Chain Analysis

Stage	Gain (dB)	Output P1dB (dBm)	Output IP3 (dBm)	NF (dB)	Current (mA)	Cumulative Performance			
						Gain (dB)	Output P1dB (dBm)	Output IP3 (dBm)	NF (dB)
RF Amplifier	13	21	41	3.5	140	13	21.0	41.0	3.5
RF Filter	-2	---	---	2.0	---	11	19.0	39.0	3.6
LO Amp / MMIC Mixer	-9	8	23	9.8	80	2	5.9	22.2	4.7
IF Amplifier	19	23	41	2.1	140	21	20.8	38.1	5.2
CV111-1	**Cumulative Performance**				**360**	**21.0**	**20.8**	**38.1**	**5.2**



Printed Circuit Board Material:
.014" FR-4, 4 layers, .062" total thickness



CV111-1: The application circuit can be broken up into four main functions as denoted in the colored dotted areas above: RF/IF diplexing (purple; this is only used with the cellular-band CV products), amplifier matching (green), filtering (red), and dc biasing (blue). There are various placeholders for chip components in the circuit schematic so that a common PCB can be used for all WJ single-branch converters. Additional placeholders for other optional functions such as filtering are also included.

RF / IF Amplifier Matching: The RF amplifier requires a matching element (C12) for optimal gain and input return loss performance. The IF amplifier requires matching elements to optimize the performance of the amplifier to the desired IF center frequency. Since IF bandwidths are typically on the order of 5 to 10%, a simple two element matching network, in the form of either a high-pass or low-pass filter structure, is sufficient to match the MMIC IF amplifier over these narrow bandwidths. Proper component values for other IF center frequencies can be provided by emailing to applications.engineering@wj.com.

RF Bandpass Filtering: Bandpass filtering is recommended to achieve the best noise figure performance with the downconverter. The bandpass filter, implemented with a SAW filter on the application circuit, allows for the suppression of noise from the image frequency. It is permissible to not use a filter and use a 2 dB pad with R6, R7, and R16 instead with slightly degraded noise figure performance.

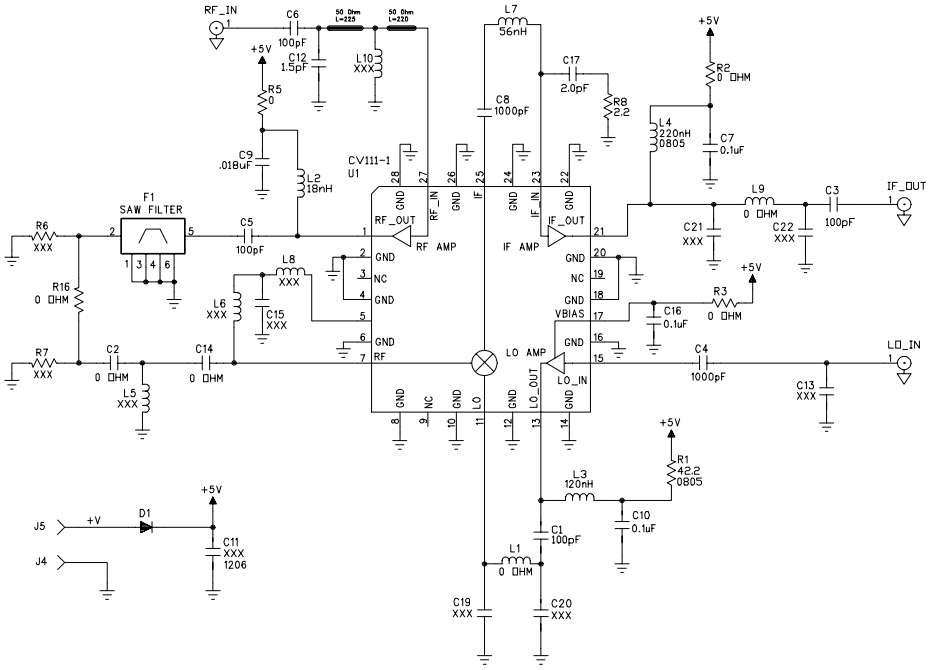
External Diplexer: This is only used with the cellular-band CV products. The mixer performs the diplexing internally for the CV111-1; therefore the components shown in the diplexer section should be loaded as follows: C2 = C14 = 0 Ω.

IF and LO Lowpass Filtering (optional): Filtering of unwanted RF and LO signals are typically performed in the IF chain. This filtering function may be realized using lumped elements; placeholders (L9, C21, C22) are provided in the application circuit to allow for lumped-element filtering to be implemented if desired. The LO lowpass filter is used only in the cellular-band CV products; it should not be used for this product. L1 should be loaded with a 0 Ω jumper.

DC biasing: DC bias must be provided for the RF, LO and IF amplifiers in the converter. R1 sets the operating current for the last stage of the LO amplifier and is chosen to optimize the mixer LO drive level. Proper RF chokes and bypass capacitors are chosen for proper amplifier biasing at the intended frequency of operation. The "+5 V" dc bias should be supplied directly from a voltage regulator.

Downconverting Application Circuit: CV111-1PCB240RX
RF = 1850 – 1910 MHz, IF = 240 MHz

(Targeted for PCS-band Receive Path Downconversion Applications)



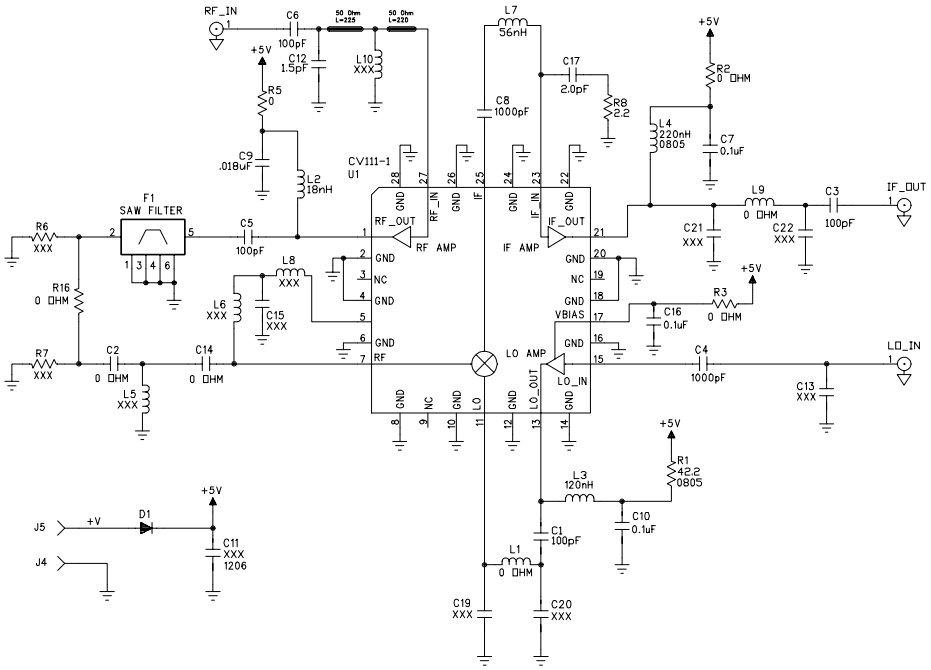
Bill of Materials

Ref. Desig.	Component
R1	42.2 Ω chip resistor, size 0805
R2, R3, R5 R16, C2, C14, L1, L9	0 Ω chip resistor
R6, R7, C11 C13, C15, C19 C20, C21, C22 L5, L6, L8, L10	DNP
R8	2.2 Ω chip resistor
C1, C3, C5, C6	100 pF chip capacitor
C4, C8	1000 pF chip capacitor
C7, C10, C16	0.1 µF chip capacitor
C9	0.018 µF chip capacitor
C12	1.5 pF chip capacitor
C17	2.0 pF chip capacitor
L2	18 nH chip inductor
L3	120 nH chip inductor
L4	220 nH chip inductor, size 0805
L7	56 nH chip inductor
F1	SAWTEK Filter 855849 1850 – 1910 MHz BW
D1	Jumper wire (or 0 Ω resistor)
U1	CV111-1 WJ Converter

All components are of size 0603 unless otherwise specified.
DNP represents "Do Not Place"

Downconverting Application Circuit: CV111-1PCB240TX
RF = 1930 – 1990 MHz, IF = 240 MHz

(Targeted for PCS-band Transmit Path Error Correction Feedback Applications)



Bill of Materials

Ref. Desig.	Component
R1	42.2 Ω chip resistor, size 0805
R2, R3, R5 R16, C2, C14, L1, L9	0 Ω chip resistor
R6, R7, C11 C13, C15, C19 C20, C21, C22 L5, L6, L8, L10	DNP
R8	2.2 Ω chip resistor
C1, C3, C5, C6	100 pF chip capacitor
C4, C8	1000 pF chip capacitor
C7, C10, C16	0.1 µF chip capacitor
C9	0.018 µF chip capacitor
C12	1.5 pF chip capacitor
C17	2.0 pF chip capacitor
L2	18 nH chip inductor
L3	120 nH chip inductor
L4	220 nH chip inductor, size 0805
L7	56 nH chip inductor
F1	SAWTEK Filter 855817 1920 – 1980 MHz BW
D1	Jumper wire (or 0 Ω resistor)
U1	CV111-1 WJ Converter

All components are of size 0603 unless otherwise specified.
DNP represents "Do Not Place"

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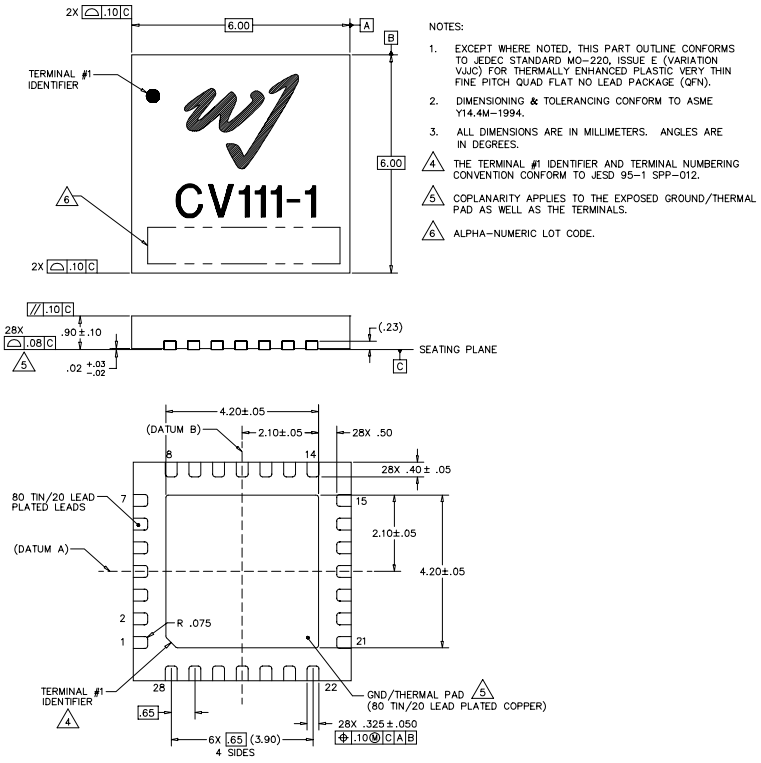
Product Information

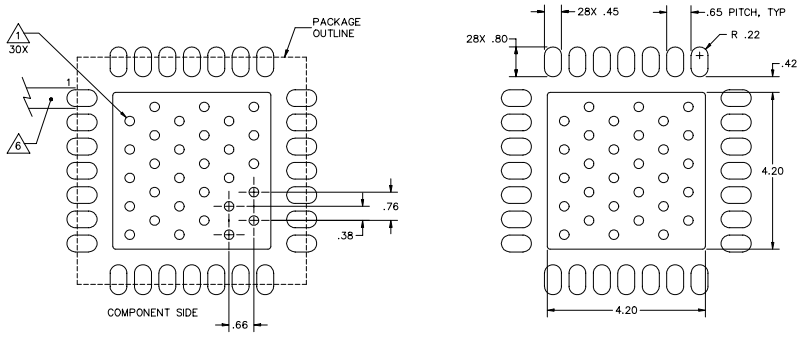
Outline Drawing

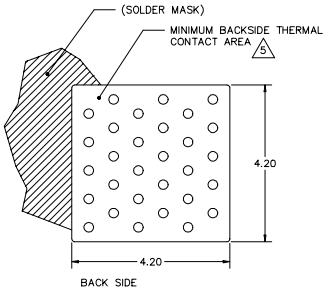


NOTES:

1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-220, ISSUE E (VARIATION VJJC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95-1 SPP-012.
5. COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
6. ALPHA-NUMERIC LOT CODE.

Mounting Configuration / Land Pattern





NOTES:

1. GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCE OF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL, PLATED THRU DIAMETER OF .25mm (.010").
2. ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
3. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL.
4. ADD MOUNTING SCREWS NEAR THE PART TO FASTEN THE BOARD TO A HEATSINK. ENSURE THAT THE GROUND/THERMAL VIA REGION CONTACTS THE HEATSINK.
5. DO NOT PUT SOLDER MASK ON THE BACK SIDE OF THE PC BOARD IN THE REGION WHERE THE BOARD CONTACTS THE HEATSINK.
6. RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.
7. USE 1 OZ. COPPER MINIMUM.
8. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

Product Marking

The component will be lasermarked with a "CV111-1" product label with a four-digit alphanumeric lot code on the top surface of the package. Tape and reel specifications for this part will be located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Classification:	Class 1B
Value:	Passes ≥ 500 V to <1000 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
ESD Classification:	Class III
Value:	Passes ≥ 500 V to <1000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101
MSL Rating:	Level 1 at +250 °C convection reflow
Standard:	JEDEC Standard J-STD-020B

Functional Pin Layout

Pin	FUNCTION	Pin	FUNCTION
1	RF Amp Output	15	LO Amp Input
2	GND	16	GND
3	N/C	17	LO Amp Bias
4	GND	18	GND
5	N/C	19	N/C
6	GND	20	GND
7	Mixer RF Input	21	IF Amp Output/Bias
8	GND	22	GND
9	N/C	23	IF Amp Input
10	GND	24	GND
11	Mixer LO Input	25	Mixer IF Output
12	GND	26	GND
13	LO Amp Output	27	RF Amp Input
14	GND	28	GND

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