DATA SHEET

SKY65146-21: 806-849 MHz, 3.5 V Broadband Power Amplifier

Applications

- iDEN® (806-825 MHz)
- TETRA (806-825 MHz)
- TDMA (824-849 MHz)
- AMPS (824-849 MHz)
- WLLs

Features

- Low voltage, positive bias supply: 3.5 V
- High gain = 39 dB
- High saturated output power = +35.6 dBm
- High efficiency: 51% PAE
- Good linearity
- Dual-mode operation
- Large dynamic range
- Internal RF match
- Power-down control
- Small, MCM (28-pin, 10 x 14 mm) package (MSL3, 260 °C per JEDEC J-STD-020)

NEW Skyworks offers lead (Pb)-free RoHS (Restriction of Hazardous Substances) compliant packaging.

Description

The SKY65146-21 is a fully-matched Microwave Monolithic Integrated Circuit (MMIC) Power Amplifier (PA) with high efficiency and good linearity. The device is designed for private mobile radios, Wireless Local Loops (WLLs), and Time Division Multiple Access/Advanced Mobile Phone System (TDMA/AMPS) mobile units operating in the 806 to 849 MHz cellular bandwidth.

The SKY65146-21 contains all the active circuitry, which includes onboard bias circuitry and the interstage matching circuit. The input/output match is realized off-chip within the module package to optimize efficiency and high power performance into a 50 Ω load.

Primary bias to the SKY65146-21 is supplied directly from a single cell lithium ion, or other suitable, battery with a nominal output of 3.5 V. No external supply side switch is needed since typical "off" leakage is a only a few microamperes with full primary voltage supplied from the battery.

The SKY65146-21 is fabricated using Skyworks high reliability Heterojunction Bipolar Transistor (HBT) GaAs process. The device is mounted in a 28-pin, 10.04 x 14.04 mm Multi-Chip Module (MCM) package, which allows for a highly manufacturable low cost solution.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

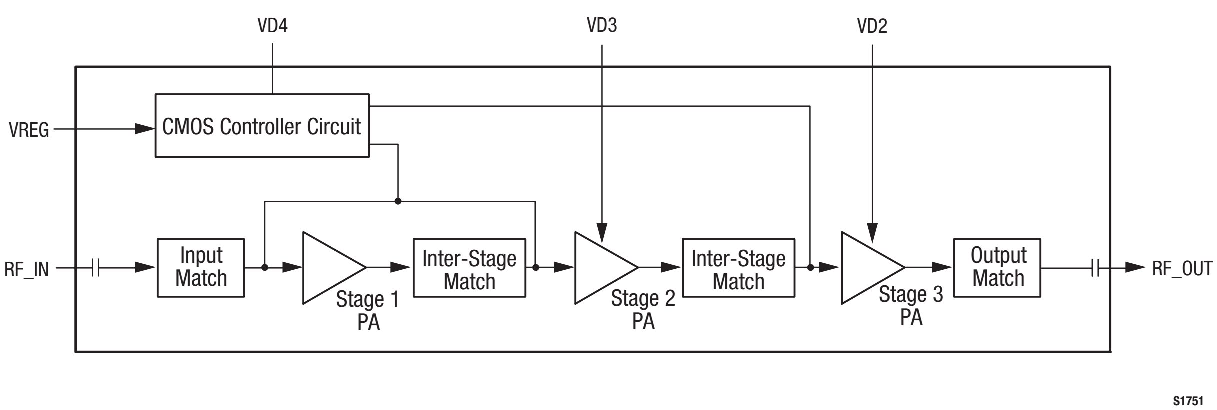


Figure 1. SKY65146-21 Block Diagram

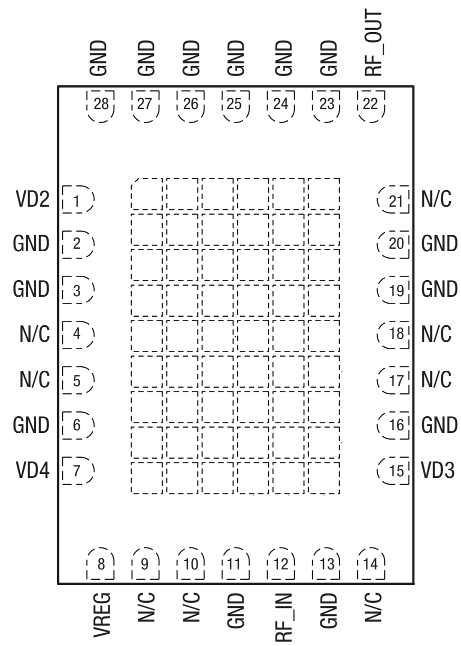


Figure 2. SKY65146-21 Pinout – 28-Pin MCM (Top View)

Table 1. SKY65146-21 Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	VD2	Supply voltage for output (final) stage collector bias (typically 3.5 V)	15	VD3	Supply voltage for driver collector bias (typically 3.5 V)
2	GND	Ground	16	GND	Ground
3	GND	Ground	17	N/C	No connection
4	N/C	No connection	18	N/C	No connection
5	N/C	No connection	19	GND	Ground
6	GND	Ground	20	GND	Ground
7	VD4	Supply voltage for base bias circuitry to all stages (typically 3.5 V)	21	N/C	No connection
8	VREG	Regulated bias enable control voltage (0 V = off, 2.75 V = on)	22	RF_OUT	806 to 849 MHz RF output signal (50 Ω)
9	N/C	No connection	23	GND	Ground
10	N/C	No connection	24	GND	Ground
11	GND	Ground	25	GND	Ground
12	RF_IN	806 to 849 MHz RF input signal (50 Ω)	26	GND	Ground
13	GND	Ground	27	GND	Ground
14	N/C	No connection	28	GND	Ground

Note: The center attachment pad must have a low inductance and low thermal resistance connection to the printed circuit board ground plane.

Functional Description

The SKY65146-21 is a fully-matched, three-stage, GaAs HBT PA with on-chip interstage matching and bias circuitry. The input/output match is realized off-chip, but within the module package. The PA uses series feedback on the first and second stages to provide for high gain, stability, and power of up to 4 W.

The module includes a silicon CMOS controller circuit to provide a regulated bias enable control for on/off operation (VREG, pin 8). In off mode, supply current is a few microamperes with VREG = 0 V. The module operates with all positive DC voltages while maintaining high efficiency and good linearity. The nominal operating voltage is 3.5 V for maximum power, but can be operated at slightly lower voltages for some mobile applications.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY65146-21 are provided in Table 2. The recommended operating conditions are specified in Table 3 and electrical specifications are provided in Table 4.

Performance characteristics for the SKY65146-21 are illustrated in Figures 3 through 30.

Table 2. SKY65146-21 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Maximum	Units
RF input power (Note 2)	P_{IN}		0	dBm
Supply voltage (Note 3)	V_{CC}		6.9	V
Regulated supply voltage (Note 4)	V_{REG}		V_{CC}	V
Case temperature	T_C	–40	+85	°C
Storage temperature	T_{STG}	–55	+125	°C
Junction temperature	T_J		+150	°C
Thermal resistance	Θ_{JC}		19	°C/W

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

Note 2: For pulsed operation with duty cycle < 25%.

Note 3: When amplifier is biased off (V_{REG} = 0 V).

Note 4: Voltage on VREG pin may not exceed the applied V_{CC} voltage.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 3. SKY65146-21 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	V_{CC}	3.0	3.5	4.4	V
Regulated voltage	V_{REG}	2.65	2.75	2.85	V
Operating frequency	f	806		849	MHz
Continuous RMS output power	P_{OUT_RMS}		+29	+31	dBm
Case temperature	T_C	–40	+25	+85	°C

Note 1: Voltage levels measured at the pins of the package. The Evaluation Board supply voltage levels may be different. Refer to the Evaluation Board schematic diagram in this document.

Table 4. SKY65146-21 Electrical Specifications (Note 1)
(V_{CC} = VD2 = VD3 = VD4 = 3.5 V, V_{REG} = 2.75 V, Frequency = 815 MHz, T_C = 25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Frequency range	f		806		825	MHz
Small signal gain	|S21|			38.7		dB
Power gain	G_P	P_{OUT} = +29 dBm	35.5	38.7	40.0	dBm
Input return	|S11|	Small signal	–12	–17		dB
Saturated output power	P_{SAT}	Gain compression ≤ 3 dB	+35.1	+35.6		dBm
Power-Added Efficiency	PAE	P_{OUT} = P_{SAT}	47	51		%
Current @ P_{SAT}	I_{CC_SAT}	P_{OUT} = P_{SAT}		2		A
Quiescent current	I_{CCQ}	No RF input	270	329	370	mA
Harmonics	2fo 3fo 4fo	P_{OUT} = P_{SAT} P_{OUT} = P_{SAT} P_{OUT} = P_{SAT}		–37 –60 –80		dBc dBc dBc
Noise power in the receive band	Rx_bn	f = 845 MHz, P_{OUT} = ≤ +29 dBm bandwidth = 18 kHz			–85	dBm/Hz
Noise Figure	NF	CW		6.8	8.0	dB
Stability (spurious output)	S	Output VSWR = 10:1			–36	dBm
Ruggedness (no damage)		P_{OUT} = ≤ +29 dBm	15:1			–

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Typical Performance Characteristics

(V_{CC} = VD2 = VD3 = VD4 = 3.5 V, V_{REG} = 2.75 V, Frequency = 815 MHz, T_C = 25 °C, Unless Otherwise Noted)

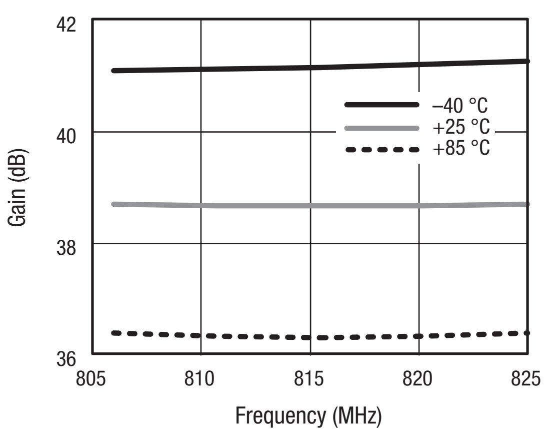


Figure 3. Gain vs Frequency Over Temperature

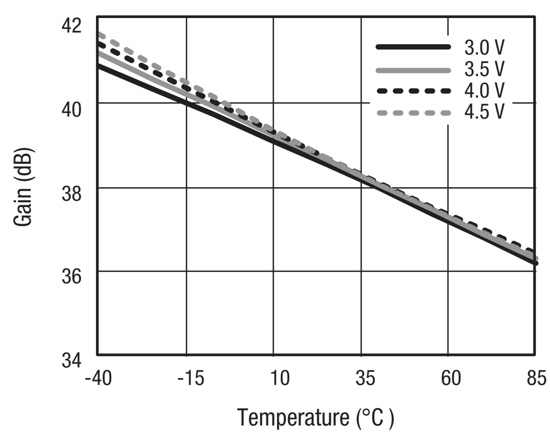


Figure 4. Gain vs Temperature Over Voltage

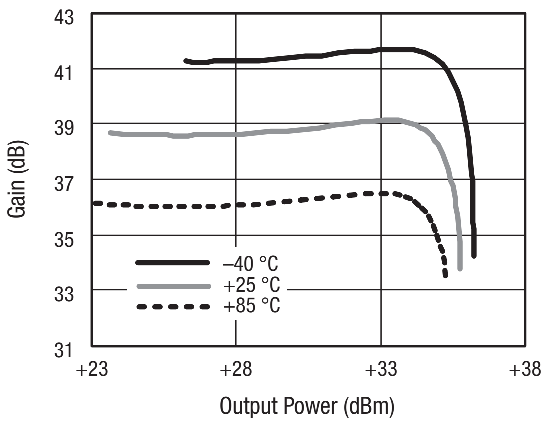


Figure 5. Gain vs Output Power Over Temperature

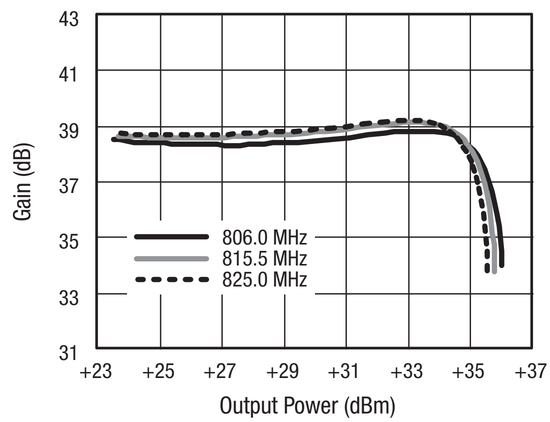


Figure 6. Gain vs Output Power Over Frequency

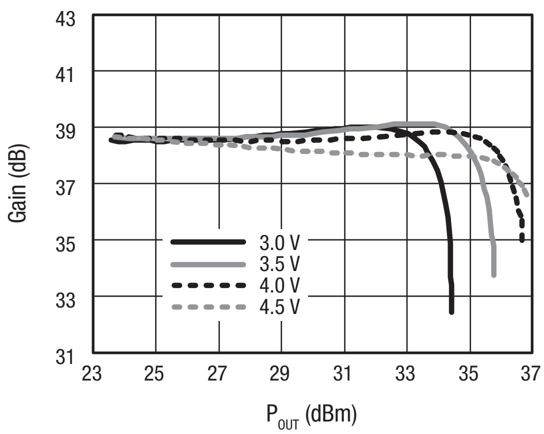


Figure 7. Gain vs Output Power Over Voltage

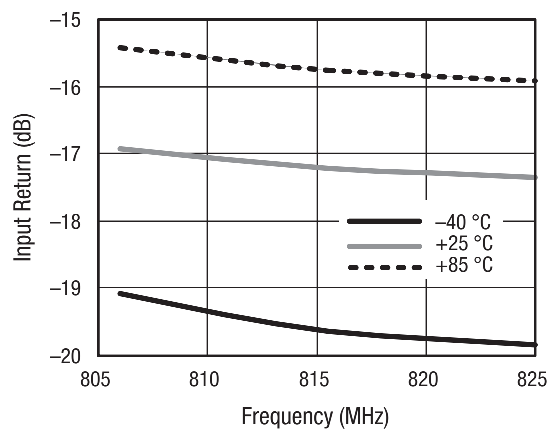


Figure 8. Input VSWR vs Frequency Over Temperature

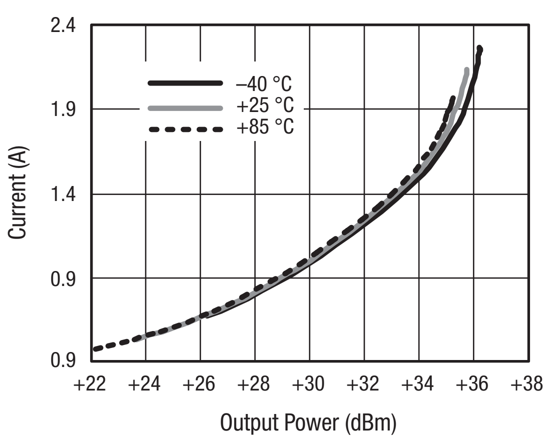


Figure 9. Current vs Output Power Over Temperature

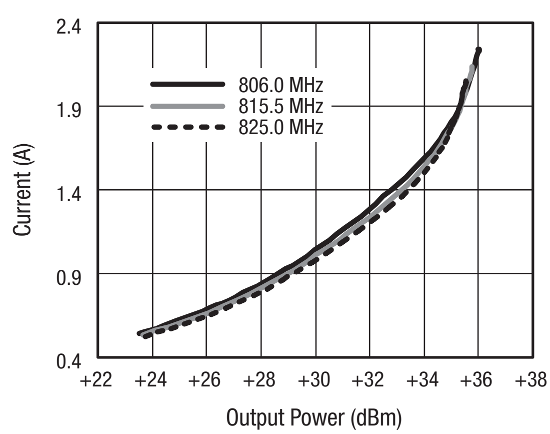


Figure 10. Current vs Output Power Over Frequency

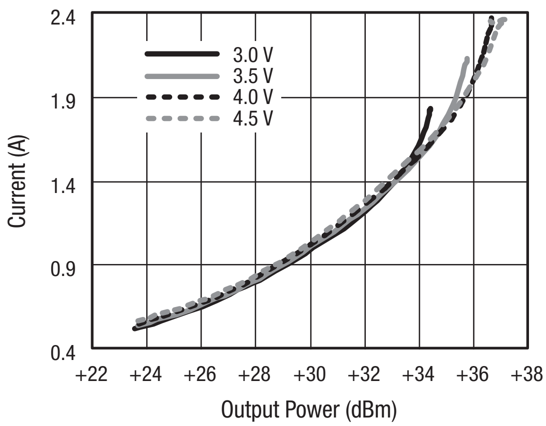


Figure 11. Current vs Output Power Over Voltage

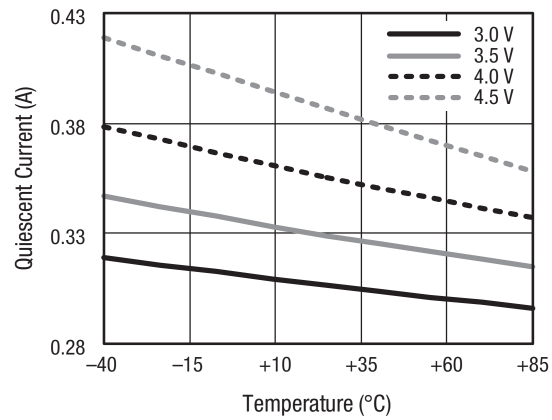


Figure 12. Quiescent Current vs Temperature Over Voltage

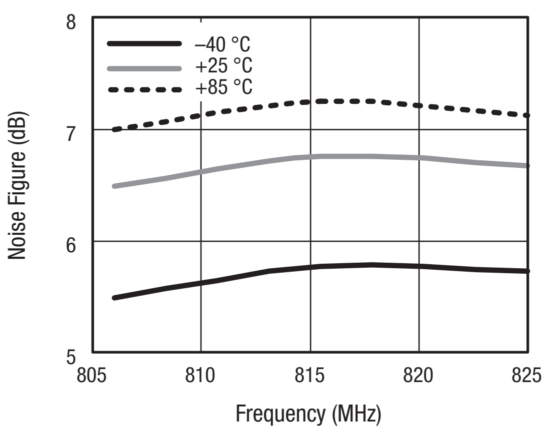


Figure 13. Noise Figure vs Frequency Over Temperature

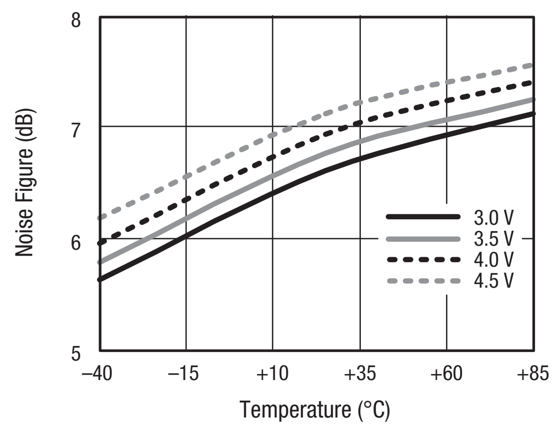


Figure 14. Noise Figure vs Temperature Over Voltage

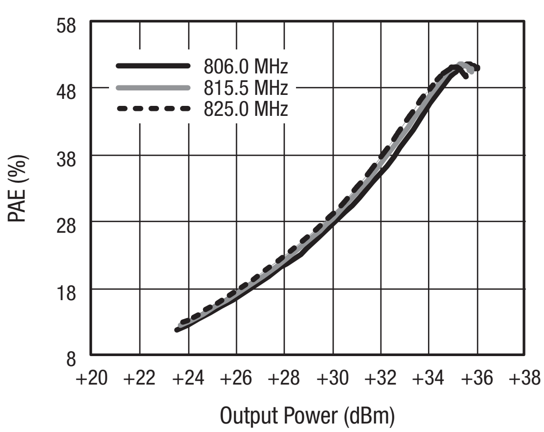


Figure 15. Power-Added Efficiency vs Output Power Over Frequency

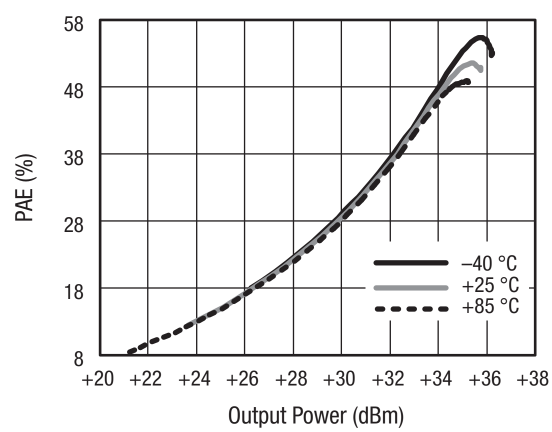


Figure 16. Power-Added Efficiency vs Output Power Over Temperature

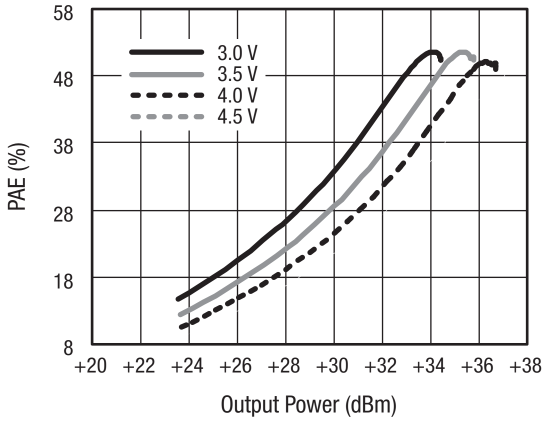


Figure 17. Power-Added Efficiency vs Output Power Over Voltage
****** NO PLOT FOR 4.5 V !!!! *****

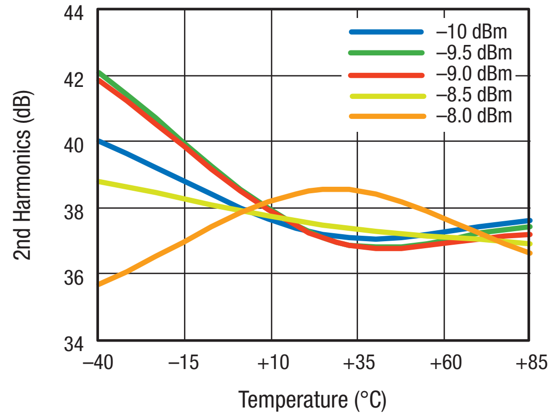


Figure 18. Second Harmonics vs Temperature Over Input Power

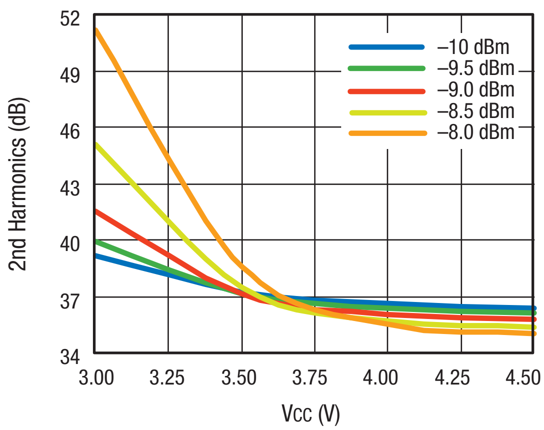


Figure 19. Second Harmonics vs Voltage Over Input Power

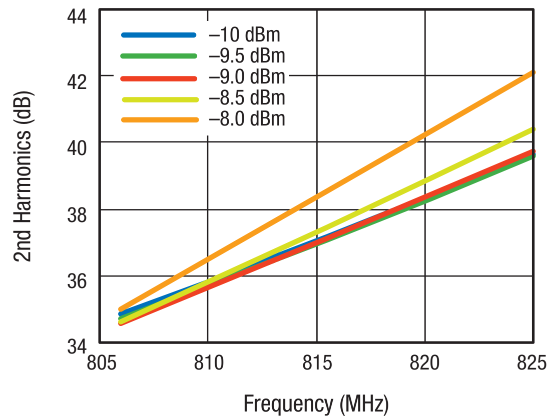


Figure 20. Second Harmonics vs Frequency Over Input Power

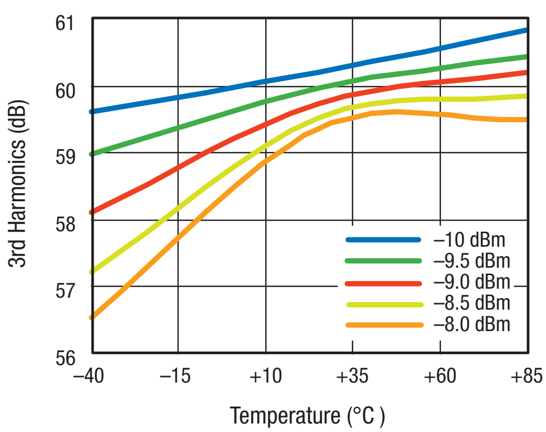


Figure 21. Third Harmonics vs Temperature Over Input Power

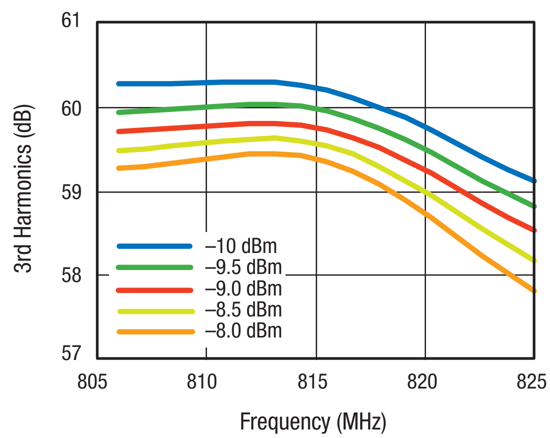


Figure 22. Third Harmonics vs Frequency Over Input Power

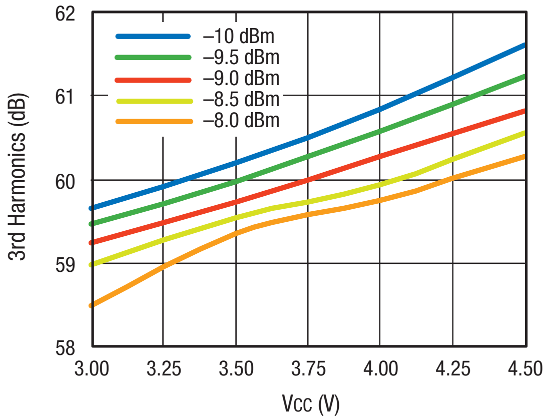


Figure 23. Third Harmonics vs Voltage Over Input Power

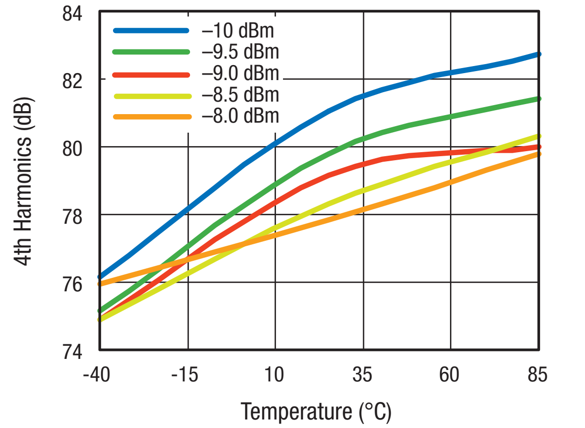


Figure 24. Fourth Harmonics vs Temperature Over Input Power

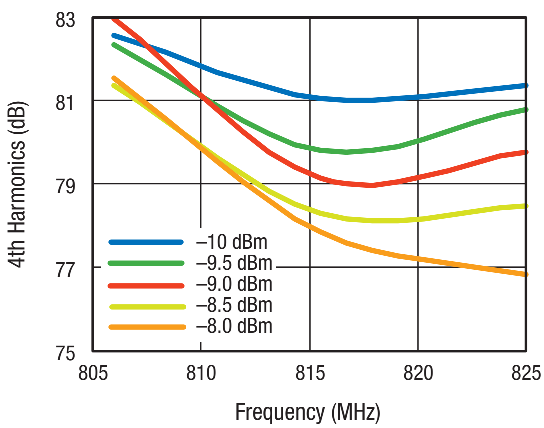


Figure 25. Fourth Harmonics vs Frequency Over Input Power

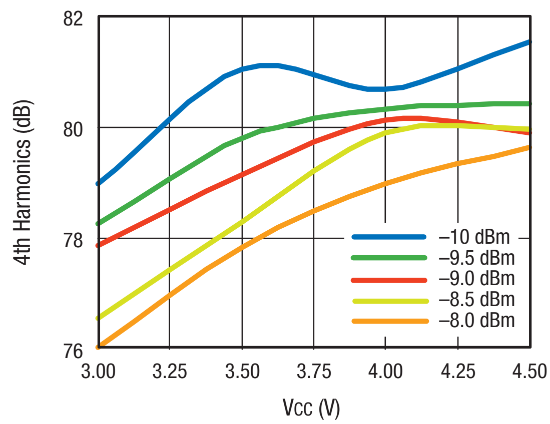


Figure 26. Fourth Harmonics vs Voltage Over Input Power

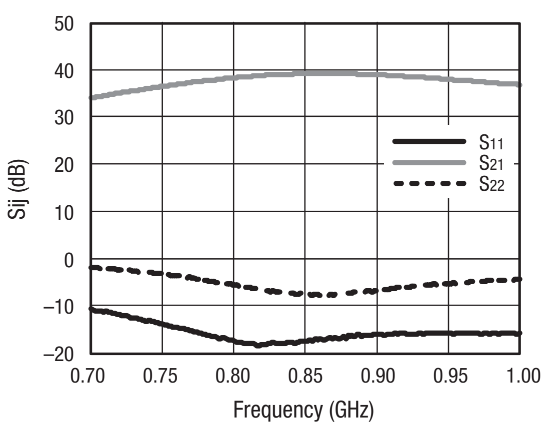


Figure 27. S-Parameters vs Frequency

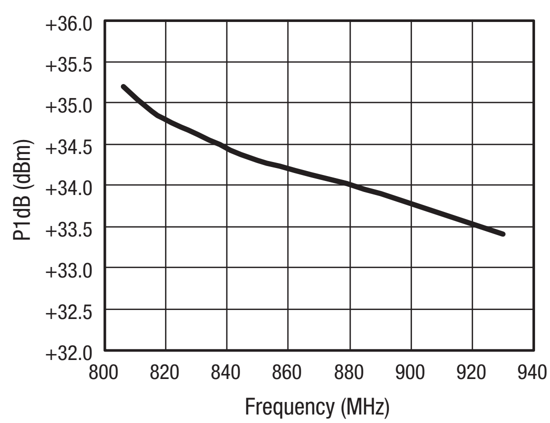


Figure 28. 1 dB Compression Point vs Frequency

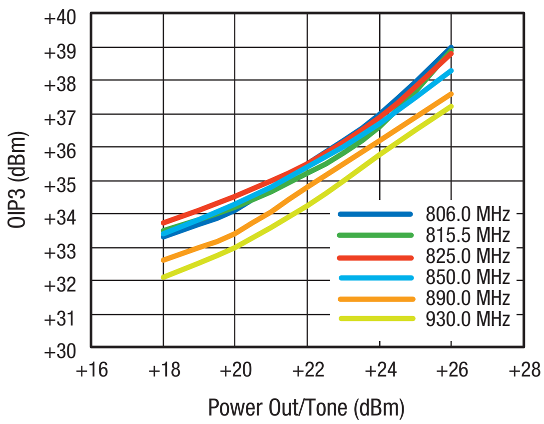


Figure 29. 3rd Order Output Intercept Point vs Output Power/Tone Over Frequency (Tone Spacing = 1 MHz)

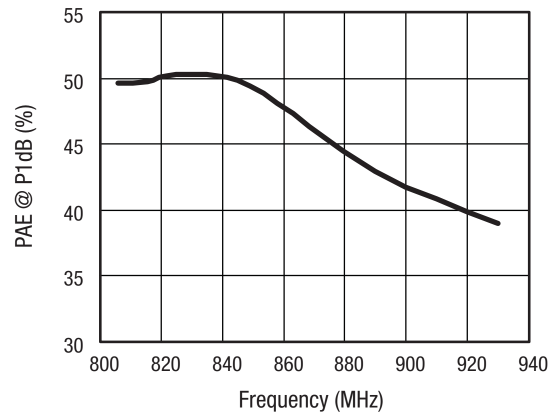


Figure 30. Power-Added Efficiency @ P1dB vs Frequency

Evaluation Board Description

The SKY65146-21 Evaluation Board is used to test the performance of the SKY65146-21 PA. An Evaluation Board schematic diagram is provided in Figure 31. Table 5 provides the Bill of Materials (BOM) list for Evaluation Board components.

An assembly drawing for the Evaluation Board is shown in Figure 32. Layer detail physical characteristics are noted in Figure 33.

Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

1. Paths to ground should be made as short as possible.
2. The ground pad of the SKY65146-21 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Since the circuit board acts as the heat sink, it must shunt as much heat as possible from the device. Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board. Multiple vias to the grounding layer are required.

NOTE: *A poor connection between the slug and ground increases junction temperature (T_J), which reduces the lifetime of the device.*

Evaluation Board Test Procedure

Step 1: Connect RF test equipment to the Evaluation Board input/output SMA connectors.

Step 2: Connect DC ground.

Step 3: Connect VD2, VD3, and VD4 to a 3.5 V supply and VREG to a 2.75 V supply. Verify that the current is approximately 329 mA.

Step 4: Apply RF signal data at a –30 dBm level and observe that the output level is approximately +8 dBm and the gain of the device is approximately 38 dB.

NOTE: *It is important to adjust the VD2, VD3, and VD4 voltage source so that +3.5 V is measured at the board. The high collector currents will drop the collector voltage significantly if long leads are used. Adjust the bias voltage to compensate.*

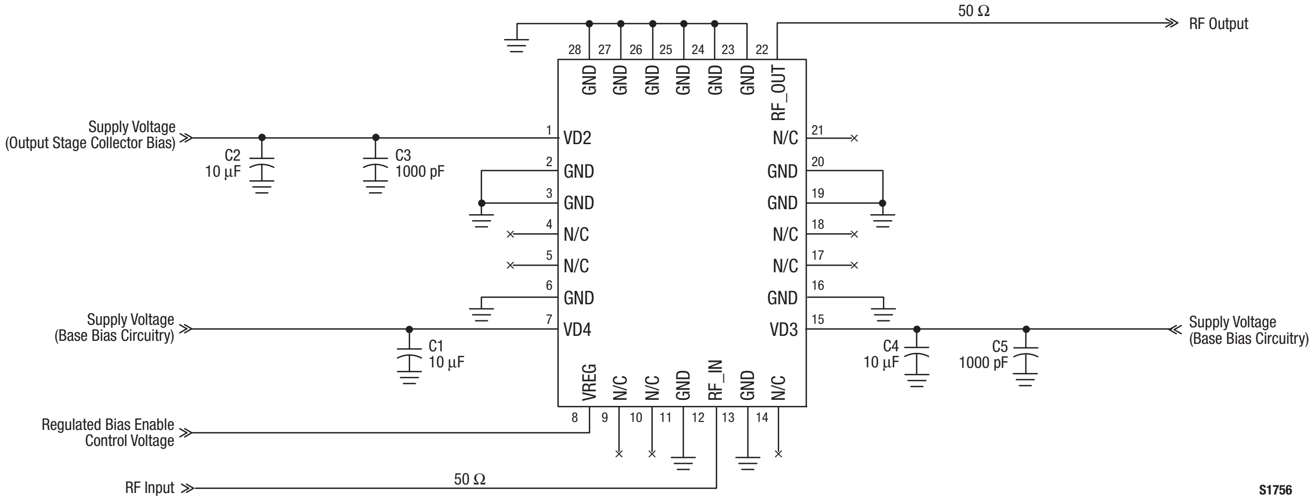
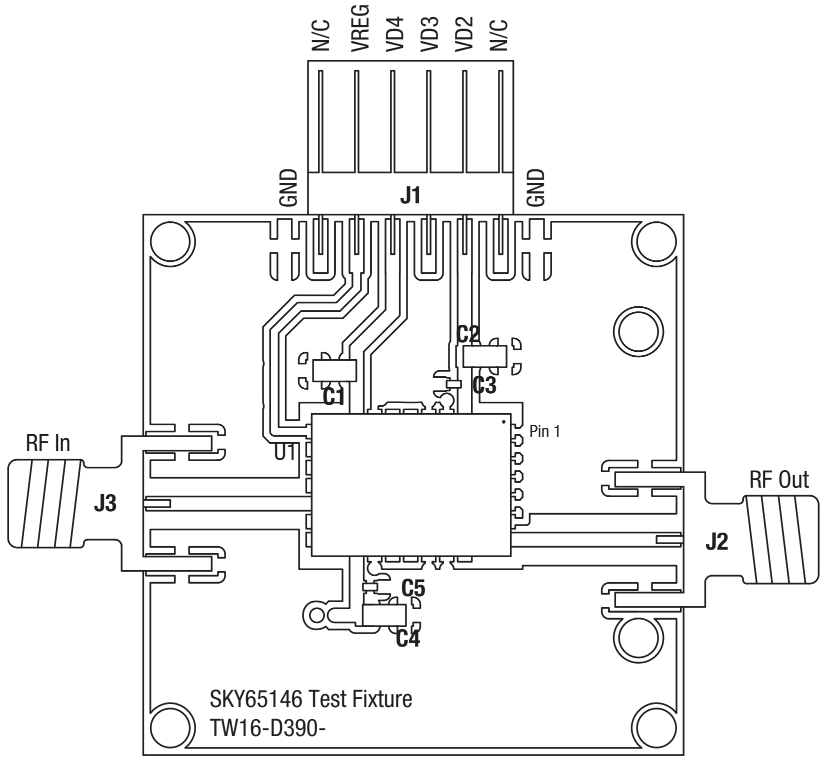


Figure 31. SKY65146-21 Evaluation Board Schematic

Table 5. SKY65146-21 Evaluation Board Bill of Materials

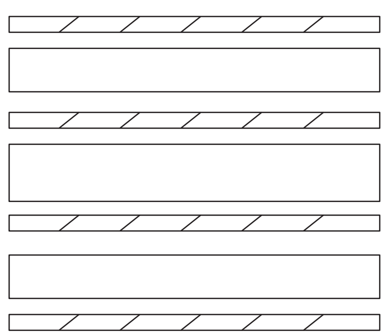
Component	Size	Value	Vendor	Part Number
C1	1206	10 µF	AVX	TAJA106M006R
C2	1206	10 µF	AVX	TAJA106M006R
C3	0402	1000 pF	Murata	GRM155R71H102KA01
C4	1206	10 µF	AVX	TAJA106M006R
C5	0402	1000 pF	Murate	GRM155R71H102KA01



Note: Capacitors C6 and C7 are shown on the Evaluation Board but are not used.

Figure 32. SKY65146-21 Evaluation Board Assembly Diagram

Cross Section



Name	Thickness (mm)	Material	ε_r
Pri	0.025	Cu	–
Lam1	0.400	Rogers 4003	3.38
L2	0.025	Cu	–
Lam2	0.600	FR4	4.00
L3	0.025	Cu	–
Lam3	0.400	FR4	4.00
L4	0.025	Cu	–

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Figure 33. Evaluation Board Layer Detail Physical Characteristics

Application Circuit Notes

Center Ground. It is extremely important to sufficiently ground the bottom ground pad of the device for both thermal and stability reasons. Multiple small vias are acceptable and will work well under the device if solder migration is an issue.

VD2 (pin 1). Supply voltage for the output (final) stage collector bias (typically 3.5 V). The VD2 pin can be bypassed using capacitors C2 and C3. The pin should be placed in the approximate location shown on the Evaluation Board, but exact placement is not critical.

GND (pins 2, 3, 6, 11, 13, 16, 19, 20, and 23 through 28). Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via that the layout allows. Multiple small vias are acceptable and will work well under the device if solder migration is an issue.

N/C (pins 4, 5, 9, 10, 14, 17, 18, and 21). These pins are open and may or may not be connected to ground.

VD4 (pin 7). Supply voltage for base bias circuitry to all stages (typically 3.5 V). The VD4 pin can be bypassed using capacitor C1. The pin should be placed in the approximate location shown on the Evaluation Board, but exact placement is not critical.

VREG (pin 8). Regulated, bias enable control voltage for the silicon CMOS controller (0 V = off; 2.75 V = on). Nominal enable voltage is between 2.65 VDC and 2.85 VDC. When this pin is set to 0 V, the PA is forced into standby mode.

RF_IN (pin 12). Amplifier RF input pin (characteristic impedance, Z_0, equals 50 Ω). The module includes an internal, onboard DC blocking capacitor. All impedance matching is provided internal to the module.

VD3 (pin 15). Supply voltage for the driver collector bias (typically 3.5 V). The VD3 pin can be bypassed using capacitors C4 and C5. The pin should be placed in the approximate location shown on the Evaluation Board, but exact placement is not critical.

RF_OUT (pin 22). Amplifier RF output pin (characteristic impedance, Z_0, equals 50 Ω). The module includes an internal, onboard DC blocking capacitor. All impedance matching is provided internal to the module.

Package Dimensions

Typical case markings are shown in Figure 34. The PCB layout footprint for the SKY65146-21 is shown in Figure 35. Package dimensions for the 28-pin MCM are shown in Figure 36, and tape and reel dimensions are provided in Figure 37.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

THE SKY65146-21 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *PCB Design and SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format. For packaging details, refer to the Skyworks Application Note, *Tape and Reel Information – RF Modules*, document number 101568.

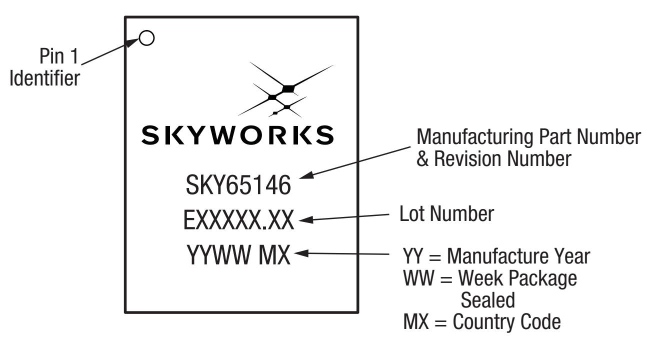


Figure 34. SKY65146-21 Typical Case Markings

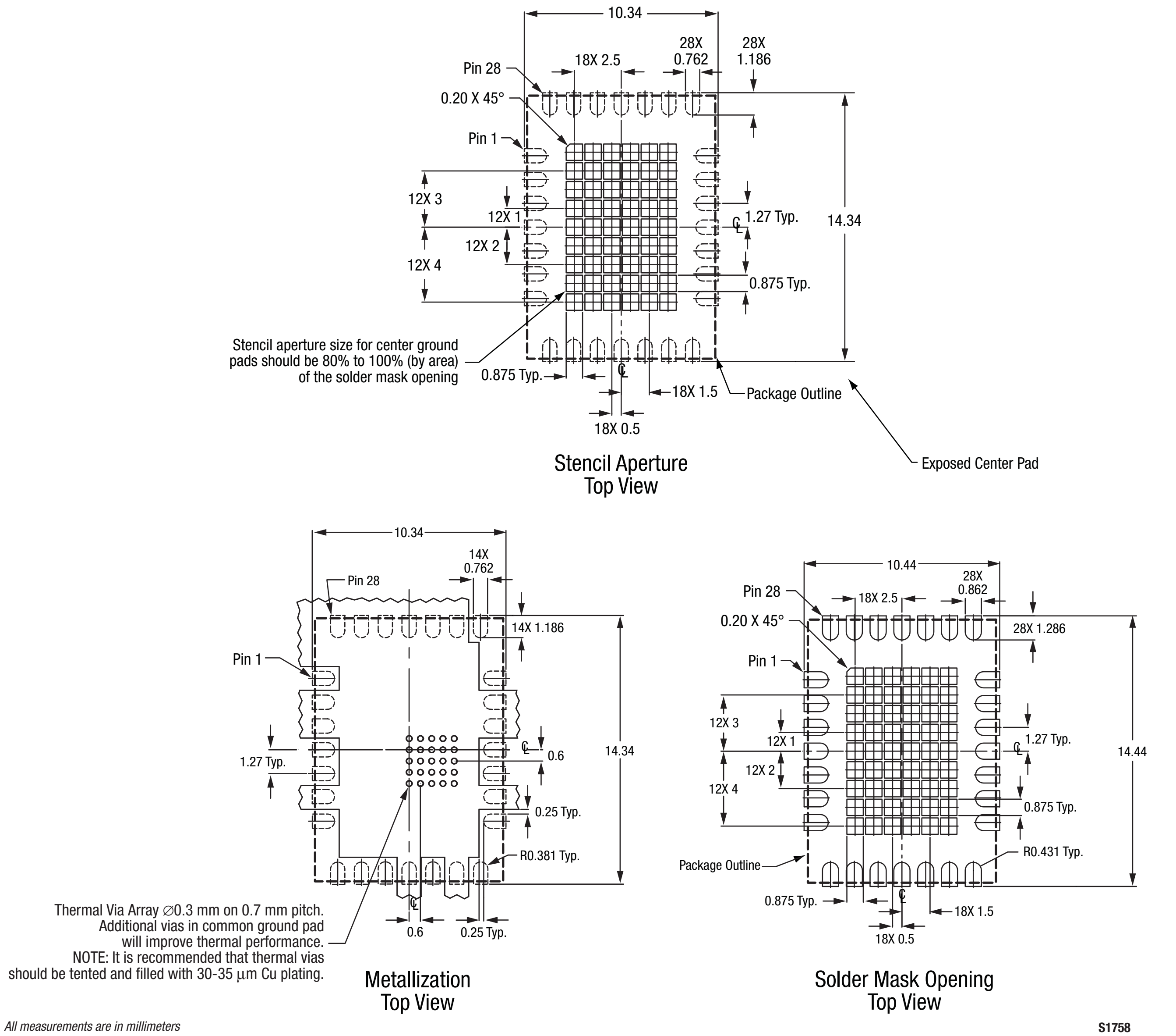
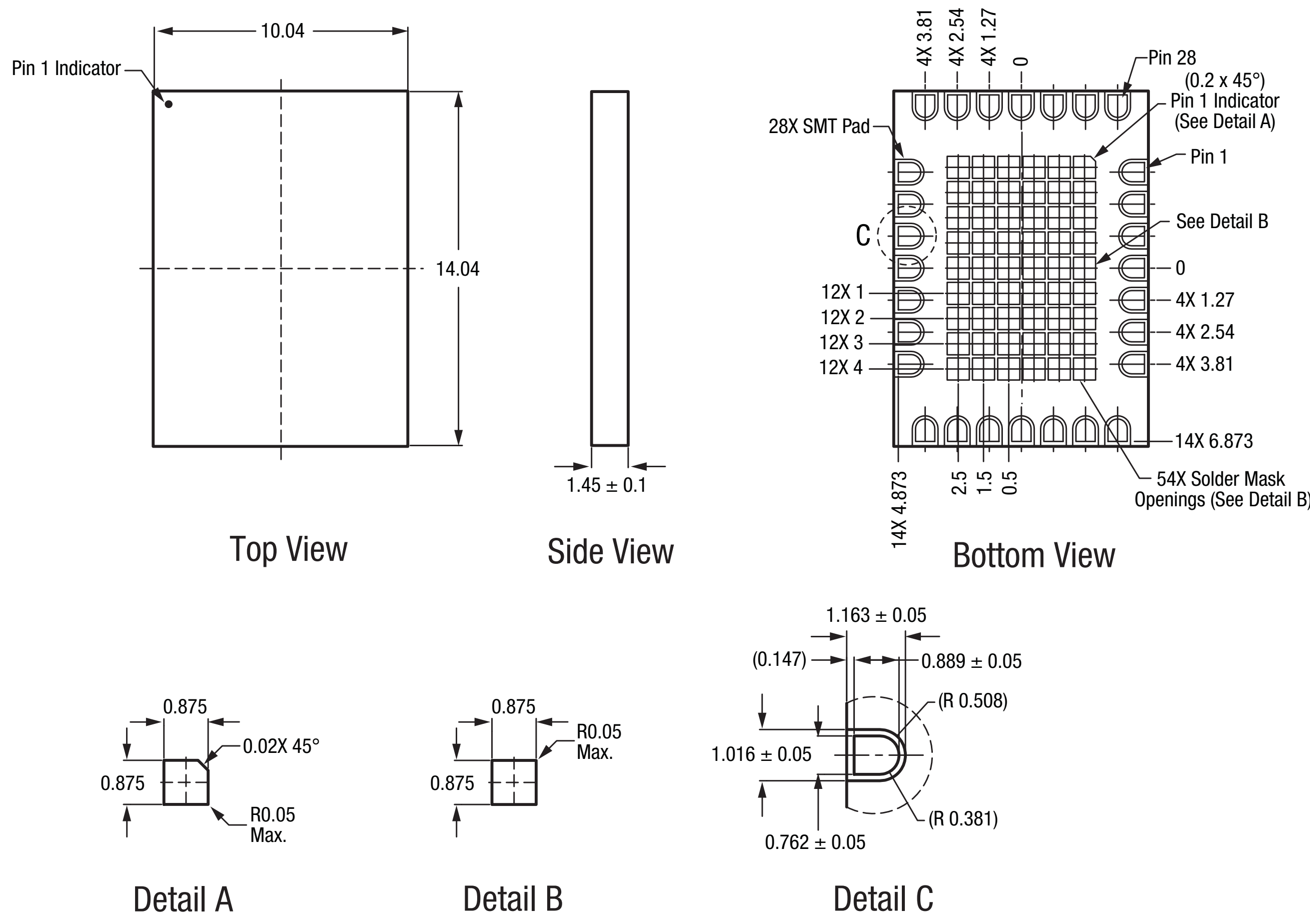


Figure 35. SKY65146-21 PCB Layout Footprint



All measurements are in millimeters.

Dimensioning and tolerancing according to ASME Y14.5M-1994.

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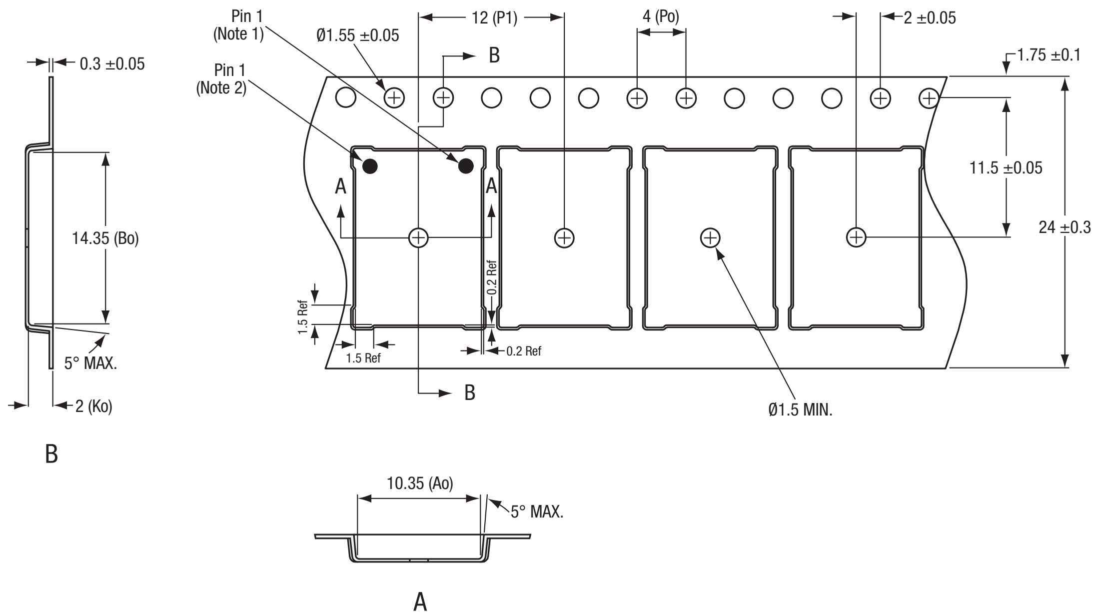
Figure 36. SKY65146-21 28-Pin MCM Package Dimensions



Notes:
1. *Orientation of pin 1 for a 10.04 x 14.04 mm package with a 1.3 mm mold cap.*
2. *Orientation of pin 1 for a 10.04 x 14.04 mm package with a 0.5 mm or 1.0 mm mold cap.*
3. *Carrier tape material: black conductive polystyrene*
4. *Cover tape material: transparent conductive PSA*
5. *Cover tape size: 21.3 mm width*
6. *All measurements are in millimeters*

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Figure 37. SKY65146-21 28-Pin MCM Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Kit Part Number
SKY65146-21 WLAN Power Amplifier	SKY65146-21 (Pb-free package)	TW16-D390