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3rd Generation Traffic Stream Processor – TSP3

M27481

Programmable Traffic Management and Protocol Interworking Processor for Access Applications

High performance network processing optimized for access & enterprise applications

The M27481 is built on the third generation traffic stream processor architecture (TSP3) and is targeted for access and enterprise applications requiring programmable traffic management and Layer 2 interworking functions. Layer 2 interworking functions include, but are not limited to, Ethernet-to-ATM bridging, IP-to-ATM, cell and packet switching, and AAL2.

Device highlights include integrated "universal-link" and Ethernet interfaces, internal SRAM for low latency context storage, hierarchical traffic management & multicast support and a Layer 2, 3 & 4 aware multi-protocol flow classification engine. The M27481 system dissipates no more than 6.25 W of power (including external SDRAM). The M27481 TSP3 architecture provides the foundation for unprecedented performance-to-price network processing while satisfying the system cost and power sensitivity associated with next-generation access and enterprise equipment.

The M27481 programmability can be leveraged to support a broad set of applications that allows a common hardware design to be used interchangeably for edge aggregation applications (e.g. fast/gigabit Ethernet, xDSL, PON, voice, IMA). M27481 can also be used to simplify intrasystem connectivity, providing an aggregation method for a large number of low speed PHY's while supporting proprietary data formats and headers over a variety of electrical interfaces. Devices within the TSP3 family are all software compatible promoting design reuse across applications, port speeds (from NxT1/E1 to 2.5 Gbps) and vendor platforms.

The M27481 device supports fine-grained hierarchical packet and cell traffic management and protocol interworking for over 2 Gbps/2.5 Mpps total throughput on up to 1,280 traffic streams. For larger numbers of streams, up to 64K, the device supports over 625 Mpbs/750Kpps total throughput. In order to shorten product development, Mindspeed Technologies™ offers a system-tested software suite, including PortMakerIII and BroadbandMaker applications. Development tools, source code licenses and consulting services are also available.

KEY FEATURES

- Optimized for access and enterprise applications
- Software-compatible with entire family of TSP3 devices
- Over 2 Gbps total throughput using internal SRAM for up to 1,280 connections; supports a maximum of 64K streams
- Fine-grained packet and cell traffic management supporting Ethernet VLAN 802.1p/q, IP DiffServ, TM 4.1 and DSL Forum TR-059 QoS
  - Queuing, hierarchical shaping & scheduling, policing, and congestion management
- Supported services include but are not limited to – Ethernet-to-ATM, IP-to-ATM, AAL2 SAR & CPS packet switching, cell and packet switching, PWE3 transport of Layer2 frames over MPLS, Frame Relay-to-ATM, GFP
- Multiple services can be combined to run simultaneously
  - any service, any port
- Broad suite of software, source code licenses, EVM, toolset, and consulting services available
- Layer 2, 3 & 4 aware flow classifications
- Supports 64 independent multi-rate PHY's

connections	*processing throughput*
up to 1,280	2+ Gbps, 2.5+ Mpps
1,281 to 64K	625+ Mpbs/750+Kpps

Flexible Communications Processing Power

The foundation of the M27481 TSP3 architecture is based on a single programmable Octave™ microprocessor core with several hardware co-processing engines controlled by software. This provides a powerful architectural advantage by combining the distinct benefits associated with both software-based (programmability) and fixed-function (wire-speed) devices.

The Octave processor is a 32-bit RISC engine, optimized to meet the demands of traffic stream processing. The processor is tightly coupled to surrounding hardware and the data path through register and instruction sets providing efficient dispatching of parallel hardware operations while performing traffic stream processing functions. The Octave processor extends the familiar RISC instruction set with specialized instructions for interworking and traffic management. The architecture is equally adept at handling packets and cells and can be used for processing single-service or multiple service applications concurrently.

Hardware Accelerated Architecture

Multiple hardware engines are integrated on-chip with a single Octave processor to achieve high performance network processing. The input data path streams into the M27481 through "universal-link" receive ports, Ethernet, and/or PCI-mapped FIFOs. Data path and host configurations are highly flexible. The multi-protocol channel descriptor look-up engine (CDL) classifies and maps each traffic stream to an Octave software process by examining header fields and converting the traffic stream into an internal data format. Example classifications performed by the CDL include Ethernet MAC, stacked VLAN tags, ATM VCI/VPI, MPLS EXP and IP (Layer 3 & 4 – such as DHCP snooping, UDP, DSCP, etc.).

All traffic streams flow throughout the context cache and data RAM (CCR). The Octave processor has very low-latency access to this memory and it is here that internetworking functions can inspect and modify the traffic stream. Per-stream context, or state, is pre-fetched and loaded into CCR enabling single-cycle context switching to the next event by the Octave processor. The Octave processor uses the integrated buffer-management engine (BME) to efficiently manage memory allocation.

The M27481 provides three external memory interfaces: one for low-cost DDR SDRAM, an I^2C interface for a boot EEPROM, and a glueless interface to an optional external CAM for extending the device's classification capabilities. The SDRAM provides buffer storage as well as channel context storage. However, for applications using up to 1280 channels, an internal channel context SRAM is provided to boost application performance by over 3x for up to 1,280 conections. Five independent DMA engines work concurrently to sustain high throughput of stream data and context through an internal high-speed crossbar memory controller. The device feeds each output port with a prioritized, wire-speed stream of data. Up to 64 multi-rate PHY's can be supported without head-of-line-blocking. The M27481's traffic scheduling system (TSS) makes bandwidth reservations and resolves scheduling conflicts based on per-stream as well as network path and tunnel parameters. It may also be used as a system resource for setting-up complex event timers. Along with the Octave processor, the TSS can be used to develop unique customizable scheduling algorithms and hierarchical shaping & scheduling schemes.

Development Tools

Mindspeed supplies an evaluation board, host driver code and extensive system development tools supporting customers using either production binary firmware products, such as PortMakerIII-AAL5™, or foundation source firmware products, such as BroadbandMaker™. The TSP3 board development kit (BDK) provides a chip model, test bench, and diagnostic code for hardware design verifications. The software development kit (SDK) is a powerful development environment for customers modifying TSP3 source code products or developing custom applications. Mindspeed consulting services are also available to design, implement, and/or test custom features or stand-alone applications.

Applications

The M27481 TSP3 fits within a variety of system architectures spanning many equipment categories including access aggregation (DSLAM, CMTS, FTTx, NG DLC), voice and wireless gateways, fixed and mobile wireless equipment, routers (enterprise and edge), multi-service switches, and Ethernet switches. The support of proprietary data formats and headers simplifies hardware development and reduces cost by absorbing peripheral FPGA devices. This device can also be used as a backplane or control plane SAR.

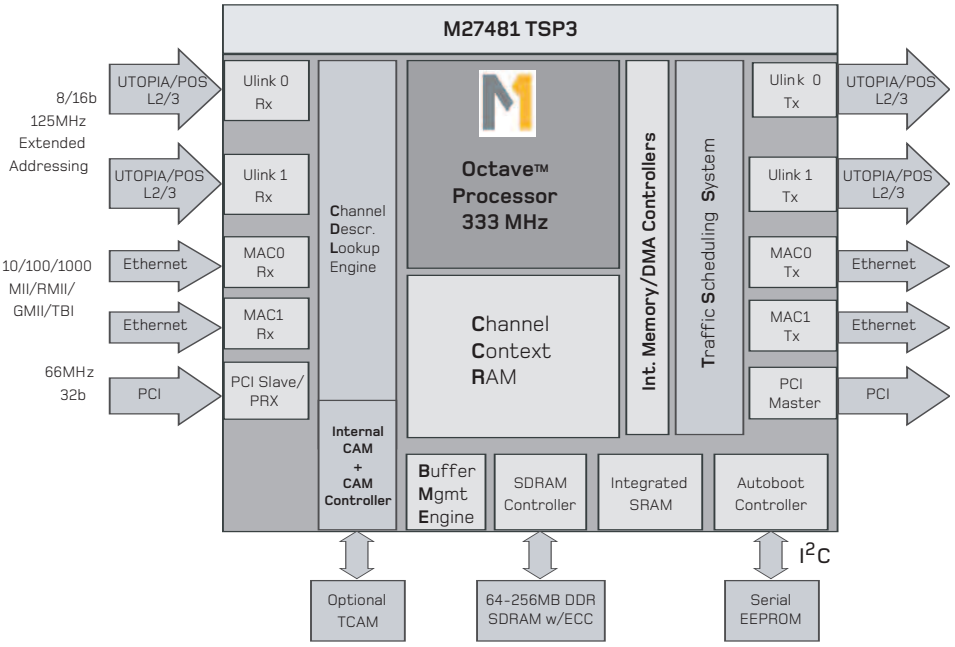

Figure 1: M27481 TSP3 Architecture

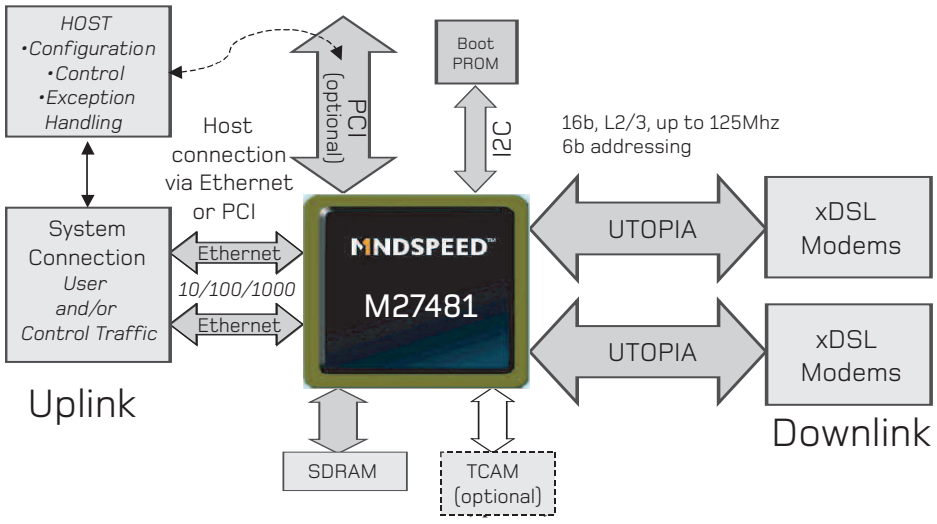

Figure 2: Typical Application: IP-DSLAM

Product Features

Physical Interfaces:

- Two bi-directional "universal link" data-path interfaces – each configurable as:
  - POS-PHY & UTOPIA Level 2, configurable for 8/16-bit modes, up to 125 MHz
  - 64 independent egress FIFO's
  - Two integrated Ethernet MACs (MII, RMII, GMII, TBI)
- DDR SDRAM interface
  - 2.6 GB sustained bandwidth, 64 to 256 MB of 64-bit, up to 166 MHz, 2.5V, with ECC
- Optional glueless interface to external CAM
  - Supporting > 100M searches per second
  - Up to 64K table entries
- PCI interface for data & control plane
  - Rev 2.1-2.3 compliant, 32-bit, up to 66 MHz, 3.3 V
- I^2C interface for boot EEPROM

Hardware Internals:

Processing Core:

- Single Octave microprocessor core – includes:
  - 32-bit RISC engine, core frequency of 333 MHz, 4 stage pipeline, single cycle instruction execution, 16 K instruction cache, 64 general purpose, 32-bit registers addressable by all instructions

Hardware Co-processing Engines:

- Channel Descriptor Lookup Engine (CDL)
  - Per flow multi-protocol classification using internal TCAM, suitable for ATM, MPLS, IP Diffserv, Ethernet, stacked VLAN tagged Ethernet frames, etc.
- Context Cache and Data RAM (CCR)
  - On-chip work area and staging area for all command and data processing events, posting and prioritization of events for the Octave processor, contains the DMA engines for moving data to and from memory and egress
- Traffic Scheduling System (TSS)
  - Performs rate shaping and scheduling for all ingress and egress traffic, 64 slot, calendar based scheduler with dual GCRA conforming shaping per connection, configurable scoreboards supporting up to 64 K packet or cell streams on up to 64 ports, non-blocking, traffic shaping of packets and cells from 64 Kbps to over 2 Gbps speeds, within 1% accuracy, token bucket port rate shaping by backpressure or internal clock
- Buffer Management Engine (BME)
  - Support for up to 8 buffer classes, dedicated to managing the free buffer memory pools

Device Physicals:

- Voltage levels: 1.2 V, 2.5 V, 3.3 V – Package: 1156 PBGA, 35mm x 35mm –Power: 5.5W maximum – operation temperature: –40°C to +85°C

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