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TSP3 Traffic Stream Processor

M27483

2.5 Gbps Programmable Traffic Management and Layer 2 Interworking Processor

The M27483 is based on a third-generation traffic stream processor architecture (TSP3) and is targeted for a variety of programmable traffic management and Layer 2 interworking functions. Unlike fixed-function traffic management devices, new features can be introduced with a software upgrade making M27483 TSP3-based hardware deployed in networks "future-proof" to evolving requirements.

The M27483 device supports a broad set of applications that allows "common card" hardware to be used interchangeably for ATM, POS, Ethernet, EoS, next-generation SONET, IMA and Frame Relay designs. In addition, all devices within the TSP3 family are software compatible, promoting design reuse across applications, port speeds and vendor platforms.

The M27483 device supports fine-grained packet and cell traffic management functions such as queuing, hierarchical shaping and scheduling, policing, switching, and congestion management on up to 256K traffic streams at 2.5 Gbps. Layer 2 interworking functions include, but are not limited to, transport of Layer 2 frames over MPLS (draft-ietf-pwe3), IP-to-ATM (AAL2, AAL5 SARing), Ethernet to ATM (RFC2684), Frame Relay-to-ATM (frf.5/.8) and IMA.

To shorten time-to-market, Mindspeed will provide a suite of production quality, tested PortMaker®III applications including AAL5 with ATM-to-MPLS interworking, packet traffic management (PTM), cell traffic management (CTM) and Ethernet-to-ATM bridging software. Source code licenses and consulting services are also available. Additional PortMakerIII applications are under development.

Flexible Communications Processing Power

The foundation of the M27483 TSP3 architecture is based on two programmable Octave™ microprocessor cores tightly coupled with several co-processing engines. This provides a powerful architectural advantage by combining the distinct benefits associated with both software-based and configurable devices.

The architecture is equally adept at handling packets and cells at up to 2.5 Gbps port speeds and can be used for processing single-service or multiple service applications concurrently (any service, any port).

KEY FEATURES

- Programmable traffic management and Layer 2 interworking processor
- Software compatible with entire family of TSP3 devices
- Supports up to 256K packet or cell streams at up to 2.5 Gbps
- Supports fine-grained packet and cell traffic management on up to 256K traffic streams
  - Queuing
  - Hierarchical shaping and scheduling
  - Policing
  - Switching
  - Congestion management
- Layer 2 interworking functions include, but are not limited to
  - Transport of Layer 2 frames over MPLS
  - IP-to-ATM (AAL2, AAL5,
  - Ethernet-to-ATM
  - Frame Relay-to-ATM
  - IMA
- Complete off-the-shelf PortMaker®III software applications and source code licenses are available
- EVM, comprehensive toolset, and consulting services

The Octave processors are 32-bit RISC engines, optimized to meet the demands of traffic stream processing. The processors are tightly coupled to surrounding hardware and the data path through register and instruction sets, providing efficient dispatching of parallel hardware operations while performing traffic stream processing functions. The Octave processors extend the familiar RISC instruction set with specialized instructions for interworking and traffic management.

Hardware Accelerated Architecture

Multiple hardware machines are integrated on-chip with two Octave processors to achieve optical wire-speed performance. The input data path streams into the M27483 through its universal receive port or FIFO ports within its PCI address space. The channel descriptor look-up engine (CDL) maps each traffic stream (up to 256K) to an Octave software process by examining header fields and converting the traffic stream into an internal data format.

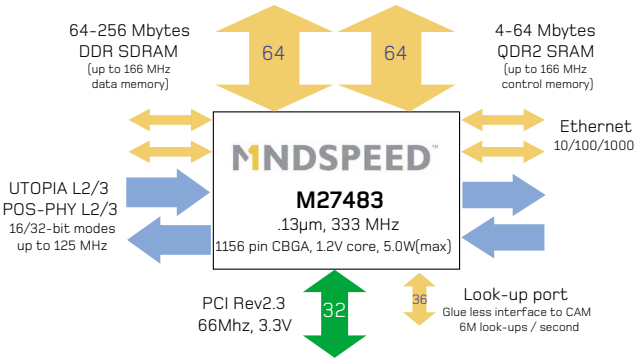

Figure 1: M27483 TSP3 External Interfaces

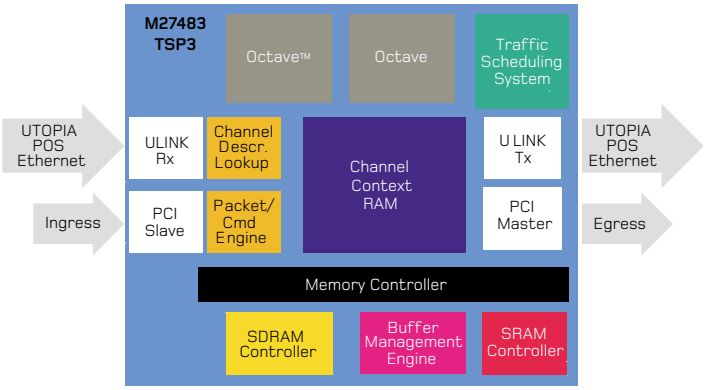

Figure 2: M27483 TSP3 Architecture

All traffic streams flow throughout the context cache and data RAM (CCR). The Octave processors have very low-latency access to this memory and it is here that internetworking functions inspect and modify the traffic stream. Per-stream context, or state, also resides in this memory as the stream is processed.

If the application requires queuing, the Octave processors use the buffer-management engine to manage memory allocation. The M27483 supports three memory interfaces: one for low-cost DDR SDRAM, another for low-latency QDR2 SRAM and an optional glueless interface to an external CAM for extending the device's classification capabilities. Five independent DMA engines work concurrently to sustain high throughput of stream data and context through an internal high-speed crossbar memory controller. The device feeds each output port with a prioritized, wire-speed stream of data. The M27483's traffic scheduling system (TSS) makes bandwidth reservations and resolves scheduling conflicts based on per-stream as well as network path and tunnel parameters.

Development Tools

Mindspeed supplies a PCI-based evaluation board, PortBuilder™III host driver and extensive system development tools with both the binary and source-code versions of PortMakerIII. The TSP3 board development kit (BDK) provides a chip model, test bench, and diagnostic code for hardware design verifications. The software development kit (SDK) is a powerful development environment for customers modifying PortMakerIII source code or developing custom applications. Mindspeed consulting services are also available.

Applications

The M27483 TSP3 fits within a variety of system architectures spanning many equipment categories including routers (edge and core), multi-service switches, Ethernet switches, edge aggregation (xDSL, cable head-ends, xPON, next-generation DLC), voice and wireless gateways and fixed and mobile wireless equipment. This device can also be used as a backplane SAR.

Product Features

Physical Interfaces

- Two bi-directional "Universal Link" datapath interfaces – each configurable as:
  - POS-PHY Level 3, Level 2, configurable for 8/16/32-bit modes, up to 125 MHz
  - UTOPIA Level 3, Level 2, configurable for 8/16/32-bit modes, up to 125 MHz
  - Four integrated Ethernet MACs
  - 64 independent egress FIFO's
- DDR SDRAM interface for packet buffering
  - 4 GB sustained bandwidth, 64 to 256 MB of 64-bit, up to 166 MHz, 2.5V, with ECC
- QDR2 SRAM for context storage
  - 10.6 GB peak bandwidth, 4 to 64 MB of 64-bit, up to 166 MHz, 1.8V, parity and ECC
- Optional glueless interface to external CAM
  - Supporting 6 million look-ups per second
  - Up to 256K table entries
- PCI interface for control plane
  - Rev 2.1-2.3 compliant, 32-bit, up to 66 MHz, 3.3V

Hardware Internals Processing Cores

- Dual Octave™ microprocessor cores – each includes:
  - 32-bit RISC engines, core frequency of 333 MHz, 4 stage pipeline, single cycle instruction execution, 16K instruction cache, 64 general purpose, 32-bit registers addressable by all instructions

Hardware Co-processing Engines

- Channel Descriptor Lookup Engine (CDL)
  - Per flow identification using TCAM, 16-byte reduction for ATM, MPLS, Diffserv, Ethernet, VLAN tagged Ethernet frames, optional use of external CAM for up to 256K table entries
- Context Cache and Data RAM (CCR)
  - On-chip work area and staging area for all command and data processing events, posting and prioritization of events for both Octave processors, contains the DMA engines for moving data to and from memory and egress ports
- Traffic Scheduling System (TSS)
  - Performs rate shaping and scheduling for all ingress and egress traffic, 128 slot, calendar based scheduler with dual GCRA conforming shaping per connection, configurable scoreboards supporting up to 256K packet or cell streams on up to 128 ports, non-blocking, traffic shaping of packets and cells from 64 Kbps to 2.5 Gbps speeds, within 1 percent accuracy, per-PHY token bucket rate shapers when PHY backpressure is not available
- Buffer Management Engine (BME)
  - Support for up to 16 buffer classes, dedicated to managing the free buffer memory pools

Device Physicals

Voltage levels: 1.2V, 1.8V, 2.5V, 3.3V – Package: 1156 CBGA, 35mm x 35mm – Power: 5.0W maximum – operation temperature: –40°C to +85°C

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