



A3L:70TT.XXI

VOLTAGE RATINGS

Part Number	V_{RRM} , V_R (V)		V_{RSM} , V_R (V) Max. non-rep. peak reverse voltage
	Max. rep. peak reverse voltage		
	$T_J = 0$ to 125°C	$T_J = -40$ to 0°C	$T_J = 25$ to 125°C
A3L:70TT.02I	200	200	300
A3L:70TT.04I	400	400	500
A3L:70TT.06I	600	600	700
A3L:70TT.08I	800	800	900
A3L:70TT.10I	1000	1000	1100
A3L:70TT.12I	1200	1200	1300
A3L:70TT.14I	1400	1330	1500
A3L:70TT.16I	1600	1520	1700

MAXIMUM ALLOWABLE RATINGS

PARAMETER	VALUE	UNITS	NOTES
T_J Junction Temperature	-40 to 125	$^\circ\text{C}$	-
T_{stg} Storage Temperature	-40 to 150	$^\circ\text{C}$	-
$I_{F(AV)}$ Max. Av. current	70	A	180° half sine wave
	@ Max. T_C	85	
$I_{F(RMS)}$ Nom. RMS current	155	A	-
I_{FSM} Max. Peak non-rep. surge current	1.4	kA	50 Hz half cycle sine wave Initial $T_J = 125^\circ\text{C}$, rated V_{RRM} applied after surge.
	1.53		60 Hz half cycle sine wave
	1.6		50 Hz half cycle sine wave Initial $T_J = 125^\circ\text{C}$, no voltage applied after surge.
	1.74		60 Hz half cycle sine wave
I^2t Max. I^2t capability	10.11	kA^2s	$t = 10\text{ms}$ Initial $T_J = 125^\circ\text{C}$, rated V_{RRM} applied after surge.
	11.02		$t = 8.3\text{ms}$
	11.52		$t = 10\text{ms}$ Initial $T_J = 125^\circ\text{C}$, no voltage applied after surge.
	12.56		$t = 8.3\text{ms}$
$I^2t^{1/2}$ Max. $I^2t^{1/2}$ capability	138.6	$\text{kA}^2\text{s}^{1/2}$	Initial $T_J = 125^\circ\text{C}$, no voltage applied after surge. I^2t for time $t_x = I^2t^{1/2} * t_x^{1/2}$. (0.1 < t_x < 10ms).
di/dt Max. Non-repetitive rate-of-rise current	150	A/ μs	$T_J = 125^\circ\text{C}$, $V_D = V_{DRM}$, $I_{TM} = 1600\text{A}$. Gate pulse: 20V, 20 Ω , 10 μs , 0.5 μs rise time, Max. repetitive di/dt is approximately 40% of non-repetitive value.
P_{GM} Max. Peak gate power	12	W	$t_p < 5\text{ms}$
$P_{G(AV)}$ Max. Av. gate power	3	W	-
$+I_{GM}$ Max. Peak gate current	150	mA	$t_p < 5\text{ms}$
$-V_{GM}$ Max. Peak negative gate voltage	2	V	-
F Mounting Force	3(5)	N.m	Upper connectors(Heatsink)



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CHARACTERISTICS

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{TM} peak on-state voltage	---	---	1.63	V	Initial $T_J = 25^\circ\text{C}$, 50-60Hz half sine, $I_{peak} = 220\text{A}$.
$V_{T(TO)}$ Threshold voltage	---	---	1	V	$T_J = 125^\circ\text{C}$ Av. power = $V_{T(TO)} * I_{T(AV)} + r_T * [I_{T(RMS)}]^2$, 180 Half Sine.
r_T Slope resistance	---	---	2.73	m Ω	Use low values for $I_{TM} < \pi$ rated $I_{T(AV)}$
I_L Latching current	---	---	400	mA	$T_C = 125^\circ\text{C}$, 12V anode. Gate pulse: 10V, 20 Ω , 100 μs .
I_H Holding current	---	---	200	mA	$T_C = 25^\circ\text{C}$, 12V anode. Initial $I_T = 15\text{A}$.
t_d Delay time	---	0.7	1.5	μs	$T_C = 25^\circ\text{C}$, $V_D = V_{DRM}$, 50A resistive load. Gate pulse: 10V, 20 Ω , 10 μs , 1 μs rise time.
t_q Turn-off time	---	125	200	μs	$T_J = 125^\circ\text{C}$, $I_{TM} = 500\text{A}$, $di/dt = 25\text{A}/\mu\text{s}$, $V_R = 50\text{V}$. $dv/dt = 20\text{V}/\mu\text{s}$ lin. to rated V_{DRM} . Gate: 0V, 100 Ω .
dv/dt Critical rate-of-rise of off-state voltage	80	140	---	V/ μs	$T_J = 125^\circ\text{C}$. Exp. to 100% or lin. Higher dv/dt values available. To 80% V_{DRM} , gate open.
I_{RM} , I_{DM} Peak reverse and off-state current	---	10	20	mA	$T_J = 125^\circ\text{C}$, Rated V_{RRM} and V_{DRM} , gate open.
I_{GT} DC gate current to trigger	---	---	300	mA	$T_C = -40^\circ\text{C}$
V_{GT} DC gate voltage to trigger	4	---	---	V	$T_C = 25^\circ\text{C}$ +12V anode-to-cathode. For recommended gate drive see "Gate Characteristics" figure.
V_{GD} DC gate voltage not to trigger	---	---	0.25	V	$T_C = 25^\circ\text{C}$, Max. Value which will not trigger with rated V_{DRM} anode.
R_{thJC} Thermal resistance, junction-to-case	---	---	0.19	$^\circ\text{C}/\text{W}$	DC operation, single side cooled.
	---	---	0.194	$^\circ\text{C}/\text{W}$	180 sine wave, single side cooled.
	---	---	0.207	$^\circ\text{C}/\text{W}$	120 rectangular wave, single side cooled.
R_{thCS} Thermal resistance, case-to-sink	---	---	0.1	$^\circ\text{C}/\text{W}$	Mtg. Surface smooth, flat and greased. Single side cooled.
wt Weight	---	110(4)	---	g(oz.)	---
Case Style	TO-240AA		JEDEC	---	---

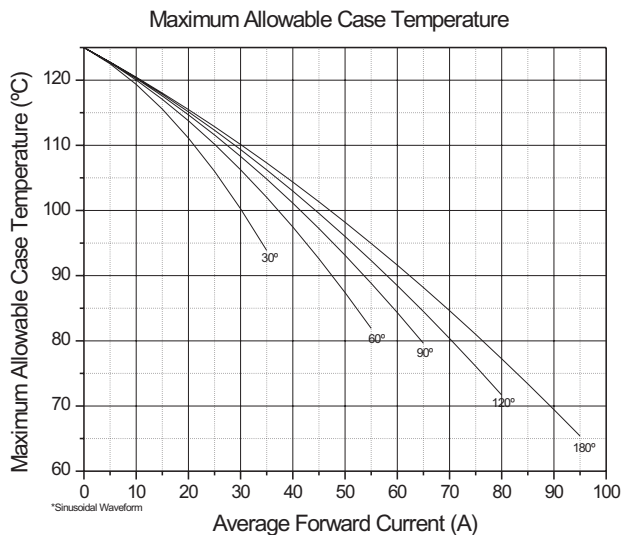


Fig. 1 - Current Ratings Characteristics

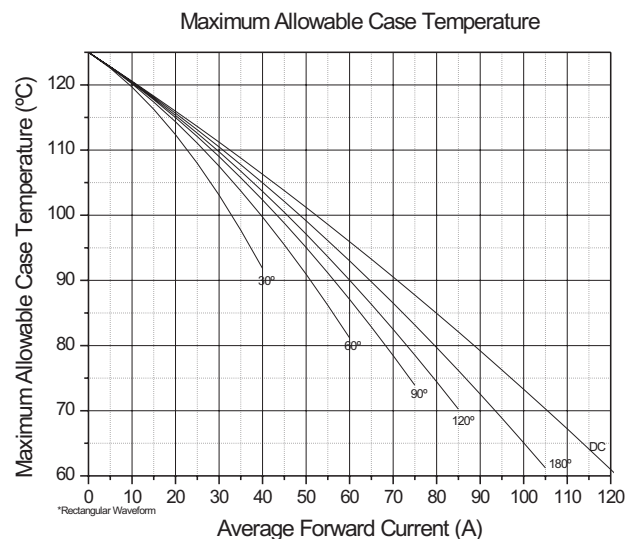


Fig. 2 - Current Ratings Characteristics



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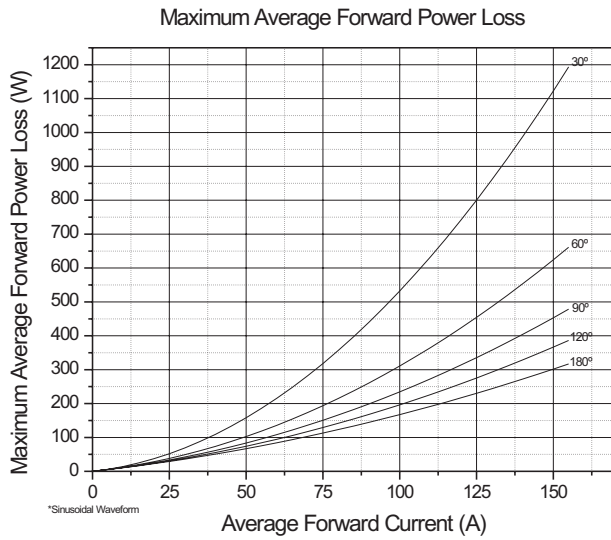


Fig.3 -Forward Power Loss Characteristics

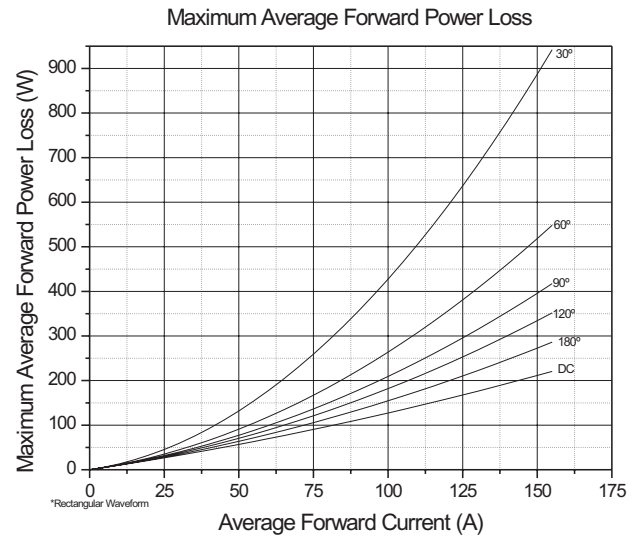


Fig. 4 - Forward Power Loss Characteristics

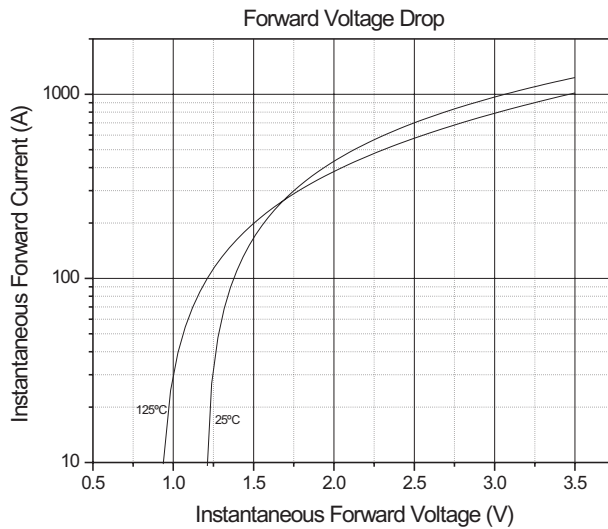


Fig. 5 - Forward Voltage Drop Characteristics

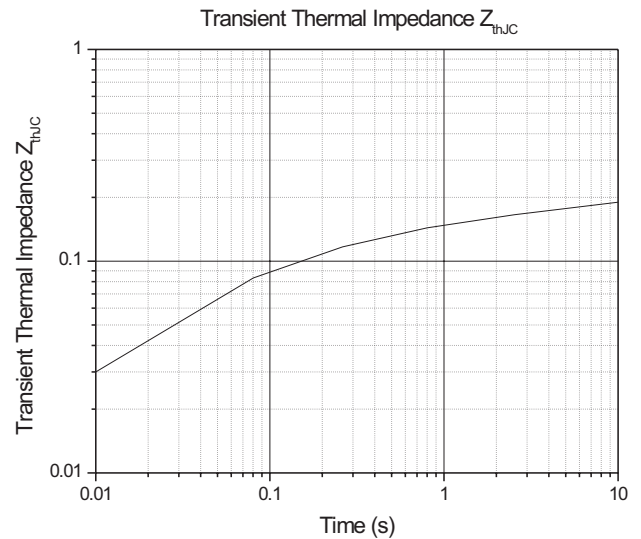


Fig. 6 - Transient Thermal Impedance



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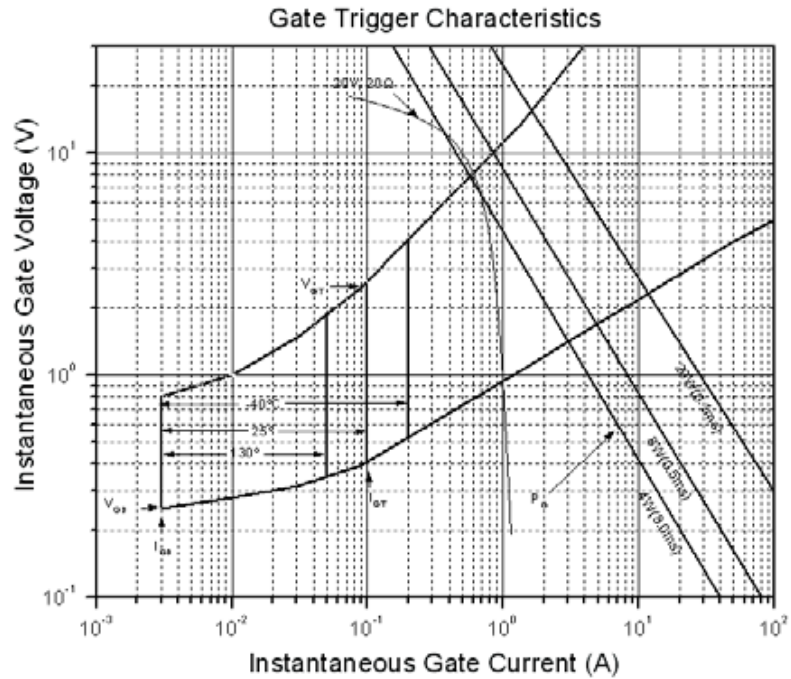


Fig. 7 - Gate Trigger Characteristics

TO-240AA

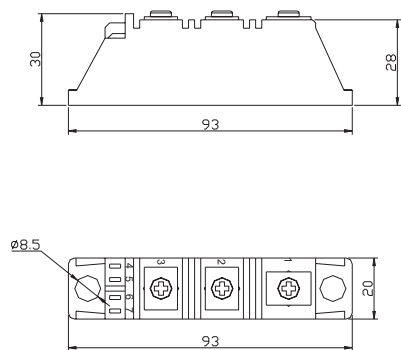


Fig. 8 - Outline Characteristics

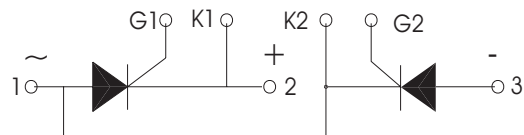


Fig. 9 - Circuit Layout