M36P0R9060N0

512 Mbit (x16, Multiple Bank, Multi-Level, Burst) Flash memory 64 Mbit (Burst) PSRAM, 1.8V supply, Mux I/O, Multi-Chip Package

Preliminary Data

Feature summary

- Multi-Chip Package
  - 1 die of 512 Mbit (32Mb x 16, Multiple Bank, Multi-Level, Burst) Flash memory
  - 1 die of 64 Mbit (4Mb x16) PSRAM
- Supply voltage
  - $V_{DDF} = V_{CCP} = V_{DDQ} = 1.7$ to 1.95V
  - $V_{PPF} = 9V$ for fast program
- Electronic signature
  - Manufacturer Code: 20h
  - Device Code: 8833
- ECOPACK® package

Flash memory

- Multiplexed Address/Data
- Synchronous / Asynchronous Read
  - Synchronous Burst Read mode: 108MHz, 66MHz
  - Asynchronous Page Read mode
  - Random Access: 96ns
- Programming time
  - 4.2μs typical Word program time using Buffer Enhanced Factory Program command
- Memory organization
  - Multiple Bank Memory Array: 64 Mbit Banks
  - Four Extended Flash Array (EFA) Blocks of 64 Kbits
- Dual operations
  - program/erase in one Bank while read in others
  - No delay between read and write operations
- Security
  - 64 bit unique device number
  - 2112 bit user programmable OTP Cells

TFBGA107 (ZAN)
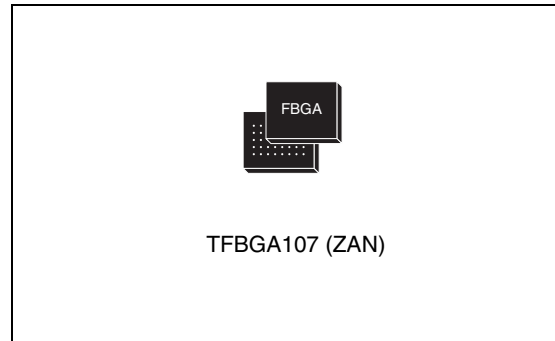
- 100,000 Program/erase cycles per block
- Block locking
  - All Blocks locked at power-up
  - Any combination of Blocks can be locked with zero latency
  - $\overline{WP}_F$ for Block Lock-Down
  - Absolute Write Protection with $V_{PPF} = V_{SS}$
- Common Flash Interface (CFI)

PSRAM

- Multiplexed Address/Data bus
- Asynchronous operating modes
  - Random Read: 70ns access time
  - Asynchronous Write
- Synchronous modes
  - Synchronous Read: Fixed length (4-, 8-, 16-, and 32-Word) or continuous burst
  - Clock Frequency: 83MHz (max)
  - Synchronous Write: continuous burst
- Low-power features
  - Partial Array Self-Refresh (PASR)
  - Deep Power-Down (DPD) mode
  - Automatic Temperature-compensated Self-Refresh

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This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1   Summary description

The M36P0R9060N0 combines two memory devices in a Multi-Chip Package:

●   512-Mbit Multiple Bank Flash memory (the M58PR512JN)

●   64-Mbit PSRAM (the M69KM096AA).

The purpose of this document is to describe how the two memory components operate with respect to each other. It must be read in conjunction with the M58PRxxxJN and M69KM096AA datasheets, where all specifications required to operate the Flash memory and PSRAM components are fully detailed.

Recommended operating conditions do not allow more than one memory to be active at the same time.

The memory is offered in a Stacked TFBGA107 package. It is supplied with all the bits erased (set to '1').
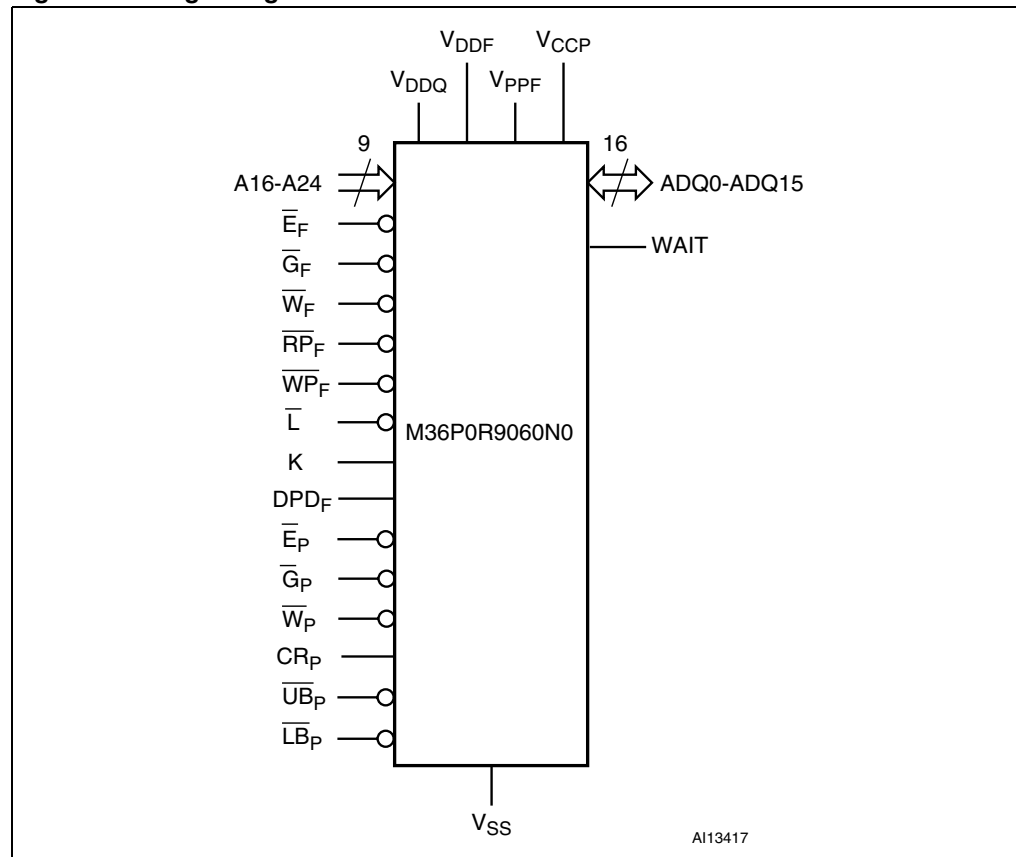
Figure 1.   **Logic diagram**

Table 1.   Signal names

A16-A24[1]	Address Inputs
ADQ0-ADQ15	Common Data Inputs/Outputs or Address inputs, Command inputs
V_{DDQ}	Common Flash and PSRAM Power Supply for I/O Buffers
V_{PPF}	Flash Memory Optional Supply Voltage for Fast Program & Erase
V_{DDF}	Flash Memory Power Supply
V_{CCP}	PSRAM Power Supply
V_{SS}	Ground
$\overline{L}$	Latch Enable input
K	Burst Clock
WAIT	Wait Output
NC	Not Connected Internally
DU	Do Not Use as Internally Connected
Flash Memory	
$\overline{E}_F$	Chip Enable input
$\overline{G}_F$	Output Enable Input
$\overline{W}_F$	Write Enable input
$\overline{RP}_F$	Reset input
$\overline{WP}_F$	Write Protect input
DPD_F	Deep Power-Down
PSRAM	
$\overline{E}_P$	Chip Enable Input
$\overline{G}_P$	Output Enable Input
$\overline{W}_P$	Write Enable Input
CR_P	Configuration Register Enable Input
$\overline{UB}_P$	Upper Byte Enable Input
$\overline{LB}_P$	Lower Byte Enable Input

1. A22-A24 are Address Inputs for the Flash memory component only.

Figure 2.   TFBGA connections (top view through package)

	1	2	3	4	5	6	7	8	9
A	●	DU	NC	NC	NC	V_{CCP}	DPD_F	V_{SS}	DU
B	DU	NC	A18	A19	V_{SS}	V_{DDF}	NC	A21	NC
C	NC	NC	$\overline{LB}_P$	A23	V_{SS}	NC	K	A22	NC
D	V_{SS}	NC	A17	A24	V_{PPF}	$\overline{W}_P$	$\overline{E}_P$	NC	NC
E	V_{SS}	NC	NC	NC	$\overline{WP}_F$	$\overline{L}$	A20	NC	NC
F	NC	NC	NC	$\overline{UB}_P$	$\overline{RP}_F$	$\overline{W}_F$	NC	NC	A16
G	V_{DDQ}	NC	ADQ8	ADQ2	ADQ10	ADQ5	ADQ13	WAIT	NC
H	V_{SS}	$\overline{G}_P$	ADQ0	ADQ1	ADQ3	ADQ12	ADQ14	ADQ7	NC
J	DU	NC	$\overline{G}_F$	ADQ9	ADQ11	ADQ4	ADQ6	ADQ15	V_{DDQ}
K	NC	$\overline{E}_F$	NC	NC	NC	V_{CCP}	NC	V_{DDQ}	CR_P
L	DU	V_{SS}	V_{SS}	V_{DDQ}	V_{DDF}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
M	DU	NC	DU	DU	DU	DU	DU	DU	DU

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2 Signal descriptions

See *Figure 1., Logic diagram* and *Table 1., Signal names*, for a brief overview of the signals connected to this device.

2.1 Address Inputs (ADQ0-ADQ15 and A16-A24)

Addresses A0-A21 are common inputs for the Flash memory and PSRAM components. Addresses A22 and A24 are inputs for the Flash memory component only.
The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the Program/Erase Controller.

2.2 Data Input/Output (ADQ0-ADQ15)

The Data I/O output the data stored at the selected address during a Bus Read operation or input a command or the data to be programmed during a Bus Write operation.

2.3 Latch Enable ($\overline{L}$)

The Latch Enable pin is common to the Flash memory and PSRAM components.

For details of how the Latch Enable signal behaves, please refer to the datasheets of the respective memory components: M69KM096AA for the PSRAM and M58PRxxxJN for the Flash memory.

2.4 Clock (K)

The Clock input pin is common to the Flash memory and PSRAM components.

For details of how the Clock signal behaves, please refer to the datasheets of the respective memory components: M69KM096AA for the PSRAM and M58PRxxxJN for the Flash memory.

2.5   Wait (WAIT)

WAIT is an output pin common to the Flash memory and PSRAM components. However the WAIT signal does not behave in the same way for the PSRAM and the Flash memory.

For details of how it behaves, please refer to the M69KM096AA datasheet for the PSRAM and to the M58PRxxxJN datasheet for the Flash memory.

2.6   Flash Chip Enable input ($\overline{E}_F$)

The Chip Enable input activates the control logic, input buffers, decoders and sense amplifiers of the Flash memory. When Chip Enable is Low, V_{IL}, and Reset is High, V_{IH}, the device is in active mode. When Chip Enable is at V_{IH} the Flash memory are deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

It is not allowed to have $\overline{E}_F$ at V_{IL} and $\overline{E}_P$ at V_{IL} at the same time. Only one memory component can be enabled at a time.

2.7   Flash Output Enable inputs ($\overline{G}_F$)

The Output Enable input controls the data outputs during Flash memory Bus Read operations.

2.8   Flash Write Enable ($\overline{W}_F$)

The Write Enable input controls the Bus Write operation of the Flash memory Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

2.9   Flash Write Protect ($\overline{WP}_F$)

Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is Low, V_{IL}, Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at High, V_{IH}, Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. (See the Lock Status Table in the M58PRxxxJN datasheet).

2.10   Flash Reset ($\overline{RP}_F$)

The Reset input provides a hardware reset of the Flash memories. When Reset is at V_{IL}, the memory is in Reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I_{DD2}. Refer to the M58PRxxxJN datasheet, for the value of I_{DD2}. After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Exiting Reset mode the device enters Asynchronous Read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to V_{RPH} (refer to the M58PRxxxJN datasheet).

2.11 PSRAM Chip Enable input ($\overline{E}_P$)

The Chip Enable input activates the PSRAM when driven Low (asserted). When deasserted (V_{IH}), the device is disabled, and goes automatically in low-power Standby mode or Deep Power-down mode, according to the RCR (Refresh Configuration Register) setting.

2.12 PSRAM Write Enable ($\overline{W}_P$)

Write Enable, $\overline{W}_P$ controls the Bus Write operation of the PSRAM. When asserted (V_{IL}), the device is in Write mode and Write operations can be performed either to the configuration registers or to the memory array.

2.13 PSRAM Output Enable ($\overline{G}_P$)

When held Low, V_{IL}, the Output Enable, $\overline{G}_P$ enables the Bus Read operations of the PSRAM.

2.14 PSRAM Upper Byte Enable ($\overline{UB}_P$)

The Upper Byte En-able, $\overline{UB}_P$ gates the data on the Upper Byte Data Inputs/Outputs (DQ8-DQ15) to or from the upper part of the selected address during a Write or Read operation.

2.15 PSRAM Lower Byte Enable ($\overline{LB}_P$)

The Lower Byte Enable, $\overline{LB}_P$ gates the data on the Lower Byte Data Inputs/Outputs (DQ0-DQ7) to or from the lower part of the selected address during a Write or Read operation.

If both $\overline{LB}_P$ and $\overline{UB}_P$ are disabled (High), the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as $\overline{E}_P$ remains Low.

2.16 PSRAM Configuration Register Enable (CR_P)

When this signal is driven High, V_{IH}, bus read or write operations access either the value of the Refresh Configuration Register (RCR) or the Bus Configuration Register (BCR) according to the value of A19.

2.17 Deep Power-Down input (DPD$_F$)

The Deep Power-Down input is used to put the device in a Deep Power-Down mode.

When the device is in Standby mode and the Enhanced Configuration Register bit ECR15 is set, asserting the Deep Power-Down input will cause the memory to enter the Deep Power-Down mode.

When the device is in the Deep Power-Down mode, the memory cannot be modified and the data is protected.

The polarity of the DPD pin is determined by ECR14. The Deep Power-Down input is active Low by default.

2.18 V$_{DDF}$ Supply Voltage

V$_{DDF}$ provides the power supply to the internal core of the Flash memory. It is the main power supply for all Flash memory operations (Read, Program and Erase).

2.19 V$_{CCP}$ Supply Voltage

The V$_{CCP}$ Supply Voltage is the core supply voltage.

2.20 V$_{DDQ}$ Supply Voltage

V$_{DDQ}$ provides the power supply for the Flash memory and PSRAM I/O pins. This allows all Outputs to be powered independently of the Flash memory and PSRAM core power supplies, V$_{DDF}$ and V$_{CCP}$

2.21 V$_{PPF}$ Program Supply Voltage

V$_{PPF}$ is both a control input and a power supply pin for the Flash memory. The two functions are selected by the voltage range applied to the pin.

If V$_{PPF}$ is kept in a low voltage range (0V to V$_{DDQ}$) V$_{PPF}$ is seen as a control input. In this case a voltage lower than V$_{PPLK}$ gives an absolute protection against Program or Erase, while V$_{PPF}$ > V$_{PP1}$ enables these functions (see the M58PRxxxJN datasheet for the relevant values). V$_{PPF}$ is only sampled at the beginning of a Program or Erase; a change in its value after the operation has started does not have any effect and Program or Erase operations continue.

If V$_{PPF}$ is in the range of V$_{PPH}$ it acts as a power supply pin. In this condition V$_{PPF}$ must be stable until the Program/Erase algorithm is completed.

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2.22   V$_{SS}$ Ground

V$_{SS}$ is the common ground reference for all voltage measurements in the Flashmemory (core and I/O Buffers) and PSRAM chips. It must be connected to the system ground.

Note: Each Flash memory device in a system should have their supply voltage (V$_{DDF}$) and the program supply voltage V$_{PPF}$ decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See *Figure 5., AC measurement load circuit*. The PCB track widths should be sufficient to carry the required V$_{PPF}$ program and erase currents**.**

3 Functional description

The PSRAM and Flash memory components have separate power supplies but share the same grounds. They are distinguished by two Chip Enable inputs: $\overline{E}_F$ for the Flash memory and $\overline{E}_P$ for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is a simultaneous read operations on the Flash memory and the PSRAM which would result in a data bus contention. Therefore it is recommended to put the other device in the high impedance state when reading the selected device.

Figure 3. Functional block diagram
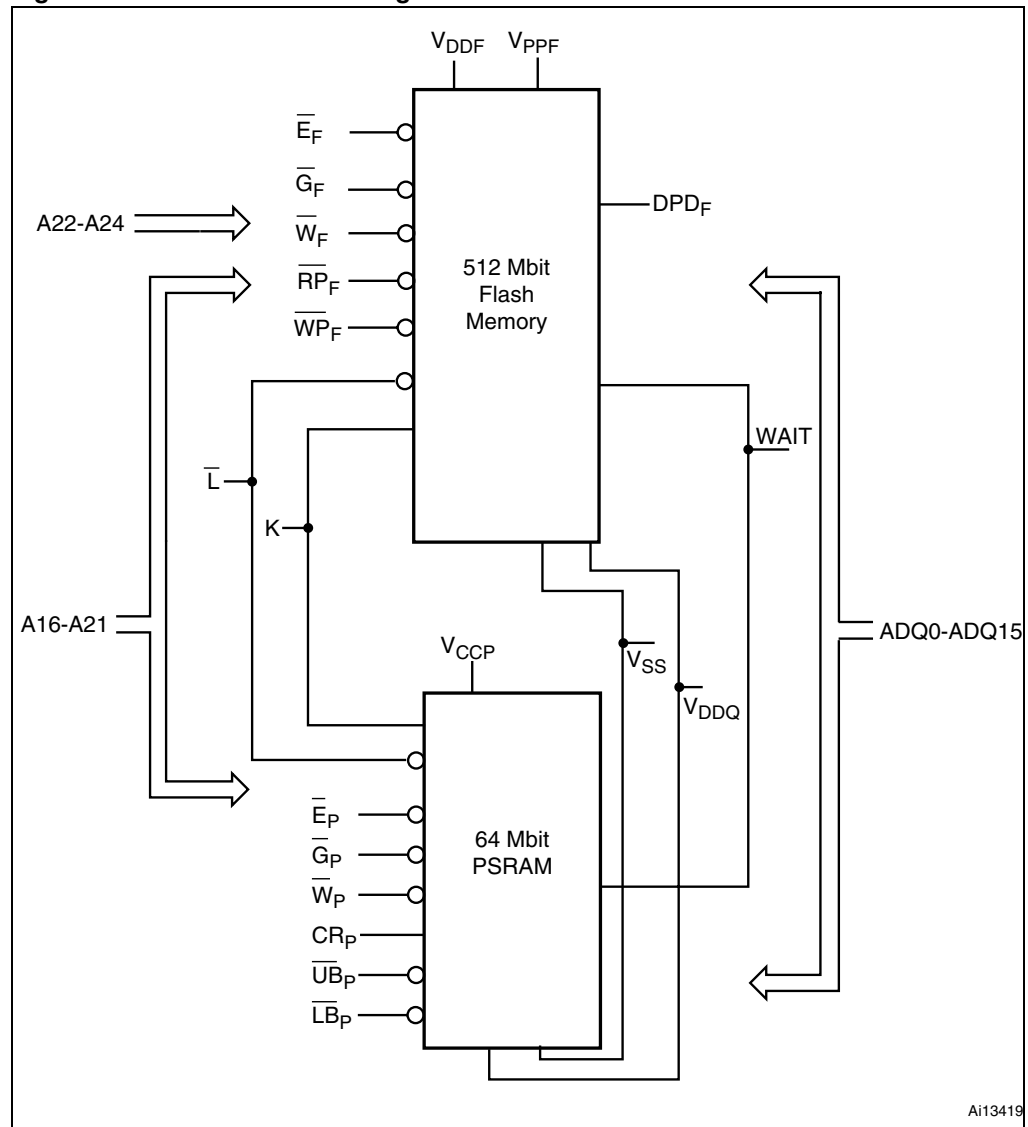
Table 2. Main operating modes[1]

Operation[2]	$\overline{E}_F$	$\overline{G}_F$	$\overline{W}_F$	$\overline{RP}_F$	DPD_F [3]	WAIT[4]	$\overline{L}$	$\overline{E}_P$	$\overline{W}_P$	$\overline{G}_P$	$\overline{UB}_P$ / $\overline{LB}_P$	CR_P	A19	A18	A16, A17, A20, A21	ADQ15-ADQ0
Flash memory — Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	de-a.[5]		V_{IH}	PSRAM must be disabled								Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	de-a.[5]		V_{IH}									Data Input
Address Latch	V_{IL}	V_{IH}	V_{IH}	V_{IH}	de-a.[5]		V_{IL}									Data Output or Hi-Z[6]
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	de-a.[5]	Hi-Z	V_{IH}	Any PSRAM mode is allowed								Hi-Z
Standby	V_{IH}	X	X	V_{IH}	de-a.[5]	Hi-Z	X									Hi-Z
Reset	X	X	X	V_{IL}	de-a.[5]	Hi-Z	X									Hi-Z
Deep Power-Down	V_{IH}	X	X	V_{IH}	asserted[7]	Hi-Z	X									Hi-Z
PSRAM — Read	Flash memory must be disabled						‾_/	V_{IH}	V_{IL}	V_{IL}	V_{IL}		Address In Valid			Address In/ Data Out Valid
Write							‾_/	V_{IL}	V_{IH}	V_{IL}	V_{IL}		Address In Valid			Address In/ Data In Valid
Read CR (CR controlled method)							V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}		00(RCR) 10(BCR) X1(DIDR)		X	Address In/ BCR, RCR or DIDR Content Valid
Output Disable/No Operation	Any Flash memory mode is allowed						X	V_{IH}	X	X	V_{IL}		X	X	X	High-Z
Deep Power-Down[8]								V_{IH}	X	X	X	X	X	X	X	High-Z
Standby								V_{IH}	X	X	X	X	V_{IL}	X	X	High-Z

1. X = Don't care, de-a. = de-asserted, CR = Configuration Register.

2. The Clock signal, K, must remain Low in asynchronous operating mode.

3. The DPD signal polarity depends on the value of the ECR14 bit.

4. WAIT signal polarity is configured using the Set Configuration Register command.

5. If ECR15 is set to '0', the device cannot enter the Deep Power-Down mode, even if DPD is asserted.

6. Depends on $\overline{G}$.

7. ECR15 has to be set to '1' for the device to enter Deep Power-Down.

8. The device enters Deep Power-Down mode by driving the Chip Enable signal, $\overline{E}$, from Low to High, with bit 4 of the RCR set to '0'. The device remains in Deep Power-Down mode until $\overline{E}$ goes Low again and is held Low for $t_{ELEH(DP)}$.

4 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the Numonyx SURE Program and other relevant quality documents.

Table 3.   **Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature	−30	85	°C
T_{BIAS}	Temperature Under Bias	−30	85	°C
T_{STG}	Storage Temperature	−55	125	°C
V_{IO}	Input or Output Voltage	−0.2	2.45	V
V_{DDF}	Flash Memory Supply Voltage	−1.0	3.0	V
V_{CCP}	PSRAM Supply Voltage	−0.2	2.45	V
V_{DDQ}	Input/Output Supply Voltage	−0.2	2.45	V
V_{PPF}	Flash Memory Program Voltage	−1	11.5	V
I_O	Output Short Circuit Current		100	mA
t_{VPPH}	Time for V_{PPF} at V_{PPH}		100	hours

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 4., Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC measurement conditions

Parameter	Flash Memory		PSRAM		Unit
	Min	Max	Min	Max	
V_{DDF} Supply Voltage	1.7	1.95	–	–	V
V_{CCP} Supply Voltage	–	–	1.7	1.95	V
V_{DDQ} Supply Voltage	1.7	1.95	1.7	1.95	V
V_{PPF} Supply Voltage (Factory environment)	8.5	9.5	–	–	V
V_{PPF} Supply Voltage (Application environment)	–0.4	V_{DDQ} +0.4	–	–	V
Ambient Operating Temperature	–30	85	–30	85	°C
Load Capacitance (C_L)	30		30		pF
Impedance Output (Z_0)	50				Ω
Output Circuit Protection Resistance (R)	50				Ω
Input Rise and Fall Times		3		2	ns
Input Pulse Voltages	0 to V_{DDQ}		0 to V_{DDQ}		V
Input and Output Timing Ref. Voltages	V_{DDQ}/2		V_{DDQ}/2		V

Figure 4. AC measurement I/O waveform
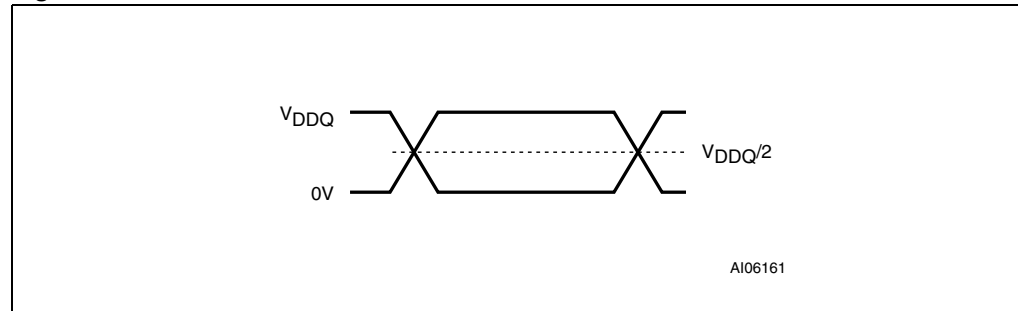
Figure 5. AC measurement load circuit
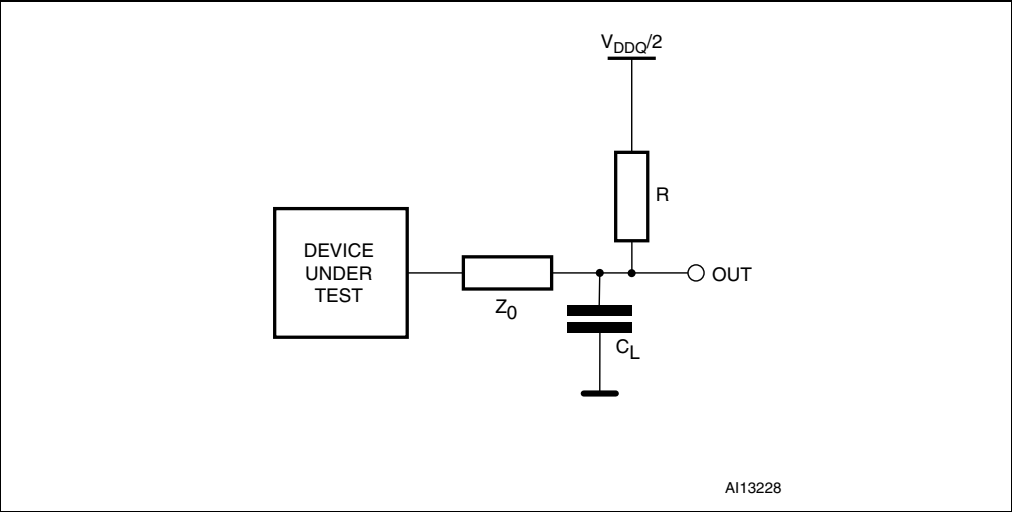
1. V_{DD} means $V_{DDF} = V_{CCP}$.

Table 5. Capacitance[1]

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	–	14	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	–	14	pF

1. Sampled only, not 100% tested.

Please refer to the M58PRxxxJN and M69KM096AA datasheets for further DC and AC characteristics values and illustrations.

6 Package mechanical

In order to meet environmental requirements, Numonyx offers these devices in ECOPACK®
packages. These packages have a Lead-free second level interconnect. The category of
second Level Interconnect is marked on the package and on the inner box label, in
compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 6.   TFBGA 107 8x11mm - 9x12 active ball array, 0.8mm pitch, package outline
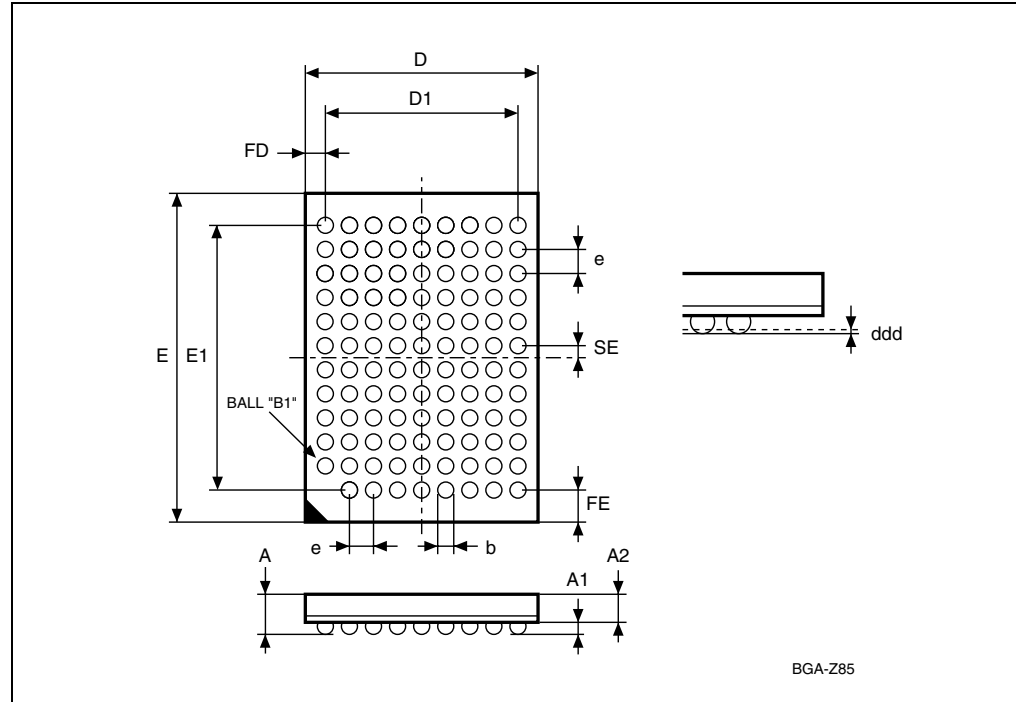
1. Drawing is not to scale.

Table 6.   **Stacked TFBGA107 8x11mm - 9x12 active ball array, 0.8mm pitch, package data**

Symbol	millimeters			inches		
	Typ	**Min**	**Max**	**Typ**	**Min**	**Max**
A			1.20			0.047
A1		0.20			0.008	
A2	0.85			0.033		
b	0.35	0.30	0.40	0.014	0.012	0.016
D	8.00	7.90	8.10	0.315	0.311	0.319
D1	6.40			0.252		
ddd			0.10			0.004
E	11.00	10.90	11.10	0.433	0.429	0.437
E1	8.80			0.346		
e	0.80			0.031		
FD	0.80			0.031		
FE	1.10			0.043		
SE	0.40			0.016		

7 Part numbering

Table 7.   **Ordering information scheme**

Example: M36   P   0   R   9   0   6   0   N   0   ZAC   E

Device Type

M36 = Multi-Chip Package (Flash + PSRAM)

Flash 1 Architecture

P = Multi-Level, Multiple Bank, Large Buffer

Flash 2 Architecture

0 = No Die

Operating Voltage

R = V_{DDF} = V_{CCP} = V_{DDQ} = 1.7 to 1.95V

Flash 1 Density

9 = 512 Mbits

Flash 2 Density

0 = No Die

RAM 1 Density

6 = 64 Mbits

RAM 2 Density

0 = No Die

Parameter Blocks Location

N = Even Block Flash Memory Configuration, Mux I/O

Product Version

0 = 90nm Flash technology, 96ns speed; 0.11µm PSRAM technology, 70ns speed

Package

ZAN = stacked TFBGA107 C stacked footprint.

Option

E = ECOPACK Package, Standard packing

F = ECOPACK Package, Tape & Reel packing

Note: *Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the Numonyx Sales Office nearest to you.*

8 Revision history

Table 8. Document revision history

Date	Revision	Changes
21-Jul-2006	0.1	Initial release.
30-Nov-2007	0.2	Applied Numonyx branding.

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Please Read Carefully: