S71WS-P based MCP Products

1.8 Volt-only x16 Simultaneous Read/Write, Burst Mode Flash Memory with CellularRAM

Data Sheet

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S71WS-P_00 **Revision** A **Amendment** 10 **Issue Date** October 19, 2007

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Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

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Questions regarding these document designations may be directed to your local sales office.

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Data Sheet

Features

- **Power supply voltage of 1.7 to 1.95V**
- **Flash access time: 80 ns, 25 ns**
- **Flash burst frequencies: 66 MHz, 80 MHz, 108 MHz**
- **pSRAM Access time: 70 ns, 20 ns**
- **pSRAM burst frequency: 66 MHz, 80 MHz, 104 MHz**
- **Package:**
  - 8.0 x 11.6 mm MCP
- **Operating Temperature**
  - –25°C to +85°C (wireless)

The S71WS series is a product line of stacked packages and consists of:

- One or two S29WS-P NOR flash memory die
- CellularRAM die

The products covered by this document are listed in the table below.

Device	CellularRAM Density (Mb)	
	64 Mb	128 Mb
S29WS512P	S71WS512PC0	S71WS512PD0
S29WS256P	S71WS256PC0	S71WS256PD0
S29WS128P	S71WS128PC0	

Note:
For a full list of OPNs, please contact the local sales representative or refer to the Ordering Information valid combinations tables.

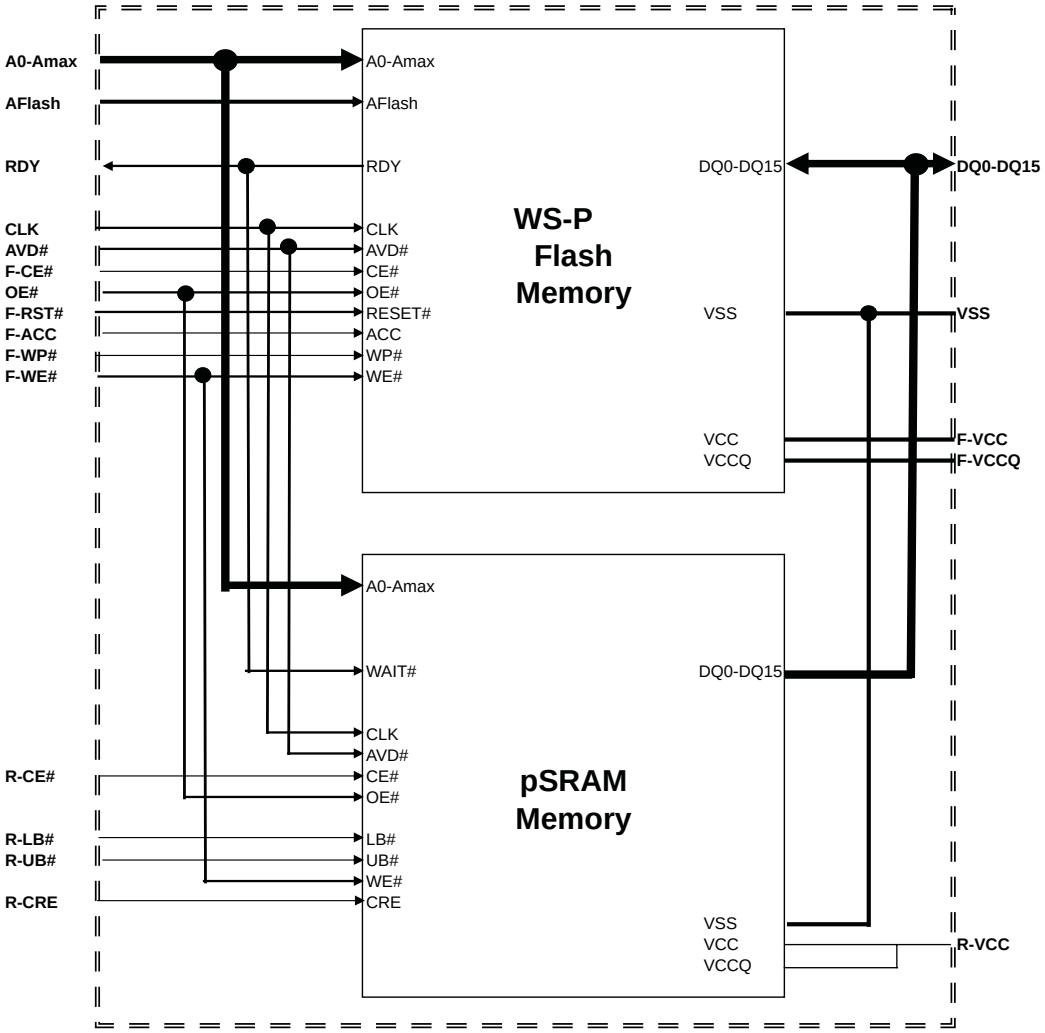
For detailed specifications, please refer to the individual data sheets.

Document	Publication Identification Number (PID)
S29WS-P	S29WS-P_00
128 M CellularRAM Type 2	Cellram_04
128 M/64 M CellularRAM Type 3	Cellram_07
Cellurlar RAM Application Note for Qimonda	cellram_sw_reg_entry_an

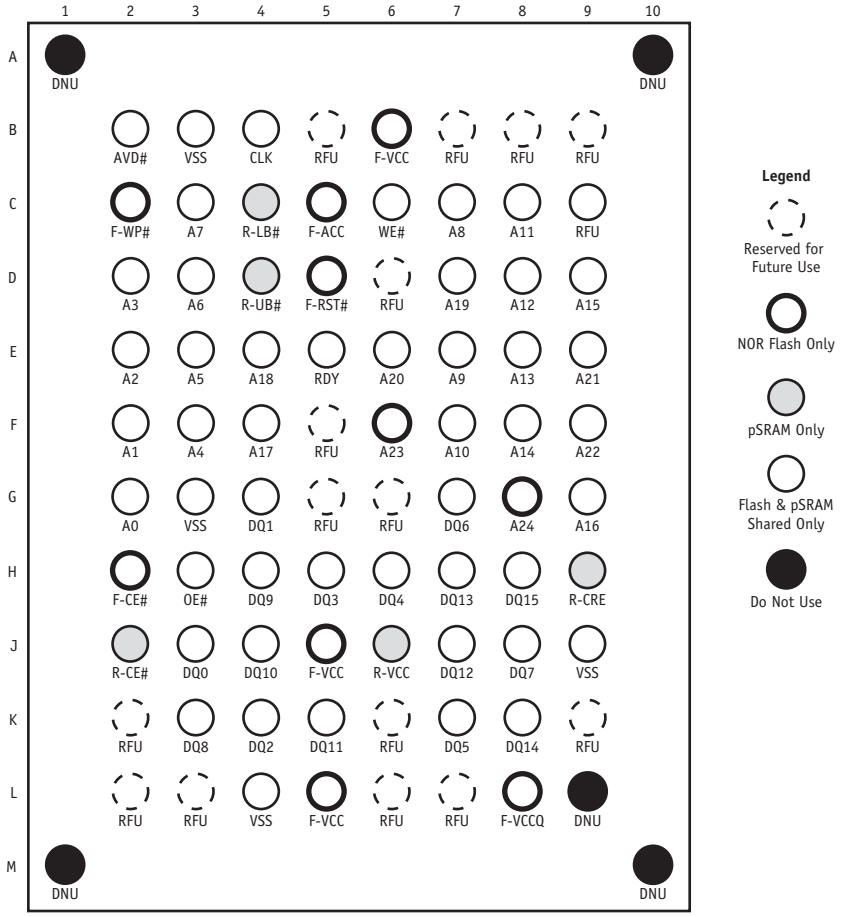
1. Product Selector Guide

Device	Model Number	Flash Density (Mb)	CellularRAM Density (Mb)	Flash Speed (MHz)	CellularRAM Speed (MHz)	CellularRAM Supplier	Package
S71WS512PD0HF3	HL	512	128	104	104	Type 2	84 ball MCP 8x11.6x1.2 mm
S71WS512PD0HF3	SL			104			
S71WS512PD0HF3	SR			80			
S71WS512PC0HF3	SL	512	64	104	104	Type 2	84 ball MCP 8x11.6x1.2 mm
S71WS512PC0HF3	SR			80			
S71WS512PC0HF3	SV			66			
S71WS512PC0HF3	S2			54			
S71WS512PC0HF3	SW			Asynchronous			
S71WS256PD0HF3	HL	256	128	104	104	Type 2	84 ball MCP 8x11.6x1.2 mm
S71WS256PD0HF3	HR			80			
S71WS256PD0HF3	SL			104	104	Type 2	
S71WS256PD0HF3	SR			80			
S71WS256PD0HF3	SV			66			
S71WS256PD0HF3	TL			104	104	Type 3	
S71WS256PC0HF3	SL	256	64	104	104	Type 2	
S71WS256PC0HF3	SR			80			
S71WS256PC0HF3	SV			66			
S71WS128PC0HF3	SL	128	64	104	104	Type 2	84 ball MCP 8x11.6x1.2 mm
S71WS128PC0HF3	SR			80			
S71WS128PC0HF3	SV			66			
S71WS128PC0HF3	TR	128	64	80	104	Type 3	

2. MCP Block Diagram



3. Connection Diagrams



Note

1. V_{CC} pins must ramp simultaneously.

MCP	Flash-only Addresses	Shared Addresses
S71WS512PD0	A24-A23	A22-A0
S71WS512PC0	A24-A22	A21-A0
S71WS256PD0	A24-A23	A22-A0
S71WS256PC0	A24-A22	A21-A0
S71WS128PC0	A24-A22	A21-A0

3.1 Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

3.2 Look-ahead Ballout for Future Designs

Please refer to the Design-in Scalable Wireless Solutions with Spansion Products application note (publication number: Design_Scalable_Wireless_A0_E). Contact your local Spansion sales representative for more details.

3.3 NOR Flash and pSRAM Input/Output Descriptions

Signal	Description	Flash	pSRAM
Amax-A0	NOR Flash Address inputs	X	X
DQ15-DQ0	Flash Data input/output, shared between NOR and ORNAND Flash. DQ0-DQ7 shared for x8 ORNAND	X	X
F-CE#	NOR Flash Chip-enable input #1. Asynchronous relative to CLK for Burst Mode.	X	
OE#	Output Enable input. Asynchronous relative to CLK for Burst mode.	X	X
WE#	Write Enable input.	X	X
F-V_{CC}	NOR Flash device power supply (1.7 V - 1.95 V).	X	
F-V_{CCQ}	Input/Output Buffer power supply.	X	
V_{SS}	Ground	X	X
RFU	Reserved for Future Use		
RDY	Flash ready output. Indicates the status of the Burst read. V_{OL} = data valid. The Flash RDY pin is shared with the WAIT pin of the pSRAM.	X	X
CLK	NOR Flash Clock, shared with CLK of burst-mode pSRAM.. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.	X	X
AVD#	NOR Flash Address Valid input. Shared with AVD# of burst-mode pSRAM. Indicates to device that the valid address is present on the address inputs. V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH}= device ignores address inputs	X	X
F-RST#	NOR Flash hardware reset input. V_{IL}= device resets and returns to reading array data	X	
F-WP#	NOR Flash hardware write protect input. V_{IL} = disables program and erase functions in the four outermost sectors.	X	
F-ACC	NOR Flash accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.	X	
R-CE#	Chip-enable input for pSRAM		X
R-CRE	Control Register Enable (pSRAM). For CellularRAM only.		X
R-VCC	pSRAM Power Supply		X
R-UB#	Upper Byte Control (pSRAM)		X
R-LB#	Lower Byte Control (pSRAM)		X
DNU	Do Not Use		

4. Ordering Information

The order number is formed by a valid combinations of the following:

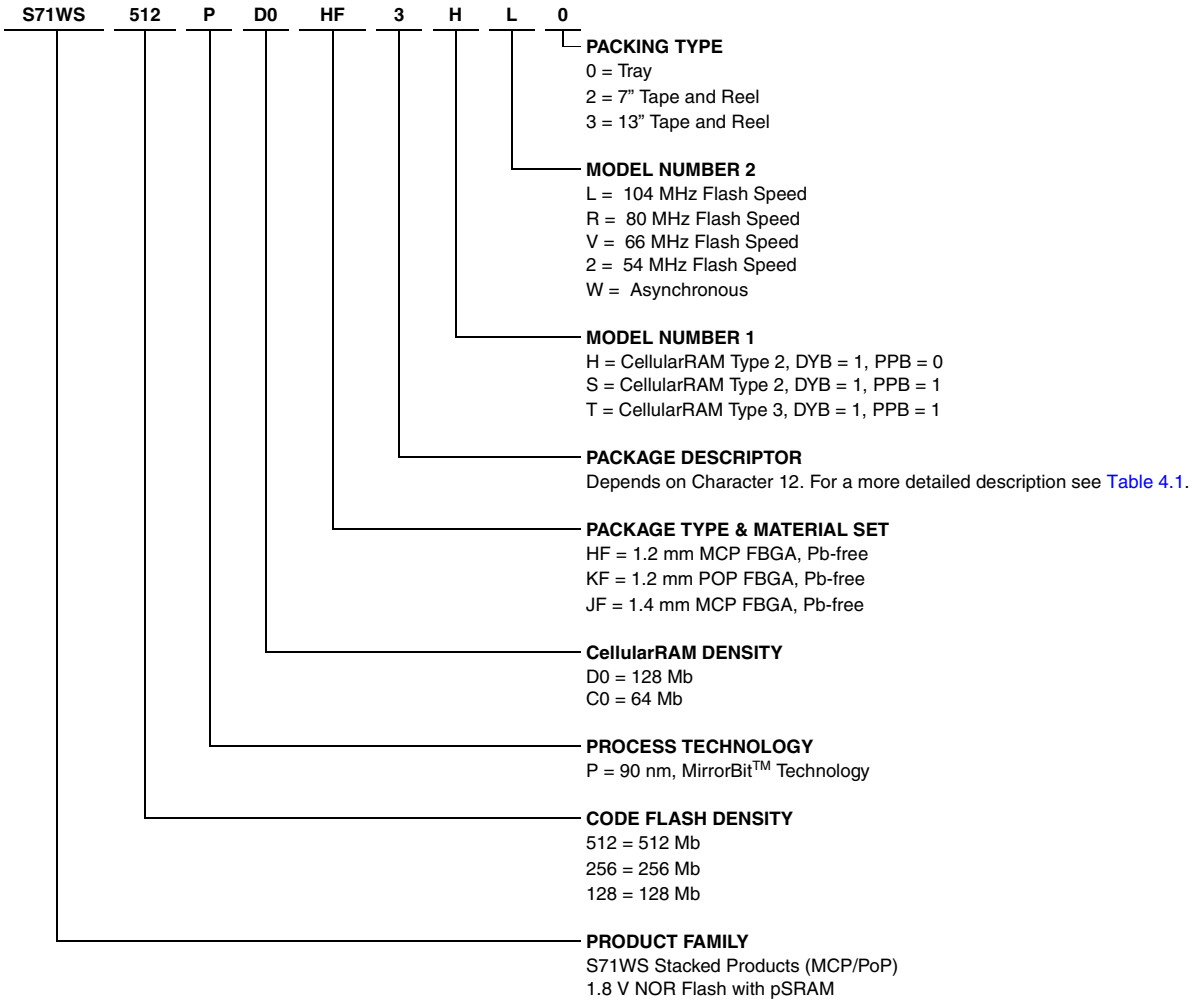


Table 4.1 Character Position Descriptions

Character 12	Character 14	Character 14 Description		
		Package Area	Package Ball Count	Raw Ball Size
H or J	0	7x9 mm	56	0.35 mm
	1	7x9 mm	80	
	2	8x11.6 mm	64	
	3	8x11.6 mm	84	
	4	9x12 mm	84	
	5	9x12 mm	115	
	6	9x12 mm	137	
	7	11x13 mm	84	
	8	11x13 mm	115	
	9	11x13 mm	137	
K	A	11x11 mm	112	0.45 mm
	B	11x11 mm	112	0.50 mm
	D	12x12 mm	128	0.45 mm
	F	12x12 mm	128	0.50 mm
	G	14x14 mm	152	0.45 mm
	H	14x14 mm	152	0.50 mm
	J	15x15 mm	160	0.45 mm
	K	15x15 mm	160	0.50 mm
	L	17x17 mm	192	0.45 mm
	M	17x17 mm	192	0.50 mm

4.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

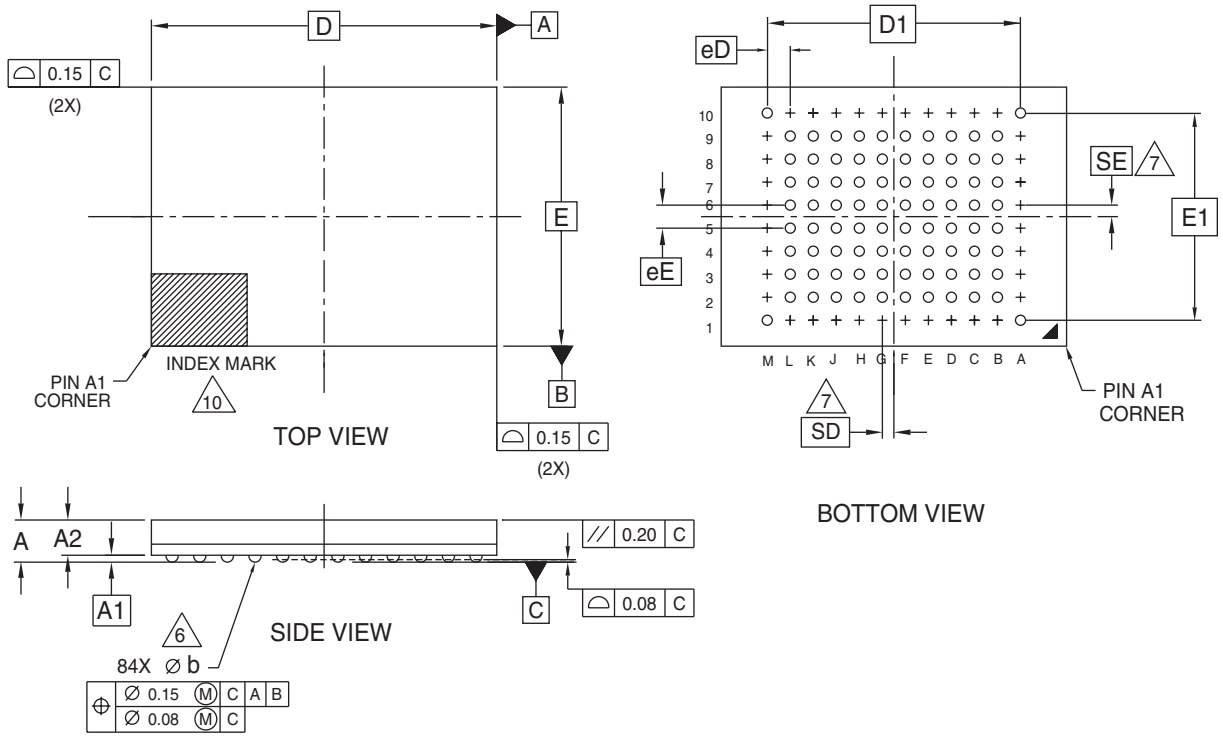
Valid Combination							
Product Family	Code Flash Denisty (Mb)	Process Technology	CellularRAM Density	Package Type / Material	Model Number Combo	Flash & CellularRAM Speed	Packing Type
					CellularRAM Type / DYB/PPB		
S71WS	128	P	C0, D0	HF3	H	R,L	0,2,3 (Note 1)
	256				S	W,2,V,R,L	
	512				T	R,L	
			D0	JF4	H	R,L	

Notes:

1. *Packing Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading* S *and packing type designator from ordering part number.*

5. Physical Dimensions

5.1 TLA084— 84-ball Fine Pitch Ball Grid Array (FBGA) 8x11.6mm Package



PACKAGE	TLA 084			
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		11.60 BSC.		BODY SIZE
E		8.00 BSC.		BODY SIZE
D1		8.80 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		12		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		84		BALL COUNT
Ø b	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10, E1,E10,F1,F10,G1,G10, H1,H10,J1,J10,K1,K10,L1,L10, M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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6. Revision History

6.1 Revision A (February 21, 2006)

Initial release.

6.2 Revision A1 (April 12, 2006)

Added the S71WS512PC0

6.3 Revision A2 (August 21, 2006)

Added the S71WS512PD0 108MHz OPN

6.4 Revision A3 (November 7, 2006)

Added the S71WS256PD0 MCP

Added the S71WS256PC0 MCP

6.5 Revision A4 (December 8, 2006)

Added new CellularRAM Type 3

Revised Valid Combination table

Revised Product Selector Guide

6.6 Revision A5 (January 11, 2007)

Added S71WS128PC0 MCP offering

6.7 Revision A6 (February 5, 2007)

Added the S71WS512PD0JF4 OPN

6.8 Revision A7 (March 27, 2007)

Added the S71WS512PD0HF3SR OPN

6.9 Revision A8 (July 30, 2007)

Added 80 MHz S71WS128PC0 to Valid Combinations

6.10 Revision A9 (September 4, 2007)

Added 54 MHz and Asynchronous S71WS512PC0 MCP

Revised Valid Combinations

6.11 Revision A10 (October 19, 2007)

Add 104 MHz, 80 Mhz and 66 MHz S71WS256PC, S71WS256PD and S71WS128PC MCP products

Removed the S71WS512PD0JF MCP

Colophon

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