S71WS-J Based MCPs

Stacked Multi-Chip Product (MCP) Package-on-Package (PoP) 128/64 Megabit (8M/4M x 16-bit) CMOS 1.8 Volt-only, Simultaneous Read/Write, Burst Mode Flash Memory with CellularRAM

Data Sheet

ADVANCE INFORMATION

Notice to Readers: The Advance Information status indicates that this document contains information on one or more products under development at Spansion LLC. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion LLC reserves the right to change or discontinue work on this proposed product without notice.

Publication Number S71WS-J_03 **Revision** A **Amendment** 3 **Issue Date** November 28, 2005

Notice On Data Sheet Designations

Spansion LLC issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Spansion LLC is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion LLC therefore places the following conditions upon Advance Information content:

> "This document contains information on one or more products under development at Spansion LLC. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion LLC reserves the right to change or discontinue work on this proposed product without notice."

Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. The Preliminary status of this document indicates that product qualification has been completed, and that initial production has begun. Due to the phases of the manufacturing process that require maintaining efficiency and quality, this document may be revised by subsequent versions or modifications due to changes in technical specifications."

Combination

Some data sheets will contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document will distinguish these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with DC Characteristics table and AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion LLC deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local AMD or Fujitsu sales office.

S71WS-J Based MCPs

Stacked Multi-Chip Product (MCP) Package-on-Package (PoP) 128/64 Megabit (8M/4M x 16-bit) CMOS 1.8 Volt-only, Simultaneous Read/Write, Burst Mode Flash Memory with CellularRAM

Data Sheet

ADVANCE INFORMATION

Distinctive Characteristics

MCP Features

- **Power supply voltage of 1.7 to 1.95V**
- **Speed: 66MHz**
- **Packages**
  - 8 x 11.6mm, 84 ball FBGA
  - 12 x 12 x 1.10 mm, 128 ball PoP, 0.50 mm ball
- **Operating Temperature**
  - –25°C to +85°C

General Description

The S71WS series is a product line of stacked memory packages (MCP and PoP) and consists of:

- One or more flash memory die
- pSRAM

The products covered by this document are listed in the table below. For details about their specifications, please refer to the individual constituent datasheets for further details:

		Flash Memory Density		
		256Mb	128Mb	64Mb
pSRAM Density	64Mb	S71WS256JC0	S71WS128JC0	
	32Mb		S71WS128JB0	S71WS064JB0
	16Mb		S71WS128JA0	S71WS064JA0

Publication Number S71WS-J_03 **Revision** A **Amendment** 3 **Issue Date** November 28, 2005

Table of Contents

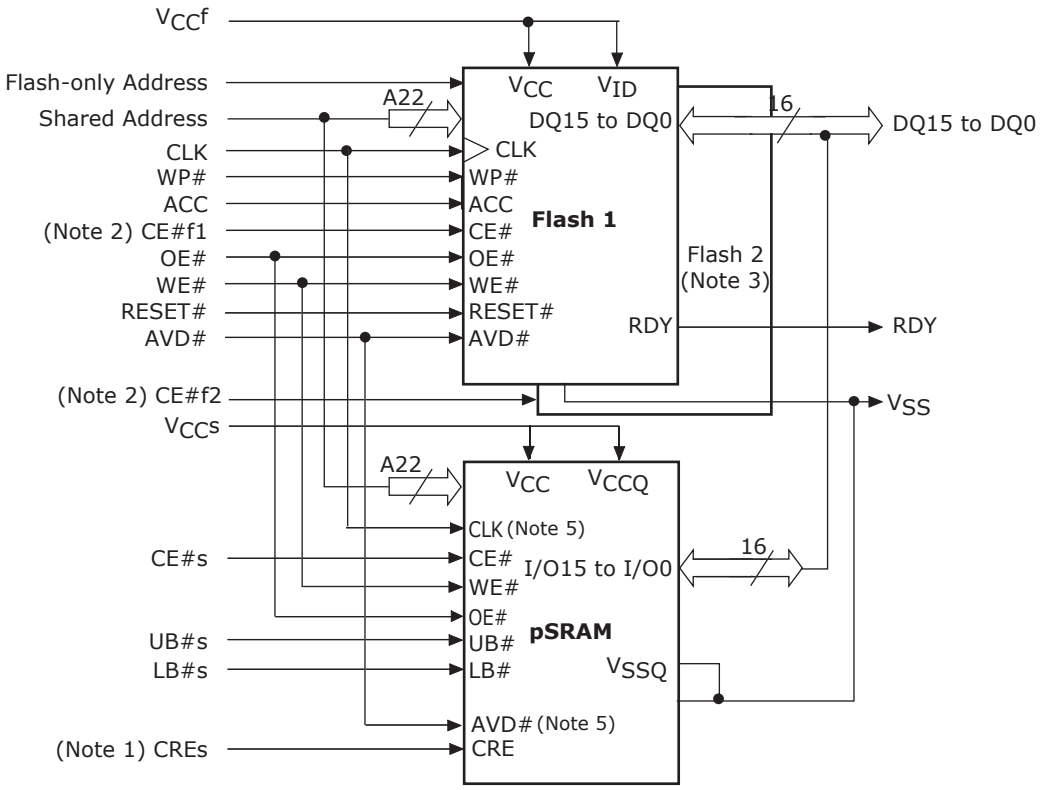
Tables

Figures

1 Product Selector Guide

Device-Model#	Flash Density	pSRAM Density	Flash Speed (MHz)	pSRAM Speed (MHz/ns)	Supplier	Package
S71WS064JA0KFW5A	64Mb	16Mb	66	66/70	Cellular RAM Type 2	12x12x1.10 mm .50 mm ball size 128-ball PoP
S71WS064JB0-2A		32Mb			Cellular RAM Type 2	7x9x1.2 mm 80-ball, MCP
S71WS128JA0-AA	128Mb	16Mb			Cellular RAM Type 2	8x11.6x1.2mm 84-ball, MCP
S71WS128JB0-AA		32Mb			Cellular RAM Type 2	
S71WS128JC0-AA		64Mb			Cellular RAM Type 2	
S71WS256JC0-TA	256Mb				Cellular RAM Type 2	8x11.6x1.4mm 84-ball, MCP

2 Product Block Diagram



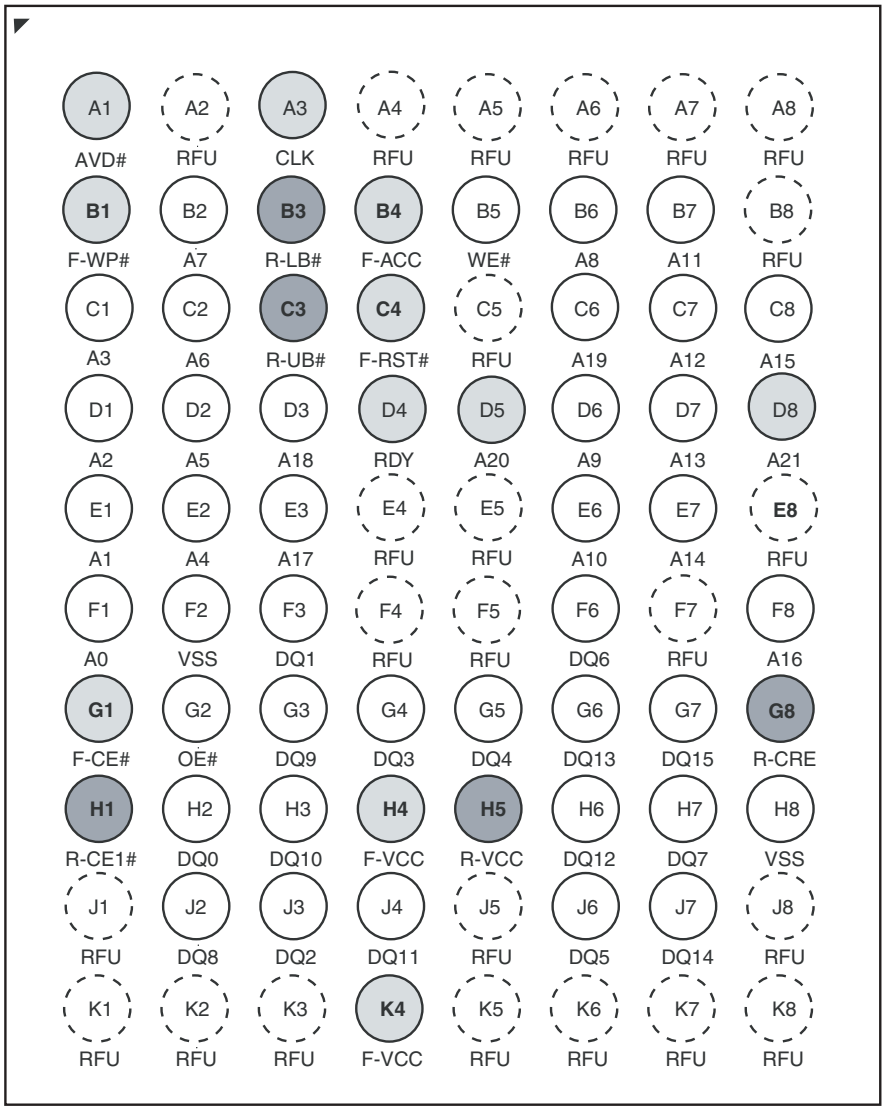
Notes:

1. *CREs is only present in CellularRAM-compatible pSRAM.*
2. *For 1 Flash = pSRAM, CE#f1 = CE#. For 2 Flash + pSRAM, CE# = CE#f1 and CE#f2 is the chip-enable pin for the second Flash.*
3. *Only needed for S71WS256JC0.*
4. *CLK and AVD# not applicable for 16Mb pSRAM.*

3 Connection Diagram (CellularRAM Type-based)

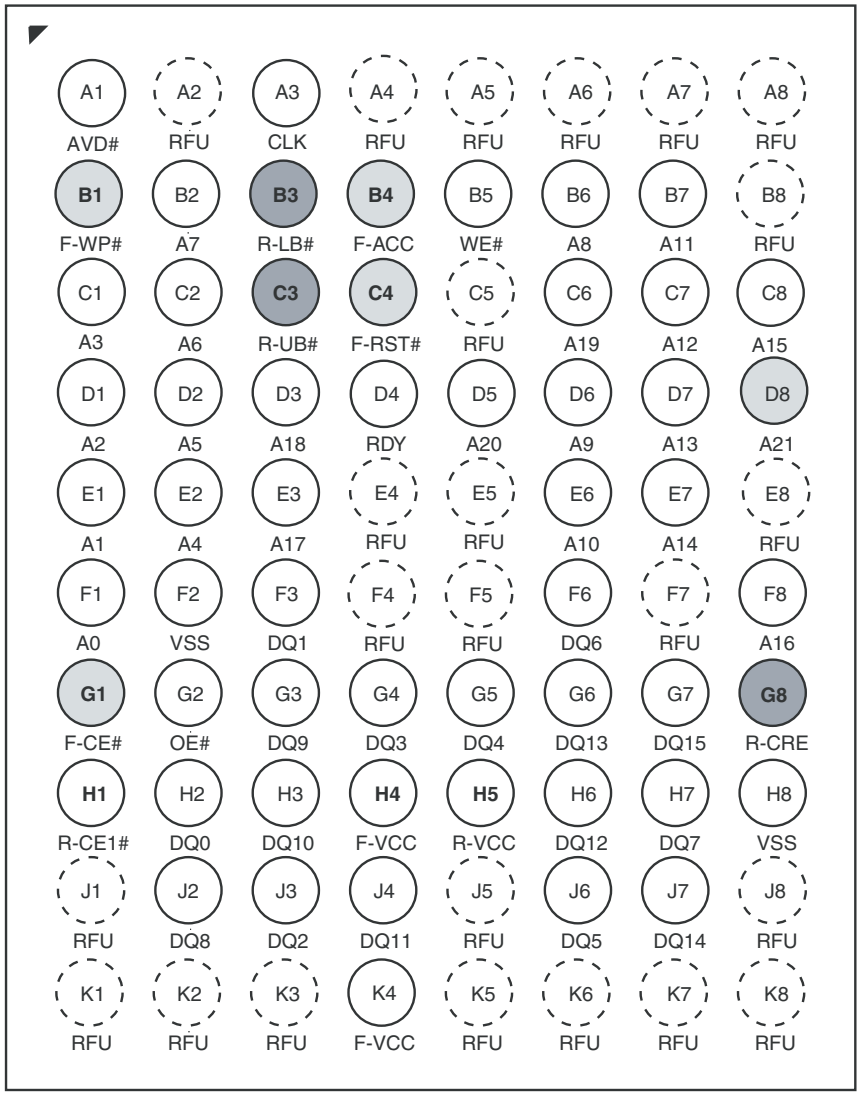
3.1 S71WS064JA0

80-ball Fine-Pitch Ball Grid Array MCP
(Top View, Balls Facing Down)



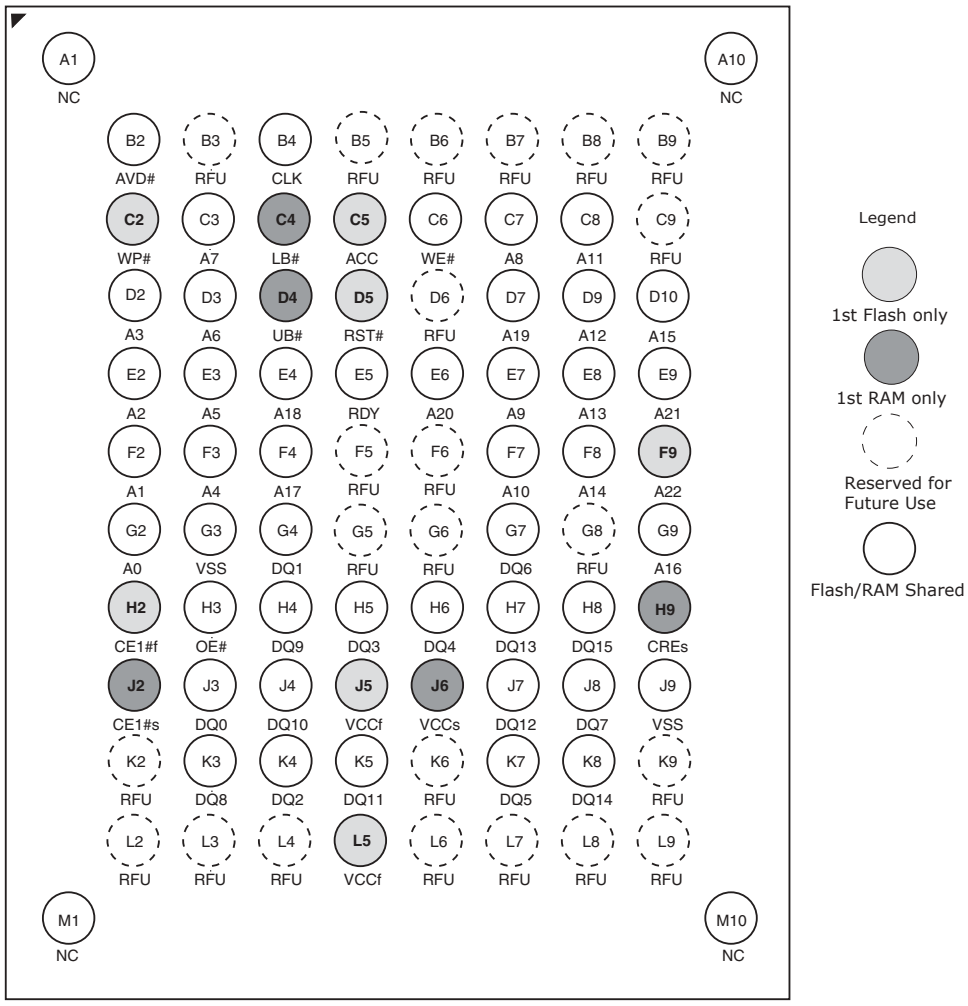
3.2 S71WS064JB0

80-ball Fine-Pitch Ball Grid Array MCP
(Top View, Balls Facing Down)



3.3 S71WS128J and S71WS256J

84-ball Fine-Pitch Ball Grid Array MCP
(Top View, Balls Facing Down)



Notes:

1. *In stacked products based on a single S29WS-J Flash Die, ball B5 is RFU. In MCP's based on two S29WS-J (S71WS256J), ball B5 is CE#f2 or F2-CE#.*
2. *Addresses are shared between Flash and RAM depending on the density of the pSRAM.*

MCP	Flash-only Addresses	Shared Addresses
S71WS064JA0	A21-A20	A19-A0
S71WS128JA0	A22-A20	A19-A0
S71WS128JB0	A22-A21	A19-A0
S71WS128JC0	A22	A21-A0
S71WS256JC0	A22	A21-A0

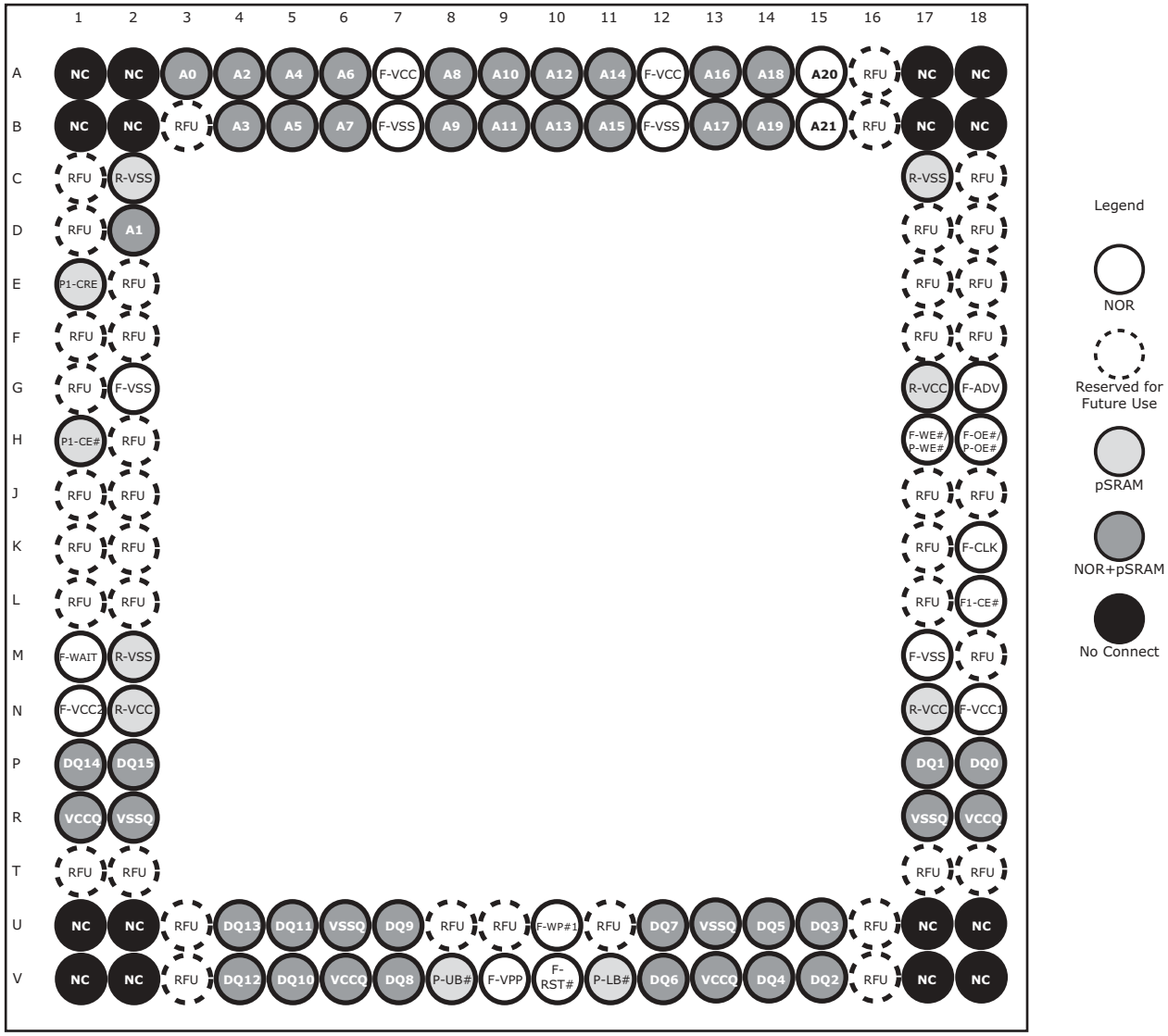
3.4 Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

3.5 S71WS064JA0

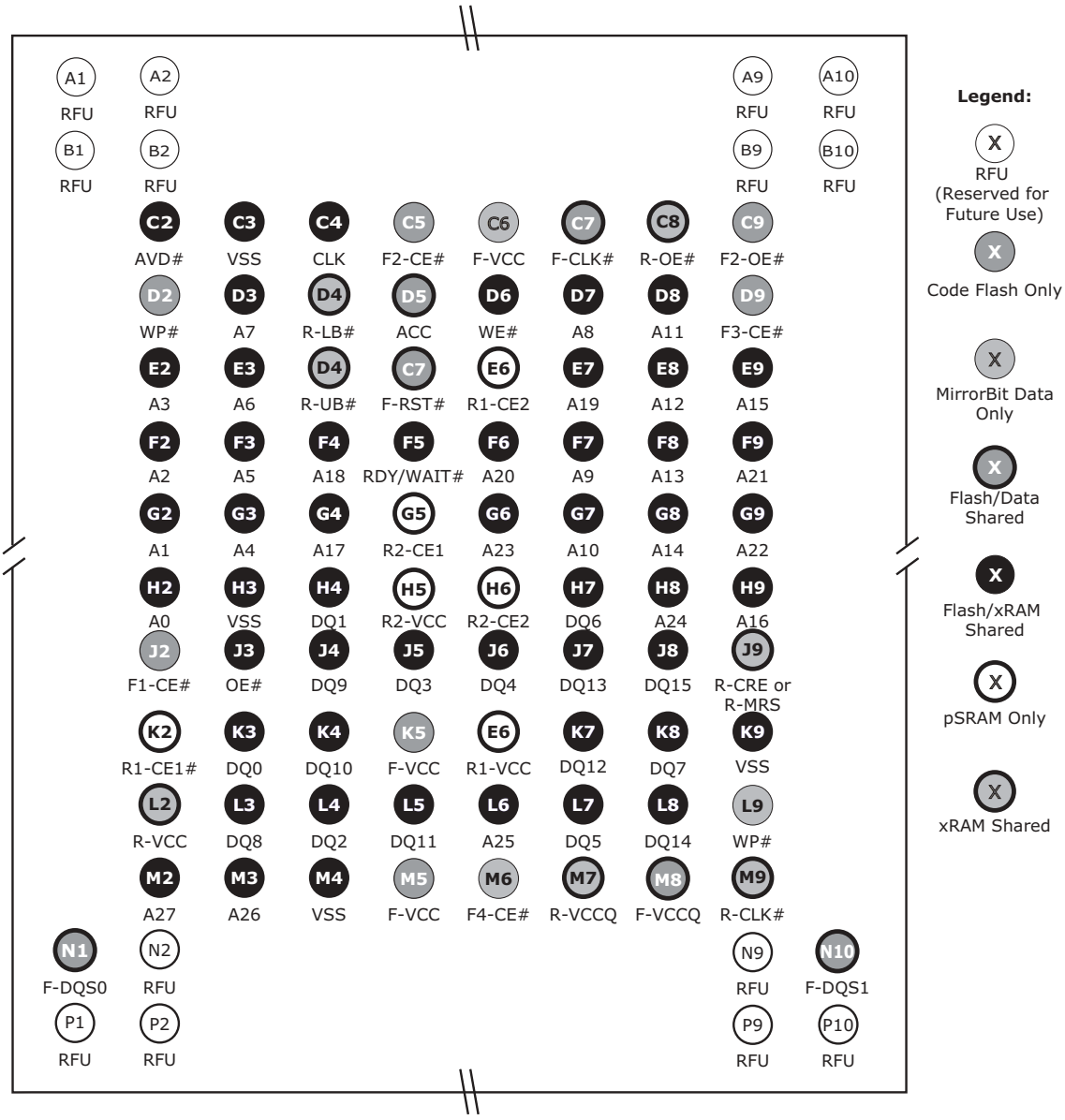
128-ball Fine-Pitch Ball Grid Array PoP
(Top View, Balls Facing Down)



Note: *The V_{CC} and V_{CCQ} (V_{IO}) signals must be ramped simultaneously to ensure a successful power up sequence.*

4 MCP Lookahead Connection Diagram

Contact your local Spansion representative for a complete PoP lookahead pinout.



Notes:

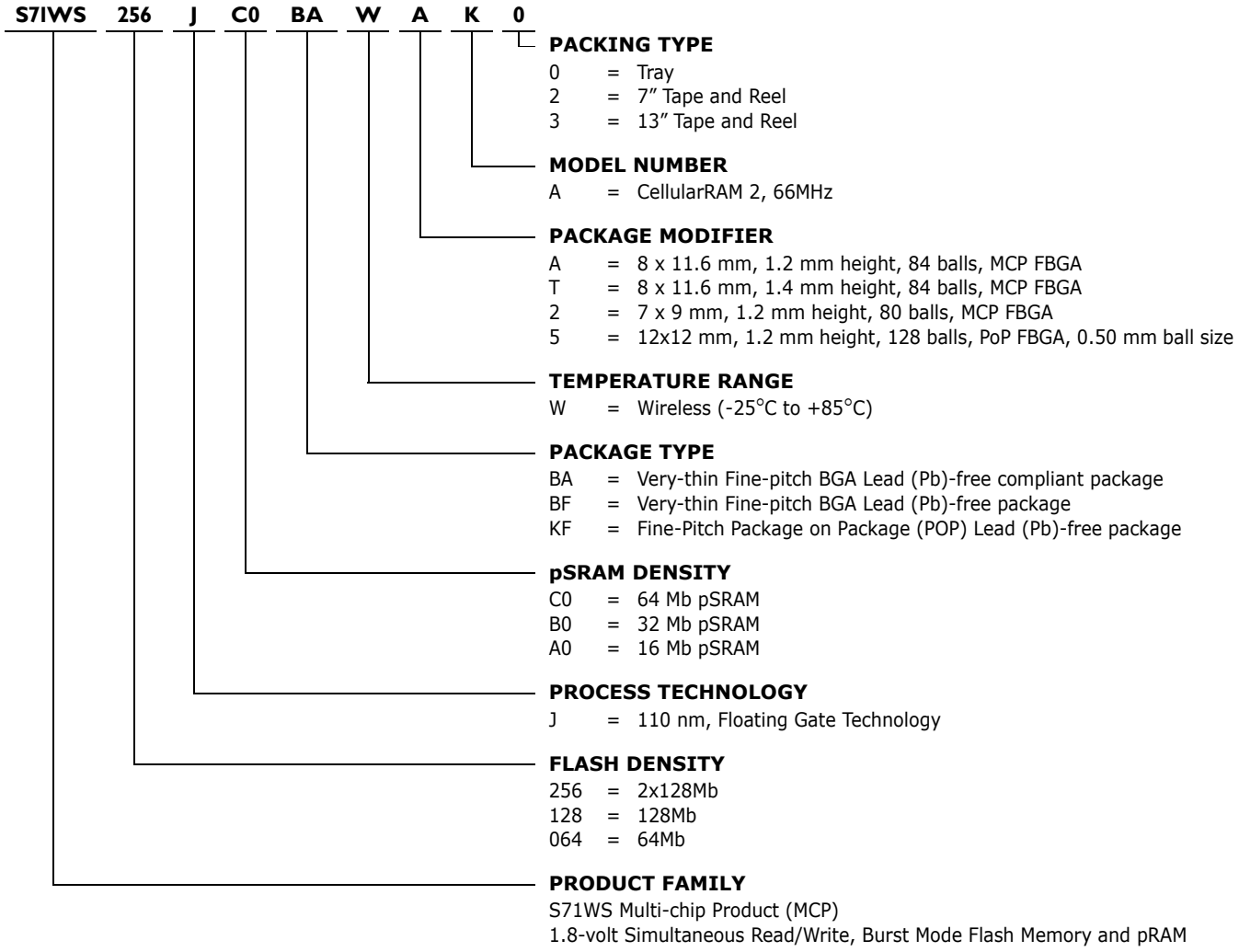
1. *F1 and F2 denote XIP/Code Flash, while F3 and F4 denote Data/Companion Flash.*
2. *In addition to being defined as F2-CE#, Ball C5 can also be assigned as F1-CE2# for code flash that has two chip enable signals.*
3. *For MCPs requiring 3.0V Vcc and 1.8V Vio, use the 1.8V Look-ahead Pinout in order to accommodate extra AVD, MRS and CLK pins for the pSRAM (if needed).*
4. *Refer to Application Note on pinout subsets to match the package size offerings.*

5 Input/Output Descriptions

A22-A0	=	Address inputs
DQ15-DQ0	=	Data input/output
OE#	=	Output Enable input. Asynchronous relative to CLK for the Burst mode.
WE#	=	Write Enable input.
V_{SS}	=	Ground
NC	=	No Connect; not connected internally
RDY	=	Ready output. Indicates the status of the Burst read (shared with WAIT# pin of RAM).
CLK	=	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at V_{IL} or V_{IH} while in asynchronous mode
AVD#	=	Address Valid input. Indicates to device that the valid address is present on the address inputs. Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched. High = device ignores address inputs
RESET#	=	Hardware reset input. Low = device resets and returns to reading array data
WP#	=	Hardware write protect input. At V_{IL}, disables program and erase functions in the four outermost sectors. Should be at V_{IH} for all other conditions.
ACC	=	Accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.
CE1#s	=	Chip-enable input for pSRAM.
CE#f1	=	Chip-enable input for Flash 1. Asynchronous relative to CLK for Burst Mode.
CREs	=	Control Register Enable (pSRAM).
V_{CC}f	=	Flash 1.8 Volt-only single power supply.
V_{CC}s	=	pSRAM Power Supply.
UB#s	=	Upper Byte Control (pSRAM).
LB#s	=	Lower Byte Control (pSRAM).
CE#f2	=	Chip-enable input for Flash 2. Asynchronous relative to CLK for burst mode (needed only for S71WS256J).
RFU	=	Reserved for future use.
CE2s	=	Chip-enable input for pSRAM

6 Ordering Information

The order number is formed by a valid combinations of the following:



Valid Combinations

Base Ordering Part Number	pSRAM Density	Package Type	Temperature	Package Modifier	Model Number	Packing Type
S71WS064J	A0	KF	W	5	A	0, 2, 3 1
	B0	BA, BF		2		
S71WS128J	A0, B0, C0	BA, BF		A		
S71WS256J	C0	BA, BF		T		

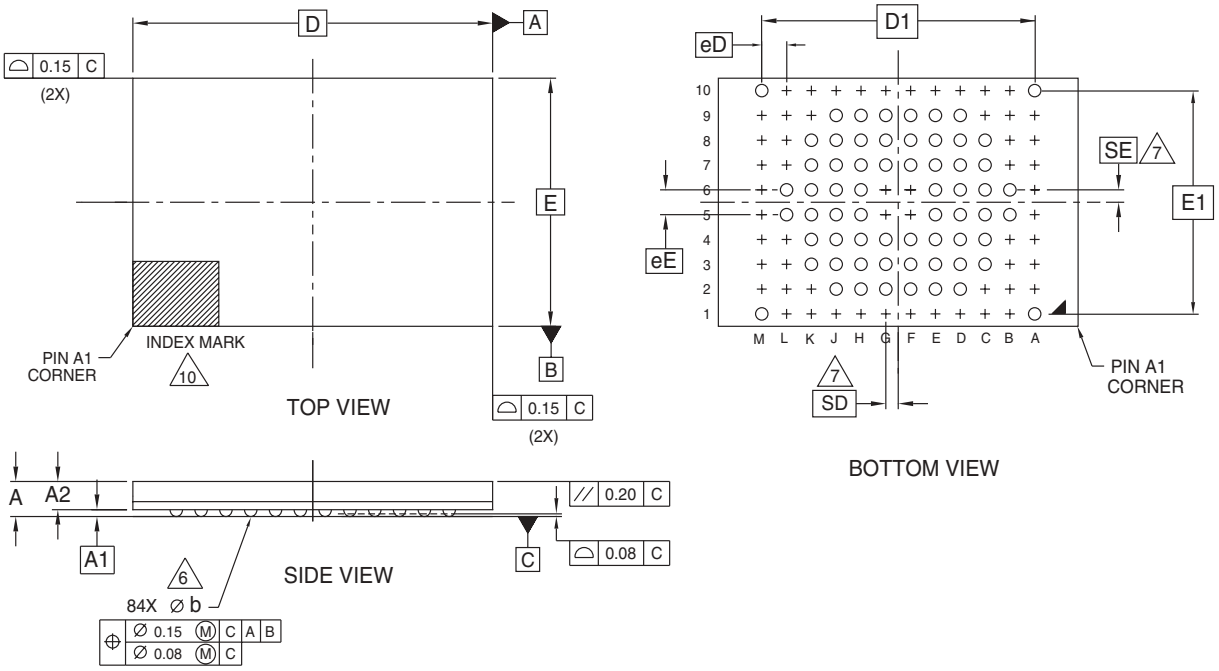
Notes:
1. *Packing Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

7 Physical Dimensions

7.1 TLA084 – 84-ball Fine-Pitch Ball Grid Array (FBGA) 8 x 11.6 mm Package



PACKAGE	TLA 084			
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		11.60 BSC.		BODY SIZE
E		8.00 BSC.		BODY SIZE
D1		8.80 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		12		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		84		BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10, E1,E10,F1,F10,G1,G10, H1,H10,J1,J10,K1,K10,L1,L10, M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

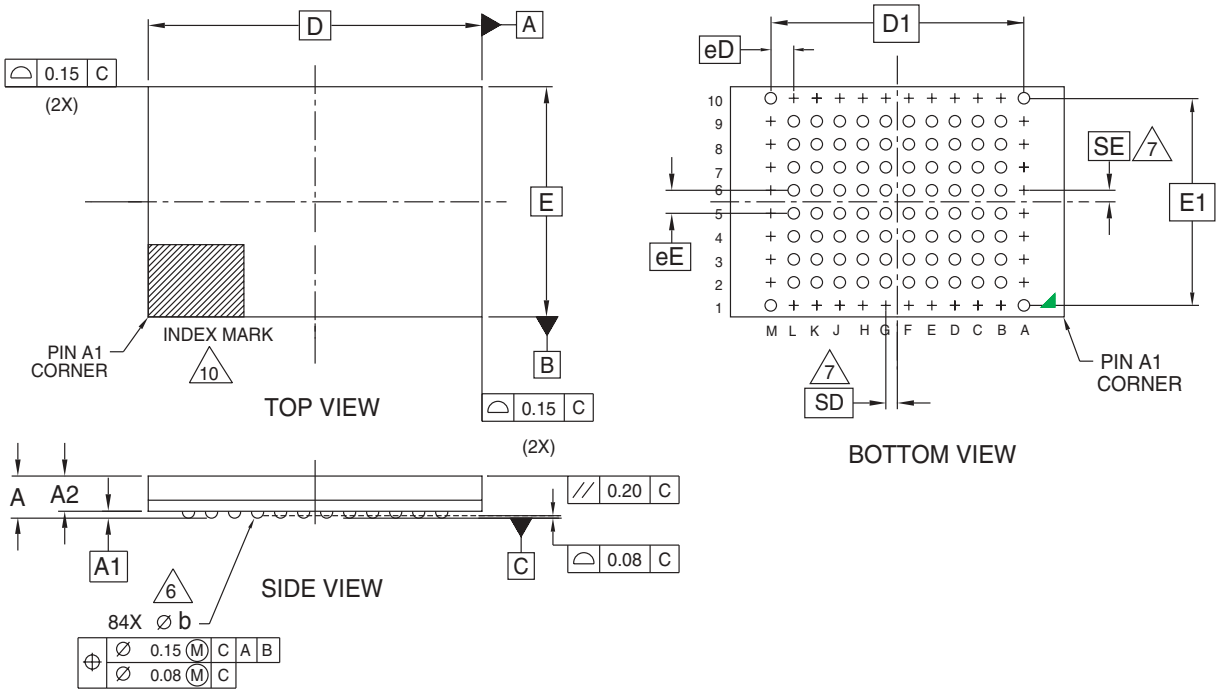
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3372 \ 16-038.22a

7.2 FTA084 – 84-ball Fine-Pitch Ball Grid Array (FBGA) 8 x 11.6 mm Package



PACKAGE	FTA 084			NOTE
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	---	---	1.40	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	1.02	---	1.17	BODY THICKNESS
D	11.60 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	84			BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10,E1,E10 F1,F10,G1,G10,H1,H10 J1,J10,K1,K10,L1,L10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

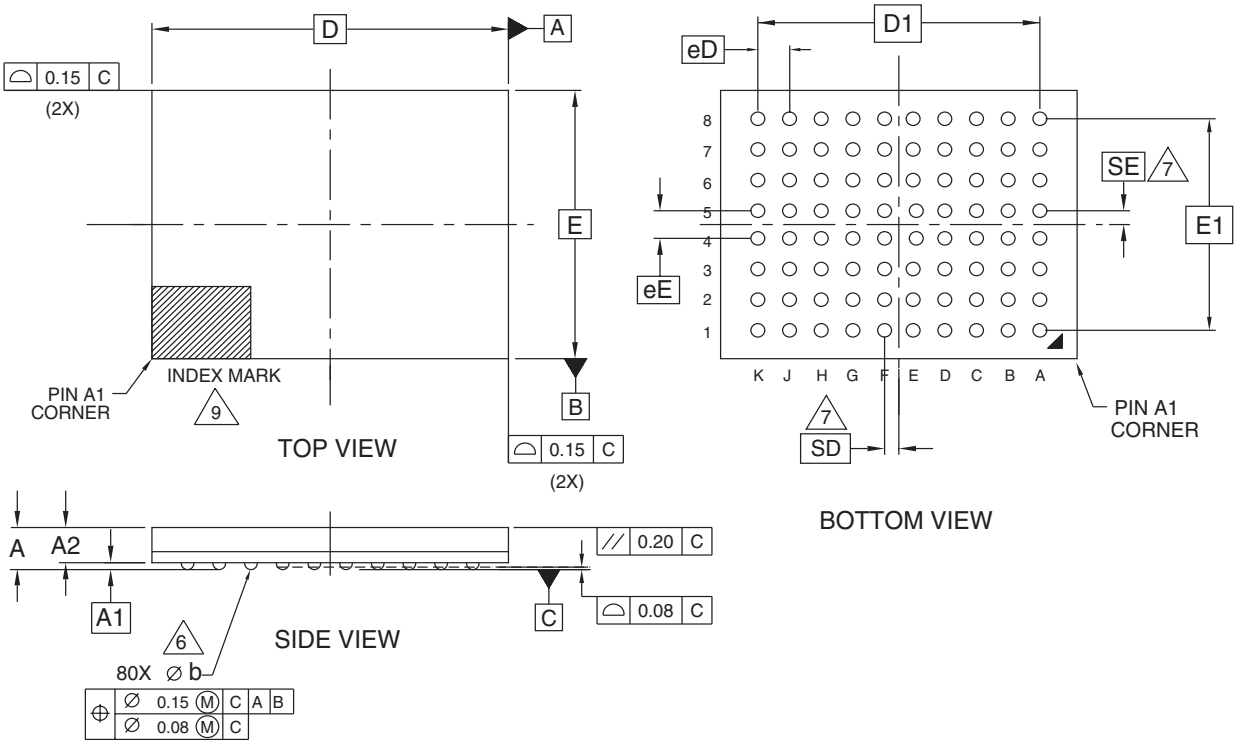
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3388 \ 16-038.21a

7.3 TSC080 - Fine-Pitch Ball Grid Array (FBGA) 7 x 9 mm Package



PACKAGE	TSC 080			
JEDEC	N/A			
D x E	9.00 mm x 7.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		9.00 BSC.		BODY SIZE
E		7.00 BSC.		BODY SIZE
D1		7.20 BSC.		MATRIX FOOTPRINT
E1		5.60 BSC.		MATRIX FOOTPRINT
MD		10		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
n		80		BALL COUNT
Øb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
				DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

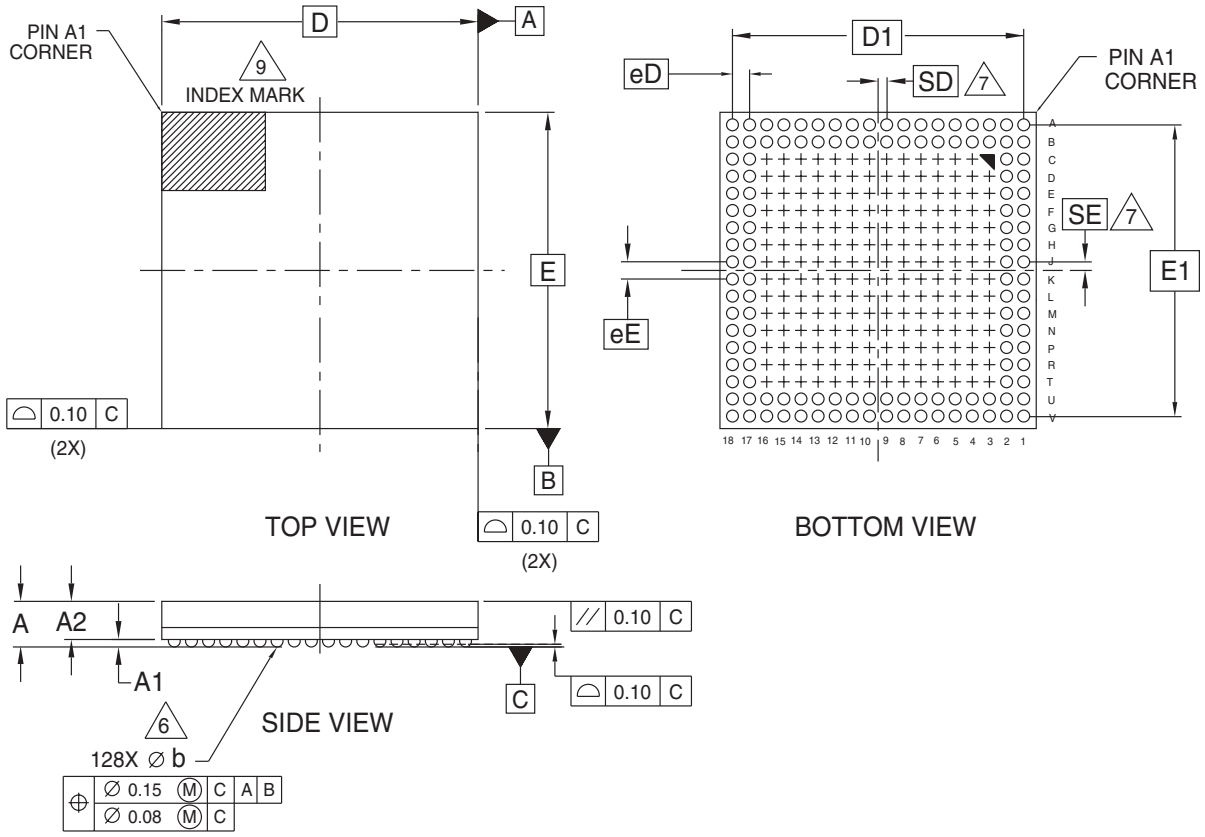
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3496 \ 16-038.22 \ 5.20.05

7.4 ALG128 - 128-ball Fine-Pitch Ball Grid Array (FBGA) 12 x 12 mm Package



PACKAGE	ALG128			
JEDEC	N/A			
D x E	12.00 mm x 12.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.10	PROFILE
A1	0.40	---	---	BALL HEIGHT
A2	0.55	---	0.65	BODY THICKNESS
D		12.00 BSC.		BODY SIZE
E		12.00 BSC.		BODY SIZE
D1		11.05 BSC.		MATRIX FOOTPRINT
E1		11.05 BSC.		MATRIX FOOTPRINT
MD		18		MATRIX SIZE D DIRECTION
ME		18		MATRIX SIZE E DIRECTION
n		128		BALL COUNT
N		128		MAXIMUM NUMBER OF BALLS
R		2		NUMBER OF LAND PERIMETERS
Øb	0.45	0.50	0.55	BALL DIAMETER
eE		0.65 BSC.		BALL PITCH
eD		0.65 BSC		BALL PITCH
SE / SD		0.325 BSC.		SOLDER BALL PLACEMENT
		C3-C16,D3-D16,E3-E16, F3-F16,G3-G16,H3-H16, J3-J16,K3-K16,L3-L16, M3-M16,N3-N16,P3-P16, R3-R16,T3-T16		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3.0, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

   N IS THE MAXIMUM NUMBER OF BALLS ON THE FBGA PACKAGE.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

   DATUM C IS THE SEATING PLANE AND IS DEFINED BY THE CROWNS OF THE SOLDER BALLS.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

3526 16-038.24 \ 10.26.05

S29WS128J/064J

128/64 Megabit (8/4 M x 16-Bit) CMOS 1.8 Volt-only Simultaneous Read/Write, Burst Mode Flash Memory

Data Sheet

Distinctive Characteristics

Architectural Advantages

- **Single 1.8 volt read, program and erase (1.65 to 1.95 volt)**
- **Manufactured on 0.11 µm process technology**
- **Simultaneous Read/Write operation**
  - Data can be continuously read from one bank while executing erase/program functions in other bank
  - Zero latency between read and write operations
  - Four bank architecture: WS128J: 16Mb/48Mb/48Mb/16Mb, WS064J: 8Mb/24Mb/24Mb/8Mb
- **Programable Burst Interface**
  - 2 Modes of Burst Read Operation
  - Linear Burst: 8, 16, and 32 words with wrap-around
  - Continuous Sequential Burst
- **Secured Silicon Sector region**
  - 128 words accessible through a command sequence, 64words for the Factory Secured Silicon Sector and 64words for the Customer Secured Silicon Sector.
- **Sector Architecture**
  - 4 Kword x 16 boot sectors, eight at the top of the address range, and eight at the bottom of the address range
  - **WS128J:** 4 Kword X 16, 32 Kword x 254 sectors
    Bank A : 4 Kword x 8, 32 Kword x 31 sectors
    Bank B : 32 Kword x 96 sectors
    Bank C : 32 Kword x 96 sectors
    Bank D : 4 Kword x 8, 32 Kword x 31 sectors
  - **WS064J:** 4 Kword x 16, 32 Kword x 126 sectors.
    Bank A : 4 Kword x 8, 32 Kword x 15 sectors
    Bank B : 32 Kword x 48 sectors
    Bank C : 32 Kword x 48 sectors
    Bank D : 4 Kword x 8, 32 Kword x 15 sectors
- **Cyclling Endurance : 1,000,000 cycles per sector typical**
- **Data retention : 20-years typical**

Performance Characteristics

- **Read access times at 80/66 MHz**
  - Synchronous latency of 71/56 ns (at 30 pF)
  - Asynchronous random access times of 55/55 ns (at 30 pF)
- **Power dissipation (typical values, C_L = 30 pF)**
  - Burst Mode Read: 18 mA @ 80Mhz
  - Simultaneous Operation: 60 mA @ 80Mhz
  - Program/Erase: 15 mA
  - Standby mode: 0.2 µA

Hardware Features

- **Handshaking feature available**
  - Provides host system with minimum possible latency by monitoring RDY
- **Hardware reset input (RESET#)**
  - Hardware method to reset the device for reading array data
- **WP# input**
  - Write protect (WP#) function allows protection of four outermost boot sectors, regardless of sector protect status
- **Persistent Sector Protection**
  - A command sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector
  - Sectors can be locked and unlocked in-system at V_{CC} level
- **Password Sector Protection**
  - A sophisticated sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector using a user-defined 64-bit password
- **ACC input: Acceleration function reduces programming time; all sectors locked when ACC = V_{IL}**
- **CMOS compatible inputs, CMOS compatible outputs**
- **Low V_{CC} write inhibit**

Software Features

- **Supports Common Flash Memory Interface (CFI)**
- **Software command set compatible with JEDEC 42.4 standards**
  - Backwards compatible with Am29BDS, Am29BDD, Am29BL, and MBM29BS families
- **Data# Polling and toggle bits**
  - Provides a software method of detecting program and erase operation completion
- **Erase Suspend/Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences

Publication Number S29WS-J_M0 **Revision** A **Amendment** 4 **Issue Date** June 24, 2005

General Description

The S29WS128J/064J/S29WS064J is a 128/64 Mbit, 1.8 Volt-only, simultaneous Read/Write, Burst Mode Flash memory device, organized as 8,388,608/4,194,304 words of 16 bits each. This device uses a single V_{CC} of 1.65 to 1.95 V to read, program, and erase the memory array. A 12.0-volt V_{HH} on ACC may be used for faster program performance if desired. The device can also be programmed in standard EPROM programmers.

At 80 MHz, the device provides a burst access of 9.1 ns at 30 pF with a latency of 46 ns at 30 pF. At 66 MHz, the device provides a burst access of 11.2 ns at 30 pF with a latency of 56 ns at 30 pF. The device operates within the wireless temperature range of -25°C to +85°C, and is offered in Various FBGA packages.

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into four banks. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The device is divided as shown in the following table:

Bank	Quantity		Size
	128Mb	64 Mb	
A	8	8	4 Kwords
	31	15	32 Kwords
B	96	48	32 Kwords
C	96	48	32 Kwords
D	31	15	32 Kwords
	8	8	4 Kwords

The device uses Chip Enable (CE#), Write Enable (WE#), Address Valid (AVD#) and Output Enable (OE#) to control asynchronous read and write operations. For burst operations, the device additionally requires Ready (RDY), and Clock (CLK). This implementation allows easy interface with minimal glue logic to a wide range of microprocessors/microcontrollers for high performance read operations.

The burst read mode feature gives system designers flexibility in the interface to the device. The user can preset the burst length and wrap through the same memory space, or read the flash array in continuous mode.

The clock polarity feature provides system designers a choice of active clock edges, either rising or falling. The active clock edge initiates burst accesses and determines when data will be output.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The **Erase Suspend/Erase Resume** feature enables the user to put erase or program on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the Secured Silicon Sector area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region. Program suspend is also offered.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read boot-up firmware from the Flash memory device.

The host system can detect whether a program or erase operation is complete by using the device status bit DQ7 (Data# Polling) and DQ6/DQ2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The device also offers two types of data protection at the sector level. When at V_{IL}, **WP#** locks the four outermost boot sectors.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

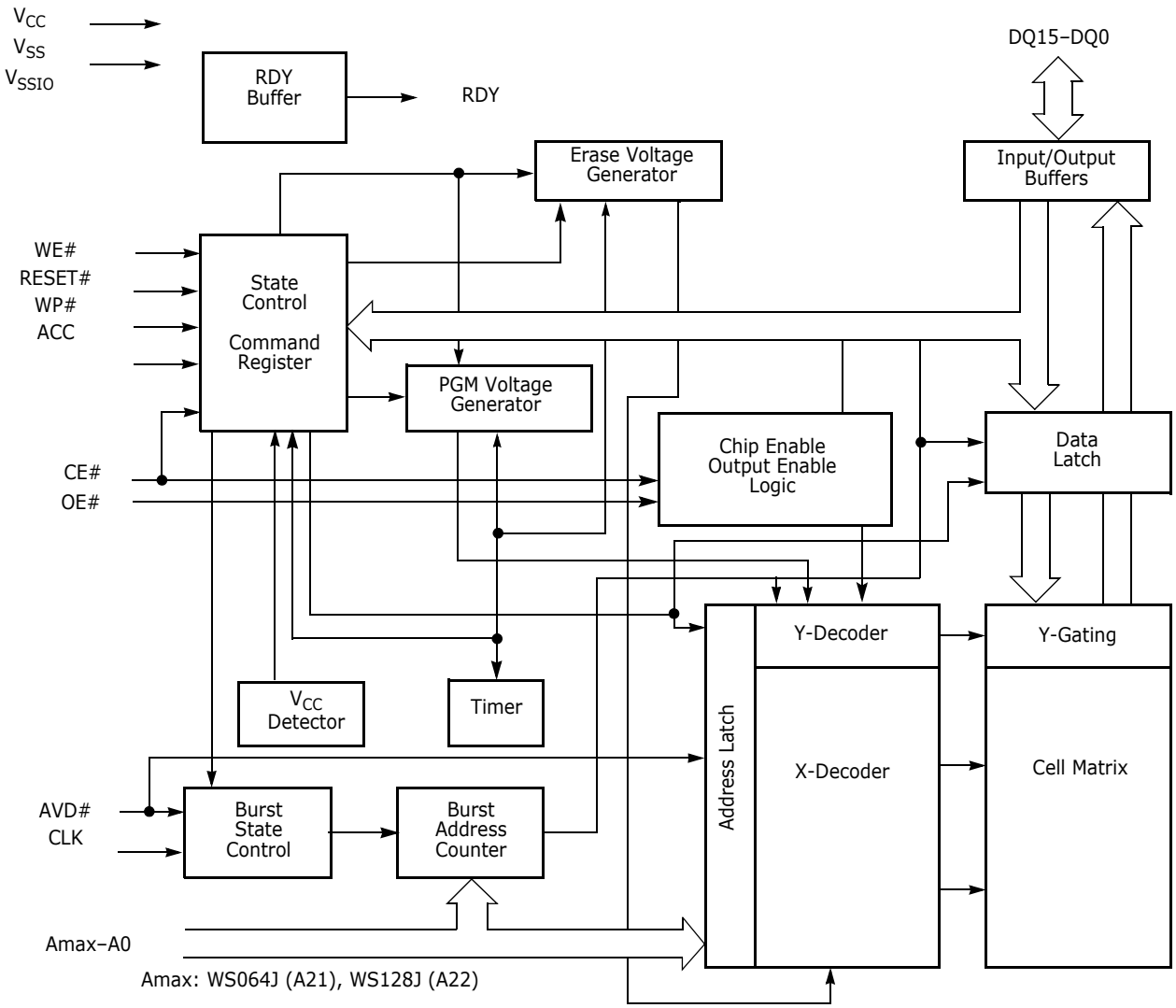
Spansion™ Flash memory products combine years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunnelling. The data is programmed using hot electron injection.

8 Product Selector Guide

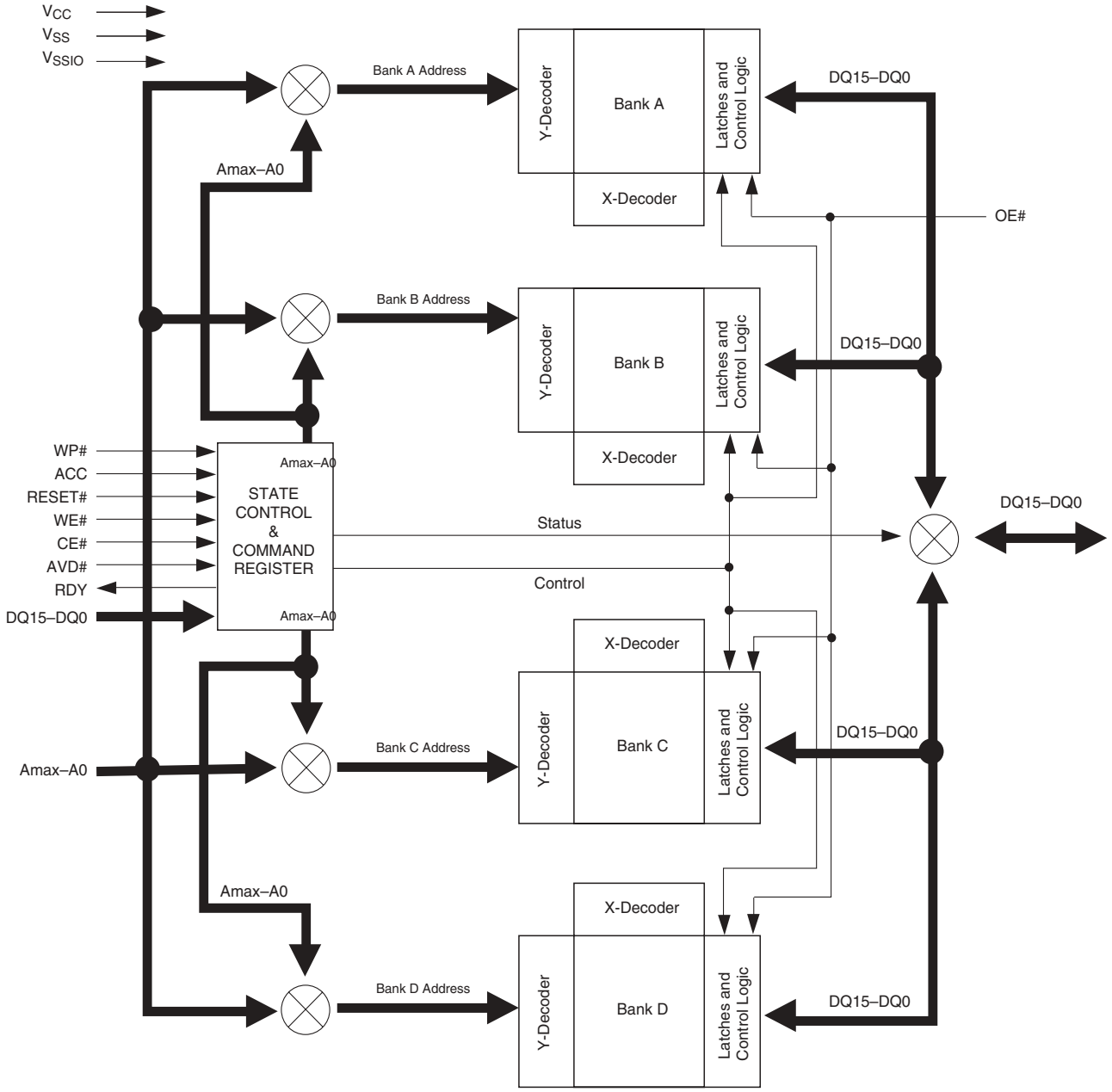
Synchronous/Burst			**Asynchronous**		
Speed Option	**66 MHz**	**80 MHz (Note)**	**Speed Option**	**66 MHz**	**80 MHz (Note)**
Max Latency, ns (t_{IACC})	56	71	Max Access Time, ns (t_{ACC})	55	55
Max Burst Access Time, ns (t_{BACC})	11.2	9.1	Max CE# Access, ns (t_{CE})	55	55
Max OE# Access, ns (t_{OE})	11.2	9.1	Max OE# Access, ns (t_{OE})	11.2	9.1

Note: *80 MHz option is available for S29WS064J only.*

9 Block Diagram



10 Block Diagram of Simultaneous Operation Circuit



Note: *Amax: WS064J (A21), WS128J (A22)*

11 Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 11.1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 11.1 Device Bus Operations

Operation	CE#	OE#	WE#	A22–0	DQ15–0	RESET#	CLK (See Note)	AVD#
Asynchronous Read - Addresses Latched	L	L	H	Addr In	I/O	H	X	
Asynchronous Read - Addresses Steady State	L	L	H	Addr In	I/O	H	X	L
Asynchronous Write	L	H	L	Addr In	I/O	H	X	L
Synchronous Write	L	H	L	Addr In	I/O	H		
Standby (CE#)	H	X	X	HIGH Z	HIGH Z	H	X	X
Hardware Reset	X	X	X	HIGH Z	HIGH Z	L	X	X
Burst Read Operations								
Load Starting Burst Address	L	X	H	Addr In	X	H		
Advance Burst to next address with appropriate Data presented on the Data Bus	L	L	H	HIGH Z	Burst Data Out	H		H
Terminate current Burst read cycle	H	X	H	HIGH Z	HIGH Z	H		X
Terminate current Burst read cycle via RESET#	X	X	H	HIGH Z	HIGH Z	L	X	X
Terminate current Burst read cycle and start new Burst read cycle	L	X	H	HIGH Z	I/O	H		

Legend: *L = Logic 0, H = Logic 1, X = Don't Care*
Note: *Default active edge of CLK is the rising edge.*

11.1 Requirements for Asynchronous ReadOperation (Non-Burst)

To read data from the memory array, the system must first assert a valid address on Amax–A0(A22-A0 for WS128J and A21-A0 for WS064J), while driving AVD# and CE# to V_{IL}. WE# should remain at V_{IH}. The rising edge of AVD# latches the address. The data will appear on DQ15–DQ0. Since the memory array is divided into four banks, each bank remains enabled for read access until the command register contents are altered.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the outputs. The output enable access time (t_{OE}) is the delay from the falling edge of OE# to valid data at the output.

The internal state machine is set for reading array data in asynchronous mode upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

11.2 Requirements for Synchronous (Burst) Read Operation

The device is capable of continuous sequential burst operation and linear burst operation of a preset length. When the device first powers up, it is enabled for asynchronous read operation.

Prior to entering burst mode, the system should determine how many wait states are desired for the initial word (t_{IACC}) of each burst access, what mode of burst operation is desired, which edge of the clock will be the active clock edge, and how the RDY signal will transition with valid data. The system would then write the configuration register command sequence. See "Set Configuration Register Command Sequence" section on page 63 and "Command Definitions" section on page 63 for further details.

Once the system has written the "Set Configuration Register" command sequence, the device is enabled for synchronous reads only.

The initial word is output t_{IACC} after the active edge of the first CLK cycle. Subsequent words are output t_{BACC} after the active edge of each successive clock cycle, which automatically increments the internal address counter. Note that the device has a fixed internal address boundary that occurs every 64 words, starting at address 00003Fh.

During the time the device is outputting data at this fixed internal address boundary (address 00003Fh, 00007Fh, 0000BFh, etc.), a two cycle latency (66MHz) or a three cycle latency(80MHz) occurs before data appears for the next address (address 000040h, 000080h, 0000C0h, etc.).

Additionally, when the device is read from an odd address, one wait state is inserted when the address pointer crosses the first boundary that occurs every 16 words. For instance, if the device is read from 000011h, 000013h, … ,00001Fh (odd), one wait state is inserted before the data of 000020h is output. This wait is inserted only at the boundary of the first 16 words. Then, if the device is read from the odd address within the last 16 words of 64 word boundary (address 000031h,000033h, … , 00003Fh), a three-cycle latency occurs before data appears for the next address (address 000040h). During the boundary crossing condition, the system must assert an additional wait state for WS128J model numbers 10 and 11.

The RDY output indicates this condition to the system by pulsing deactive (low). See Figure 22.23, "Latency with Boundary Crossing," on page 108.

The device will continue to output sequential burst data, wrapping around to address 000000h after it reaches the highest addressable memory location, until the system drives CE# high, RESET# low, or AVD# low in conjunction with a new address. See Table 11.1, "Device Bus Operations," on page 28.

If the host system crosses the bank boundary while reading in burst mode, and the device is not programming or erasing, a two-cycle latency will occur as described above in the subsequent bank. If the host system crosses the bank boundary while the device is programming or erasing, the device will provide read status information. The clock will be ignored. After the host has completed status reads, or the device has completed the program or erase operation, the host can restart a burst operation using a new address and AVD# pulse.

8-, 16-, and 32-Word Linear Burst with Wrap Around

The remaining three burst read modes are of the linear wrap around design, in which a fixed number of words are read from consecutive addresses. In each of these modes, the burst addresses read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode (see Table 11.2.)

Table 11.2 Burst Address Groups

Mode	Group Size	Group Address Ranges
8-word	8 words	0-7h, 8-Fh, 10-17h,...
16-word	16 words	0-Fh, 10-1Fh, 20-2Fh,...
32-word	32 words	00-1Fh, 20-3Fh, 40-5Fh,...

As an example: if the starting address in the 8-word mode is 39h, the address range to be read would be 38-3Fh, and the burst sequence would be 39-3A-3B-3C-3D-3E-3F-38h-etc. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group. In a similar fashion, the 16-word and 32-word Linear Wrap modes begin their burst sequence on the starting address written to the device, and then wrap back to the first address in the selected address group. **Note that in these three burst read modes the address pointer does not cross the boundary that occurs every 128 or 64 words; thus, no wait states are inserted (except during the initial access).**

The RDY pin indicates when data is valid on the bus.

11.3 Configuration Register

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, active clock edge, RDY configuration, and synchronous mode active.

11.4 Handshaking

The device is equipped with a handshaking feature that allows the host system to simply monitor the RDY signal from the device to determine when the initial word of burst data is ready to be read. The host system should use the programmable wait state configuration to set the number of wait states for optimal burst mode operation. The initial word of burst data is indicated by the active edge of RDY after OE# goes low.

For optimal burst mode performance, the host system must set the appropriate number of wait states in the flash device depending on clock frequency. See "Set Configuration Register Command Sequence" section on page 63 for more information.

11.5 Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in another bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 22.26, "Back-to-Back Read/Write Cycle Timings," on page 111 shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the DC Characteristics table for read-while-program and read-while-erase current specifications.

11.6 Writing Commands/Command Sequences

The device has the capability of performing an asynchronous or synchronous write operation. While the device is configured in Asynchronous read mode, it is able to perform Asynchronous write operations only. CLK is ignored in the Asynchronous programming mode. When in the Synchronous read mode configuration, the device is able to perform both Asynchronous and Synchronous write operations. CLK and WE# address latch is supported in the Synchronous programming mode. During a synchronous write operation, to write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive AVD# and CE# to V_{IL}, and OE# to V_{IH} when providing an address to the device, and drive WE# and CE# to V_{IL}, and OE# to V_{IH}. when writing commands or data. During an asynchronous write operation, the system must drive CE# and WE# to V_{IL} and OE# to V_{IH} when

providing an address, command, and data. Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE#. The asynchronous and synchronous programing operation is independent of the Set Device Read Mode bit in the Configuration Register (see Table 14.4, "Configuration Register," on page 67).

The device features an Unlock Bypass mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 13.5, "WS128J Sector Address Table," on page 49 and Table 13.6, "WS064J Sector Address Table," on page 57 indicate the address space that each sector occupies. The device address space is divided into four banks. A "bank address" is the address bits required to uniquely select a bank. Similarly, a "sector address" is the address bits required to uniquely select a sector.

I_{CC2} in the "DC Characteristics" section on page 89 represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

11.7 Accelerated Program Operation

The device offers accelerated program operations through the ACC function. ACC is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this input, the device automatically enters the aforementioned Unlock Bypass mode and uses the higher voltage on the input to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the ACC input returns the device to normal operation. Note that sectors must be unlocked prior to raising ACC to V_{HH}. *Note that the ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, the ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result*.

When at V_{IL}, ACC locks all sectors. ACC should be at V_{IH} for all other conditions.

11.8 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output from the internal register (which is separate from the memory array) on DQ15–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins must be as shown in Table 11.3, "Autoselect Codes (High Voltage Method)," on page 32. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table , "," on page 33 and Table , "," on page 35). Table 11.3 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15–DQ0. However, the autoselect codes can also be accessed in-system through the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 14.5, "Command Definitions," on page 77. *Note that if a Bank Address (BA) on address bits A22, A21, and A20 for the WS128J (A21:A19 for the WS064J) is asserted during the third write cycle of the autoselect command, the host system can read autoselect data that bank and then immediately read array data from the other bank, without exiting the autoselect mode.*

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 14.5, "Command Definitions," on page 77. This method does not require V_{ID}. Autoselect mode may only be entered and used when in the asynchronous read mode. Refer to the "Autoselect Command Sequence" section on page 68 for more information.

Table II.3 Autoselect Codes (High Voltage Method)

Description		CE#	OE#	WE#	RESET#	Amax to A12	A11 to A10	A9	A8	A7	A6	A5 to A4	A3	A2	A1	A0	DQ15 to DQ0
Manufacturer ID: Spansion		L	L	H	H	X	X	V_{ID}	X	X	L	X	L	L	L	L	0001h
Device ID	Read Cycle 1	L	L	H	H	X	X	V_{ID}	X	L	L	L	L	L	L	H	227Eh
	Read Cycle 2												H	H	H	L	2218h (WS128J) 221Eh (WS064J)
	Read Cycle 3												H	H	H	H	2200h (WS128J) 2201h (WS064J)
Sector Protection Verification		L	L	H	H	SA	X	V_{ID}	X	L	L	L	L	L	H	L	0001h (protected), 0000h (unprotected)
Indicator Bits		L	L	H	H	X	X	V_{ID}	X	X	L	X	L	L	H	H	DQ15 - DQ8 = 0 DQ7 - Factory Lock Bit 1 = Locked, 0 = Not Locked DQ6 -Customer Lock Bit 1 = Locked, 0 = Not Locked DQ5 = Handshake Bit 1 = Reserved, 0 = Standard Handshake DQ4 & DQ3 - Boot Code DQ2 - DQ0 = 001
Hardware Sector Group Protection		L	L	H	H	SA	X	V_{ID}	X	X	X	L	L	L	H	L	0001h (protected), 0000h (unprotected)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, BA = Bank Address, SA = Sector Address, X = Don't care.*

Notes:

1. *The autoselect codes may also be accessed in-system via command sequences.*
2. *PPB Protection Status is shown on the data bus*

II.9 Sector/Sector Block Protection and Unprotection

The hardware sector protection feature disables both programming and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection can be implemented via two methods.

(Note: For the following discussion, the term "sector" applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Table , "," on page 33 and Table , "," on page 35).)

Table 11.4 S29WSI28J/064J Boot Sector/Sector Block Addresses for Protection/Unprotection (Sheet 1 of 3)

Sector	A22–A12	Sector/ Sector Block Size
SA0	00000000000	4 Kwords
SA1	00000000001	4 Kwords
SA2	00000000010	4 Kwords
SA3	00000000011	4 Kwords
SA4	00000000100	4 Kwords
SA5	00000000101	4 Kwords
SA6	00000000110	4 Kwords
SA7	00000000111	4 Kwords
SA8	00000001XXX,	32 Kwords
SA9	00000010XXX,	32 Kwords
SA10	00000011XXX,	32 Kwords
SA11–SA14	000001XXXXX	128 (4x32) Kwords
SA15–SA18	000010XXXXX	128 (4x32) Kwords
SA19–SA22	000011XXXXX	128 (4x32) Kwords
SA23-SA26	000100XXXXX	128 (4x32) Kwords
SA27-SA30	000101XXXXX	128 (4x32) Kwords
SA31-SA34	000110XXXXX	128 (4x32) Kwords
SA35-SA38	000111XXXXX	128 (4x32) Kwords
SA39-SA42	001000XXXXX	128 (4x32) Kwords
SA43-SA46	001001XXXXX	128 (4x32) Kwords
SA47-SA50	001010XXXXX	128 (4x32) Kwords
SA51–SA54	001011XXXXX	128 (4x32) Kwords
SA55–SA58	001100XXXXX	128 (4x32) Kwords
SA59–SA62	001101XXXXX	128 (4x32) Kwords
SA63–SA66	001110XXXXX	128 (4x32) Kwords
SA67–SA70	001111XXXXX	128 (4x32) Kwords
SA71–SA74	010000XXXXX	128 (4x32) Kwords
SA75–SA78	010001XXXXX	128 (4x32) Kwords
SA79–SA82	010010XXXXX	128 (4x32) Kwords
SA83–SA86	010011XXXXX	128 (4x32) Kwords
SA87–SA90	010100XXXXX	128 (4x32) Kwords
SA91–SA94	010101XXXXX	128 (4x32) Kwords
SA95–SA98	010110XXXXX	128 (4x32) Kwords
SA99–SA102	010111XXXXX	128 (4x32) Kwords
SA103–SA106	011000XXXXX	128 (4x32) Kwords
SA107–SA110	011001XXXXX	128 (4x32) Kwords
SA111–SA114	011010XXXXX	128 (4x32) Kwords
SA115–SA118	011011XXXXX	128 (4x32) Kwords
SA119–SA122	011100XXXXX	128 (4x32) Kwords

Table 11.4 S29WS128J/064J Boot Sector/Sector Block Addresses for Protection/Unprotection (Sheet 2 of 3)

Sector	A22–A12	Sector/ Sector Block Size
SA123–SA126	011101XXXXX	128 (4x32) Kwords
SA127–SA130	011110XXXXX	128 (4x32) Kwords
SA131-SA134	011111XXXXX	128 (4x32) Kwords
SA135-SA138	100000XXXXX	128 (4x32) Kwords
SA139-SA142	100001XXXXX	128 (4x32) Kwords
SA143-SA146	100010XXXXX	128 (4x32) Kwords
SA147-SA150	100011XXXXX	128 (4x32) Kwords
SA151–SA154	100100XXXXX	128 (4x32) Kwords
SA155–SA158	100101XXXXX	128 (4x32) Kwords
SA159–SA162	100110XXXXX	128 (4x32) Kwords
SA163–SA166	100111XXXXX	128 (4x32) Kwords
SA167–SA170	101000XXXXX	128 (4x32) Kwords
SA171–SA174	101001XXXXX	128 (4x32) Kwords
SA175–SA178	101010XXXXX	128 (4x32) Kwords
SA179–SA182	101011XXXXX	128 (4x32) Kwords
SA183–SA186	101100XXXXX	128 (4x32) Kwords
SA187–SA190	101101XXXXX	128 (4x32) Kwords
SA191–SA194	101110XXXXX	128 (4x32) Kwords
SA195–SA198	101111XXXXX	128 (4x32) Kwords
SA199–SA202	110000XXXXX	128 (4x32) Kwords
SA203–SA206	110001XXXXX	128 (4x32) Kwords
SA207–SA210	110010XXXXX	128 (4x32) Kwords
SA211–SA214	110011XXXXX	128 (4x32) Kwords
SA215–SA218	110100XXXXX	128 (4x32) Kwords
SA219–SA222	110101XXXXX	128 (4x32) Kwords
SA223–SA226	110110XXXXX	128 (4x32) Kwords
SA227–SA230	110111XXXXX	128 (4x32) Kwords
SA231–SA234	111000XXXXX	128 (4x32) Kwords
SA235–SA238	111001XXXXX	128 (4x32) Kwords
SA239–SA242	111010XXXXX	128 (4x32) Kwords
SA243–SA246	111011XXXXX	128 (4x32) Kwords
SA247–SA250	111100XXXXX	128 (4x32) Kwords
SA251–SA254	111101XXXXX	128 (4x32) Kwords
SA255–SA258	111110XXXXX	128 (4x32) Kwords
SA259	11111100XXX	32 Kwords
SA260	11111101XXX	32 Kwords
SA261	11111110XXX	32 Kwords
SA262	11111111000	4 Kwords
SA263	11111111001	4 Kwords

Table 11.4 S29WSI28J/064J Boot Sector/Sector Block Addresses for Protection/Unprotection (Sheet 3 of 3)

Sector	A22–A12	Sector/ Sector Block Size
SA264	11111111010	4 Kwords
SA265	11111111011	4 Kwords
SA266	11111111100	4 Kwords
SA267	11111111101	4 Kwords
SA268	11111111110	4 Kwords
SA269	11111111111	4 Kwords

Table 11.5 S29WS064J Boot Sector/Sector Block Addresses for Protection/Unprotection (Sheet 1 of 2)

Sector	A21–A12	Sector/ Sector Block Size
SA0	0000000000	4 Kwords
SA1	0000000001	4 Kwords
SA2	0000000010	4 Kwords
SA3	0000000011	4 Kwords
SA4	0000000100	4 Kwords
SA5	0000000101	4 Kwords
SA6	0000000110	4 Kwords
SA7	0000000111	4 Kwords
SA8	0000001XXX	32 Kwords
SA9	0000010XXX	32 Kwords
SA10	0000011XXX	32 Kwords
SA11–SA14	00001XXXXX	128 (4x32) Kwords
SA15–SA18	00010XXXXX	128 (4x32) Kwords
SA19–SA22	00011XXXXX	128 (4x32) Kwords
SA23-SA26	00100XXXXX	128 (4x32) Kwords
SA27-SA30	00101XXXXX	128 (4x32) Kwords
SA31-SA34	00110XXXXX	128 (4x32) Kwords
SA35-SA38	00111XXXXX	128 (4x32) Kwords
SA39-SA42	01000XXXXX	128 (4x32) Kwords
SA43-SA46	01001XXXXX	128 (4x32) Kwords
SA47-SA50	01010XXXXX	128 (4x32) Kwords
SA51–SA54	01011XXXXX	128 (4x32) Kwords
SA55–SA58	01100XXXXX	128 (4x32) Kwords
SA59–SA62	01101XXXXX	128 (4x32) Kwords
SA63–SA66	01110XXXXX	128 (4x32) Kwords
SA67–SA70	01111XXXXX	128 (4x32) Kwords
SA71–SA74	10000XXXXX	128 (4x32) Kwords
SA75–SA78	10001XXXXX	128 (4x32) Kwords
SA79–SA82	10010XXXXX	128 (4x32) Kwords

Table II.5 S29WS064J Boot Sector/Sector Block Addresses for Protection/Unprotection (Sheet 2 of 2)

Sector	A21–A12	Sector/ Sector Block Size
SA83–SA86	10011XXXXX	128 (4x32) Kwords
SA87–SA90	10100XXXXX	128 (4x32) Kwords
SA91–SA94	10101XXXXX	128 (4x32) Kwords
SA95–SA98	10110XXXXX	128 (4x32) Kwords
SA99–SA102	10111XXXXX	128 (4x32) Kwords
SA103–SA106	11000XXXXX	128 (4x32) Kwords
SA107–SA110	11001XXXXX	128 (4x32) Kwords
SA111–SA114	11010XXXXX	128 (4x32) Kwords
SA115–SA118	11011XXXXX	128 (4x32) Kwords
SA119–SA122	11100XXXXX	128 (4x32) Kwords
SA123–SA126	11101XXXXX	128 (4x32) Kwords
SA127–SA130	11110XXXXX	128 (4x32) Kwords
SA131	1111100XXX	32 Kwords
SA132	1111101XXX	32 Kwords
SA133	1111110XXX	32 Kwords
SA134	1111111000	4 Kwords
SA135	1111111001	4 Kwords
SA136	1111111010	4 Kwords
SA137	1111111011	4 Kwords
SA138	1111111100	4 Kwords
SA139	1111111101	4 Kwords
SA140	1111111110	4 Kwords
SA141	1111111111	4 Kwords

I2 Advanced Sector Protection/Unprotection

The Advanced Sector Protection/Unprotection feature disables or enables programming or erase operations in any or all sectors and can be implemented through software and/or hardware methods, which are independent of each other. This section describes the various methods of protecting data stored in the memory array. An overview of these methods in shown in Figure 12.1.

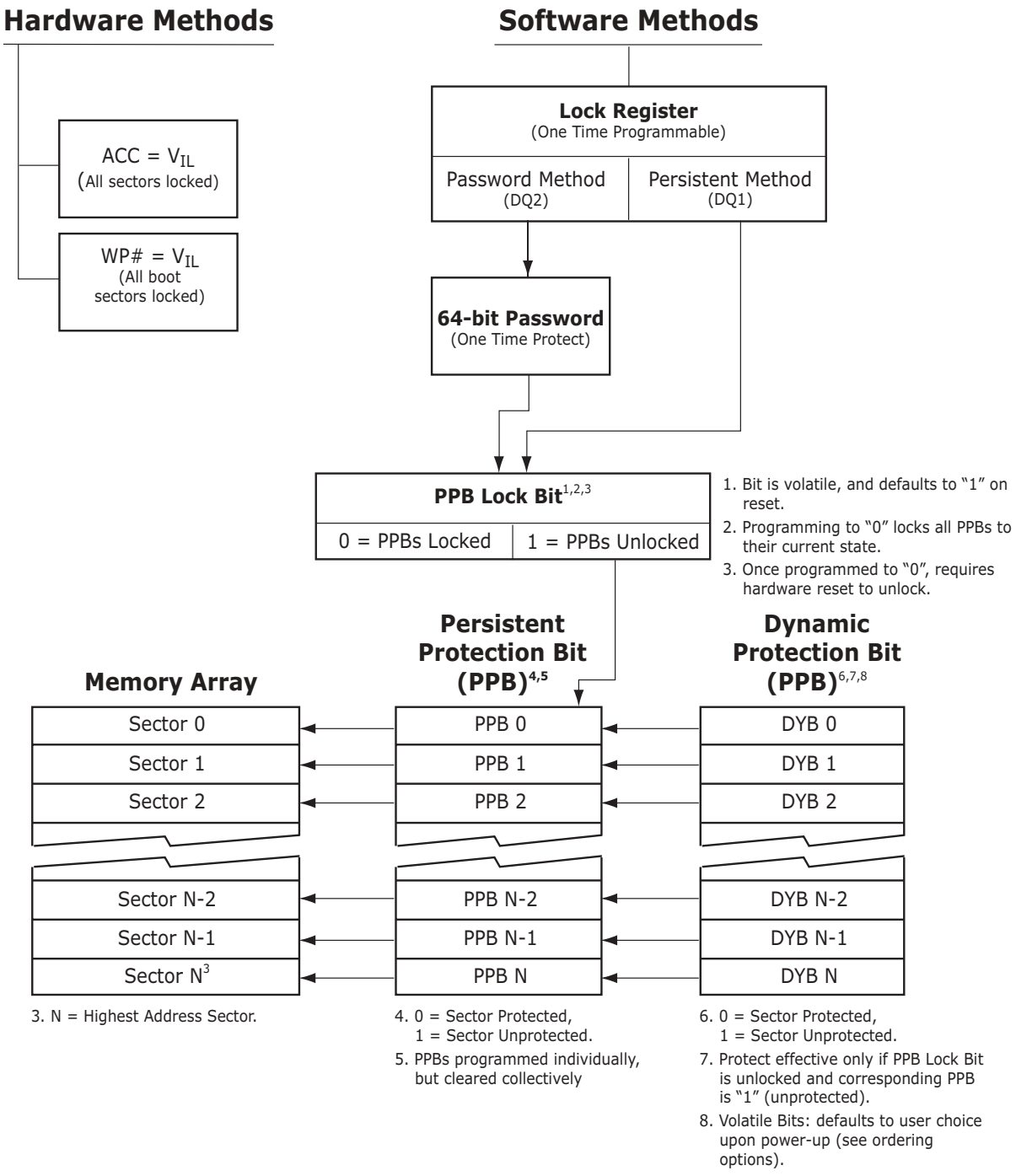


Figure I2.1 Advanced Sector Protection/Unprotection

12.1 Lock Register

As shipped from the factory, all devices default to the persistent mode when power is applied, and all sectors are unprotected, unless otherwise chosen through the DYB ordering option. The device programmer or host system must then choose which sector protection method to use. Programming (setting to "0") any one of the following two one-time programmable, non-volatile bits locks the part permanently in that mode:

- Lock Register Persistent Protection Mode Lock Bit (DQ1)
- Lock Register Password Protection Mode Lock Bit (DQ2)

Table 12.1 Lock Register

Device	DQ15-05	DQ4	DQ3	DQ2	DQ1	DQ0
S29WS256N	1	1	1	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	Customer SecSi Sector Protection Bit
S29WS128N/ S29WS064N	Undefined	DYB Lock Boot Bit 0 = sectors power up protected 1 = sectors power up unprotected	PPB One-Time Programmable Bit 0 = All PPB erase command disabled 1 = All PPB Erase command enabled	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	SecSi Sector Protection Bit

Notes

1. If the password mode is chosen, the password must be programmed before setting the corresponding lock register bit.
2. After the Lock Register Bits Command Set Entry command sequence is written, reads and writes for Bank 0 are disabled, while reads from other banks are allowed until exiting this mode.
3. If both lock bits are selected to be programmed (to zeros) at the same time, the operation aborts.
4. Once the Password Mode Lock Bit is programmed, the Persistent Mode Lock Bit is permanently disabled, and no changes to the protection scheme are allowed. Similarly, if the Persistent Mode Lock Bit is programmed, the Password Mode is permanently disabled.

After selecting a sector protection method, each sector can operate in any of the following three states:

1. *Constantly locked.* The selected sectors are protected and can not be reprogrammed unless PPB lock bit is cleared via a password, hardware reset, or power cycle.
2. *Dynamically locked.* The selected sectors are protected and can be altered via software commands.
3. *Unlocked.* The sectors are unprotected and can be erased and/or programmed.

These states are controlled by the bit types described in Sections 12.2–12.6.

12.2 Persistent Protection Bits

The Persistent Protection Bits are unique and nonvolatile for each sector and have the same endurances as the Flash memory. Preprogramming and verification prior to erasure are handled by the device, and therefore do not require system monitoring.

Notes

1. Each PPB is individually programmed and all are erased in parallel.
2. While programming PPB for a sector, array data can be read from any other bank, except Bank 0 (used for Data# Polling) and the bank in which sector PPB is being programmed.
3. Entry command disables reads and writes for the bank selected.
4. Reads within that bank return the PPB status for that sector.
5. Reads from other banks are allowed while writes are not allowed.
6. All Reads must be performed using the Asynchronous mode.
7. The specific sector address (A23-A14 WS256N, A22-A14 WS128N, A21-A14 WS064N) are written at the same time as the program command.
8. If the PPB Lock Bit is set, the PPB Program or erase command does not execute and times-out without programming or erasing the PPB.
9. There are no means for individually erasing a specific PPB and no specific sector address is required for this operation.
10. Exit command must be issued after the execution which resets the device to read mode and re-enables reads and writes for Bank 0
11. The programming state of the PPB for a given sector can be verified by writing a PPB Status Read Command to the device as described by the flow chart shown in Figure 12.2.

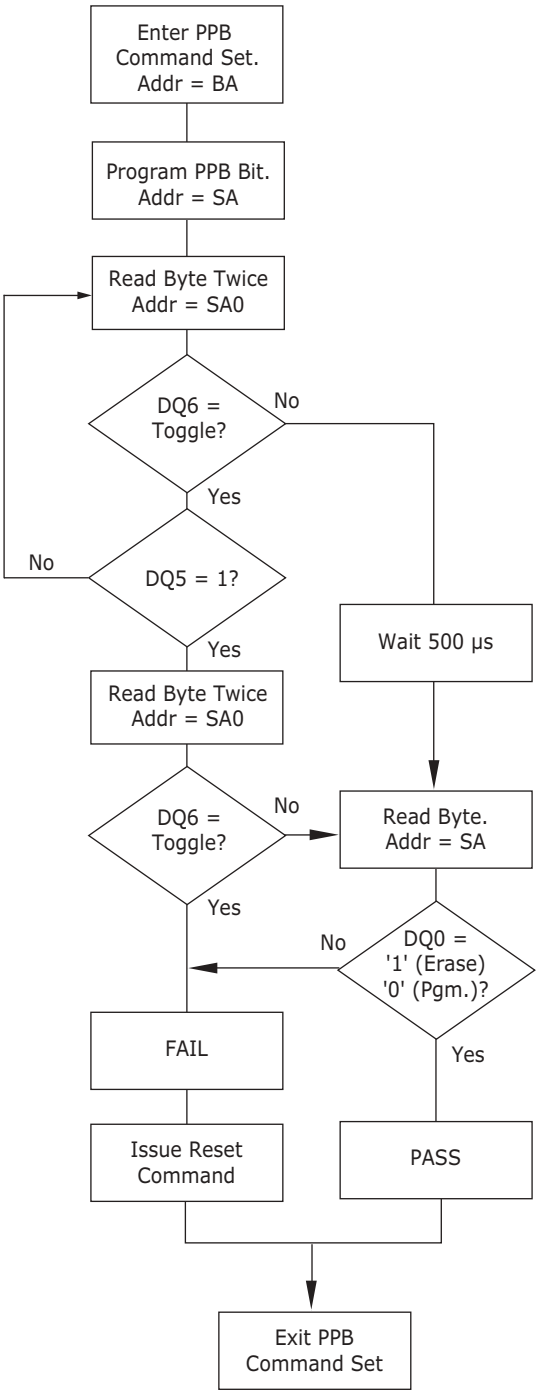


Figure I2.2 PPB Program/Erase Algorithm

12.3 Dynamic Protection Bits

Dynamic Protection Bits are volatile and unique for each sector and can be individually modified. DYBs only control the protection scheme for unprotected sectors that have their PPBs cleared (erased to "1"). By issuing the DYB Set or Clear command sequences, the DYBs are set (programmed to "0") or cleared (erased to "1"), thus placing each sector in the protected or unprotected state respectively. This feature allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed.

Notes

1. The DYBs can be set (programmed to "0") or cleared (erased to "1") as often as needed.

When the parts are first shipped, the PPBs are cleared (erased to "1") and upon power up or reset, the DYBs can be set or cleared depending upon the ordering option chosen.

2. If the option to clear the DYBs after power up is chosen, (erased to "1"), then the sectorsmay be modified depending upon the PPB state of that sector (see Table 12.2).
3. The sectors would be in the protected state If the option to set the DYBs after power up is chosen (programmed to "0").
4. It is possible to have sectors that are persistently locked with sectors that are left in the dynamic state.
5. The DYB Set or Clear commands for the dynamic sectors signify protected or unprotected state of the sectors respectively. However, if there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock Bit must be cleared by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB Lock Bit once again locks the PPBs, and the device operates normally again.
6. To achieve the best protection, it is recommended to execute the PPB Lock Bit Set command early in the boot code and protect the boot code by holding WP# = V_{IL}. Note that the PPB and DYB bits have the same function when ACC = V_{HH} as they do when ACC =V_{IH}.

12.4 Persistent Protection Bit Lock Bit

The Persistent Protection Bit Lock Bit is a global volatile bit for all sectors. When set (programmed to "0"), it locks all PPBs and when cleared (programmed to "1"), allows the PPBs to be changed. There is only one PPB Lock Bit per device.

Notes

1. No software command sequence unlocks this bit unless the device is in the password protection mode; only a hardware reset or a power-up clears this bit.
2. The PPB Lock Bit must be set (programmed to "0") only after all PPBs are configured to the desired settings.

I2.5 Password Protection Method

The Password Protection Method allows an even higher level of security than the Persistent Sector Protection Mode by requiring a 64 bit password for unlocking the device PPB Lock Bit. In addition to this password requirement, after power up and reset, the PPB Lock Bit is set "0" to maintain the password mode of operation. Successful execution of the Password Unlock command by entering the entire password clears the PPB Lock Bit, allowing for sector PPBs modifications.

Notes

1. There is no special addressing order required for programming the password. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent access.
2. The Password Program Command is only capable of programming "0"s. Programming a "1" after a cell is programmed as a "0" results in a time-out with the cell as a "0".
3. The password is all "1"s when shipped from the factory.
4. All 64-bit password combinations are valid as a password.
5. There is no means to verify what the password is after it is set.
6. The Password Mode Lock Bit, once set, prevents reading the 64-bit password on the data bus and further password programming.
7. The Password Mode Lock Bit is not erasable.
8. The lower two address bits (A1–A0) are valid during the Password Read, Password Program, and Password Unlock.
9. The exact password must be entered in order for the unlocking function to occur.
10. The Password Unlock command cannot be issued any faster than 1 µs at a time to prevent a hacker from running through all the 64-bit combinations in an attempt to correctly match a password.
11. Approximately 1 µs is required for unlocking the device after the valid 64-bit password is given to the device.
12. Password verification is only allowed during the password programming operation.
13. All further commands to the password region are disabled and all operations are ignored.
14. If the password is lost after setting the Password Mode Lock Bit, there is no way to clear the PPB Lock Bit.
15. Entry command sequence must be issued prior to any of any operation and it disables reads and writes for Bank 0. Reads and writes for other banks excluding Bank 0 are allowed.
16. If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode.
17. A program or erase command to a protected sector enables status polling and returns to read mode without having modified the contents of the protected sector.
18. The programming of the DYB, PPB, and PPB Lock for a given sector can be verified by writing individual status read commands DYB Status, PPB Status, and PPB Lock Status to the device.

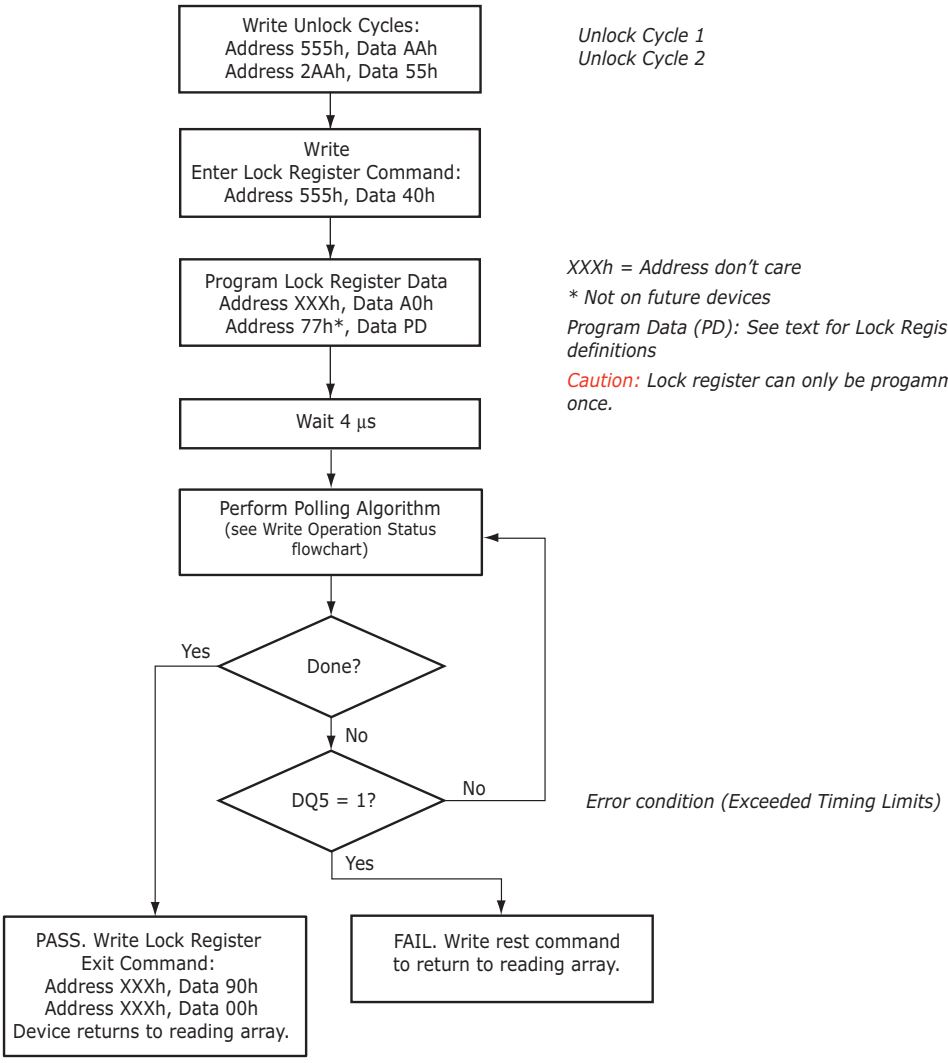


Figure I2.3 Lock Register Program Algorithm

I2.6 Advanced Sector Protection Software Examples

Table I2.2 Sector Protection Schemes

Unique Device PPB Lock Bit 0 = locked I = unlocked		Sector PPB 0 = protected I = unprotected	Sector DYB 0 = protected I = unprotected	Sector Protection Status
Any Sector	0	0	x	Protected through PPB
Any Sector	0	0	x	Protected through PPB
Any Sector	0	1	1	Unprotected
Any Sector	0	1	0	Protected through DYB
Any Sector	1	0	x	Protected through PPB
Any Sector	1	0	x	Protected through PPB
Any Sector	1	1	0	Protected through DYB
Any Sector	1	1	1	Unprotected

Table 12.2 contains all possible combinations of the DYB, PPB, and PPB Lock Bit relating to the status of the sector. In summary, if the PPB Lock Bit is locked (set to "0"), no changes to the PPBs are allowed. The PPB Lock Bit can only be unlocked (reset to "1") through a hardware reset or power cycle. See also Figure 12.1 for an overview of the Advanced Sector Protection feature.

I2.7 Hardware Data Protection Methods

The device offers two main types of data protection at the sector level via hardware control:

- When WP# is at V_{IL}, the four outermost sectors are locked (device specific).
- When ACC is at V_{IL}, all sectors are locked.

There are additional methods by which intended or accidental erasure of any sectors can be prevented via hardware means. The following subsections describes these methods:

WP# Method

The Write Protect feature provides a hardware method of protecting the four outermost sectors. This function is provided by the WP# pin and overrides the previously discussed Sector Protection/Unprotection method.

If the system asserts V_{IL} on the WP# pin, the device disables program and erase functions in the "outermost" boot sectors. The outermost boot sectors are the sectors containing both the lower and upper set of sectors in a dual-boot-configured device.

If the system asserts V_{IH} on the WP# pin, the device reverts to whether the boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected.

Note that the WP# pin must not be left floating or unconnected as inconsistent behavior of the device may result.

The WP# pin must be held stable during a command sequence execution

ACC Method

This method is similar to above, except it protects all sectors. Once ACC input is set to V_{IL}, all program and erase functions are disabled and hence all sectors are protected.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down.

The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch Protection"

Noise pulses of less than 3 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Power-Up Write Inhibit

If WE# = CE# = RESET# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

13 Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 13.1-13.4. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 13.1-13.4. The system must write the reset command to return the device to the autoselect mode.

Table 13.1 CFI Query Identification String

Addresses	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string "QRY"
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table I3.2 System Interface String

Addresses	Data	Description
1Bh	0017h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0019h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0003h	Typical timeout per single byte/word write 2^N µs
20h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	0009h	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0004h	Max. timeout for byte/word write 2^N times typical
24h	0000h	Max. timeout for buffer write 2^N times typical
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table I3.3 Device Geometry Definition

Addresses	Data	Description
27h	0018h (WS128J) 0017h (WS064J)	Device Size = 2^N byte
28h 29h	0001h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0000h 0000h	Max. number of bytes in multi-byte write = 2^N (00h = not supported)
2Ch	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h	00FDh (WS128J) 007Dh (WS064J)	Erase Block Region 2 Information
32h 33h 34h	0000h 0000h 0001h	
35h 36h 37h 38h	0007h 0000h 0020h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information

Table I3.4 Primary Vendor-Specific Extended Query

Addresses	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string "PRI"
43h	0031h	Major version number, ASCII
44h	0033h	Minor version number, ASCII
45h	000Ch	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Technology (Bits 5-2) 0011 = 0.13 µm
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0007h	Sector Protect/Unprotect scheme 07 = Advanced Sector Protection
4Ah	00E7h (WS128J) 0077h (WS064J)	Simultaneous Operation Number of Sectors in all banks except boot block
4Bh	0001h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page, 04 = 16 Word Page
4Dh	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0001h	Top/Bottom Boot Sector Flag 01h = Dual Boot Device, 02h = Bottom Boot Device, 03h = Top Boot Device
50h	0000h	Program Suspend. 00h = not supported
57h	0004h	Bank Organization: X = Number of banks
58h	0027h (WS128J) 0017h (WS064J)	Bank A Region Information. X = Number of sectors in bank
59h	0060h (WS128J) 0030h (WS064J)	Bank B Region Information. X = Number of sectors in bank
5Ah	0060h (WS128J) 0030h (WS064J)	Bank C Region Information. X = Number of sectors in bank
5Bh	0027h (WS128J) 0017h (WS064J)	Bank D Region Information. X = Number of sectors in bank

Table I3.5 WSI28J Sector Address Table (Sheet I of 8)

Bank	Sector	Sector Size	(x16) Address Range
Bank D	SA0	4 Kwords	000000h-000FFFh
	SA1	4 Kwords	001000h-001FFFh
	SA2	4 Kwords	002000h-002FFFh
	SA3	4 Kwords	003000h-003FFFh
	SA4	4 Kwords	004000h-004FFFh
	SA5	4 Kwords	005000h-005FFFh
	SA6	4 Kwords	006000h-006FFFh
	SA7	4 Kwords	007000h-007FFFh
	SA8	32 Kwords	008000h-00FFFFh
	SA9	32 Kwords	010000h-017FFFh
	SA10	32 Kwords	018000h-01FFFFh
	SA11	32 Kwords	020000h-027FFFh
	SA12	32 Kwords	028000h-02FFFFh
	SA13	32 Kwords	030000h-037FFFh
	SA14	32 Kwords	038000h-03FFFFh
	SA15	32 Kwords	040000h-047FFFh
	SA16	32 Kwords	048000h-04FFFFh
	SA17	32 Kwords	050000h-057FFFh
	SA18	32 Kwords	058000h-05FFFFh
	SA19	32 Kwords	060000h-067FFFh
	SA20	32 Kwords	068000h-06FFFFh
	SA21	32 Kwords	070000h-077FFFh
	SA22	32 Kwords	078000h-07FFFFh
	SA23	32 Kwords	080000h-087FFFh
	SA24	32 Kwords	088000h-08FFFFh
	SA25	32 Kwords	090000h-097FFFh
	SA26	32 Kwords	098000h-09FFFFh
	SA27	32 Kwords	0A0000h-0A7FFFh
	SA28	32 Kwords	0A8000h-0AFFFFh
	SA29	32 Kwords	0B0000h-0B7FFFh
	SA30	32 Kwords	0B8000h-0BFFFFh
	SA31	32 Kwords	0C0000h-0C7FFFh
	SA32	32 Kwords	0C8000h-0CFFFFh
	SA33	32 Kwords	0D0000h-0D7FFFh
	SA34	32 Kwords	0D8000h-0DFFFFh
	SA35	32 Kwords	0E0000h-0E7FFFh
	SA36	32 Kwords	0E8000h-0EFFFFh
	SA37	32 Kwords	0F0000h-0F7FFFh
	SA38	32 Kwords	0F8000h-0FFFFFh

Table I3.5 WSI28J Sector Address Table (Sheet 2 of 8)

Bank	Sector	Sector Size	(x16) Address Range
Bank C	SA39	32 Kwords	100000h-107FFFh
	SA40	32 Kwords	108000h-10FFFFh
	SA41	32 Kwords	110000h-117FFFh
	SA42	32 Kwords	118000h-11FFFFh
	SA43	32 Kwords	120000h-127FFFh
	SA44	32 Kwords	128000h-12FFFFh
	SA45	32 Kwords	130000h-137FFFh
	SA46	32 Kwords	138000h-13FFFFh
	SA47	32 Kwords	140000h-147FFFh
	SA48	32 Kwords	148000h-14FFFFh
	SA49	32 Kwords	150000h-157FFFh
	SA50	32 Kwords	158000h-15FFFFh
	SA51	32 Kwords	160000h-167FFFh
	SA52	32 Kwords	168000h-16FFFFh
	SA53	32 Kwords	170000h-177FFFh
	SA54	32 Kwords	178000h-17FFFFh
	SA55	32 Kwords	180000h-187FFFh
	SA56	32 Kwords	188000h-18FFFFh
	SA57	32 Kwords	190000h-197FFFh
	SA58	32 Kwords	198000h-19FFFFh
	SA59	32 Kwords	1A0000h-1A7FFFh
	SA60	32 Kwords	1A8000h-1AFFFFh
	SA61	32 Kwords	1B0000h-1B7FFFh
	SA62	32 Kwords	1B8000h-1BFFFFh
	SA63	32 Kwords	1C0000h-1C7FFFh
	SA64	32 Kwords	1C8000h-1CFFFFh
	SA65	32 Kwords	1D0000h-1D7FFFh
	SA66	32 Kwords	1D8000h-1DFFFFh
	SA67	32 Kwords	1E0000h-1E7FFFh
	SA68	32 Kwords	1E8000h-1EFFFFh
	SA69	32 Kwords	1F0000h-1F7FFFh
	SA70	32 Kwords	1F8000h-1FFFFFh

Table 13.5 WSI28J Sector Address Table (Sheet 3 of 8)

Bank	Sector	Sector Size	(x16) Address Range
Bank C	SA71	32 Kwords	200000h-207FFFh
	SA72	32 Kwords	208000h-20FFFFh
	SA73	32 Kwords	210000h-217FFFh
	SA74	32 Kwords	218000h-21FFFFh
	SA75	32 Kwords	220000h-227FFFh
	SA76	32 Kwords	228000h-22FFFFh
	SA77	32 Kwords	230000h-237FFFh
	SA78	32 Kwords	238000h-23FFFFh
	SA79	32 Kwords	240000h-247FFFh
	SA80	32 Kwords	248000h-24FFFFh
	SA81	32 Kwords	250000h-257FFFh
	SA82	32 Kwords	258000h-25FFFFh
	SA83	32 Kwords	260000h-267FFFh
	SA84	32 Kwords	268000h-26FFFFh
	SA85	32 Kwords	270000h-277FFFh
	SA86	32 Kwords	278000h-27FFFFh
	SA87	32 Kwords	280000h-287FFFh
	SA88	32 Kwords	288000h-28FFFFh
	SA89	32 Kwords	290000h-297FFFh
	SA90	32 Kwords	298000h-29FFFFh
	SA91	32 Kwords	2A0000h-2A7FFFh
	SA92	32 Kwords	2A8000h-2AFFFFh
	SA93	32 Kwords	2B0000h-2B7FFFh
	SA94	32 Kwords	2B8000h-2BFFFFh
	SA95	32 Kwords	2C0000h-2C7FFFh
	SA96	32 Kwords	2C8000h-2CFFFFh
	SA97	32 Kwords	2D0000h-2D7FFFh
	SA98	32 Kwords	2D8000h-2DFFFFh
	SA99	32 Kwords	2E0000h-2E7FFFh
	SA100	32 Kwords	2E8000h-2EFFFFh
	SA101	32 Kwords	2F0000h-2F7FFFh
	SA102	32 Kwords	2F8000h-2FFFFFh

Table I3.5 WSI28J Sector Address Table (Sheet 4 of 8)

Bank	Sector	Sector Size	(x16) Address Range
Bank C	SA103	32 Kwords	300000h-307FFFh
	SA104	32 Kwords	308000h-30FFFFh
	SA105	32 Kwords	310000h-317FFFh
	SA106	32 Kwords	318000h-31FFFFh
	SA107	32 Kwords	320000h-327FFFh
	SA108	32 Kwords	328000h-32FFFFh
	SA109	32 Kwords	330000h-337FFFh
	SA110	32 Kwords	338000h-33FFFFh
	SA111	32 Kwords	340000h-347FFFh
	SA112	32 Kwords	348000h-34FFFFh
	SA113	32 Kwords	350000h-357FFFh
	SA114	32 Kwords	358000h-35FFFFh
	SA115	32 Kwords	360000h-367FFFh
	SA116	32 Kwords	368000h-36FFFFh
	SA117	32 Kwords	370000h-377FFFh
	SA118	32 Kwords	378000h-37FFFFh
	SA119	32 Kwords	380000h-387FFFh
	SA120	32 Kwords	388000h-38FFFFh
	SA121	32 Kwords	390000h-397FFFh
	SA122	32 Kwords	398000h-39FFFFh
	SA123	32 Kwords	3A0000h-3A7FFFh
	SA124	32 Kwords	3A8000h-3AFFFFh
	SA125	32 Kwords	3B0000h-3B7FFFh
	SA126	32 Kwords	3B8000h-3BFFFFh
	SA127	32 Kwords	3C0000h-3C7FFFh
	SA128	32 Kwords	3C8000h-3CFFFFh
	SA129	32 Kwords	3D0000h-3D7FFFh
	SA130	32 Kwords	3D8000h-3DFFFFh
	SA131	32 Kwords	3E0000h-3E7FFFh
	SA132	32 Kwords	3E8000h-3EFFFFh
	SA133	32 Kwords	3F0000h-3F7FFFh
	SA134	32 Kwords	3F8000h-3FFFFFh

Table I3.5 WSI28J Sector Address Table (Sheet 5 of 8)

Bank	Sector	Sector Size	(x16) Address Range
Bank B	SA135	32 Kwords	400000h-407FFFh
	SA136	32 Kwords	408000h-40FFFFh
	SA137	32 Kwords	410000h-417FFFh
	SA138	32 Kwords	418000h-41FFFFh
	SA139	32 Kwords	420000h-427FFFh
	SA140	32 Kwords	428000h-42FFFFh
	SA141	32 Kwords	430000h-437FFFh
	SA142	32 Kwords	438000h-43FFFFh
	SA143	32 Kwords	440000h-447FFFh
	SA144	32 Kwords	448000h-44FFFFh
	SA145	32 Kwords	450000h-457FFFh
	SA146	32 Kwords	458000h-45FFFFh
	SA147	32 Kwords	460000h-467FFFh
	SA148	32 Kwords	468000h-46FFFFh
	SA149	32 Kwords	470000h-477FFFh
	SA150	32 Kwords	478000h-47FFFFh
	SA151	32 Kwords	480000h-487FFFh
	SA152	32 Kwords	488000h-48FFFFh
	SA153	32 Kwords	490000h-497FFFh
	SA154	32 Kwords	498000h-49FFFFh
	SA155	32 Kwords	4A0000h-4A7FFFh
	SA156	32 Kwords	4A8000h-4AFFFFh
	SA157	32 Kwords	4B0000h-4B7FFFh
	SA158	32 Kwords	4B8000h-4BFFFFh
	SA159	32 Kwords	4C0000h-4C7FFFh
	SA160	32 Kwords	4C8000h-4CFFFFh
	SA161	32 Kwords	4D0000h-4D7FFFh
	SA162	32 Kwords	4D8000h-4DFFFFh
	SA163	32 Kwords	4E0000h-4E7FFFh
	SA164	32 Kwords	4E8000h-4EFFFFh
	SA165	32 Kwords	4F0000h-4F7FFFh
	SA166	32 Kwords	4F8000h-4FFFFFh

Table 13.5 WSI28J Sector Address Table (Sheet 6 of 8)

Bank	Sector	Sector Size	(x16) Address Range
Bank B	SA167	32 Kwords	500000h-507FFFh
	SA168	32 Kwords	508000h-50FFFFh
	SA169	32 Kwords	510000h-517FFFh
	SA170	32 Kwords	518000h-51FFFFh
	SA171	32 Kwords	520000h-527FFFh
	SA172	32 Kwords	528000h-52FFFFh
	SA173	32 Kwords	530000h-537FFFh
	SA174	32 Kwords	538000h-53FFFFh
	SA175	32 Kwords	540000h-547FFFh
	SA176	32 Kwords	548000h-54FFFFh
	SA177	32 Kwords	550000h-557FFFh
	SA178	32 Kwords	558000h-55FFFFh
	SA179	32 Kwords	560000h-567FFFh
	SA180	32 Kwords	568000h-56FFFFh
	SA181	32 Kwords	570000h-577FFFh
	SA182	32 Kwords	578000h-57FFFFh
	SA183	32 Kwords	580000h-587FFFh
	SA184	32 Kwords	588000h-58FFFFh
	SA185	32 Kwords	590000h-597FFFh
	SA186	32 Kwords	598000h-59FFFFh
	SA187	32 Kwords	5A0000h-5A7FFFh
	SA188	32 Kwords	5A8000h-5AFFFFh
	SA189	32 Kwords	5B0000h-5B7FFFh
	SA190	32 Kwords	5B8000h-5BFFFFh
	SA191	32 Kwords	5C0000h-5C7FFFh
	SA192	32 Kwords	5C8000h-5CFFFFh
	SA193	32 Kwords	5D0000h-5D7FFFh
	SA194	32 Kwords	5D8000h-5DFFFFh
	SA195	32 Kwords	5E0000h-5E7FFFh
	SA196	32 Kwords	5E8000h-5EFFFFh
	SA197	32 Kwords	5F0000h-5F7FFFh
	SA198	32 Kwords	5F8000h-5FFFFFh

Table 13.5 WSI28J Sector Address Table (Sheet 7 of 8)

Bank	Sector	Sector Size	(x16) Address Range
Bank B	SA199	32 Kwords	600000h-607FFFh
	SA200	32 Kwords	608000h-60FFFFh
	SA201	32 Kwords	610000h-617FFFh
	SA202	32 Kwords	618000h-61FFFFh
	SA203	32 Kwords	620000h-627FFFh
	SA204	32 Kwords	628000h-62FFFFh
	SA205	32 Kwords	630000h-637FFFh
	SA206	32 Kwords	638000h-63FFFFh
	SA207	32 Kwords	640000h-647FFFh
	SA208	32 Kwords	648000h-64FFFFh
	SA209	32 Kwords	650000h-657FFFh
	SA210	32 Kwords	658000h-65FFFFh
	SA211	32 Kwords	660000h-667FFFh
	SA212	32 Kwords	668000h-66FFFFh
	SA213	32 Kwords	670000h-677FFFh
	SA214	32 Kwords	678000h-67FFFFh
	SA215	32 Kwords	680000h-687FFFh
	SA216	32 Kwords	688000h-68FFFFh
	SA217	32 Kwords	690000h-697FFFh
	SA218	32 Kwords	698000h-69FFFFh
	SA219	32 Kwords	6A0000h-6A7FFFh
	SA220	32 Kwords	6A8000h-6AFFFFh
	SA221	32 Kwords	6B0000h-6B7FFFh
	SA222	32 Kwords	6B8000h-6BFFFFh
	SA223	32 Kwords	6C0000h-6C7FFFh
	SA224	32 Kwords	6C8000h-6CFFFFh
	SA225	32 Kwords	6D0000h-6D7FFFh
	SA226	32 Kwords	6D8000h-6DFFFFh
	SA227	32 Kwords	6E0000h-6E7FFFh
	SA228	32 Kwords	6E8000h-6EFFFFh
	SA229	32 Kwords	6F0000h-6F7FFFh
	SA230	32 Kwords	6F8000h-6FFFFFh

Table 13.5 WSI28J Sector Address Table (Sheet 8 of 8)

Bank	Sector	Sector Size	(x16) Address Range
Bank A	SA231	32 Kwords	700000h-707FFFh
	SA232	32 Kwords	708000h-70FFFFh
	SA233	32 Kwords	710000h-717FFFh
	SA234	32 Kwords	718000h-71FFFFh
	SA235	32 Kwords	720000h-727FFFh
	SA236	32 Kwords	728000h-72FFFFh
	SA237	32 Kwords	730000h-737FFFh
	SA238	32 Kwords	738000h-73FFFFh
	SA239	32 Kwords	740000h-747FFFh
	SA240	32 Kwords	748000h-74FFFFh
	SA241	32 Kwords	750000h-757FFFh
	SA242	32 Kwords	758000h-75FFFFh
	SA243	32 Kwords	760000h-767FFFh
	SA244	32 Kwords	768000h-76FFFFh
	SA245	32 Kwords	770000h-777FFFh
	SA246	32 Kwords	778000h-77FFFFh
	SA247	32 Kwords	780000h-787FFFh
	SA248	32 Kwords	788000h-78FFFFh
	SA249	32 Kwords	790000h-797FFFh
	SA250	32 Kwords	798000h-79FFFFh
	SA251	32 Kwords	7A0000h-7A7FFFh
	SA252	32 Kwords	7A8000h-7AFFFFh
	SA253	32 Kwords	7B0000h-7B7FFFh
	SA254	32 Kwords	7B8000h-7BFFFFh
	SA255	32 Kwords	7C0000h-7C7FFFh
	SA256	32 Kwords	7C8000h-7CFFFFh
	SA257	32 Kwords	7D0000h-7D7FFFh
	SA258	32 Kwords	7D8000h-7DFFFFh
	SA259	32 Kwords	7E0000h-7E7FFFh
	SA260	32 Kwords	7E8000h-7EFFFFh
	SA261	32 Kwords	7F0000h-7F7FFFh
	SA262	4 Kwords	7F8000h-7F8FFFh
	SA263	4 Kwords	7F9000h-7F9FFFh
	SA264	4 Kwords	7FA000h-7FAFFFh
	SA265	4 Kwords	7FB000h-7FBFFFh
	SA266	4 Kwords	7FC000h-7FCFFFh
	SA267	4 Kwords	7FD000h-7FDFFFh
	SA268	4 Kwords	7FE000h-7FEFFFh
	SA269	4 Kwords	7FF000h-7FFFFFh

Table I3.6 WS064J Sector Address Table (Sheet I of 6)

Bank	Sector	Sector Size	(x16) Address Range
Bank D	SA0	4 Kwords	000000h-000FFFh
	SA1	4 Kwords	001000h-001FFFh
	SA2	4 Kwords	002000h-002FFFh
	SA3	4 Kwords	003000h-003FFFh
	SA4	4 Kwords	004000h-004FFFh
	SA5	4 Kwords	005000h-005FFFh
	SA6	4 Kwords	006000h-006FFFh
	SA7	4 Kwords	007000h-007FFFh
	SA8	32 Kwords	008000h-00FFFFh
	SA9	32 Kwords	010000h-017FFFh
	SA10	32 Kwords	018000h-01FFFFh
	SA11	32 Kwords	020000h-027FFFh
	SA12	32 Kwords	028000h-02FFFFh
	SA13	32 Kwords	030000h-037FFFh
	SA14	32 Kwords	038000h-03FFFFh
	SA15	32 Kwords	040000h-047FFFh
	SA16	32 Kwords	048000h-04FFFFh
	SA17	32 Kwords	050000h-057FFFh
	SA18	32 Kwords	058000h-05FFFFh
	SA19	32 Kwords	060000h-067FFFh
	SA20	32 Kwords	068000h-06FFFFh
	SA21	32 Kwords	070000h-077FFFh
	SA22	32 Kwords	078000h-07FFFFh

Table I3.6 WS064J Sector Address Table (Sheet 2 of 6)

Bank	Sector	Sector Size	(x16) Address Range
Bank C	SA23	32 Kwords	080000h-087FFFh
	SA24	32 Kwords	088000h-08FFFFh
	SA25	32 Kwords	090000h-097FFFh
	SA26	32 Kwords	098000h-09FFFFh
	SA27	32 Kwords	0A0000h-0A7FFFh
	SA28	32 Kwords	0A8000h-0AFFFFh
	SA29	32 Kwords	0B0000h-0B7FFFh
	SA30	32 Kwords	0B8000h-0BFFFFh
	SA31	32 Kwords	0C0000h-0C7FFFh
	SA32	32 Kwords	0C8000h-0CFFFFh
	SA33	32 Kwords	0D0000h-0D7FFFh
	SA34	32 Kwords	0D8000h-0DFFFFh
	SA35	32 Kwords	0E0000h-0E7FFFh
	SA36	32 Kwords	0E8000h-0EFFFFh
	SA37	32 Kwords	0F0000h-0F7FFFh
	SA38	32 Kwords	0F8000h-0FFFFFh
	SA39	32 Kwords	100000h-107FFFh
	SA40	32 Kwords	108000h-10FFFFh
	SA41	32 Kwords	110000h-117FFFh
	SA42	32 Kwords	118000h-11FFFFh
	SA43	32 Kwords	120000h-127FFFh
	SA44	32 Kwords	128000h-12FFFFh
	SA45	32 Kwords	130000h-137FFFh
	SA46	32 Kwords	138000h-13FFFFh

Table I3.6 WS064J Sector Address Table (Sheet 3 of 6)

Bank	Sector	Sector Size	(x16) Address Range
Bank C	SA47	32 Kwords	140000h-147FFFh
	SA48	32 Kwords	148000h-14FFFFh
	SA49	32 Kwords	150000h-157FFFh
	SA50	32 Kwords	158000h-15FFFFh
	SA51	32 Kwords	160000h-167FFFh
	SA52	32 Kwords	168000h-16FFFFh
	SA53	32 Kwords	170000h-177FFFh
	SA54	32 Kwords	178000h-17FFFFh
	SA55	32 Kwords	180000h-187FFFh
	SA56	32 Kwords	188000h-18FFFFh
	SA57	32 Kwords	190000h-197FFFh
	SA58	32 Kwords	198000h-19FFFFh
	SA59	32 Kwords	1A0000h-1A7FFFh
	SA60	32 Kwords	1A8000h-1AFFFFh
	SA61	32 Kwords	1B0000h-1B7FFFh
	SA62	32 Kwords	1B8000h-1BFFFFh
	SA63	32 Kwords	1C0000h-1C7FFFh
	SA64	32 Kwords	1C8000h-1CFFFFh
	SA65	32 Kwords	1D0000h-1D7FFFh
	SA66	32 Kwords	1D8000h-1DFFFFh
	SA67	32 Kwords	1E0000h-1E7FFFh
	SA68	32 Kwords	1E8000h-1EFFFFh
	SA69	32 Kwords	1F0000h-1F7FFFh
	SA70	32 Kwords	1F8000h-1FFFFFh

Table I3.6 WS064J Sector Address Table (Sheet 4 of 6)

Bank	Sector	Sector Size	(x16) Address Range
Bank B	SA71	32 Kwords	200000h-207FFFh
	SA72	32 Kwords	208000h-20FFFFh
	SA73	32 Kwords	210000h-217FFFh
	SA74	32 Kwords	218000h-21FFFFh
	SA75	32 Kwords	220000h-227FFFh
	SA76	32 Kwords	228000h-22FFFFh
	SA77	32 Kwords	230000h-237FFFh
	SA78	32 Kwords	238000h-23FFFFh
	SA79	32 Kwords	240000h-247FFFh
	SA80	32 Kwords	248000h-24FFFFh
	SA81	32 Kwords	250000h-257FFFh
	SA82	32 Kwords	258000h-25FFFFh
	SA83	32 Kwords	260000h-267FFFh
	SA84	32 Kwords	268000h-26FFFFh
	SA85	32 Kwords	270000h-277FFFh
	SA86	32 Kwords	278000h-27FFFFh
	SA87	32 Kwords	280000h-287FFFh
	SA88	32 Kwords	288000h-28FFFFh
	SA89	32 Kwords	290000h-297FFFh
	SA90	32 Kwords	298000h-29FFFFh
	SA91	32 Kwords	2A0000h-2A7FFFh
	SA92	32 Kwords	2A8000h-2AFFFFh
	SA93	32 Kwords	2B0000h-2B7FFFh
	SA94	32 Kwords	2B8000h-2BFFFFh

Table 13.6 WS064J Sector Address Table (Sheet 5 of 6)

Bank	Sector	Sector Size	(x16) Address Range
Bank B	SA95	32 Kwords	2C0000h-2C7FFFh
	SA96	32 Kwords	2C8000h-2CFFFFh
	SA97	32 Kwords	2D0000h-2D7FFFh
	SA98	32 Kwords	2D8000h-2DFFFFh
	SA99	32 Kwords	2E0000h-2E7FFFh
	SA100	32 Kwords	2E8000h-2EFFFFh
	SA101	32 Kwords	2F0000h-2F7FFFh
	SA102	32 Kwords	2F8000h-2FFFFFh
	SA103	32 Kwords	300000h-307FFFh
	SA104	32 Kwords	308000h-30FFFFh
	SA105	32 Kwords	310000h-317FFFh
	SA106	32 Kwords	318000h-31FFFFh
	SA107	32 Kwords	320000h-327FFFh
	SA108	32 Kwords	328000h-32FFFFh
	SA109	32 Kwords	330000h-337FFFh
	SA110	32 Kwords	338000h-33FFFFh
	SA111	32 Kwords	340000h-347FFFh
	SA112	32 Kwords	348000h-34FFFFh
	SA113	32 Kwords	350000h-357FFFh
	SA114	32 Kwords	358000h-35FFFFh
	SA115	32 Kwords	360000h-367FFFh
	SA116	32 Kwords	368000h-36FFFFh
	SA117	32 Kwords	370000h-377FFFh
	SA118	32 Kwords	378000h-37FFFFh

Table 13.6 WS064J Sector Address Table (Sheet 6 of 6)

Bank	Sector	Sector Size	(x16) Address Range
Bank A	SA119	32 Kwords	380000h-387FFFh
	SA120	32 Kwords	388000h-38FFFFh
	SA121	32 Kwords	390000h-397FFFh
	SA122	32 Kwords	398000h-39FFFFh
	SA123	32 Kwords	3A0000h-3A7FFFh
	SA124	32 Kwords	3A8000h-3AFFFFh
	SA125	32 Kwords	3B0000h-3B7FFFh
	SA126	32 Kwords	3B8000h-3BFFFFh
	SA127	32 Kwords	3C0000h-3C7FFFh
	SA128	32 Kwords	3C8000h-3CFFFFh
	SA129	32 Kwords	3D0000h-3D7FFFh
	SA130	32 Kwords	3D8000h-3DFFFFh
	SA131	32 Kwords	3E0000h-3E7FFFh
	SA132	32 Kwords	3E8000h-3EFFFFh
	SA133	32 Kwords	3F0000h-3F7FFFh
	SA134	4 Kwords	3F8000h-3F8FFFh
	SA135	4 Kwords	3F9000h-3F9FFFh
	SA136	4 Kwords	3FA000h-3FAFFFh
	SA137	4 Kwords	3FB000h-3FBFFFh
	SA138	4 Kwords	3FC000h-3FCFFFh
	SA139	4 Kwords	3FD000h-3FDFFFh
	SA140	4 Kwords	3FE000h-3FEFFFh
	SA141	4 Kwords	3FF000h-3FFFFFh

14 Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 14.5, "Command Definitions," on page 77 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data. Refer to the AC Characteristics section for timing diagrams.

14.1 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data in asynchronous mode. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. After completing a programming operation in the Erase Suspend mode, the system may once again read array data from any non-erase-suspended sector within the same bank. See the "Erase Suspend/Erase Resume Commands" section on page 72 for more information.

The system must issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the "Reset Command" section on page 67 for more information.

See also "Requirements for Asynchronous ReadOperation (Non-Burst)" section on page 28 and "Requirements for Synchronous (Burst) Read Operation" section on page 29 for more information. The Asynchronous Read and Synchronous/Burst Read tables provide the read parameters, and Figure 22.3, "CLK Synchronous Burst Mode Read (rising active CLK)," on page 93, Figure 22.5, "Synchronous Burst Mode Read," on page 94, and Figure 22.8, "Asynchronous Mode Read with Latched Addresses," on page 96 show the timings.

14.2 Set Configuration Register Command Sequence

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, active clock edge, RDY configuration, and synchronous mode active. The configuration register must be set before the device will enter burst mode.

The configuration register is loaded with a three-cycle command sequence. The first two cycles are standard unlock sequences. On the third cycle, the data should be C0h, address bits A11–A0 should be 555h, and address bits A19–A12 set the code to be latched. The device will power up or after a hardware reset with the default setting, which is in asynchronous mode. The register must be set before the device can enter synchronous mode. The configuration register can not be changed during device operations (program, erase, or sector lock).

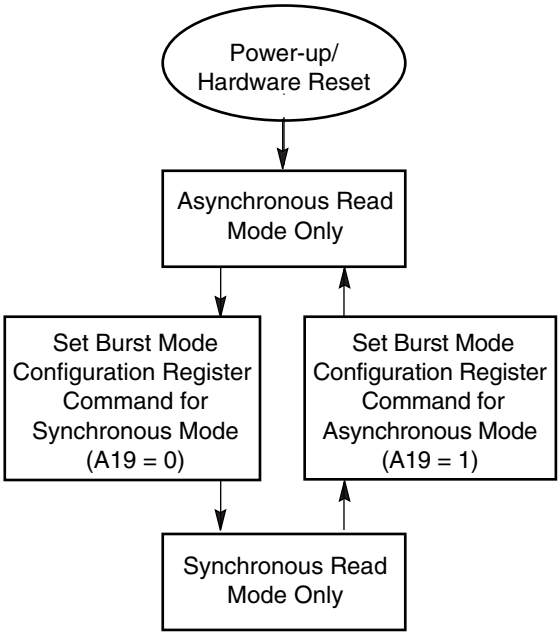


Figure 14.1 Synchronous/Asynchronous State Diagram

14.2.1 Read Mode Setting

On power-up or hardware reset, the device is set to be in asynchronous read mode. This setting allows the system to enable or disable burst mode during system operations. Address A19 determines this setting: "1' for asynchronous mode, "0" for synchronous mode.

14.2.2 Programmable Wait State Configuration

The programmable wait state feature informs the device of the number of clock cycles that must elapse after AVD# is driven active before data will be available. This value is determined by the input frequency of the device. Address bits A14–A12 determine the setting (see Table 14.1, "Programmable Wait State Settings," on page 65).

The wait state command sequence instructs the device to set a particular number of clock cycles for the initial access in burst mode. The number of wait states that should be programmed into the device is directly related to the clock frequency.

Table 14.1 Programmable Wait State Settings

AI4	AI3	AI2	Total Initial Access Cycles
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	7 (default)
1	1	0	Reserved
1	1	1	Reserved

Notes:

1. *Upon power-up or hardware reset, the default setting is seven wait states.*
2. *RDY will default to being active with data when the Wait State Setting is set to a total initial access cycle of 2.*

It is recommended that the wait state command sequence be written, even if the default wait state value is desired, to ensure the device is set as expected. A hardware reset will set the wait state to the default setting.

14.2.3 Standard wait-state Handshaking Option

The host system must set the appropriate number of wait states in the flash device depending upon the clock frequency. The host system should set address bits A14–A12 to 010 for a clock frequency of 66/80 MHz for the system/device to execute at maximum speed.

Table 14.2 describes the recommended number of clock cycles (wait states) for various conditions.

Table 14.2 Wait States for Standard wait-state Handshaking

Burst Mode	Typical No. of Clock Cycles after AVD# Low	
	66 MHz	80 MHz
8-Word or 16-Word or Continuous	4	6 or 7
32-Word	5	7

Notes:

1. *In the 8-, 16- and 32-word burst read modes, the address pointer does not cross 64-word boundaries (addresses which are multiples of 3Fh).*
2. *For WS128J model numbers 10 and 11, an additional clock cycle is required for boundary crossings while in Continuous read mode.*

The host system must set the appropriate number of wait states in the flash device depending upon the clock frequency. Note that the host system must set again the number of wait state when the host system change the clock frequency. For example, the host system must set from 6 or 7 wait state to less than 5 wait states when the host system change the clock frequency from 80MHz to less than 80MHz. The autoselect function allows the host system to determine whether the flash device is enabled for handshaking. See the "Autoselect Command Sequence" section on page 68 for more information.

14.2.4 Read Mode Configuration

The device supports four different read modes: continuous mode, and 8, 16, and 32 word linear wrap around modes. A continuous sequence begins at the starting address and advances the address pointer until the burst operation is complete. If the highest address in the device is reached during the continuous burst read mode, the address pointer wraps around to the lowest address.

For example, an eight-word linear read with wrap around begins on the starting address written to the device and then advances to the next 8 word boundary. The address pointer then returns to the 1st word after the previous eight word boundary, wrapping through the starting location. The sixteen- and thirty-two linear wrap around modes operate in a fashion similar to the eight-word mode.

Table 14.3 shows the address bits and settings for the four read modes.

Table I4.3 Read Mode Settings

Burst Modes	Address Bits	
	AI6	AI5
Continuous	0	0
8-word linear wrap around	0	1
16-word linear wrap around	1	0
32-word linear wrap around	1	1

Note: *Upon power-up or hardware reset the default setting is continuous.*

14.2.5 Burst Active Clock Edge Configuration

By default, the device will deliver data on the rising edge of the clock after the initial synchronous access time. Subsequent outputs will also be on the following rising edges, barring any delays. The device can be set so that the falling clock edge is active for all synchronous accesses. Address bit A17 determines this setting; "1" for rising active, "0" for falling active.

14.2.6 RDY Configuration

By default, the device is set so that the RDY pin will output V_{OH} whenever there is valid data on the outputs. The device can be set so that RDY goes active one data cycle before active data. Address bit A18 determines this setting; "1" for RDY active with data, "0" for RDY active one clock cycle before valid data. Only the combination of wait state 2 and RDY active one clock cycle before data is not supported. In asynchronous mode, RDY is an open-drain output.

I4.3 Configuration Register

Table 14.4 shows the address bits that determine the configuration register settings for various device functions.

Table I4.4 Configuration Register

Address Bit	Function	Settings (Binary)
A19	Set Device Read Mode	0 = Synchronous Read (Burst Mode) Enabled 1 = Asynchronous Mode (default)
A18	RDY	0 = RDY active one clock cycle before data 1 = RDY active with data (default)
A17	Clock	0 = Burst starts and data is output on the falling edge of CLK 1 = Burst starts and data is output on the rising edge of CLK (default)
A16	Read Mode	Synchronous Mode
A15		00 = Continuous (default) 01 = 8-word linear with wrap around 10 = 16-word linear with wrap around 11 = 32-word linear with wrap around
A14	Programmable Wait State	000 = Data is valid on the 2nd active CLK edge after AVD# transition to V_{IH} 001 = Data is valid on the 3rd active CLK edge after AVD# transition to V_{IH} 010 = Data is valid on the 4th active CLK edge after AVD# transition to V_{IH} 011 = Data is valid on the 5th active CLK edge after AVD# transition to V_{IH} 100 = Data is valid on the 6th active CLK edge after AVD# transition to V_{IH} 101 = Data is valid on the 7th active CLK edge after AVD# transition to V_{IH} (default) 110 = Reserved 111 = Reserved
A13		
A12		

Note: *Device is in the default state upon power-up or hardware reset.*

I4.4 Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins (prior to the third cycle). This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

14.5 Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 14.5, "Command Definitions," on page 77 shows the address and data requirements. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. No subsequent data will be made available if the autoselect data is read in synchronous mode. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence. Read commands to other banks will return data from the array. The following table describes the address requirements for the various autoselect functions, and the resulting data. BA represents the bank address, and SA represents the sector address. The device ID is read in three cycles.

Description	Address	Read Data
Manufacturer ID	(BA) + 00h	0001h
Device ID, Word 1	(BA) + 01h	227Eh
Device ID, Word 2	(BA) + 0Eh	2218h (WS128J) 221Eh (WS064J)
Device ID, Word 3	(BA) + 0Fh	2200h (WS128J) 2201h (WS064J)
Sector Protection Verification	(SA) + 02h	0001 (locked), 0000 (unlocked)
Indicator Bits	(BA) + 03h	DQ15 - DQ8 = 0 DQ7 - Factory Lock Bit 1 = Locked, 0 = Not Locked DQ6 -Customer Lock Bit 1 = Locked, 0 = Not Locked DQ5 - Handshake Bit 1 = Reserved, 0 = Standard Handshake DQ4 & DQ3 - Boot Code 00 = Dual Boot Sector, 01 = Top Boot Sector, 10 = Bottom Boot Sector DQ2 - DQ0 = 001

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

14.6 Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. The Secured Silicon Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Table 14.5, "Command Definitions," on page 77 shows the address and data requirements for both command sequences.

The following commands are not allowed when the Secured Silicon is accessible.

- CFI
- Unlock Bypass Entry
- Unlock Bypass Program
- Unlock Bypass Reset
- Erase Suspend/Resume
- Chip Erase

14.7 Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 14.5, "Command Definitions," on page 77 shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by monitoring DQ7 or DQ6/DQ2. Refer to the "Write Operation Status" section on page 80 for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from "0" back to a "1." Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bit to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

14.7.1 Unlock Bypass Command Sequence

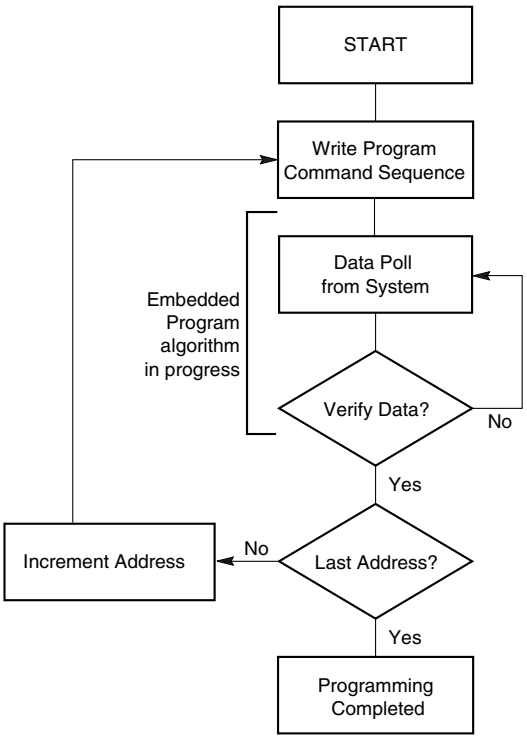
The unlock bypass feature allows the system to primarily program to a array faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. The host system may also initiate the chip erase and sector

erase sequences in the unlock bypass mode. The erase command sequences are four cycles in length instead of six cycles. Table 14.5, "Command Definitions," on page 77 shows the requirements for the unlock bypass command sequences.

During the unlock bypass mode, only the Read, Unlock Bypass Program, Unlock Bypass Sector Erase, Unlock Bypass Chip Erase, and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need only contain the data 00h. The array then returns to the read mode.

The device offers accelerated program operations through the ACC input. When the system asserts V_{HH} on this input, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the ACC input to accelerate the operation.

Figure 14.2, "Program Operation," on page 70 illustrates the algorithm for the program operation. Refer to the Erase/Program Operations table in the AC Characteristics section for parameters, and Figure 22.11, "Asynchronous Program Operation Timings: AVD# Latched Addresses," on page 100 and Figure 22.13, "Synchronous Program Operation Timings: WE# Latched Addresses," on page 102 for timing diagrams.



Note: *See Table 14.5 for program command sequence.*

Figure 14.2 Program Operation

14.8 Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 14.5, "Command Definitions," on page 77 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6/DQ2. Refer to the "Write Operation Status" section on page 80 for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

The host system may also initiate the chip erase command sequence while the device is in the unlock bypass mode. The command sequence is two cycles cycles in length instead of six cycles. See Table 14.5, "Command Definitions," on page 77 for details on the unlock bypass command sequences.

Figure 14.3, "Erase Operation," on page 73 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations table in the AC Characteristics section for parameters and timing diagrams.

14.9 Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 14.5, "Command Definitions," on page 77 shows the address and data requirements for the sector erase command sequence.

The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of no less than 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If any command other than 30h, B0h, F0h is input during the time-out period, the normal operation will not be guaranteed.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See "DQ3: Sector Erase Timer" section on page 85.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7 or DQ6/DQ2 in the erasing bank. Refer to the "Write Operation Status" section on page 80 for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

The host system may also initiate the sector erase command sequence while the device is in the unlock bypass mode. The command sequence is four cycles cycles in length instead of six cycles.

Figure 14.3, "Erase Operation," on page 73 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations table in the AC Characteristics on page 91 for parameters and timing diagrams.

14.10 Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the minimum 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

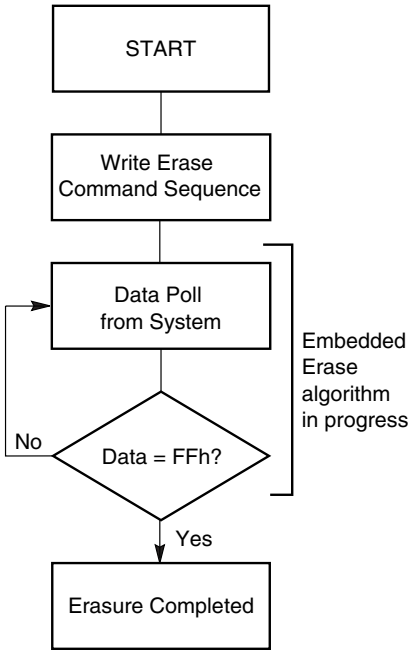
When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 35 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Figure 15, "Write Operation Status," on page 80 for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. Refer to the "Write Operation Status" section on page 80 for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the "Autoselect Mode" section on page 31 and "Autoselect Command Sequence" section on page 68 for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



Notes:

1. *See Table 14.5 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer*

Figure 14.3 Erase Operation

14.11 Password Program Command

The Password Program Command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. 4 Password Program commands are required to program the password. The user must enter the unlock cycle, password program command (38h) and the program address/data for each portion of the password when programming. There are no provisions for entering the 2-cycle unlock cycle, the password program command, and all the password data. There is no special addressing order required for programming the password. Also, when the password is undergoing programming, Simultaneous Operation is disabled. Read operations to any memory location will return the programming status except DQ7. Once programming is complete, the user must issue a Read/Reset command to the device to normal operation. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent verification. The Password Program Command is only capable of programming "0"s. Programming a "1" after a cell is programmed as a "0" results in a time-out by the Embedded Program Algorithm™ with the cell remaining as a "0". The password is all F's when shipped from the factory. All 64-bit password combinations are valid as a password.

14.12 Password Verify Command

The Password Verify Command is used to verify the Password. The Password is verifiable only when the Password Mode Locking Bit is not programmed. If the Password Mode Locking Bit is programmed and the user attempts to verify the Password, the device will always drive all F's onto the DQ data bus.

Also, the device will not operate in Simultaneous Operation when the Password Verify command is executed. Only the password is returned regardless of the bank address. The lower two address bits (A1–A0) are valid during the Password Verify. Writing the Secured Silicon Exit command returns the device back to normal operation.

14.13 Password Protection Mode Locking Bit Program Command

The Password Protection Mode Locking Bit Program Command programs the Password Protection Mode Locking Bit, which prevents further verifies or updates to the password. Once programmed, the Password Protection Mode Locking Bit cannot be erased and the Persistent Protection Mode Locking Bit program circuitry is disabled, thereby forcing the device to remain in the Password Protection Mode. After issuing "PL/68h" at the fourth bus cycle, the device requires a time out period of approximately 150 µs for programming the Password Protection Mode Locking Bit. Then by writing "PL/48h" at the fifth bus cycle, the device outputs verify data at DQ0. If DQ0 = 1, then the Password Protection Mode Locking Bit is programmed. If not, the system must repeat this program sequence from the fourth cycle of "PL/68h". Exiting the Password Protection Mode Locking Bit Program command is accomplished by writing the Secured Silicon Sector Exit command or Read/Reset command.

14.14 Persistent Sector Protection Mode Locking Bit Program Command

The Persistent Sector Protection Mode Locking Bit Program Command programs the Persistent Sector Protection Mode Locking Bit, which prevents the Password Mode Locking Bit from ever being programmed. By disabling the program circuitry of the Password Mode Locking Bit, the device is forced to remain in the Persistent Sector Protection mode of operation, once this bit is set. After issuing "SL/68h" at the fourth bus cycle, the device requires a time out period of approximately 150 µs for programming the Persistent Protect ion Mode Locking Bit. Then by writ ing "SMPL/48h" at the fifth bus cycle, the device outputs verify data at DQ0. If DQ0 = 1, then the Persistent Protection Mode Locking Bit is programmed. If not, the system must repeat this program sequence from the fourth cycle of "PL/68h". Exiting the Persistent Protection Mode Locking Bit Program command is accomplished by writing the Secured Silicon Sector Exit command or Read/Reset command.

14.15 Secured Silicon Sector Protection Bit Program Command

To protect the Secured Silicon Sector, write the Secured Silicon Sector Protect command sequence while in the Secured Silicon Sector mode. After issuing "OW/48h" at the fourth bus cycle, the device requires a time out period of approximately 150 µs to protect the Secured Silicon Sector. Then, by writing "OPBP/48" at the fifth bus cycle, the device outputs verify data at DQ0. If DQ0 = 1, then the Secured Silicon Sector is protected. If not, then the system must repeat this program sequence from the fourth cycle of "OPBP/48h". Exiting the Secured Silicon Sector Protection Mode Locking Bit Program command is accomplished by writing the Secured Silicon Sector Exit command or Read/Reset command.

14.16 PPB Lock Bit Set Command

The PPB Lock Bit Set command is used to set the PPB Lock bit if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set, it cannot be cleared unless the device is taken through a power-on clear or the Password Unlock command is executed. Upon setting the PPB Lock Bit, the PPBs are latched. If the Password Mode Locking Bit is set, the PPB Lock Bit status is reflected as set, even after a power-on reset cycle. Exiting the PPB Lock Bit Set command is accomplished by writing the Secured Silicon Exit command, only while in the Persistent Sector Protection Mode.

14.17 DPB Write/Erase/Status Command

The DPB Write command is used to set or clear a DPB for a given sector. The high order address bits (Amax–A11) are issued at the same time as the code 01h or 00h on DQ7-DQ0. All other DQ data bus pins are ignored during the data write cycle. The DPBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. If the PPB is set, the sector is protected regardless of the value of the DPB. If the PPB is cleared, setting the DPB to a 1 protects the sector from programs or erases. Since this is a volatile bit, removing power or resetting the device will clear the DPBs. The programming of the DPB for a given sector can be verified by writing a DPB Status command to the device. Exiting the DPB Write/Erase command is accomplished by writing the Read/Reset command. Exiting the DPB Status command is accomplished by writting the Secured Silicon Sector Exit command

14.18 Password Unlock Command

The Password Unlock command is used to clear the PPB Lock Bit so that the PPBs can be unlocked for modification, thereby allowing the PPBs to become accessible for modification. The exact password must be entered in order for the unlocking function to occur. This command cannot be issued any faster than 2 µs at a time to prevent a hacker from running through the all 64-bit combinations in an attempt to correctly match a password. If the command is issued before the 2 µs execution window for each portion of the unlock, the command will be ignored.

The Password Unlock function is accomplished by writing Password Unlock command and data to the device to perform the clearing of the PPB Lock Bit. The password is 64 bits long, so the user must write the Password Unlock command 4 times. A1 and A0 are used for matching. Writing the Password Unlock command is not address order specific. The lower address A1–A0= 00, the next Password Unlock command is to A1–A0= 01, then to A1–A0= 10, and finally to A1–A0= 11.

Once the Password Unlock command is entered for all four words, the RDY pin goes LOW indicating that the device is busy. Also, reading the Bank D results in the DQ6 pin toggling, indicating that the Password Unlock function is in progress. Reading the other bank returns actual array data. Approximately 1µs is required for each portion of the unlock. Once the first portion of the password unlock completes (RDY is not driven and DQ6 does not toggle when read), the Password Unlock command is issued again, only this time with the next part of the password. Four Password Unlock commands are required to successfully clear the PPB Lock Bit. As with the first Password Unlock command, the RDY signal goes LOW and reading the device results in the DQ6 pin toggling on successive read operations until complete. It is the responsibility of the microprocessor to keep track of the number of Password Unlock commands, the order, and when to read the PPB Lock bit to confirm successful password unlock. In order to relock the device into the Password Mode, the PPB Lock Bit Set command can be re-issued. Exiting the Password Unlock command is accomplished by writing the Secured Silicon Sector Exit command.

14.19 PPB Program Command

The PPB Program command is used to program, or set, a given PPB. Each PPB is individually programmed (but is bulk erased with the other PPBs). The specific sector address (Amax–A12) are written at the same time as the program command 60h with A6 = 0. If the PPB Lock Bit is set and the corresponding PPB is set for the sector, the PPB Program command will not execute and the command will time-out without programming the PPB.

After programming a PPB, two additional cycles are needed to determine whether the PPB has been programmed with margin. After 4th cycle, the device requires approximately 150 µs time out period for programming the PPB. And then after 5th cycle, the device outputs verify data at DQ0.

The PPB Program command does not follow the Embedded Program algorithm. Writing the Secured Silicon Sector Exit command or Read/Reset command return the device back to normal operation.

14.20 All PPB Erase Command

The All PPB Erase command is used to erase all PPBs in bulk. There is no means for individually erasing a specific PPB. Unlike the PPB program, no specific sector address is required. However, when the PPB erase command is written (60h) and A6 = 1, all Sector PPBs are erased in parallel. If the PPB Lock Bit is set the ALL PPB Erase command will not execute and the command will time-out without erasing the PPBs.

After erasing the PPBs, two additional cycles are needed to determine whether the PPB has been erased with margin. After 4th cycle, the device requires approximately 1.5 ms time out period for erasing the PPB. And then after 5th cycle, the device outputs verify data at DQ0.

It is the responsibility of the user to preprogram all PPBs prior to issuing the All PPB Erase command. If the user attempts to erase a cleared PPB, over-erasure may occur making it difficult to program the PPB at a later time. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed. Writing the Secured Silicon Sector Exit command or Read/Reset command return the device back to normal operation.

14.21 PPB Status Command

The programming of the PPB for a given sector can be verified by writing a PPB status verify command to the device. Writing the Secured Silicon Sector Exit command or Read/Reset command return the device back to normal operation.

14.22 PPB Lock Bit Status Command

The programming of the PPB Lock Bit for a given sector can be verified by writing a PPB Lock Bit status verify command to the device. Writing the Secured Silicon Sector Exit command or Read/Reset command return the device back to normal operation.

14.23 Command Definitions

Table 14.5 Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 1–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Asynchronous Read (Note 7)		1	RA	RD												
Reset (Note 8)		1	XXX	F0												
Autoselect (Note 9)	Manufacturer ID	4	555	AA	2AA	55	(BA) 555	90	(BA) X00	0001						
	Device ID (Note 10)	6	555	AA	2AA	55	(BA) 555	90	(BA) X01	227E	(BA)X 0E	(Note 10)	(BA) X0F	(Note 10)		
	Sector Lock Verify (Note 11)	4	555	AA	2AA	55	(SA) 555	90	(SA) X02	0000/ 0001						
	Indicator Bits	4	555	AA	2AA	55	(BA) 555	90	(BA) X03	(Note 12)						
Program		4	555	AA	2AA	55	555	A0	PA	Data						
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10		
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30		
Erase Suspend (Note 15)		1	BA	B0												
Erase Resume (Note 16)		1	BA	30												
Set Configuration Register (Note 17)		3	555	AA	2AA	55	(CR) 555	C0								
CFI Query (Note 18)		1	55	98												
Unlock Bypass Mode	Unlock Bypass Entry	3	555	AA	2AA	55	555	20								
	Unlock Bypass Program (Notes 13, 14)	2	XX	A0	PA	PD										
	Unlock Bypass Sector Erase (Notes 13, 14)	2	XX	80	SA	30										
	Unlock Bypass Erase (Notes 13, 14)	2	XX	80	XXX	10										
	Unlock Bypass Reset (Notes 13, 14)	2	XX	90	XXX	00										
Sector Protection Command Definitions																
Secured Silicon Sector	Secured Silicon Sector Entry	3	555	AA	2AA	55	555	88								
	Secured Silicon Sector Exit	4	555	AA	2AA	55	555	90	XX	00						
	Secured Silicon Protection Bit Program (Notes 19, 21)	6	555	AA	2AA	55	555	60	OW	68	OW	48	OW	RD (0)		
Password Protection	Password Program (Notes 23)	4	555	AA	2AA	55	555	38	XX0	PD0						
									XX1	PD1						
									XX2	PD2						
									XX3	PD3						
	Password Verify	4	555	AA	2AA	55	555	C8	XX0	PD0						
									XX1	PD1						
									XX2	PD2						
									XX3	PD3						
	Password Unlock (Note 23)	7	555	AA	2AA	55	555	28	XX0	PD0	XX1	PD1	XX2	PD2	XX3	PD3

Command Sequence (Note I)		Cycles	Bus Cycles (Notes I–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
PPB Commands	PPB Program (Notes 21)	6	555	AA	2AA	55	555	60	SBA + WP	68	SBA + WP	48	XX	RD (0)		
	All PPB Erase (Notes 22, 24)	6	555	AA	2AA	55	555	60	WPE	60	SBA WPE	40	XX	RD (0)		
	PPB Status (Note 25)	4	555	AA	2AA	55	SBA 555	90	SBA +WP	RD (0)						
PPB Lock Bit	PPB Lock Bit Set	3	555	AA	2AA	55	555	78								
	PPB Lock Bit Status	4	555	AA	2AA	55	(BA) 555	58	BA	RD (1)						
DPB	DPB Write	4	555	AA	2AA	55	555	48	SA	X1						
	DPB Erase	4	555	AA	2AA	55	555	48	SA	X0						
	DPB Status	4	555	AA	2AA	55	(BA) 555	58	SA	RD (0)						
Password Protection Mode Locking Bit Program (Notes 21)		6	555	AA	2AA	55	555	60	PL	68	PL	48	PL	RD (0)		
Persistent Protection Mode Locking Bit Program (Notes 21)		6	555	AA	2AA	55	555	60	SL	68	SL	48	SL	RD (0)		

Legend:

X = Don't care
RA = Address of the memory location to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the rising edge of the AVD# pulse or active edge of CLK which ever comes first.
PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.
SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits Amax–A12 uniquely select any sector.
BA = Address of the bank (WS128J: A22, A21, A20, WS064J: A21, A20, A19) that is being switched to autoselect mode, is in bypass mode, or is being erased.
SLA = Address of the sector to be locked. Set sector address (SA) and either A6 = 1 for unlocked or A6 = 0 for locked.
SBA = sector address block to be protected.
CR = Configuration Register address bits A19–A12.
OW = Address (A7–A0) is (00011010).
PD3–PD0 = Password Data. PD3–PD0 present four 16 bit combinations that represent the 64-bit Password
PWA = Password Address. Address bits A1 and A0 are used to select each 16-bit portion of the 64-bit entity.
PWD = Password Data.
PL = Address (A7-A0) is (00001010)
RD(0) = DQ0 protection indicator bit. If protected, DQ0 = 1, if unprotected, DQ0 = 0.
RD(1) = DQ1 protection indicator bit. If protected, DQ1 = 1, if unprotected, DQ1 = 0.
SL = Address (A7-A0) is (00010010)
WD= Write Data. See "Configuration Register" definition for specific write data
WP = Address (A7-A0) is (00000010)
WPE = address(A7-A0) is (01000010)

Notes:

1. *See Table 11.1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the following, all bus cycles are write cycle: read cycle, fourth through sixth cycles of the Autoselect commands, fourth cycle of the configuration register verify and password verify commands, and any cycle reading at RD(0) and RD(1).*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD, PD, WD, PWD, and PD3-PD0.*
5. *Unless otherwise noted, address bits Amax–A12 are don't cares.*
6. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.*
7. *No unlock or command cycles required when bank is reading array data.*
8. *The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information) or performing sector lock/unlock.*
9. *The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address. See the Autoselect Command Sequence section for more information.*
10. *(BA)X0Fh = 2200h (WS128J), (BA)X0Eh = 2218h (WS128J), (BA)X0Fh = 221Eh (WS064J), (BA)X0Eh = 2201h (WS064J)*
11. *The data is 0000h for an unlocked sector and 0001h for a locked sector*
12. *DQ15 - DQ8 = 0, DQ7 - Factory Lock Bit (1 = Locked, 0 = Not Locked), DQ6 -Customer Lock Bit (1 = Locked, 0 = Not Locked), DQ5 = Handshake Bit (1 = Reserved, 0 = Standard Handshake)8, DQ4 & DQ3 - Boot Code (00= Dual Boot Sector, 01= Top Boot Sector, 10= Bottom Boot Sector, 11=No Boot Sector), DQ2 - DQ0 = 001*
13. *The Unlock Bypass command sequence is required prior to this command sequence.*

14. *The Unlock Bypass Reset command is required to return to reading array data.*
15. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
16. *The Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*
17. *See "Set Configuration Register Command Sequence" for details.*
18. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
19. *Regardless of CLK and AVD# interaction or Control Register bit 15 setting, command mode verifies are always asynchronous read operations.*
20. *ACC must be at V_{HH} during the entire operation of this command*
21. *The fourth cycle programs the addressed locking bit. The fifth and sixth cycles are used to validate whether the bit has been fully programmed. If DQ0 (in the sixth cycle) reads 0, the program command must be issued and verified again.*
22. *The fourth cycle erases all PPBs. The fifth and sixth cycles are used to validate whether the bits have been fully erased. If DQ0 (in the sixth cycle) reads 1, the erase command must be issued and verified again.*
23. *The entire four bus-cycle sequence must be entered for each portion of the password.*
24. *Before issuing the erase command, all PPBs should be programmed in order to prevent over-erasure of PPBs.*
25. *In the fourth cycle, 01h indicates PPB set; 00h indicates PPB not set.*

15 Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 15.2, "Write Operation Status," on page 86 and the following subsections describe the function of these bits. DQ7 and DQ6 each offers a method for determining whether a program or erase operation is complete or in progress.

15.1 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

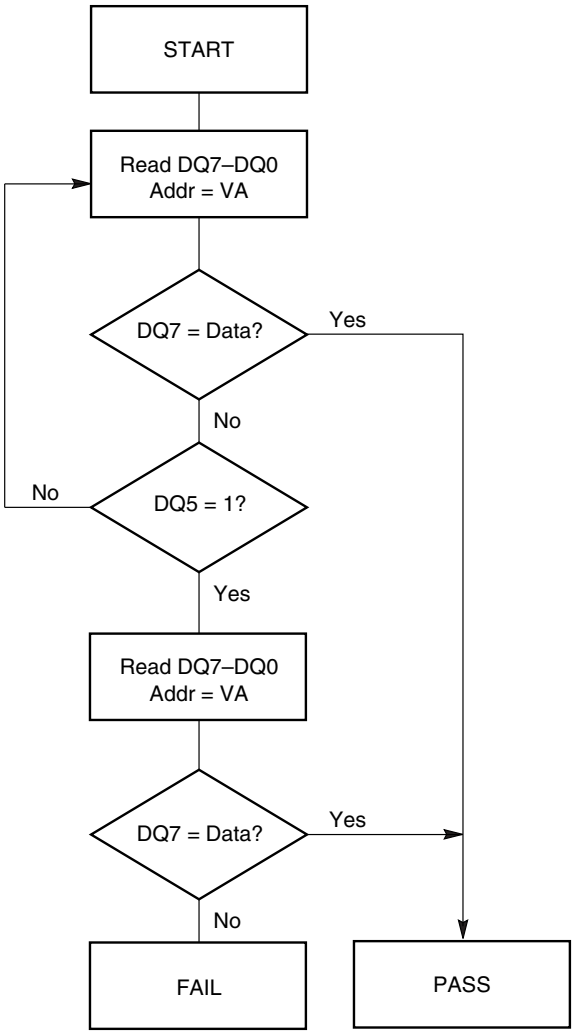
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6-DQ0 may be still invalid. Valid data on DQ7-D00 will appear on successive read cycles.

Table 15.2, "Write Operation Status," on page 86 shows the outputs for Data# Polling on DQ7. Figure 15.1, "Data# Polling Algorithm," on page 81 shows the Data# Polling algorithm. Figure 22.17, "Data# Polling Timings (During Embedded Algorithm)," on page 105 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 15.1 Data# Polling Algorithm

15.2 RDY: Ready

The RDY is a dedicated output that, when the device is configured in the Synchronous mode, indicates (when at logic low) the system should wait 1 clock cycle before expecting the next word of data. The RDY pin is only controlled by CE#. Using the RDY Configuration Command Sequence, RDY can be set so that a logic low indicates the system should wait 2 clock cycles before expecting valid data.

The following conditions cause the RDY output to be low: during the initial access (in burst mode), and after the boundary that occurs every 64 words beginning with the 64th address, 3Fh.

When the device is configured in Asynchronous Mode, the RDY is an open-drain output pin which indicates whether an Embedded Algorithm is in progress or completed. The RDY status is valid after the rising edge of the final WE# pulse in the command sequence.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is in high impedance (Ready), the device is in the read mode, the standby mode, or in the erase-suspend-read mode. Table 15.2, "Write Operation Status," on page 86 shows the outputs for RDY.

15.3 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address in the same bank, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase timeout.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

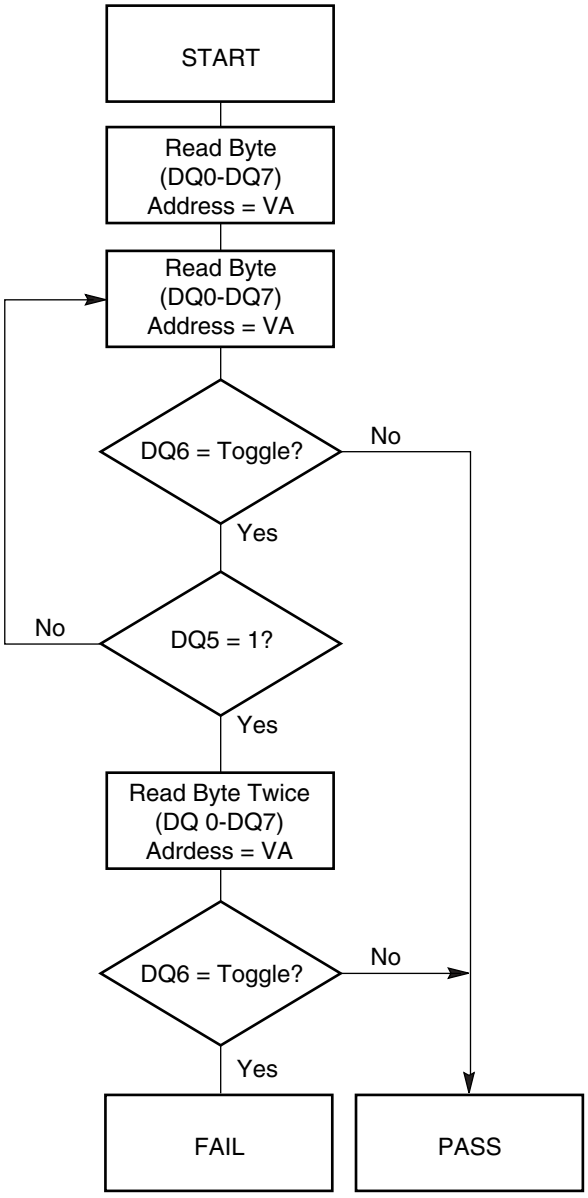
The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 ms after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

See the following for additional information: Figure 15.2, "Toggle Bit Algorithm," on page 83, DQ6: Toggle Bit I on page 82, Figure 22.18, "Toggle Bit Timings (During Embedded Algorithm)," on page 106 (toggle bit timing diagram), and Table 15.1, "DQ6 and DQ2 Indications," on page 84.

Toggle Bit I on DQ6 requires either OE# or CE# to be deasserteed and reasserted to show the change in state.



Note: *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.*

Figure I5.2 Toggle Bit Algorithm

I5.4 DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 15.1, "DQ6 and DQ2 Indications," on page 84 to compare outputs for DQ2 and DQ6.

See the following for additional information: Figure 15.2, "Toggle Bit Algorithm," on page 83, See DQ6: Toggle Bit I on page 82, Figure 22.18, "Toggle Bit Timings (During Embedded Algorithm)," on page 106, and Table 15.1, "DQ6 and DQ2 Indications," on page 84.

Table I5.1 DQ6 and DQ2 Indications

If device is	and the system reads	then DQ6	and DQ2
programming,	at any address,	toggles,	does not toggle.
actively erasing,	at an address within a sector selected for erasure,	toggles,	also toggles.
	at an address within sectors *not* selected for erasure,	toggles,	does not toggle.
erase suspended,	at an address within a sector selected for erasure,	does not toggle,	toggles.
	at an address within sectors *not* selected for erasure,	returns array data,	returns array data. The system can read from any sector not selected for erasure.
programming in erase suspend	at any address,	toggles,	is not applicable.

I5.5 Reading Toggle Bits DQ6/DQ2

Refer to Figure 15.2, "Toggle Bit Algorithm," on page 83 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively,

it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (Figure 15.2, "Toggle Bit Algorithm," on page 83).

I5.6 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." Only an erase operation can change a "0" back to a "1." Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

I5.7 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also Sector Erase Command Sequence on page 71.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 15.2 shows the status of DQ3 relative to the other status bits.

Table 15.2 Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RDY (Note 5)
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle (Note 6)	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read (Note 4)	Erase Suspended Sector	1	No toggle (Note 6)	0	N/A	Toggle	High Impedance
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	High Impedance
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.*
4. *The system may read either asynchronously or synchronously (burst) while in erase suspend.*
5. *The RDY pin acts a dedicated output to indicate the status of an embedded erase or program operation is in progress. This is available in the Asynchronous mode only.*
6. *When the device is set to Asynchronous mode, these status flags should be read by CE# toggle.*

16 Absolute Maximum Ratings

Storage Temperature, Plastic Packages . . . . . −65°C to +150°C
Ambient Temperature with Power Applied . . . . . −65°C to +125°C
Voltage with Respect to Ground:
All Inputs and I/Os except as noted below (Note 1). . . . . −0.5 V to V_{CC} + 0.5 V
V_{CC} (Note 1). . . . . −0.5 V to +2.5 V
A9, RESET#, ACC (Note 1). . . . . −0.5 V to +12.5 V
Output Short Circuit Current (Note 3) . . . . . 100 mA

Notes:

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, inputs or I/Os may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 16.1. Maximum DC voltage on input or I/Os is V_{CC} + 0.5 V. During voltage transitions outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 16.2.*
2. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
3. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

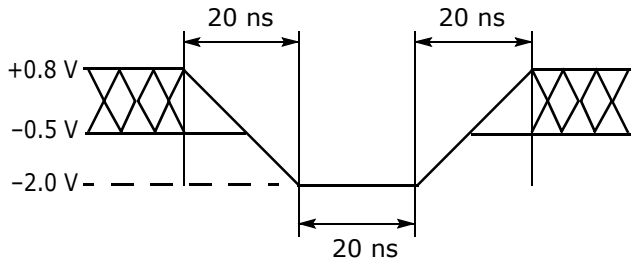


Figure 16.1 Maximum Negative Overshoot Waveform

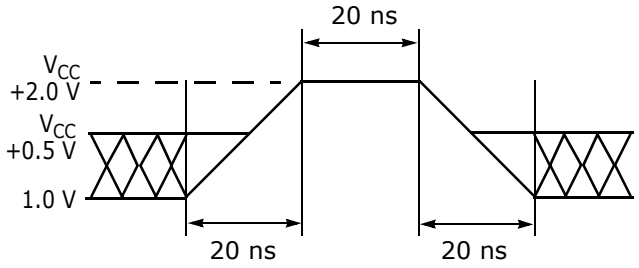


Figure 16.2 Maximum Positive Overshoot Waveform

17 Operating Ranges

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to +70°C

Wireless (W) Devices

Ambient Temperature (T_A) . . . . . –25°C to +85°C

Supply Voltages

V_{CC} Supply Voltages . . . . . 1.65 V to 1.95 V (66MHz)

. . . . . 1.70 V to 1.95 V (80MHz)

Note: *Operating ranges define those limits between which the functionality of the device is guaranteed.*

18 DC Characteristics

18.1 CMOS Compatible

Parameter	Description	Test Conditions Notes: 1		Min	Typ	Max	Unit
I_{LI}	Input Load Current	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC}max				±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC}max				±1	µA
I_{CCB}	V_{CC} Active burst Read Current	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 8	66 MHz		15	30	mA
			80 MHz		18	36	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 16	66 MHz		15	30	mA
			80 MHz		18	36	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = Continuous	66 MHz		15	30	mA
			80 MHz		18	36	mA
I_{IO1}	V_{CC} Non-active Output	OE# = V_{IH}			0.2	10	µA
I_{CC1}	V_{CC} Active Asynchronous Read Current (Note 2)	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}	10 MHz		20	30	mA
			5 MHz		12	16	mA
			1 MHz		3.5	5	mA
I_{CC2}	V_{CC} Active Write Current (Note 3)	CE# = V_{IL}, OE# = V_{IH}, ACC = V_{IH}			15	40	mA
I_{CC3}	V_{CC} Standby Current (Note 4)	CE# = RESET# = V_{CC} ± 0.2 V			0.2	50	µA
I_{CC4}	V_{CC} Reset Current	RESET# = V_{IL}, CLK = V_{IL}			0.2	50	µA
I_{CC5}	V_{CC} Active Current (Read While Write)	CE# = V_{IL}, OE# = V_{IH}	66 MHz		22	54	mA
			80 MHz		25	60	mA
I_{CC6}	V_{CC} Sleep Current	CE# = V_{IL}, OE# = V_{IH}			0.2	50	µA
I_{ACC}	Accelerated Program Current (Note 5)	CE# = V_{IL}, OE# = V_{IH}, V_{ACC} = 12.0 ± 0.5 V	V_{ACC}		7	15	mA
			V_{CC}		5	10	mA
V_{IL}	Input Low Voltage			–0.5		0.4	V
V_{IH}	Input High Voltage			V_{CC} – 0.4		V_{CC} + 0.4	
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, V_{CC} = $V_{CC\ min}$ = V_{IO}				0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, V_{CC} = $V_{CC\ min}$		V_{CC} – 0.1			V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 1.8 V		11.5		12.5	V
V_{HH}	Voltage for Accelerated Program			11.5		12.5	V
V_{LKO}	Low V_{CC} Lock-out Voltage			1.0		1.4	V

Notes:

1. *Maximum I_{CC} specifications are tested with V_{CC} = V_{CC}max.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Device enters automatic sleep mode when addresses are stable for t_{ACC} + 60 ns. Typical sleep mode current is equal to I_{CC3}.*
5. *Total current during accelerated programming is the sum of V_{ACC} and V_{CC} currents.*
6. *80 MHz applies only to the WS064J.*

19 Test Conditions

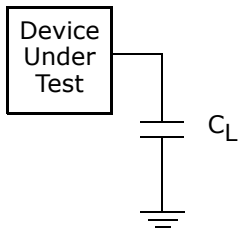
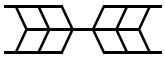


Figure 19.1 Test Setup

Table 19.1 Test Specifications

Test Condition	All Speed Options	Unit
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	2.5 - 3	ns
Input Pulse Levels	0.0–V_{CC}	V
Input timing measurement reference levels	$V_{CC}/2$	V
Output timing measurement reference levels	$V_{CC}/2$	V

20 Key to Switching Waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

21 Switching Waveforms

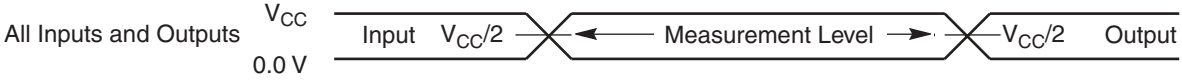


Figure 21.1 Input Waveforms and Measurement Levels

22 AC Characteristics

V_{CC} Power-up

Parameter	Description	Test Setup	Speed	Unit
t_{VCS}	V_{CC} Setup Time	Min	50	µs
t_{RSTH}	RESET# Low Hold Time	Min	50	µs

Notes:
1. *V_{CC} ramp rate is > 1V / 100µs*
2. *V_{CC} ramp rate <1V / 100µs, a Hardware Reset will be required.*

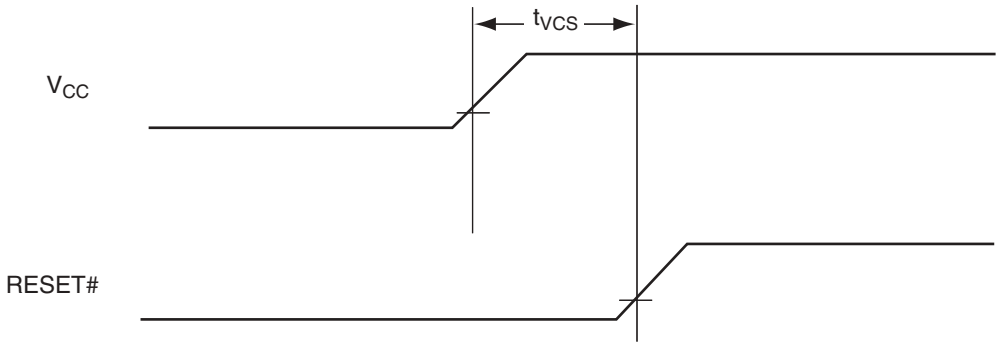
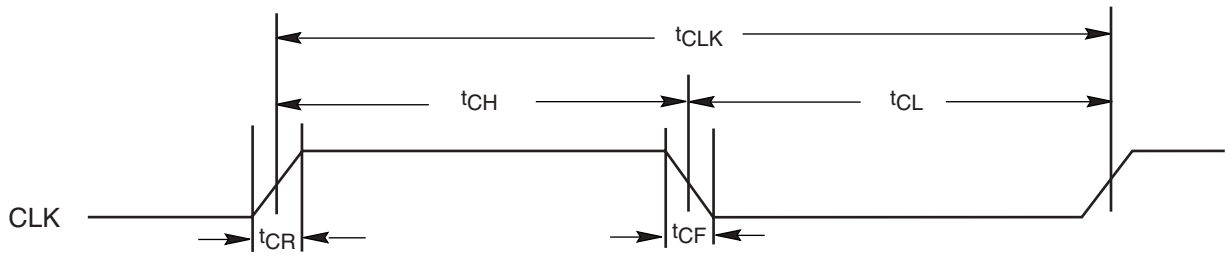


Figure 22.1 V_{CC} Power-up Diagram

22.1 CLK Characterization

Parameter	Description		66 MHz	80 MHz (WaitState=6,7)	80 MHz (WaitState less than 5)	Unit	Condition
f_{CLK}	CLK Frequency	Max	66.0	80.0	66.0	**MHz**	
		Min	15.2	66.0	18.2	**MHz**	continuous burst , CLK duty 50% +/- 10%
		Min	32.0	-	32.0	**KHz**	8/16/32-word burst, CLK duty 50% +/- 10%
t_{CLKH}	CLK high time	Min	39.6	-	33.0	**ns**	continuous burst
		Min	7	5	5	**ns**	8/16/32-word burst
t_{CLKL}	CLK Low Time	Min	7.0	5.0	5.0	**ns**	
t_{CR}	CLK Rise Time	Max	3	2.5	2.5	**ns**	
t_{CF}	CLK Fall Time						

Note: *80 MHz applies only to the WS064J.*



Note: *For WS128J (model numbers 10 and 11), and additional clock cycle is required during boundary crossing while in continuous read mode.*

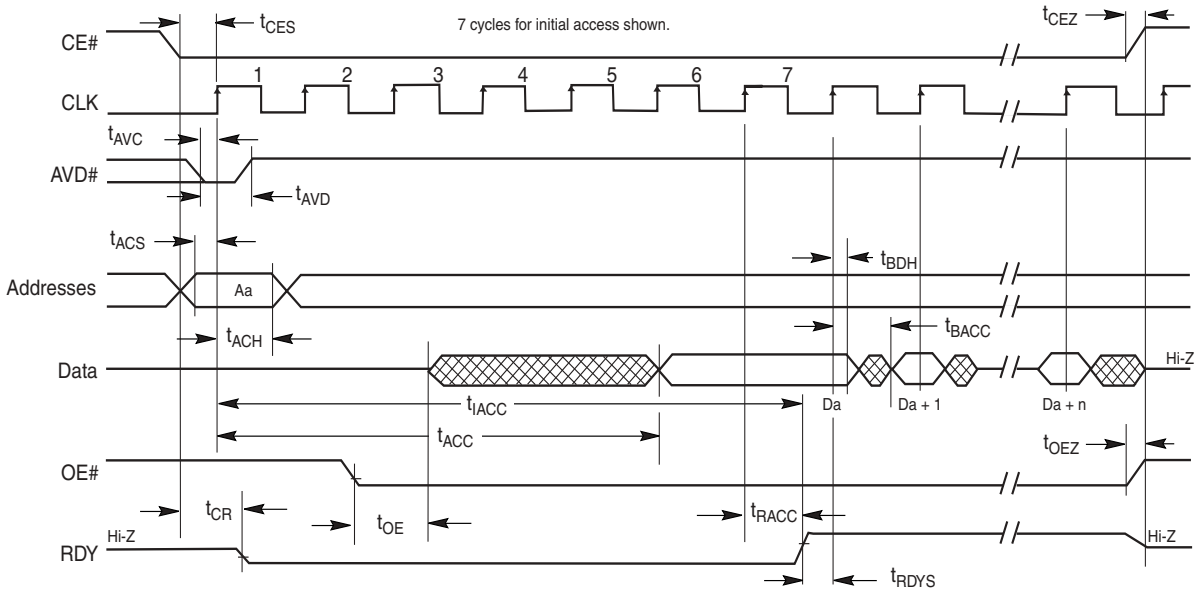
Figure 22.2 CLK Characterization

22.2 Synchronous/Burst Read

Parameter		Description		66 MHz	80 MHz (WS064J only)	Unit
JEDEC	Standard					
	t_{IACC}	Latency (Standard wait-state Handshake mode) for 8-Word and and Continuous 16-Word Burst	Max	56	71	ns
	t_{IACC}	Latency (Standard wait-state Handshake mode) for 32-Word Burst	Max	71	84	ns
	t_{BACC}	Burst Access Time Valid Clock to Output Delay	Max	11.2	9.1	ns
	t_{ACS}	Address Setup Time to CLK (Note 1)	Min	4		ns
	t_{ACH}	Address Hold Time from CLK (Note 1)	Min	5.5		ns
	t_{BDH}	Data Hold Time from Next Clock Cycle	Min	2		ns
	t_{CR}	Chip Enable to RDY Valid	Max	11.2	9.1	ns
	t_{OE}	Output Enable to Output Valid	Max	11.2	9.1	ns
	t_{CEZ}	Chip Enable to High Z	Max	8		ns
	t_{OEZ}	Output Enable to High Z	Max	8		ns
	t_{CES}	CE# Setup Time to CLK	Min	4		ns
	t_{RDYS}	RDY Setup Time to CLK	Min	4		ns
	t_{RACC}	Ready Access Time from CLK	Max	11.2	9.1	ns
	t_{AAS}	Address Setup Time to AVD# (Note 1)	Min	4		ns
	t_{AAH}	Address Hold Time to AVD# (Note 1)	Min	5.5		ns
	t_{CAS}	CE# Setup Time to AVD#	Min	0		ns
	t_{AVC}	AVD# Low to CLK	Min	4		ns
	t_{AVD}	AVD# Pulse	Min	10		ns
	t_{ACC}	Access Time	Max	55	55	ns
	t_{CKA}	CLK to access resume	Max	11.2	9.1	ns
	t_{CKZ}	CLK to High Z	Max	8		ns
	t_{OES}	Output Enable Setup Time	Min	4		ns

Notes:

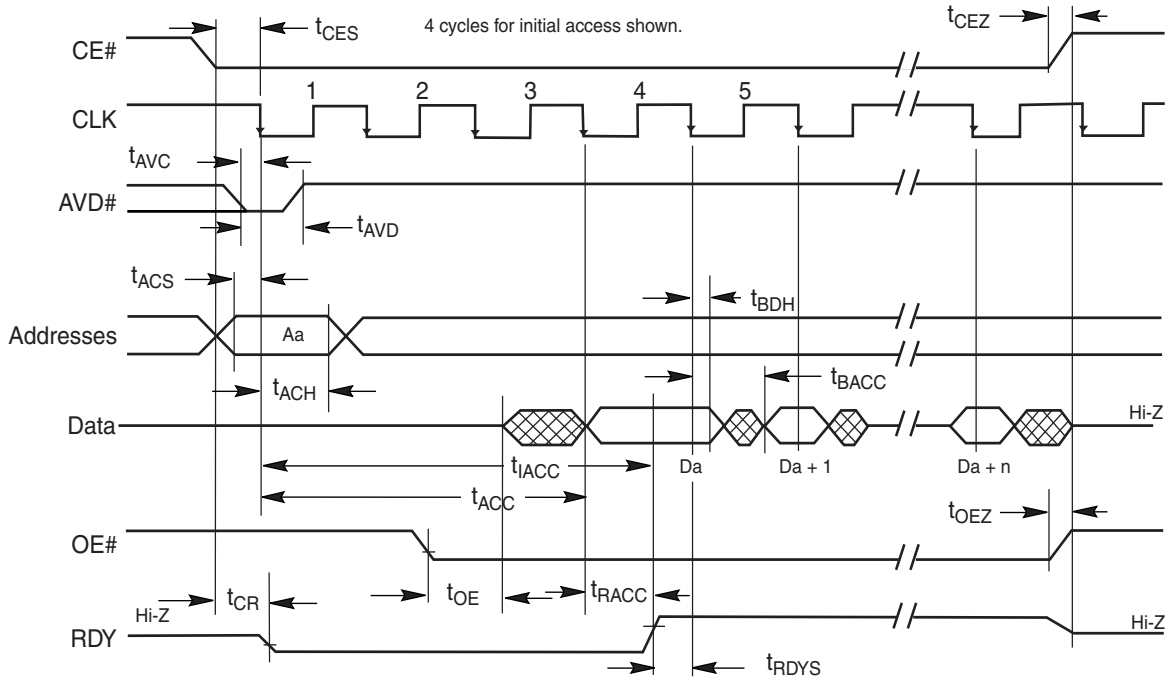
1. *Addresses are latched on the first of either the active edge of CLK or the rising edge of AVD#.*



Notes:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles.*
2. *If any burst address occurs at a 64-word boundary, two additional clock cycle when wait state is set to less than 5 or three additional clock cycle when wait state is set to 6 & 7 are inserted, and is indicated by RDY.*
3. *The device is in synchronous mode.*

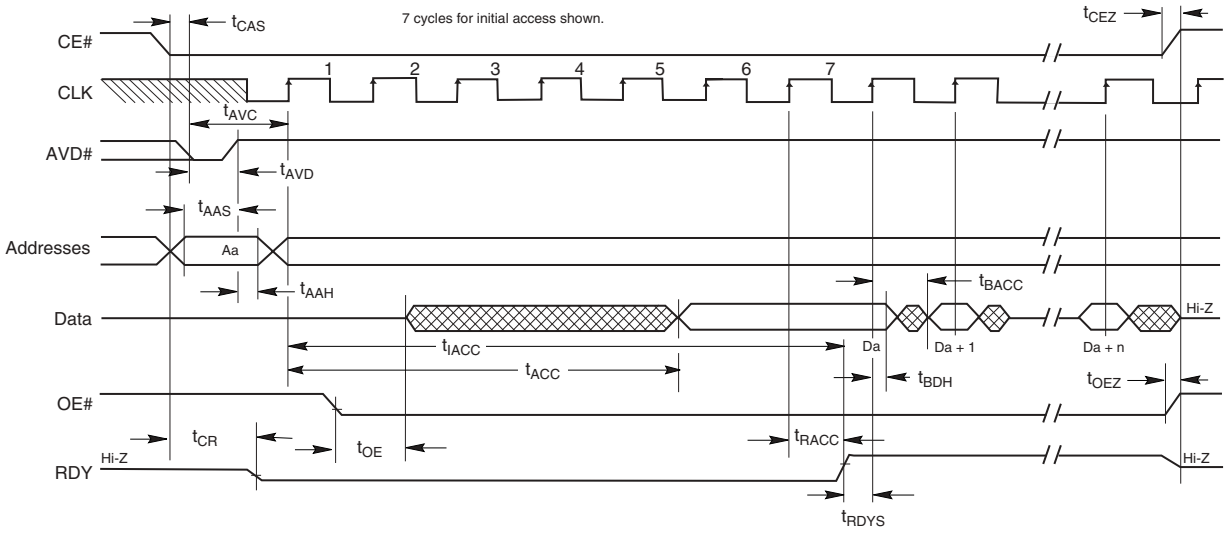
Figure 22.3 CLK Synchronous Burst Mode Read (rising active CLK)



Notes:

1. *Figure shows total number of wait states set to four cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active falling edge.*
2. *If any burst address occurs at a 64-word boundary, two additional clock cycle when wait state is set to less than 5 or three additional clock cycle when wait state is set to 6 & 7 are inserted, clock cycle are inserted, and is indicated by RDY.*
3. *The device is in synchronous mode.*

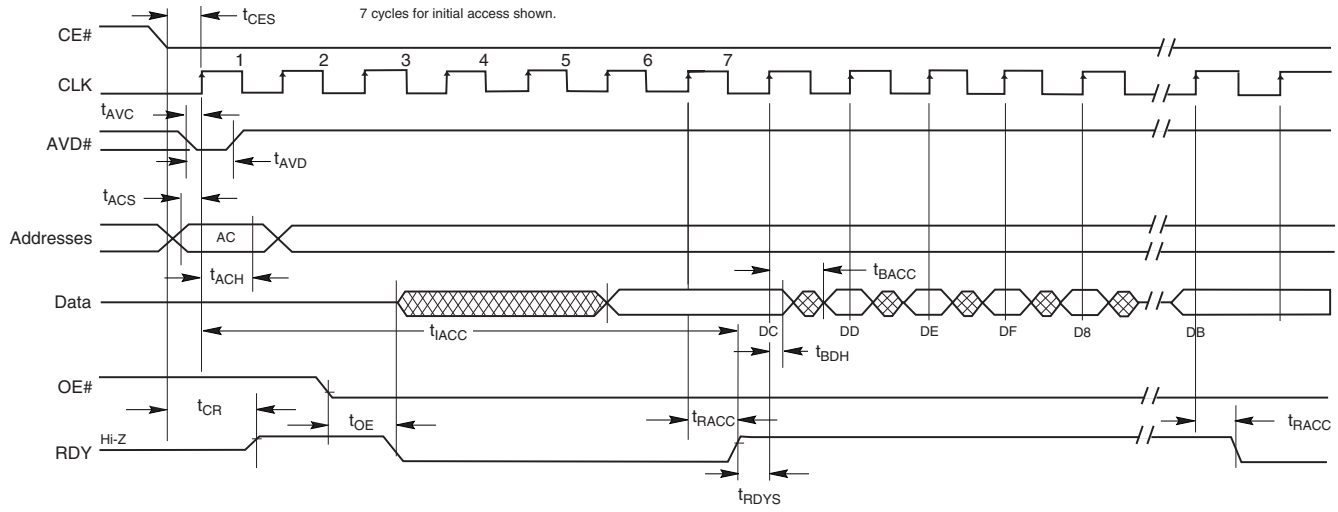
Figure 22.4 CLK Synchronous Burst Mode Read (Falling Active Clock)



Notes:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active rising edge.*
2. *If any burst address occurs at a 64-word boundary, two additional clock cycle are inserted, and is indicated by RDY.*
3. *The device is in synchronous mode.*

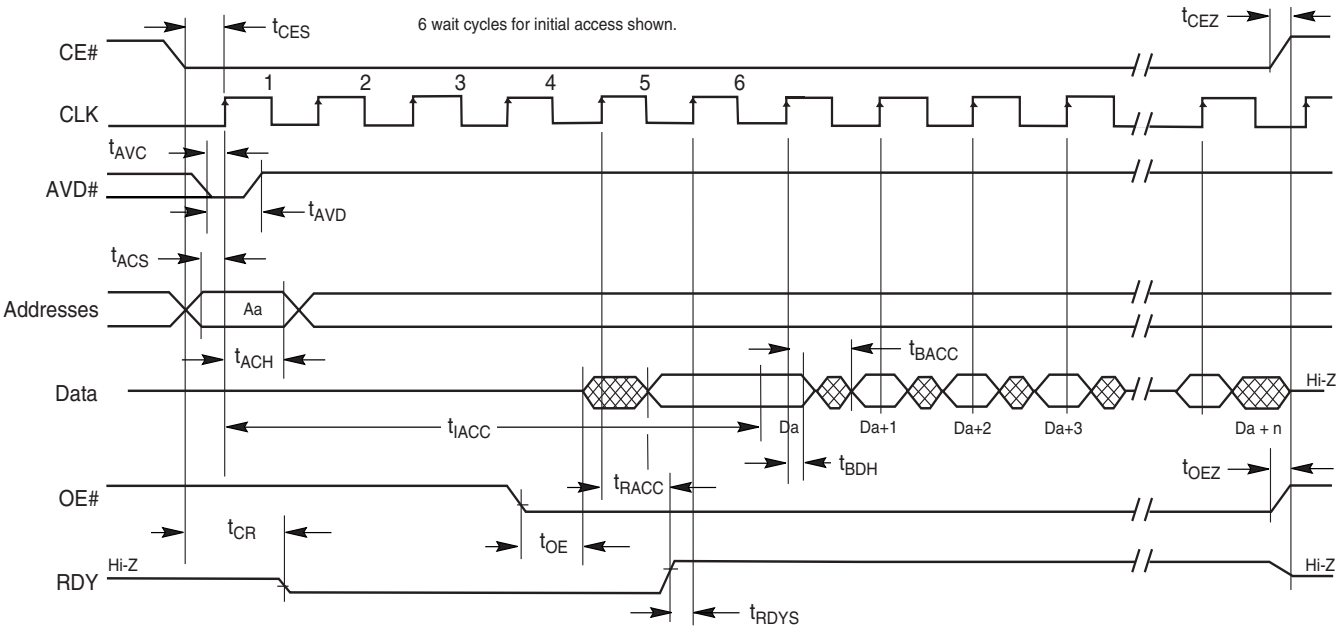
Figure 22.5 Synchronous Burst Mode Read



Notes:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active rising edge.*
2. *If any burst address occurs at a 64-word boundary, two additional clock cycle are inserted, and is indicated by RDY.*
3. *The device is in synchronous mode with wrap around.*
4. *D0-D7 in data waveform indicates the order the data within a given 8-word address range, from lowest to highest. Starting address in figure is the 4th address in range (AC)*

Figure 22.6 8-word Linear Burst with Wrap Around



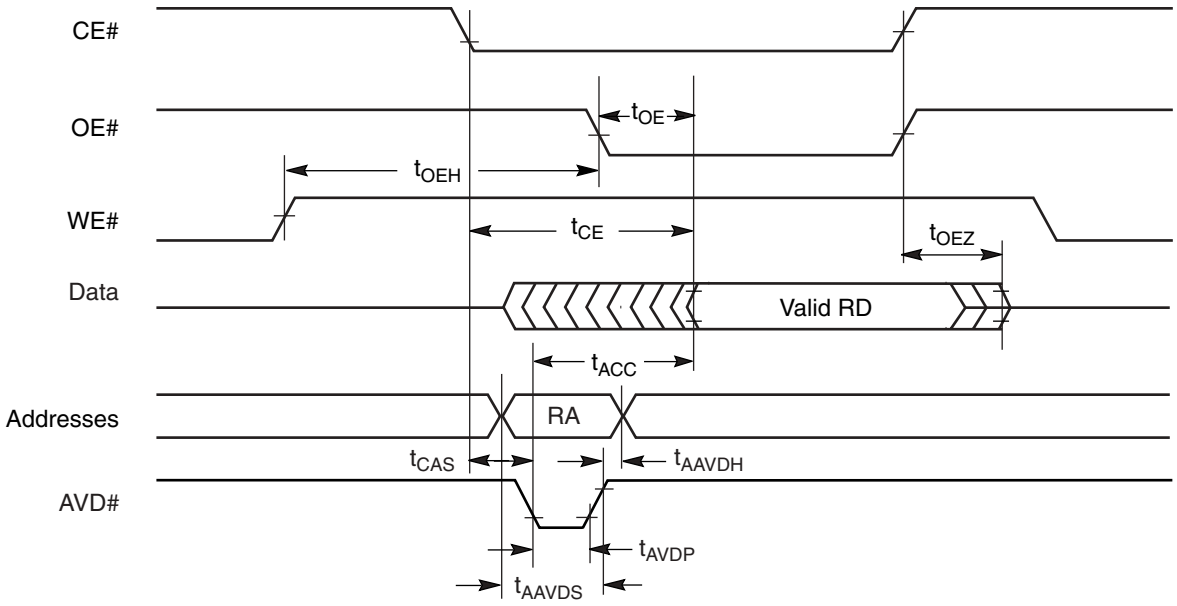
Notes:

1. *Figure assumes 6 wait states for initial access and synchronous read.*
2. *The Set Configuration Register command sequence has been written with A18=0; device will output RDY one cycle before valid data.*

Figure 22.7 Linear Burst with RDY Set One Cycle Before Data

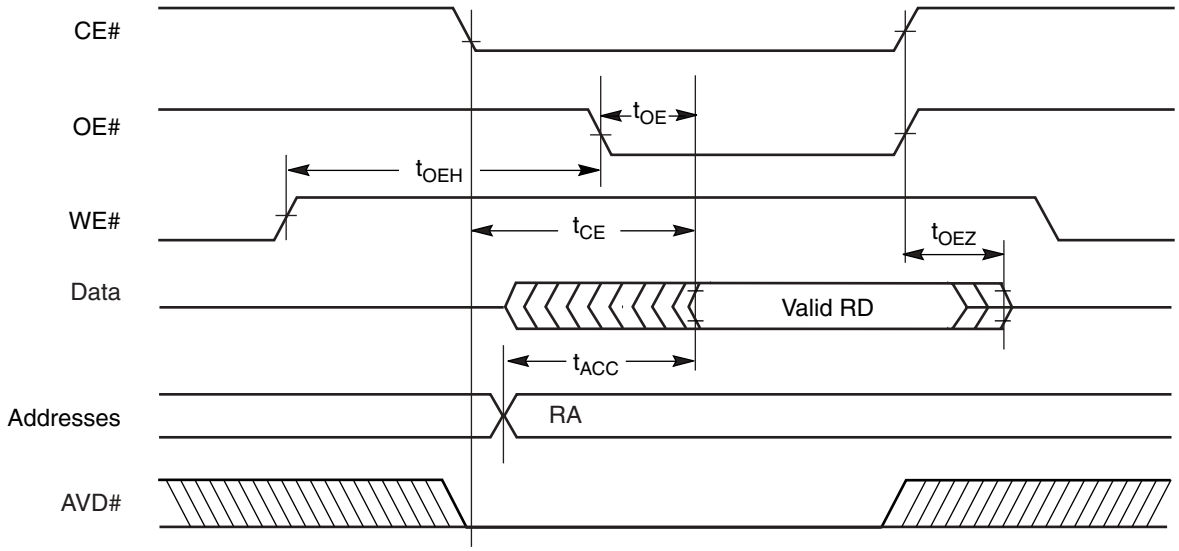
22.3 Asynchronous Mode Read

Parameter		Description			66 MHz	80 MHz (WS064J only)	Unit
JEDEC	Standard						
	t_{CE}	Access Time from CE# Low		Max	55	55	ns
	t_{ACC}	Asynchronous Access Time		Max	55	55	ns
	t_{AVDP}	AVD# Low Time		Min	10		ns
	t_{AAVDS}	Address Setup Time to Rising Edge of AVD		Min	4		ns
	t_{AAVDH}	Address Hold Time from Rising Edge of AVD		Min	5.5		ns
	t_{OE}	Output Enable to Output Valid		Max	11.2	9.1	ns
	t_{OEH}	Output Enable Hold Time	Read	Min	0		ns
			Toggle and Data# Polling	Min	8		ns
	t_{OEZ}	Output Enable to High Z		Max	8		ns
	t_{CAS}	CE# Setup Time to AVD#		Min	0		ns



Note: *RA = Read Address, RD = Read Data.*

Figure 22.8 Asynchronous Mode Read with Latched Addresses



Note: *RA = Read Address, RD = Read Data.*

Figure 22.9 Asynchronous Mode Read

22.4 Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	35	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	200	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs

Note: *Not 100% tested.*

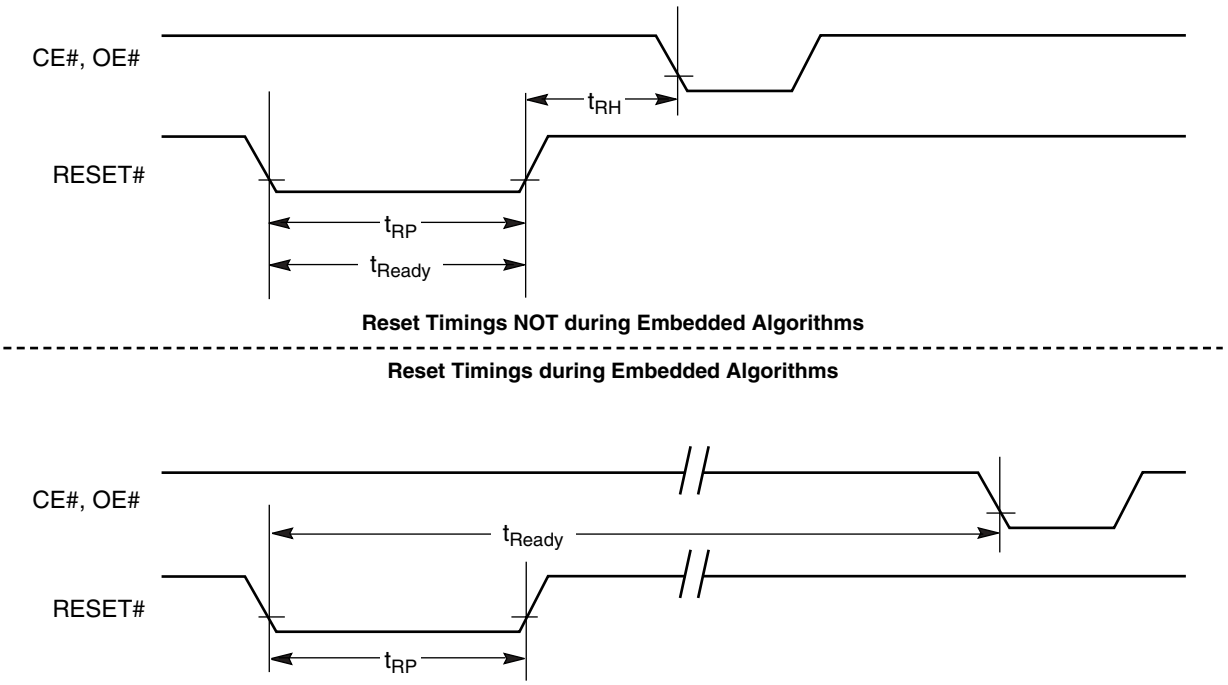


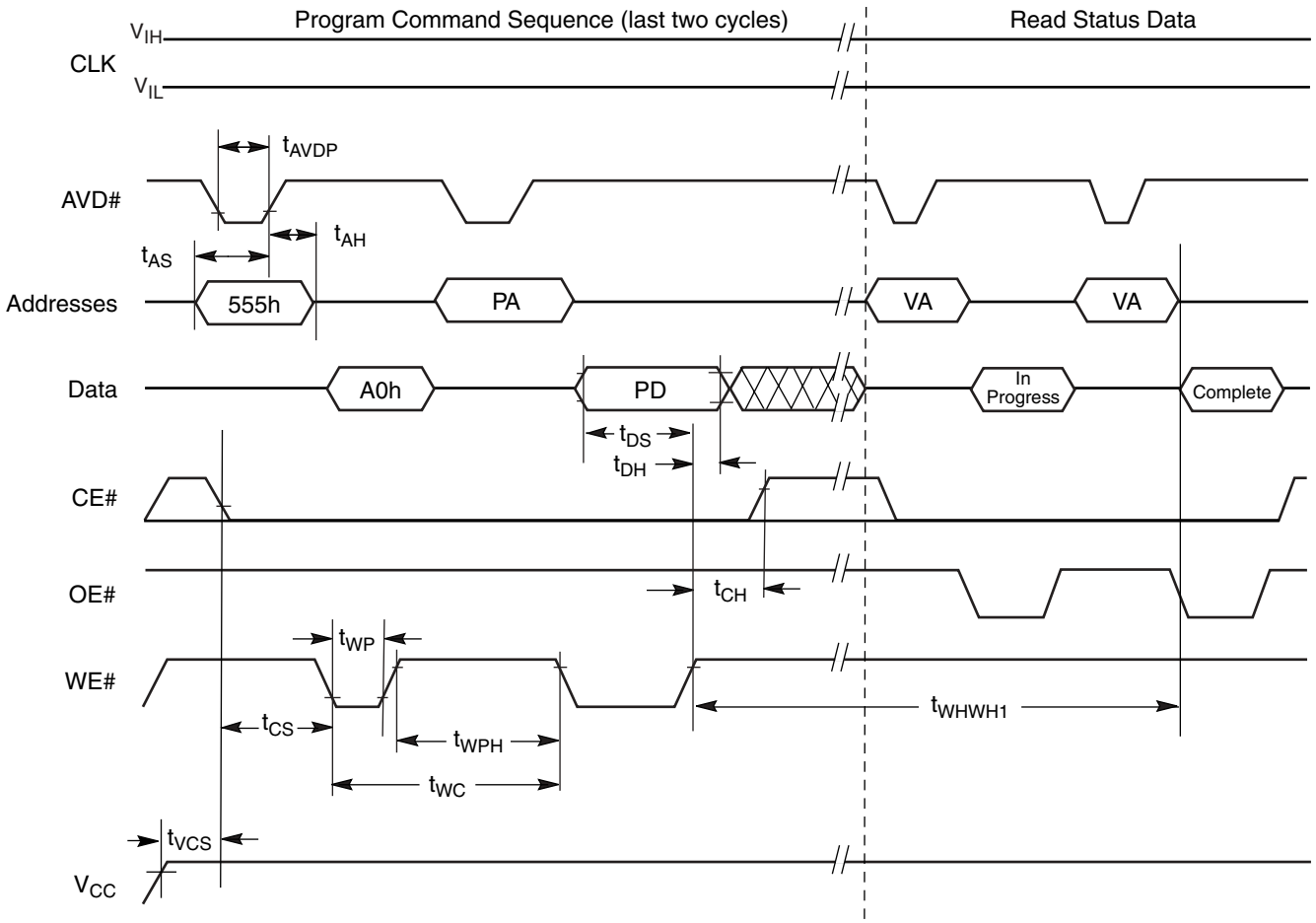
Figure 22.10 Reset Timings

22.5 Erase/Program Operations

Parameter		Description			66 MHz	80 MHz (WS064J only)	Unit
JEDEC	Standard						
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	45		ns
t_{AVWL}	t_{AS}	Address Setup Time (Notes 2, 3)	Synchronous	Min	4		ns
			Asynchronous		0		
t_{WLAX}	t_{AH}	Address Hold Time (Notes 2, 3)	Synchronous	Min	5.5		ns
			Asynchronous		20		
	t_{AVDP}	AVD# Low Time		Min	10		ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	20		ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write		Min	0		ns
	t_{CAS}	CE# Setup Time to AVD#		Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	20		ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	20		ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 4)		Typ	<7		µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation (Note 4)		Typ	<4		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Notes 4, 5)		Typ	<0.2		sec
		Chip Erase Operation (Notes 4, 5)			<104		
	t_{VID}	V_{ACC} Rise and Fall Time		Min	500		ns
	t_{VIDS}	V_{ACC} Setup Time (During Accelerated Programming)		Min	1		µs
	t_{VCS}	V_{CC} Setup Time		Min	50		µs
t_{ELWL}	t_{CS}	CE# Setup Time to WE#		Min	0		ns
	t_{AVSW}	AVD# Setup Time to WE#		Min	4		ns
	t_{AVHW}	AVD# Hold Time to WE#		Min	4		ns
	t_{AVHC}	AVD# Hold Time to CLK		Min	4		ns
	t_{CSW}	Clock Setup Time to WE#		Min	5		ns

Notes:

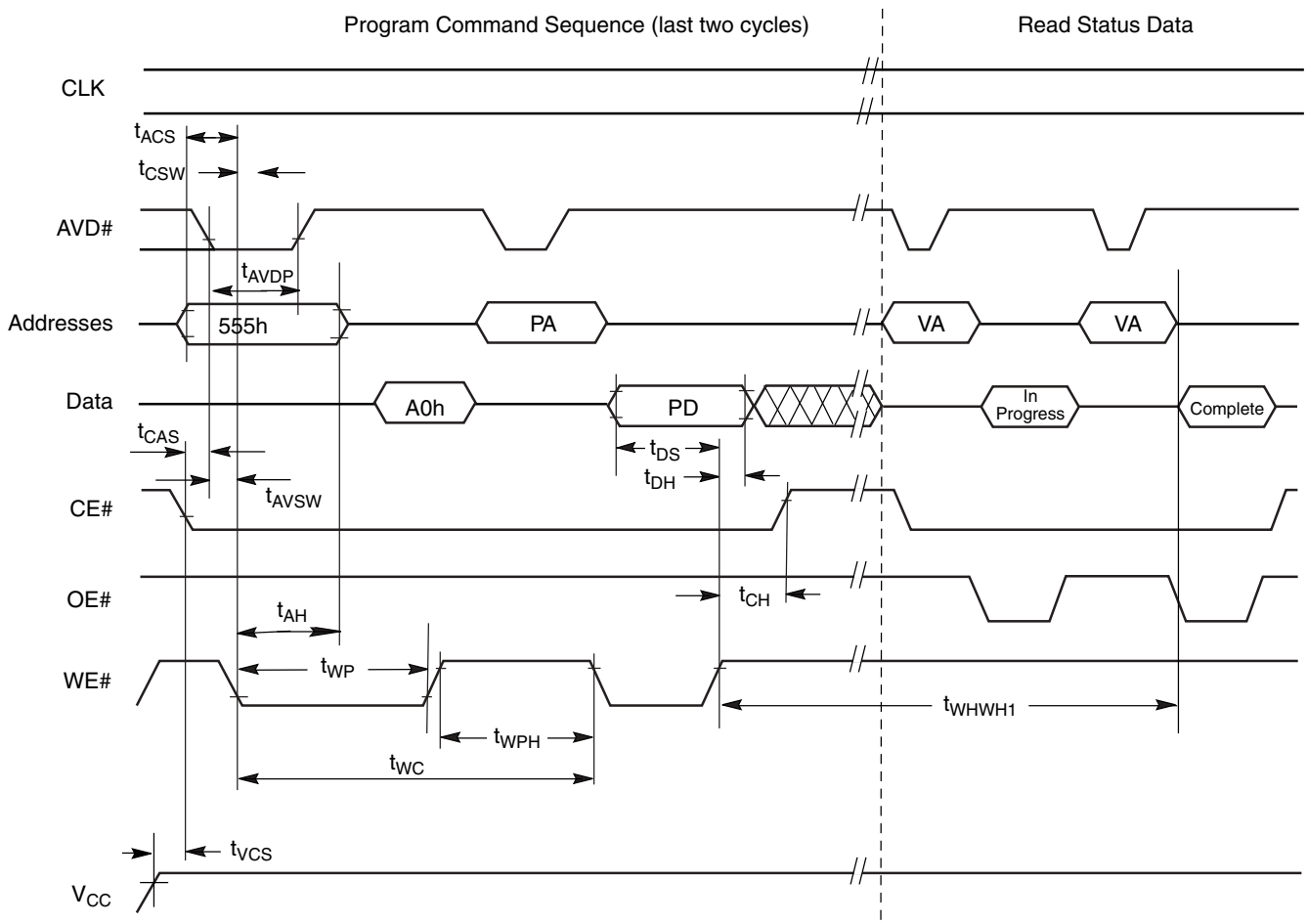
1. *Not 100% tested.*
2. *Asynchronous mode allows both Asynchronous and Synchronous program operation. Synchronous mode allows both Asynchronous and Synchronous program operation.*
3. *In asynchronous program operation timing, addresses are latched on the falling edge of WE# or rising edge of AVD#. In synchronous program operation timing, addresses are latched on the first of either the rising edge of AVD# or the active edge of CLK.*
4. *See the Erase and Programming Performance section for more information.*
5. *Does not include the preprogramming time.*



Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A22–A12 are don't care during command sequence unlock cycles.*
4. *CLK can be either V_{IL} or V_{IH}.*
5. *The Asynchronous programming operation is independent of the Set Device Read Mode bit in the Configuration Register.*

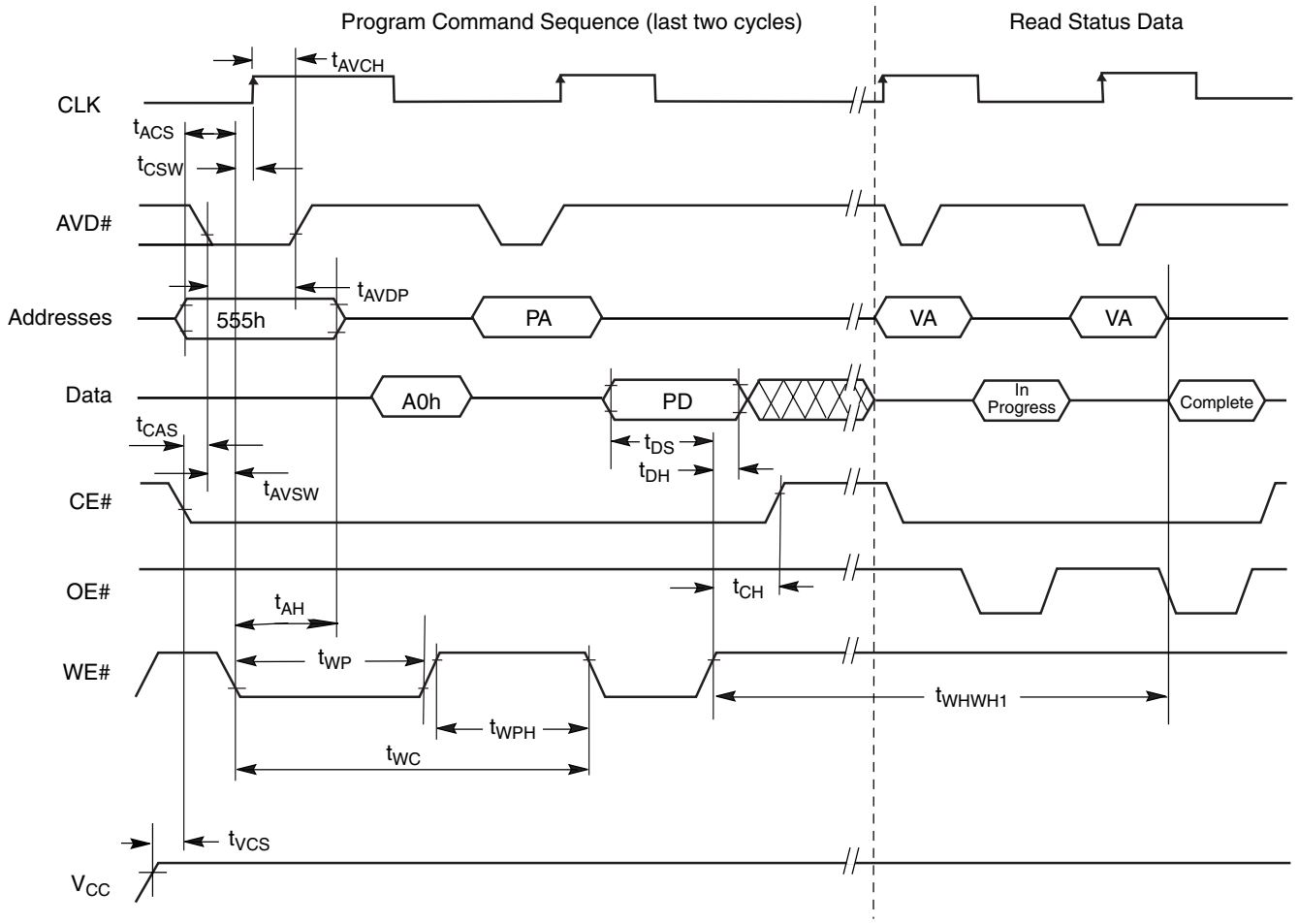
Figure 22.11 Asynchronous Program Operation Timings: AVD# Latched Addresses



Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A22–A12 are don't care during command sequence unlock cycles.*
4. *CLK can be either V_{IL} or V_{IH}.*
5. *The Asynchronous programming operation is independent of the Set Device Read Mode bit in the Configuration Register.*

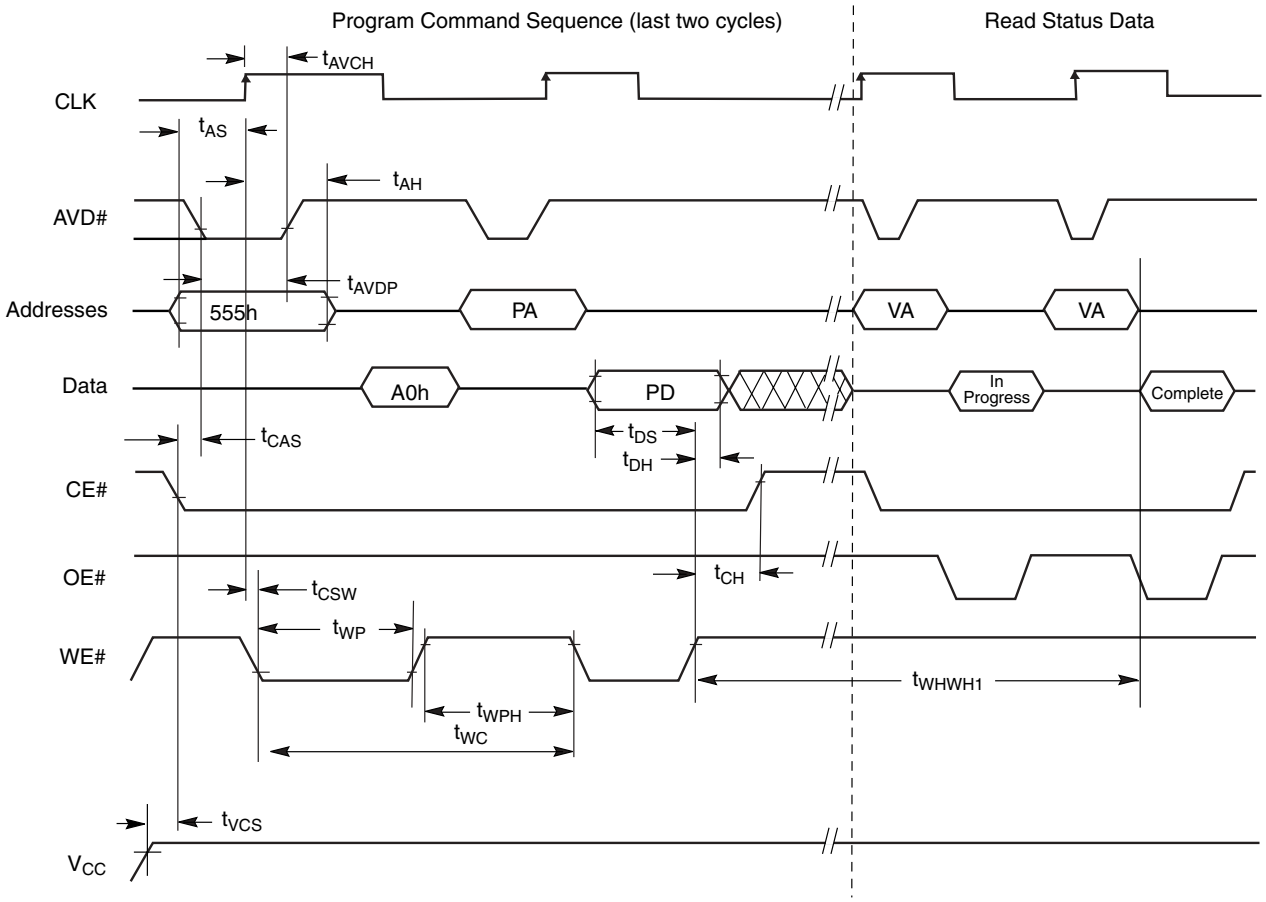
Figure 22.12 Asynchronous Program Operation Timings: WE# Latched Addresses



Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A22–A12 are don't care during command sequence unlock cycles.*
4. *Addresses are latched on the first of either the rising edge of AVD# or the active edge of CLK.*
5. *Either CE# or AVD# is required to go from low to high in between programming command sequences.*
6. *The Synchronous programming operation is dependent of the Set Device Read Mode bit in the Configuration Register. The Configuration Register must be set to the Synchronous Read Mode.*

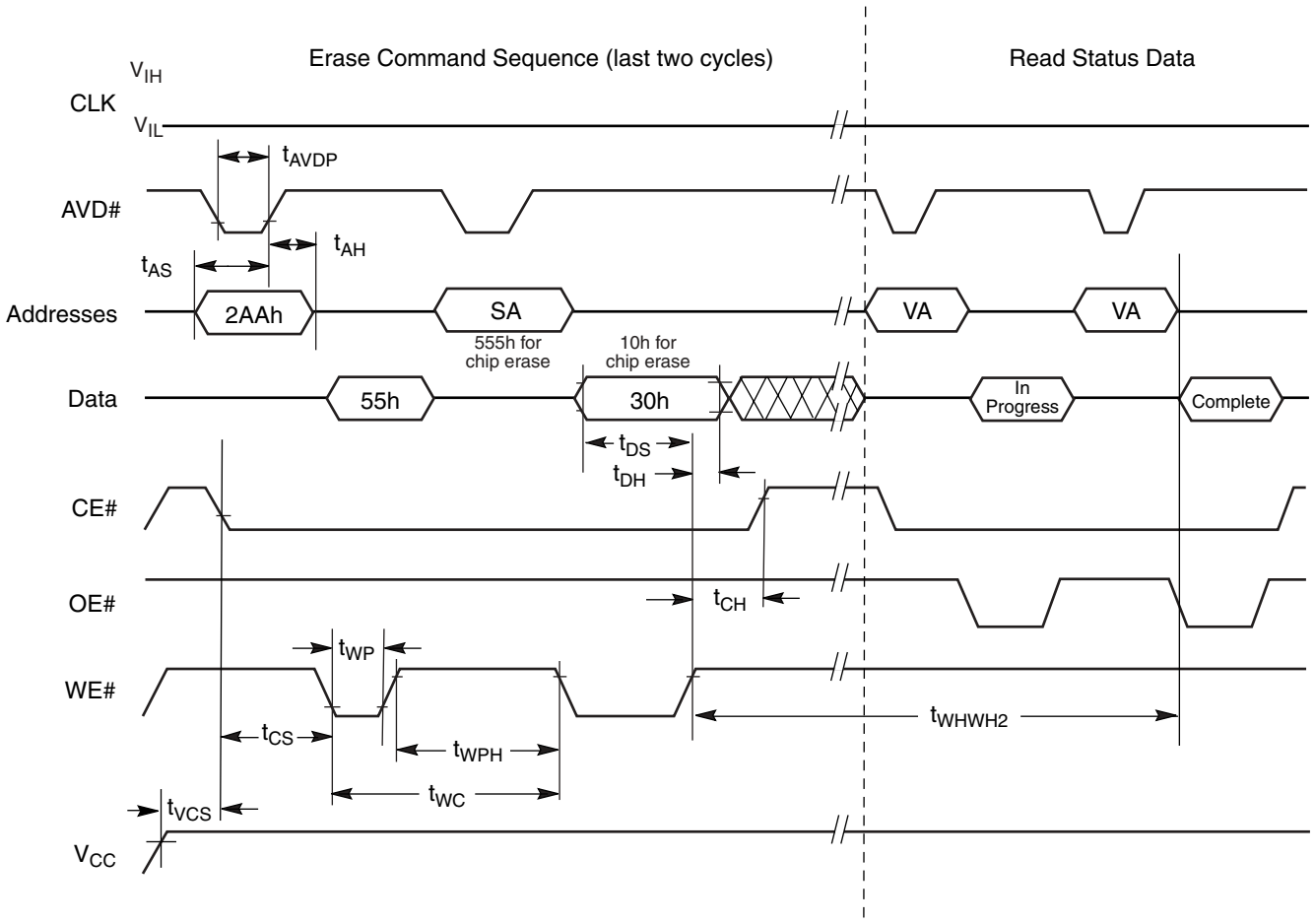
Figure 22.13 Synchronous Program Operation Timings: WE# Latched Addresses



Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A22–A12 are don't care during command sequence unlock cycles.*
4. *Addresses are latched on the first of either the rising edge of AVD# or the active edge of CLK.*
5. *Either CE# or AVD# is required to go from low to high in between programming command sequences.*
6. *The Synchronous programming operation is dependent of the Set Device Read Mode bit in the Configuration Register. The Configuration Register must be set to the Synchronous Read Mode.*

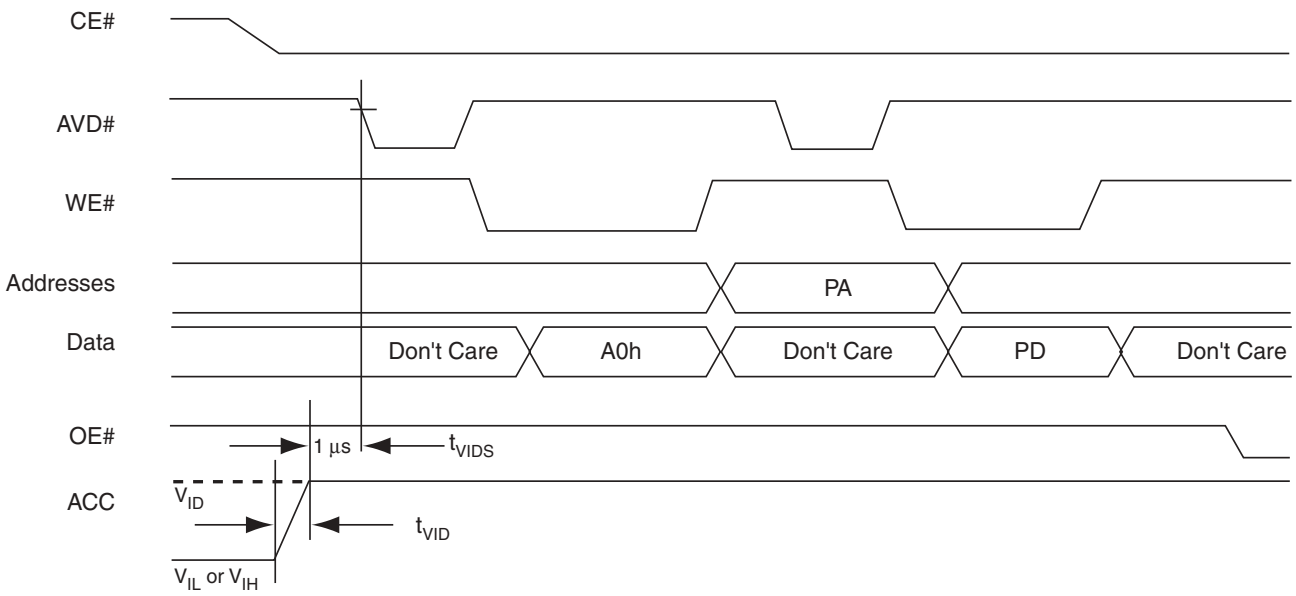
Figure 22.14 Synchronous Program Operation Timings: CLK Latched Addresses



Notes:

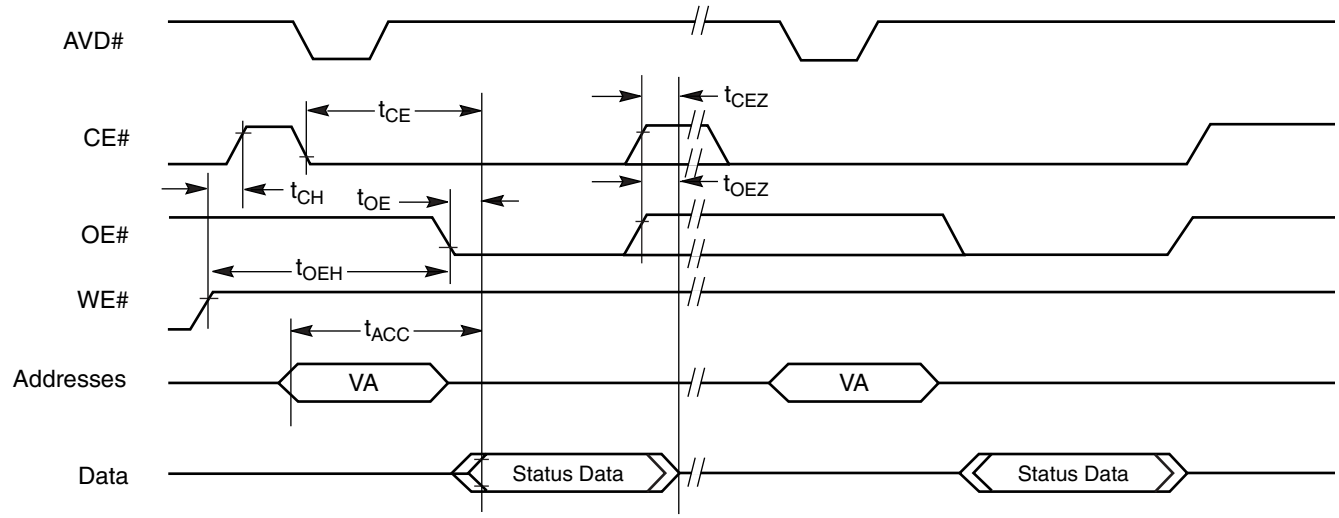
1. *SA is the sector address for Sector Erase.*
2. *Address bits A22–A12 are don't cares during unlock cycles in the command sequence.*

Figure 22.15 Chip/Sector Erase Command Sequence



Note: *Use setup and hold times from conventional program operation.*

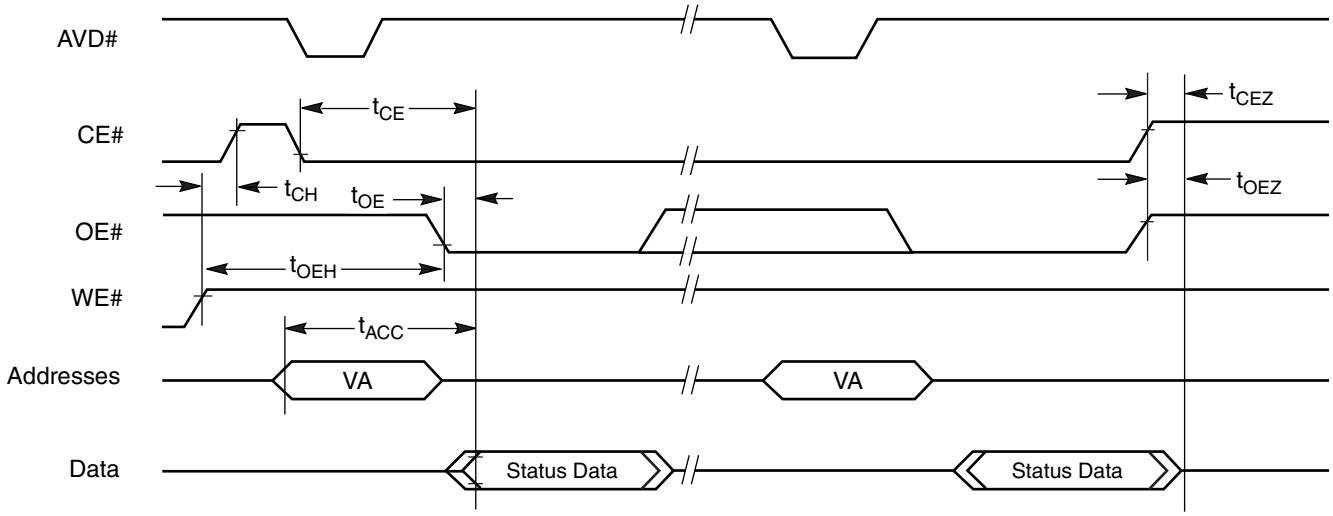
Figure 22.16 Accelerated Unlock Bypass Programming Timing



Notes:

1. *Status reads in figure are shown as asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, and Data# Polling will output true data.*
3. *While in Asynchronous mode, RDY will be low while the device is in embedded erase or programming mode.*

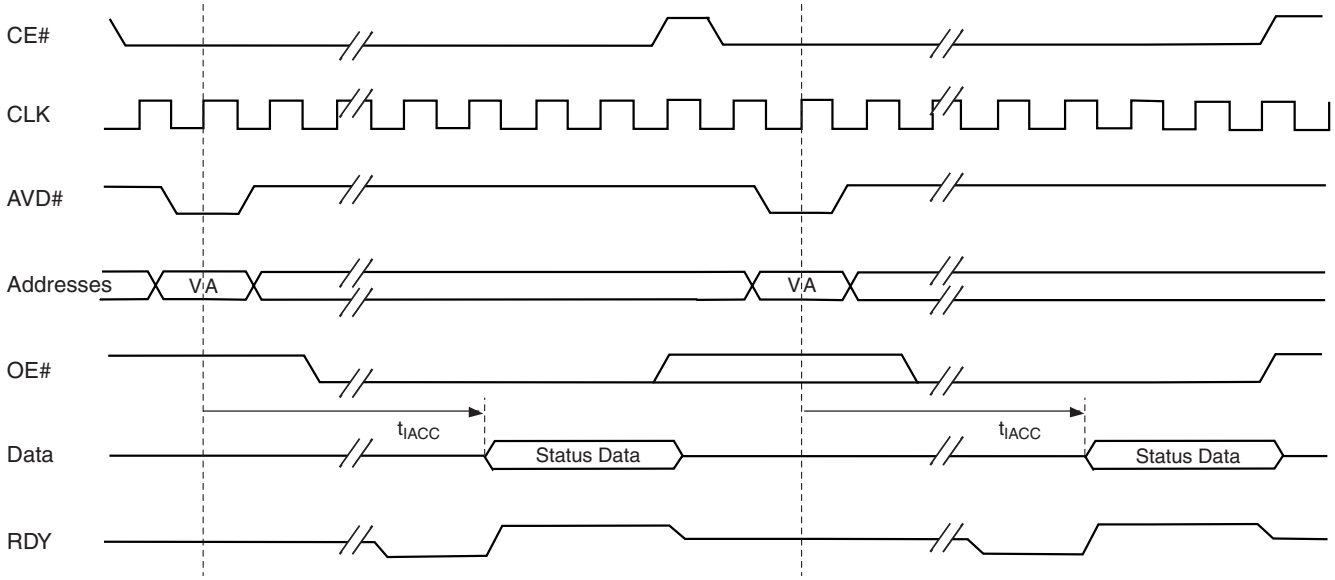
Figure 22.17 Data# Polling Timings (During Embedded Algorithm)



Notes:

1. *Status reads in figure are shown as asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.*
3. *While in Asynchronous mode, RDY will be low while the device is in embedded erase or programming mode.*

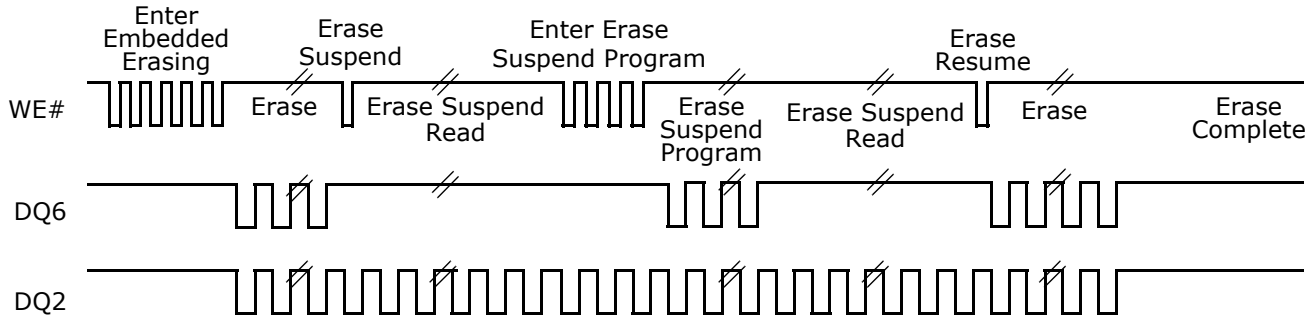
Figure 22.18 Toggle Bit Timings (During Embedded Algorithm)



Notes:

1. *The timings are similar to synchronous read timings.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.*
3. *RDY is active with data (A18 = 0 in the Configuration Register). When A18 = 1 in the Configuration Register, RDY is active one clock cycle before data.*

Figure 22.19 Synchronous Data Polling Timings/Toggle Bit Timings



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 22.20 DQ2 vs. DQ6

22.6 Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min	250	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RDY High for Temporary Sector Unprotect	Min	4	µs

Note: *Not 100% tested.*

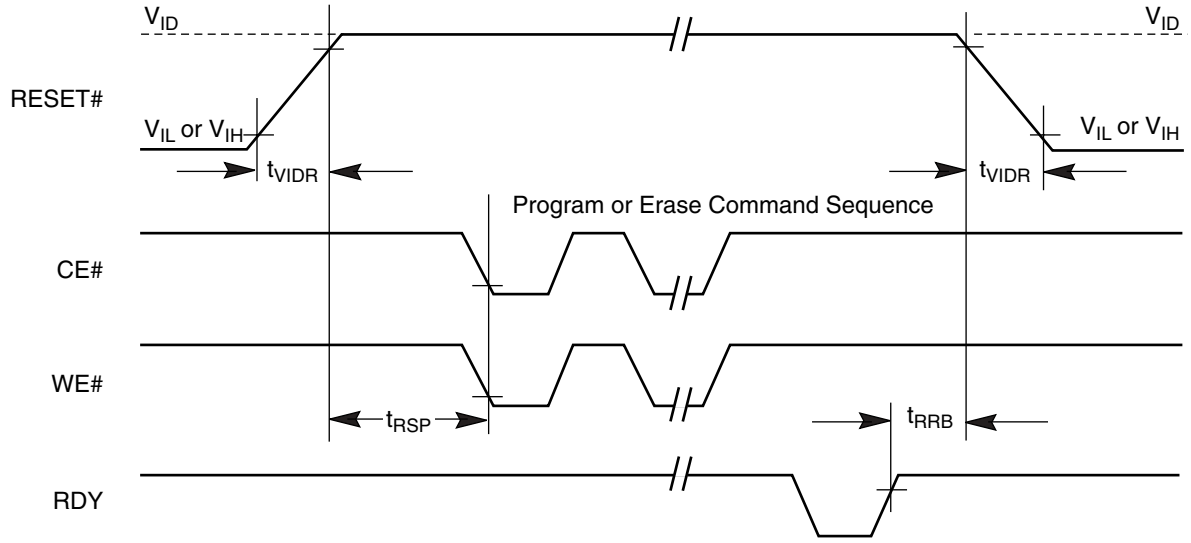
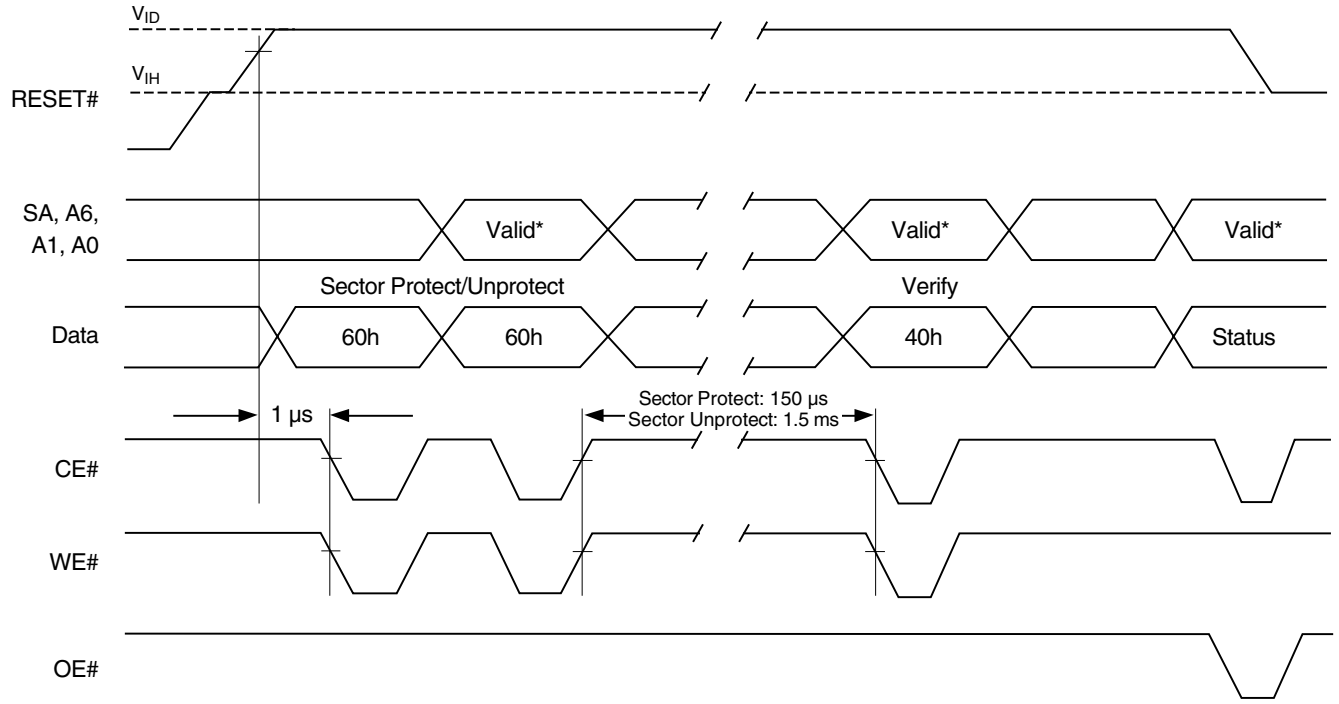
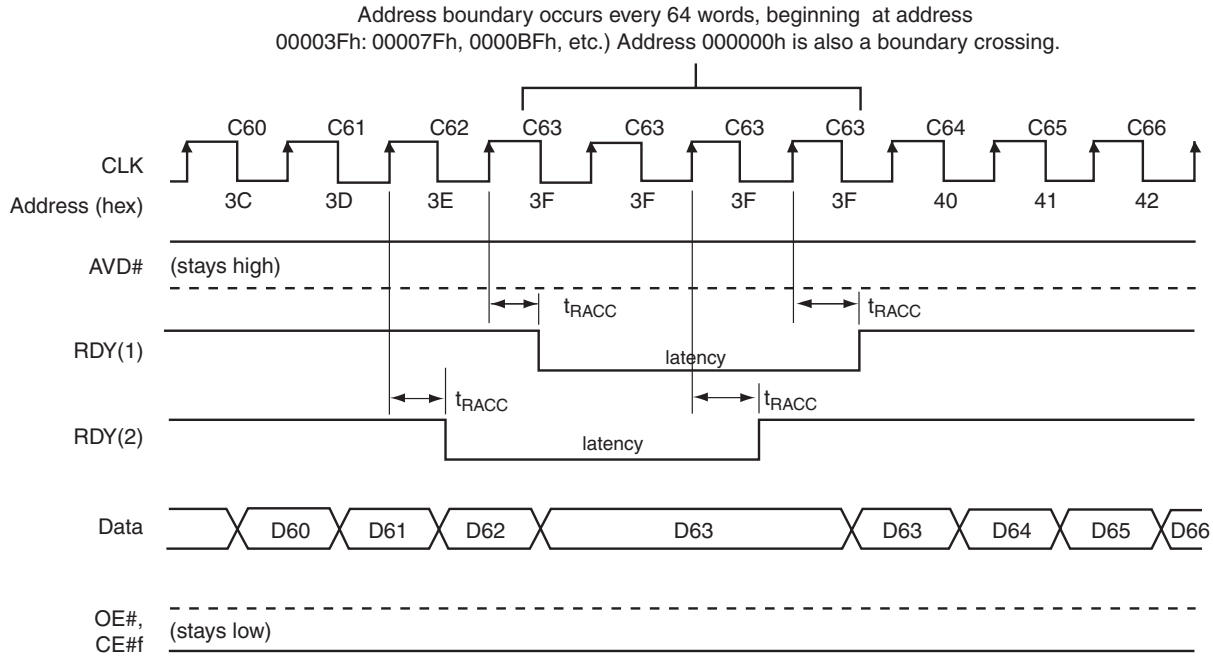


Figure 22.21 Temporary Sector Unprotect Timing Diagram



Note: *For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

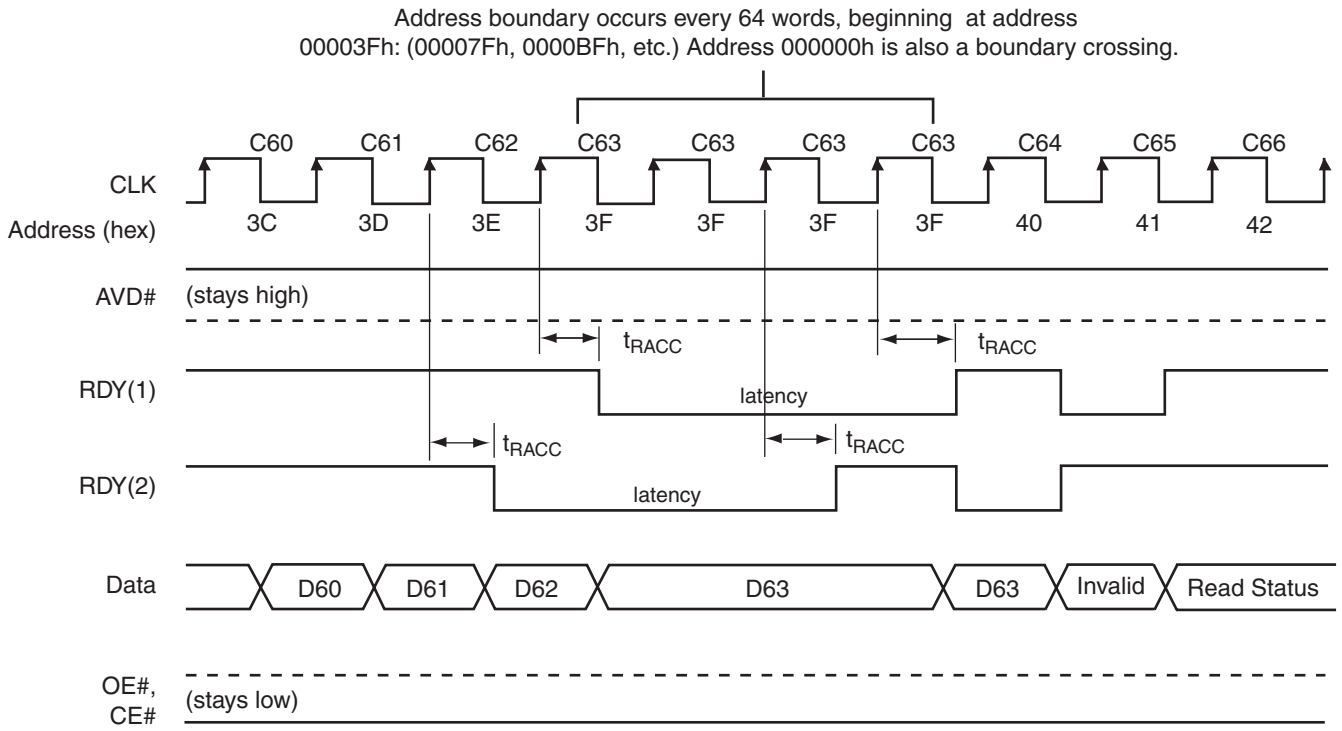
Figure 22.22 Sector/Sector Block Protect and Unprotect Timing Diagram



Notes:

1. *RDY active with data (A18 = 0 in the Configuration Register).*
2. *RDY active one clock cycle before data (A18 = 1 in the Configuration Register).*
3. *Cxx indicates the clock that triggers Dxx on the outputs; for example, C60 triggers D60. Figure shows the device not crossing a bank in the process of performing an erase or program.*
4. *If the starting address latched in is either 3Eh or 3Fh (or some 64 multiple of either), there is no additional 2 cycle latency at the boundary crossing.*

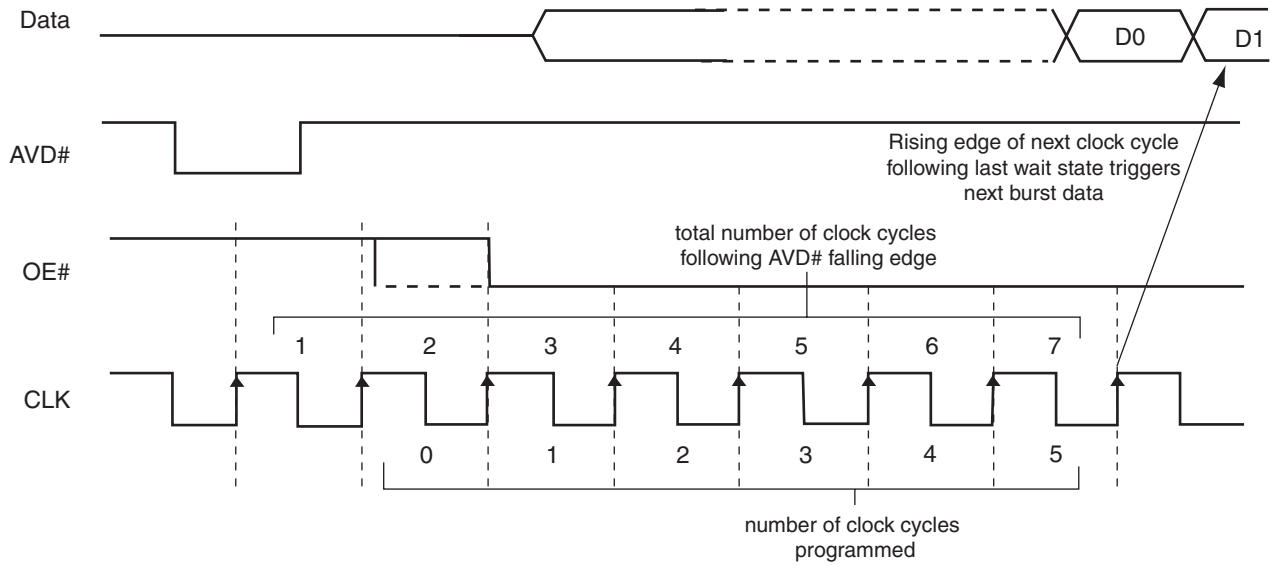
Figure 22.23 Latency with Boundary Crossing



Notes:

1. *RDY active with data (A18 = 0 in the Configuration Register).*
2. *RDY active one clock cycle before data (A18 = 1 in the Configuration Register).*
3. *Cxx indicates the clock that triggers Dxx on the outputs; for example, C60 triggers D60. Figure shows the device crossing a bank in the process of performing an erase or program.*

Figure 22.24 Latency with Boundary Crossing into Program/Erase Bank



Wait State Decoding Addresses:

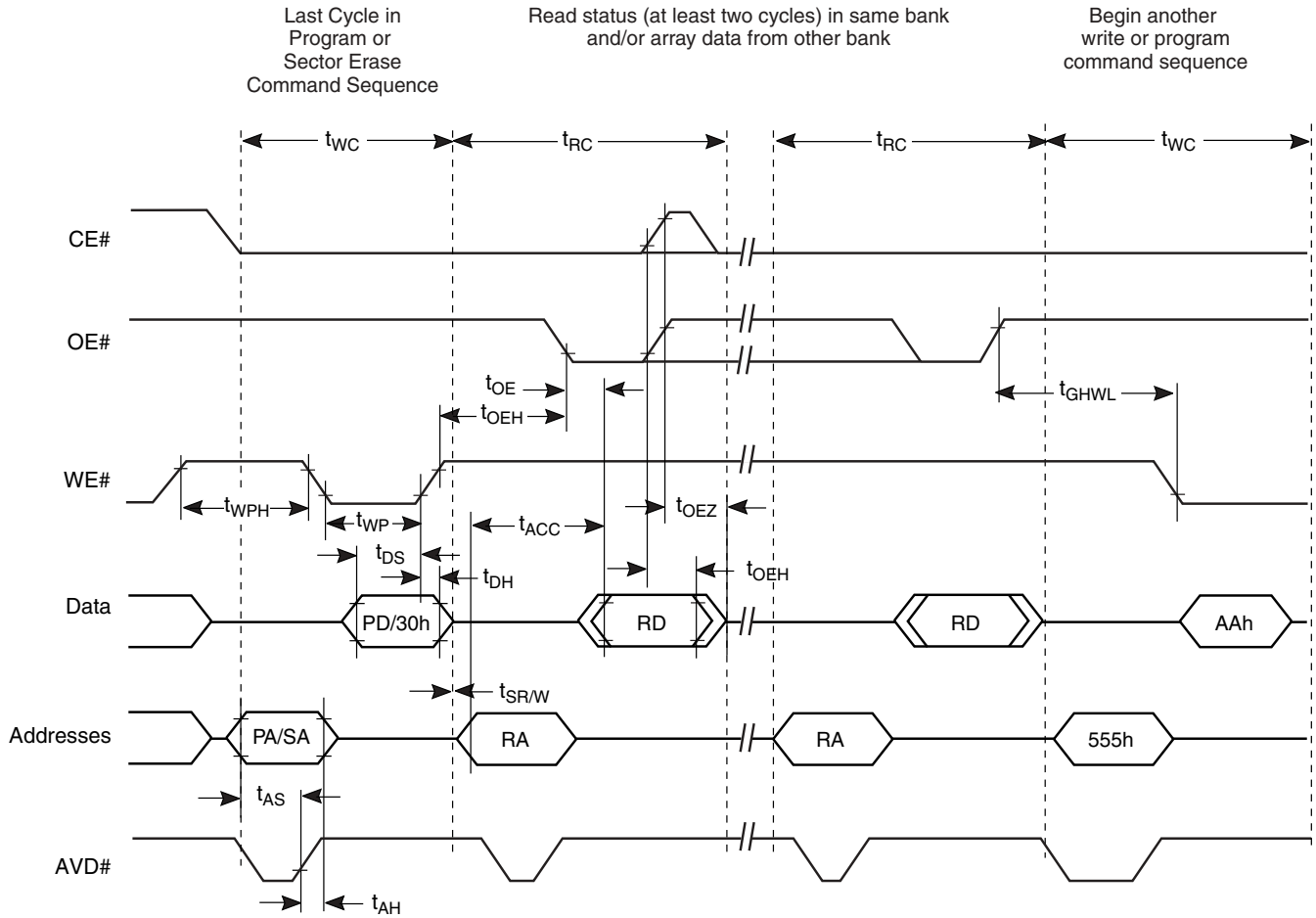
A14, A13, A12 = "111" ⇒ Reserved

A14, A13, A12 = "110" ⇒ Reserved

A14, A13, A12 = "101" ⇒ 5 programmed, 7 total
A14, A13, A12 = "100" ⇒ 4 programmed, 6 total
A14, A13, A12 = "011" ⇒ 3 programmed, 5 total
A14, A13, A12 = "010" ⇒ 2 programmed, 4 total
A14, A13, A12 = "001" ⇒ 1 programmed, 3 total
A14, A13, A12 = "000" ⇒ 0 programmed, 2 total

Note: Figure assumes address D0 is not at an address boundary, active clock edge is rising, and wait state is set to "101".

Figure 22.25 Example of Wait States Insertion



Note: *Breakpoints in waveforms indicate that system may alternately read array data from the "non-busy bank" while checking the status of the program or erase operation in the "busy" bank. The system should read status twice to ensure valid information.*

Figure 22.26 Back-to-Back Read/Write Cycle Timings

23 Erase and Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	32 Kword	<0.4	<2	s	Excludes 00h programming prior to erasure (Note 4)
	4 Kword	<0.2	<2		
Chip Erase Time	128J	<103		s	
	064J	<53			
Word Programming Time		<6	<100	µs	Excludes system level overhead (Note 5)
Accelerated Word Programming Time		<4	<67	µs	
Chip Programming Time (Note 3)	128J	<50.4		s	Excludes system level overhead (Note 5)
	064J	<25.2			
Accelerated Chip Programming Time	128J	<33		s	
	064J	<17			

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 1.8 V V_{CC}, 100K cycles. Additionally, programming typicals assumes a checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 1.65 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 14.5, "Command Definitions," on page 77 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 100,000 cycles.*

24 Flash Revision Summary

24.1 Revision A0 (July 22, 2004)

Initial release.

24.2 Revision A1 (October 6, 2004)

Cosmetic changes.

24.3 Revision A2 (December 10, 2004)

Remove all in terms of 104 MHz speed bin.

Change statement of command during time-out period of sector erase.

Change exit command statement about password program command

Change exit command statement about password protection mode locking bit program command

Change exit command statement about persistentsector protection mode locking bit program command

Change exit command statement about Secured Silicon sector protection bit program command

Change exit command statement about PPB program command

Change exit command statement about All PPB erase command

Change exit command statement about PPB/PPB lock bit status command

Change PPB command table.

Remove note 19 in command table.

Change waveform about boundary crossing.

Remove DC spec output disable status in synchronous read mode.

Change the word from SMPL to PL , from OPBP to OW.

Change the statement PPB Lock Bit Set Command.

Delete V_{IO} pin

Added description at "RDY Configuration" in page56

Modified t_{AH} in Asynchronous mode to 20ns in page89

24.4 Revision A3 (February 19, 2005)

Change "Secsi" to "Secured Silicon"

Add migration statement.

Modify "Sync Latency", "Asyn Access time" @80MHz

Update "Product Selector Guide" on tACC, tCE, tIACC@80MHz

Modify Table 15("Wait States for Standard Wait-state Handshaking")

Change "Supply Voltage" to "1.70V to 1.95V for 80MHz parts

Modify "CLK Characterization" table

24.5 Revision A4 (June 24, 2005)

Added information for "Revision 1" for boundary crossing while in Continuous read mode

Removed all references to WS128J 80 MHz and WS064J Industrial grades

CellularRAM Type 2

64 Megabit
Burst CellularRAM

ADVANCE INFORMATION

Features

- **Single device supports asynchronous, page, and burst operations**
- **V_{CC}, V_{CCQ} Voltages**
  - 1.70 V–1.95 V V_{CC}
  - 1.70 V–3.30 V V_{CCQ}
- **Random Access Time: 70 ns**
- **Burst Mode Write Access**
  - Continuous burst
- **Burst Mode Read Access**
  - 4, 8, or 16 words, or continuous burst
- **Page Mode Read Access**
  - Sixteen-word page size
  - Interpage Read access: 70ns
  - Intrapage Read access: 20ns
- **Low-Power Consumption**
  - Asynchronous Read < 25 mA
  - Intrapage Read < 15 mA
  - Initial access, burst Read < 35 mA
  - Continuous burst Read < 15m A
  - Standby: 120 µA
  - Deep power-down < 10 µA
- **Low-Power Features**
  - Temperature Compensated Refresh (TCR)
  - Partial Array Refresh (PAR)
  - Deep Power-Down (DPD) Mode

General Description

CellularRAM™ products are High-speed, CMOS dynamic random access memories developed for low-power, portable applications. These devices include an industry standard burst mode Flash interface that dramatically increases Read/Write bandwidth compared with other low-power SRAM or Pseudo SRAM offerings.

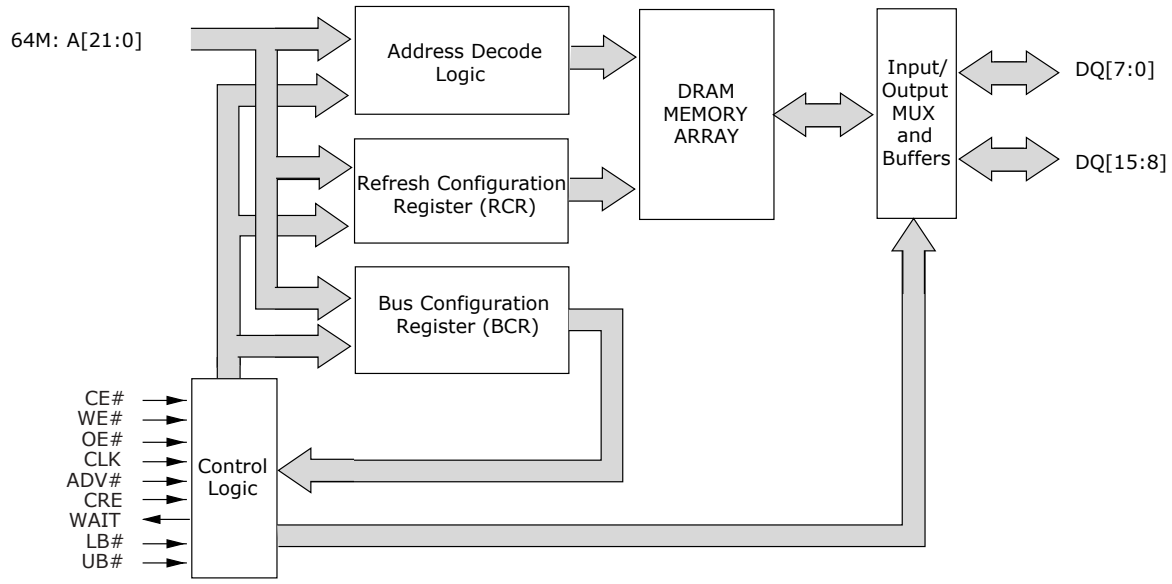
To operate seamlessly on a burst Flash bus, CellularRAM products incorporate a transparent self-refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device Read/Write performance.

Two user-accessible control registers define device operation. The bus configuration register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

Special attention has been focused on standby current consumption during self refresh. CellularRAM products include three mechanisms to minimize standby current. Partial array refresh (PAR) enables the system to limit refresh to only that part of the DRAM array that contains essential data. Temperature compensated refresh (TCR) adjusts the refresh rate to match the device temperature—the refresh rate decreases at lower temperatures to minimize current consumption during standby. Deep power-down (DPD) enables the system to halt the refresh operation altogether when no vital information is stored in the device. The system-configurable refresh mechanisms are accessed through the RCR.

Publication Number CellRam_03 **Revision** A **Amendment** 0 **Issue Date** March 9, 2005

25 Functional Block Diagram



Note: *Functional block diagrams illustrate simplified device operation. See truth table, ball descriptions, and timing diagrams for detailed information.*

Figure 25.1 Functional Block Diagram

Table 25.1 Signal Descriptions

Symbol	Type	Description
64M: A[21:0]	Input	Address Inputs: Inputs for addresses during Read and Write operations. Addresses are internally latched during Read and Write cycles. The address lines are also used to define the value to be loaded into the BCR or the RCR.
CLK	Input	Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK is static (High or Low) during asynchronous access Read and Write operations and during Page Read Access operations.
ADV#	Input	Address Valid: Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV# during asynchronous Read and Write operations. ADV# can be held Low during asynchronous Read and Write operations.
CRE	Input	Configuration Register Enable: When CRE is High, Write operations load the RCR or BCR.
CE#	Input	Chip Enable: Activates the device when Low. When CE# is High, the device is disabled and goes into standby or deep power-down mode.
OE#	Input	Output Enable: Enables the output buffers when Low. When OE# is High, the output buffers are disabled.
WE#	Input	Write Enable: Determines if a given cycle is a Write cycle. If WE# is Low, the cycle is a Write to either a configuration register or to the memory array.
LB#	Input	Lower Byte Enable. DQ[7:0]
UB#	Input	Upper Byte Enable. DQ[15:8]
DQ[15:0]	Input/ Output	Data Inputs/Outputs.
Wait	Output	Wait: Provides data-valid feedback during burst Read and Write operations. The signal is gated by CE#. Wait is used to arbitrate collisions between refresh and Read/Write operations. Wait is asserted when a burst crosses a row boundary. Wait is also used to mask the delay associated with opening a new internal page. Wait is asserted and should be ignored during asynchronous and page mode operations. Wait is High-Z when CE# is High.
V_{CC}	Supply	Device Power Supply: (1.7V–1.95V) Power supply for device core operation.
V_{CCQ}	Supply	I/O Power Supply: (1.7V–3.30V) Power supply for input/output buffers.
V_{SS}	Supply	V_{SS} must be connected to ground.
V_{SSQ}	Supply	V_{SS}Q must be connected to ground.

Note: *The CLK and ADV# inputs can be tied to V_{SS} if the device is always operating in asynchronous or page mode. Wait will be asserted but should be ignored during asynchronous and page mode operations.*

Table 25.2 Bus Operations—Asynchronous Mode

Mode	Power	CLK (Note 1)	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	Wait (Note 2)	DQ[15:0] (Note 3)	Notes
Read	Active	X	L	L	L	H	L	L	Low-Z	Data-Out	4
Write	Active	X	L	L	X	L	L	L	Low-Z	Data-In	4
Standby	Standby	X	X	H	X	X	L	X	High-Z	High-Z	5, 6
No Operation	Idle	X	X	L	X	X	L	X	Low-Z	X	4, 6
Configuration Register	Active	X	L	L	H	L	H	X	Low-Z	High-Z	
DPD	Deep Power-down	X	X	H	X	X	X	X	High-Z	High-Z	7

Notes:

1. *CLK may be High or Low, but must be static during synchronous Read, synchronous Write, burst suspend, and DPD modes; and to achieve standby power during standby and active modes.*
2. *The Wait polarity is configured through the bus configuration register (BCR[10]).*
3. *When LB# and UB# are in select mode (Low), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.*
4. *The device will consume active power in this mode whenever addresses are changed.*
5. *When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.*
6. *V_{IN} = V_{CC}Q or 0V; all device balls must be static (unswitched) to achieve standby current.*
7. *DPD is maintained until RCR is reconfigured.*

Table 25.3 Bus Operations—Burst Mode

Mode	Power	CLK (Note 1)	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	Wait (Note 2)	DQ[15:0] (Note 3)	Notes
Async Read	Active	X	L	L	L	H	L	L	Low-Z	Data-Out	4
Async Write	Active	X	L	L	X	L	L	L	Low-Z	Data-In	4
Standby	Standby	X	X	H	X	X	L	X	High-Z	High-Z	5, 6
No Operation	Idle	X	X	L	X	X	L	X	Low-Z	X	4, 6
Initial Burst Read	Active		L	L	X	H	L	L	Low-Z	Data-Out	4, 8
Initial Burst Write	Active		L	L	H	L	L	X	Low-Z	Data-In	4, 8
Burst Continue	Active		H	L	X	X	L	X	Low-Z	Data-In or Data-Out	4, 8
Burst Suspend	Active	X	X	L	H	X	L	X	Low-Z	High-Z	4, 8
Configuration Register	Active		L	L	H	L	H	X	Low-Z	High-Z	8
DPD	Deep Power-Down	X	X	H	X	X	X	X	High-Z	High-Z	7

Notes:

1. *CLK may be High or Low, but must be static during asynchronous Read, synchronous Write, burst suspend, and DPD modes; and to achieve standby power during standby and active modes.*
2. *The Wait polarity is configured through the bus configuration register (BCR[10]).*
3. *When LB# and UB# are in select mode (Low), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.*
4. *The device will consume active power in this mode whenever addresses are changed.*
5. *When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.*
6. *V_{IN} = V_{CC}Q or 0V; all device balls must be static (unswitched) to achieve standby current.*
7. *DPD is maintained until RCR is reconfigured.*
8. *Burst mode operation is initialized through the bus configuration register (BCR[15]).*

26 Functional Description

The CellularRAM bus interface supports both asynchronous and burst mode transfers. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous Read protocol.

26.1 Power-Up Initialization

CellularRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings (see Table 29.1 and Table 29.4). V_{CC} and V_{CCQ} must be applied simultaneously. When they reach a stable level at or above 1.7V, the device will require 150 µs to complete its self-initialization process. During the initialization period, CE# should remain High. When initialization is complete, the device is Ready for normal operation.

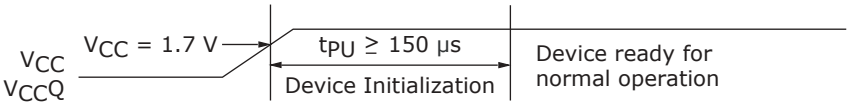


Figure 26.1 Power-Up Initialization Timing

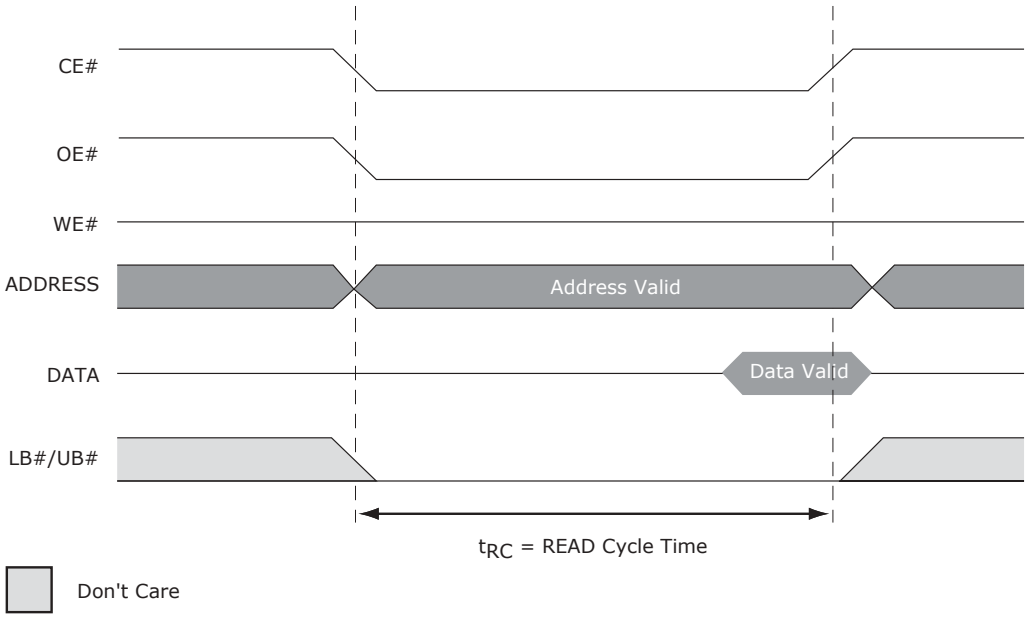
27 Bus Operating Modes

CellularRAM products incorporate a burst mode interface found on Flash products targeting low-power, wireless applications. This bus interface supports asynchronous, page mode, and burst mode Read and Write transfers. The specific interface supported is defined by the value loaded into the BCR. Page mode is controlled by the refresh configuration register (RCR[7]).

27.1 Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry standard SRAM control bus (CE#, OE#, WE#, LB#/ UB#). Read operations (Figure 27.1) are initiated by bringing CE#, OE#, and LB#/UB# Low while keeping WE# High. Valid data will be driven out of the I/Os after the specified access time has elapsed. Write operations (Figure 27.2) occur when CE#, WE#, and LB#/ UB# are driven Low. During asynchronous Write operations, the OE# level is a *don't care*, and WE# will override OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). Asynchronous operations (page mode disabled) can either use the ADV input to latch the address, or ADV can be driven Low during the entire Read/Write operation.

During asynchronous operation, the CLK input must be held static (High or Low, no transitions). Wait will be driven while the device is enabled and its state should be ignored. WE# low time must be limited to t_{CEM}.



Note: *ADV must remain Low for page mode operation.*

Figure 27.1 Read Operation (ADV# Low)

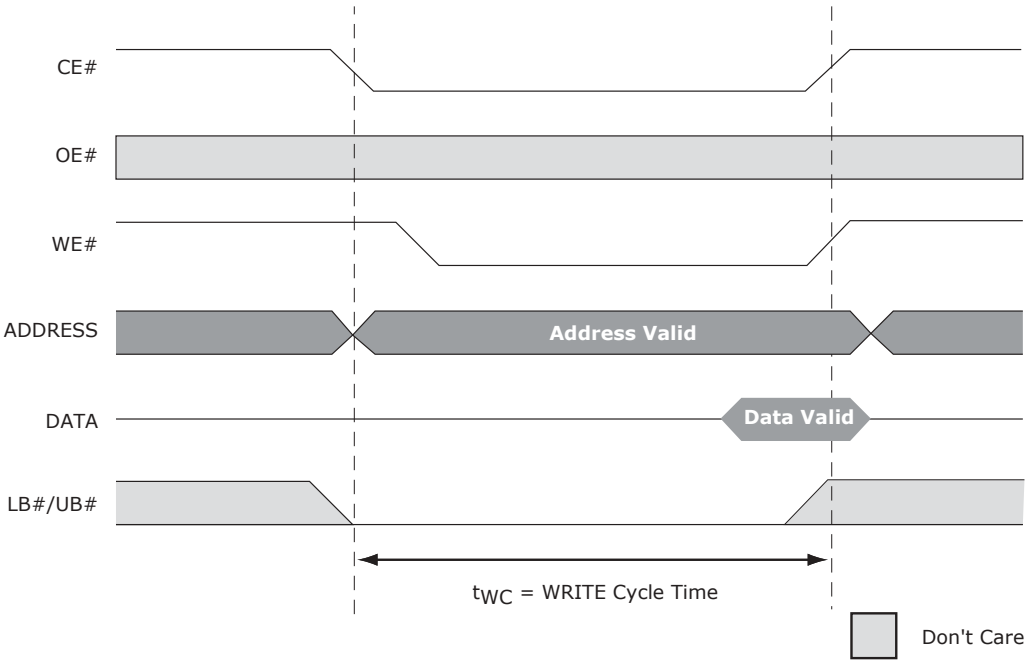


Figure 27.2 Write Operation (ADV# Low)

27.2 Page Mode Read Operation

Page mode is a performance-enhancing extension to the legacy asynchronous Read operation. In page mode-capable products, an initial asynchronous Read access is performed, then adjacent addresses can be Read quickly by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Addresses A[4] and higher must remain fixed during the entire page mode access. Figure 27.3 shows the timing for a page mode access. Page mode takes advantage of the fact that adjacent addresses can be Read in a shorter period of time than random addresses. Write operations do not include comparable page mode functionality.

During asynchronous page mode operation, the CLK input must be static (HIGH or LOW - no transitions). CE# must be driven High upon completion of a page mode access. WAIT is driven while the device is enabled and its state should be ignored. Page mode is enabled by setting RCR[7] to High. ADV must be driven Low during all page mode Read accesses. The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than t_{CEM}.

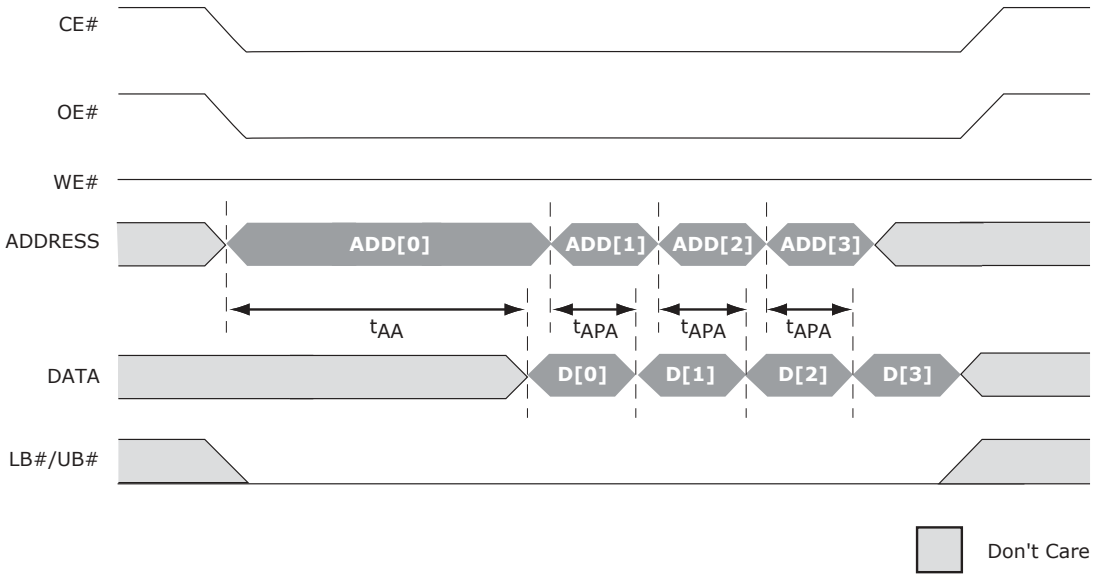


Figure 27.3 Page Mode Read Operation (ADV# Low)

27.3 Burst Mode Operation

Burst mode operations enable High-speed synchronous Read and Write operations. Burst operations consist of a multi-clock sequence that must be performed in an ordered fashion. After CE# goes Low, the address to access is latched on the rising edge of the next clock that ADV# is Low. During this first clock rising edge, WE# indicates whether the operation is going to be a Read (WE# = High, Figure 27.4) or Write (WE# = Low, Figure 27.5).

The size of a burst can be specified in the BCR either as a fixed length or continuous. Fixed-length bursts consist of four, eight, or sixteen words. Continuous bursts have the ability to start at a specified address and burst through the entire memory.

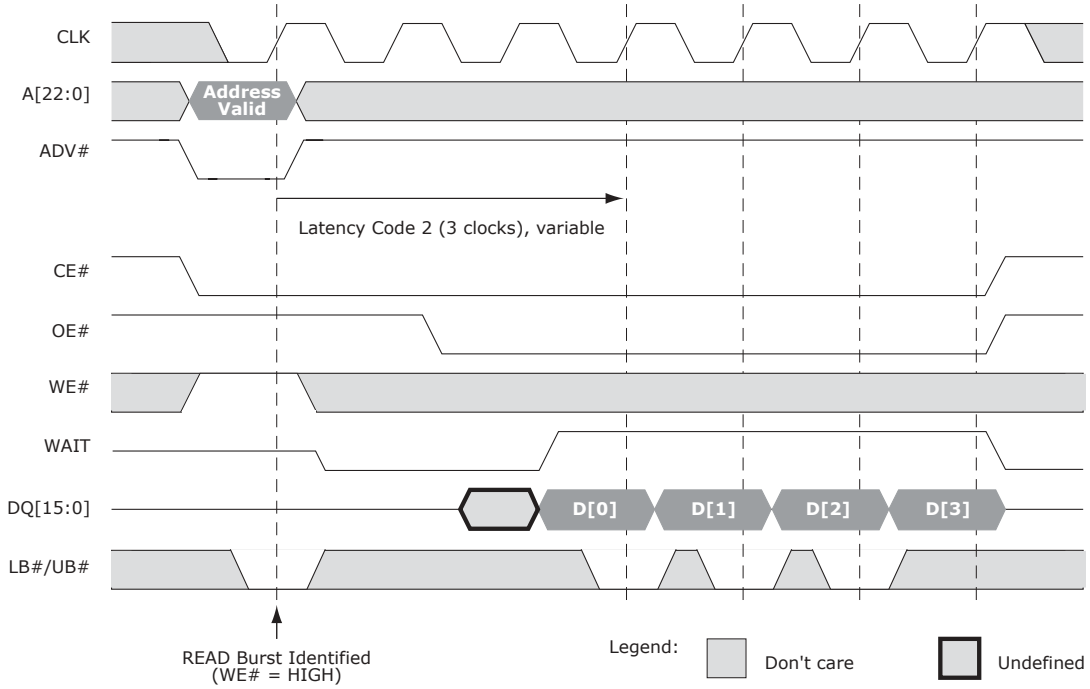
The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and CellularRAM device.

The WAIT output is asserted as soon as CE# goes LOW, and is de-asserted to indicate when data is to be transferred into (or out of) the memory. WAIT is again asserted if the burst crosses the boundary between 128-word rows. Once the CellularRAM device has restored the previous row's

data and accessed the next row, Wait will be deasserted and the burst can continue (see Figure 33.9).

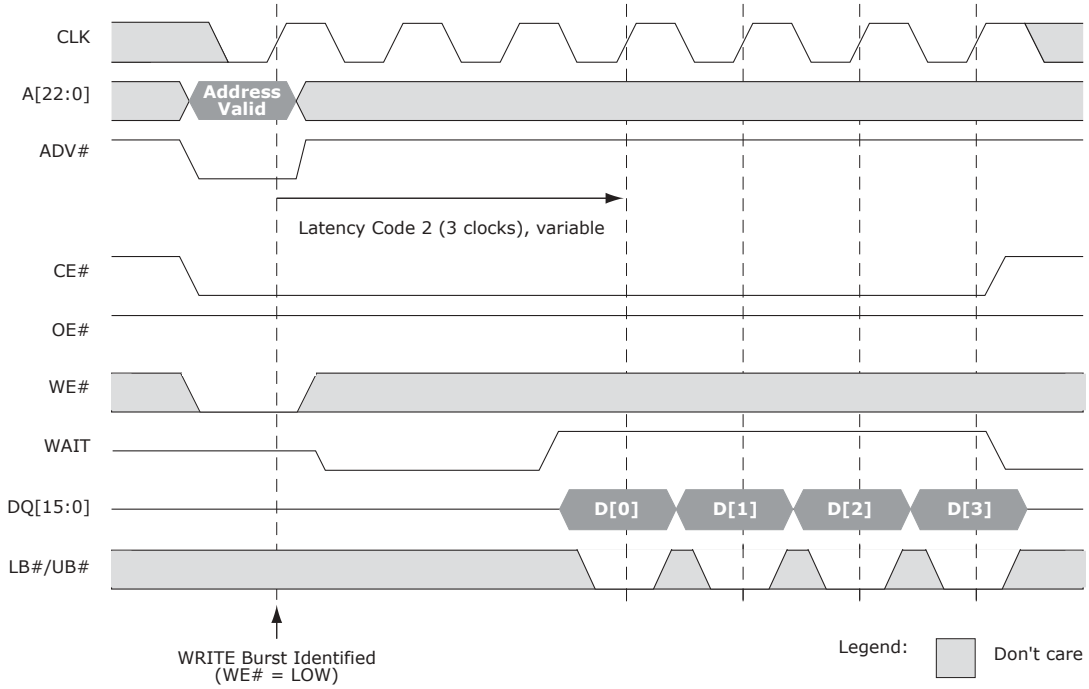
To access other devices on the same bus without the timing penalty of the initial latency for a new burst, burst mode can be suspended. Bursts are suspended by stopping CLK. CLK can be stopped High or Low. If another device will use the data bus while the burst is suspended, OE# should be taken High to disable the CellularRAM outputs; otherwise, OE# can remain Low. Note that the Wait output will continue to be active, and as a result no other devices should directly share the Wait connection to the controller. To continue the burst sequence, OE# is taken Low, then CLK is restarted after valid data is available on the bus.

The CE# low time is limited by refresh considerations. CE# must not stay low longer than t_{CEM} unless row boundaries are crossed at least every t_{CEM}. If a burst suspension causes CE# to remain Low for longer than t_{CEM}, CE# should be taken High and the burst restarted with a new CE# Low/ ADV# low cycle.



Note: *Non-default BCR settings: Variable latency; latency code two (three clocks); Wait active Low; Wait asserted during delay.*

Figure 27.4 Burst Mode Read (4-word burst)



Note: *Non-default BCR settings: Variable latency; latency code two (three clocks); Wait active Low; Wait asserted during delay.*

Figure 27.5 Burst Mode Write (4-word burst)

27.4 Mixed-Mode Operation

The device can support a combination of synchronous Read and asynchronous Write operations when the BCR is configured for synchronous operation. The asynchronous Write operation requires that the clock (CLK) remain static (High or Low) during the entire sequence. The ADV# signal can be used to latch the target address, or it can remain Low during the entire Write operation. CE# can remain Low when transitioning between mixed-mode operations with fixed latency enabled. Note that the t_{CKA} period is the same as a Read or Write cycle. This time is required to ensure adequate refresh. Mixed-mode operation facilitates a seamless interface to legacy burst mode Flash memory controllers. See Figure 33.17, Asynchronous Write Followed by Burst Read (timing diagram).

27.5 Wait Operation

The Wait output on a CellularRAM device is typically connected to a shared, system-level Wait signal (Figure 27.6). The shared Wait signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus.

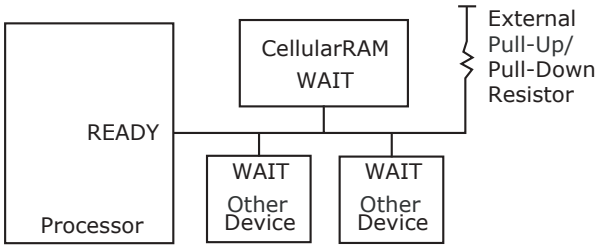


Figure 27.6 Wired or Wait Configuration

Once a Read or Write operation has been initiated, Wait goes active to indicate that the CellularRAM device requires additional time before data can be transferred. For Read operations, Wait will remain active until valid data is output from the device. For Write operations, Wait will indicate to the memory controller when data will be accepted into the CellularRAM device. When Wait transitions to an inactive state, the data burst will progress on successive clock edges.

CE# must remain asserted during Wait cycles (Wait asserted and Wait configuration BCR[8] = 1). Bringing CE# High during Wait cycles may cause data corruption. (Note that for BCR[8] = 0, the actual Wait cycles end one cycle after Wait de-asserts, and for row boundary crossings, start one cycle after the Wait signal asserts.)

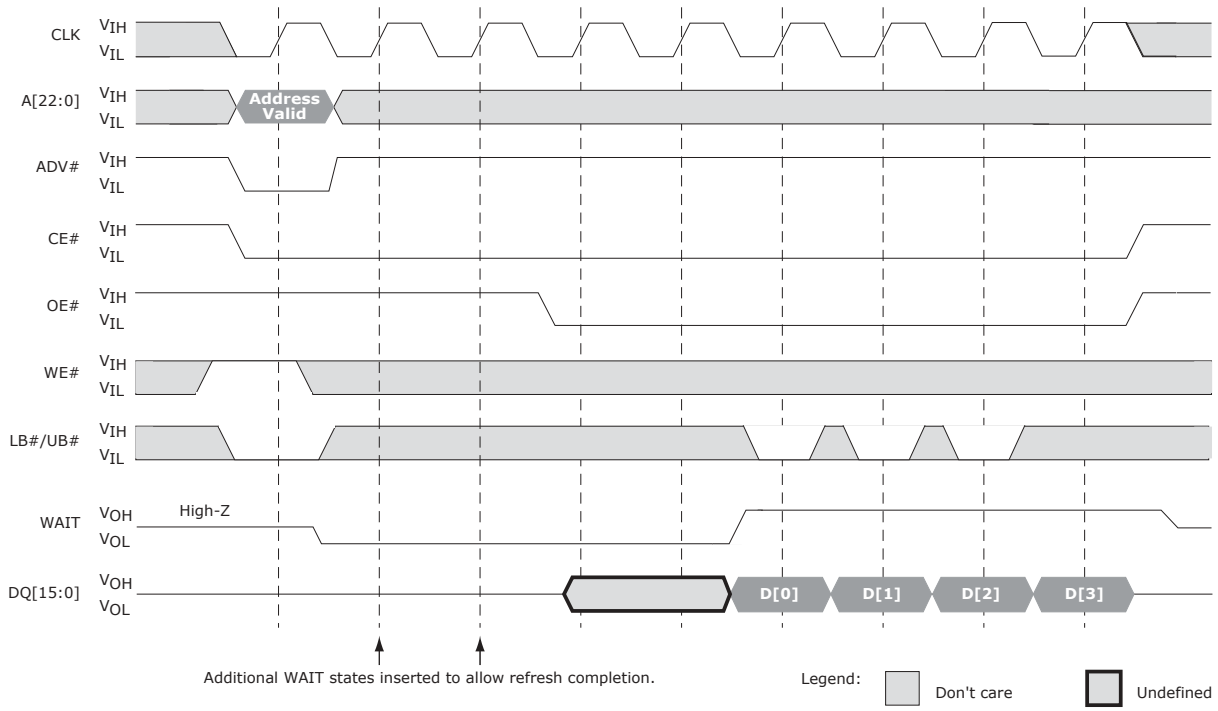
The WAIT output also performs an arbitration role when a Read or Write operation is launched while an on-chip refresh is in progress. If a collision occurs, the Wait pin is asserted for additional clock cycles until the refresh has completed (Figure 27.7 and Figure 27.8). When the refresh operation has completed, the Read or Write operation will continue normally.

Wait is also asserted when a continuous Read or Write burst crosses the boundary between 128-word rows. The Wait assertion allows time for the new row to be accessed, and permits any pending refresh operations to be performed.

27.6 LB#/UB# Operation

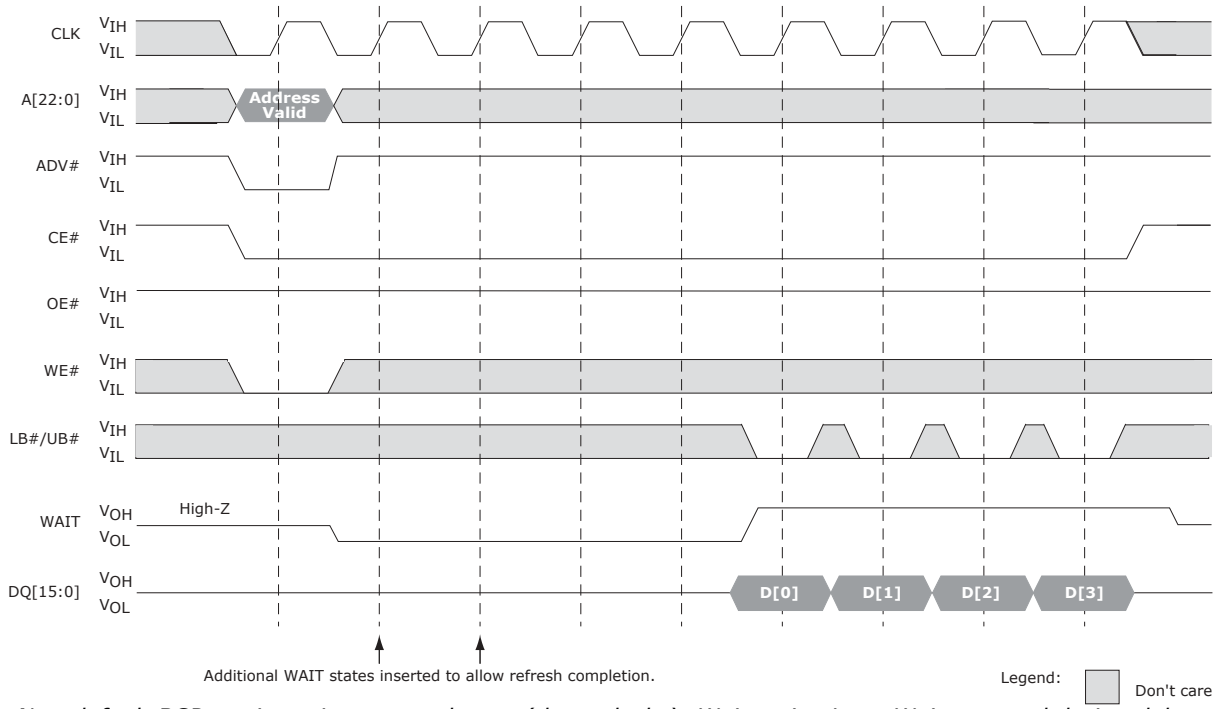
The LB# enable and UB# enable signals support byte-wide data transfers. During Read operations, the enabled byte(s) are driven onto the DQs. The DQs associated with a disabled byte are put into a High-Z state during a Read operation. During Write operations, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During an asynchronous Write cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first.

When both the LB# and UB# are disabled (High) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains Low.



Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*

Figure 27.7 Refresh Collision During Read Operation



Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*

Figure 27.8 Refresh Collision During Write Operation

28 Low-Power Operation

28.1 Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation. Standby operation occurs when CE# is High.

The device will enter a reduced power state upon completion of a Read or Write operation, or when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

28.2 Temperature Compensated Refresh

Temperature compensated refresh (TCR) is used to adjust the refresh rate depending on the device operating temperature. DRAM technology requires increasingly frequent refresh operation to maintain data integrity as temperatures increase. More frequent refresh is required due to increased leakage of the DRAM capacitive storage elements as temperatures rise. A decreased refresh rate at lower temperatures will facilitate a savings in standby current.

TCR allows for adequate refresh at four different temperature thresholds (+15°C, +45°C, +70°C, and +85°C). The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. For example, if the case temperature is 50°C, the system can minimize self refresh current consumption by selecting the 70°C setting. The +15°C and +45°C settings would result in inadequate refreshing and cause data corruption.

28.3 Partial Array Refresh

Partial array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, three-quarter array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (Table 29.5). Read and Write operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

28.4 Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled by rewriting the RCR, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume. During this 150µs period, the current consumption will be higher than the specified standby levels, but considerably lower than the active current specification.

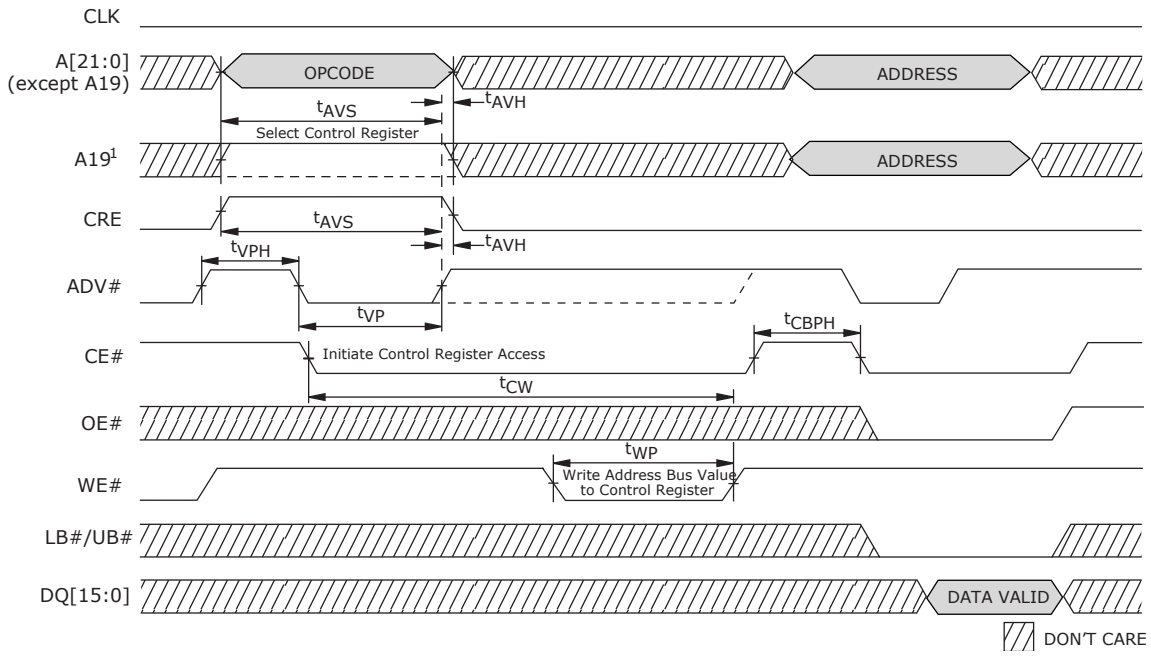
DPD cannot be enabled or disabled by writing to the RCR using the software access sequence; the RCR should be accessed using CRE instead.

29 Configuration Registers

Two user-accessible configuration registers define the device operation. The bus configuration register (BCR) defines how the CellularRAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up, and can be updated any time the devices are operating in a standby state.

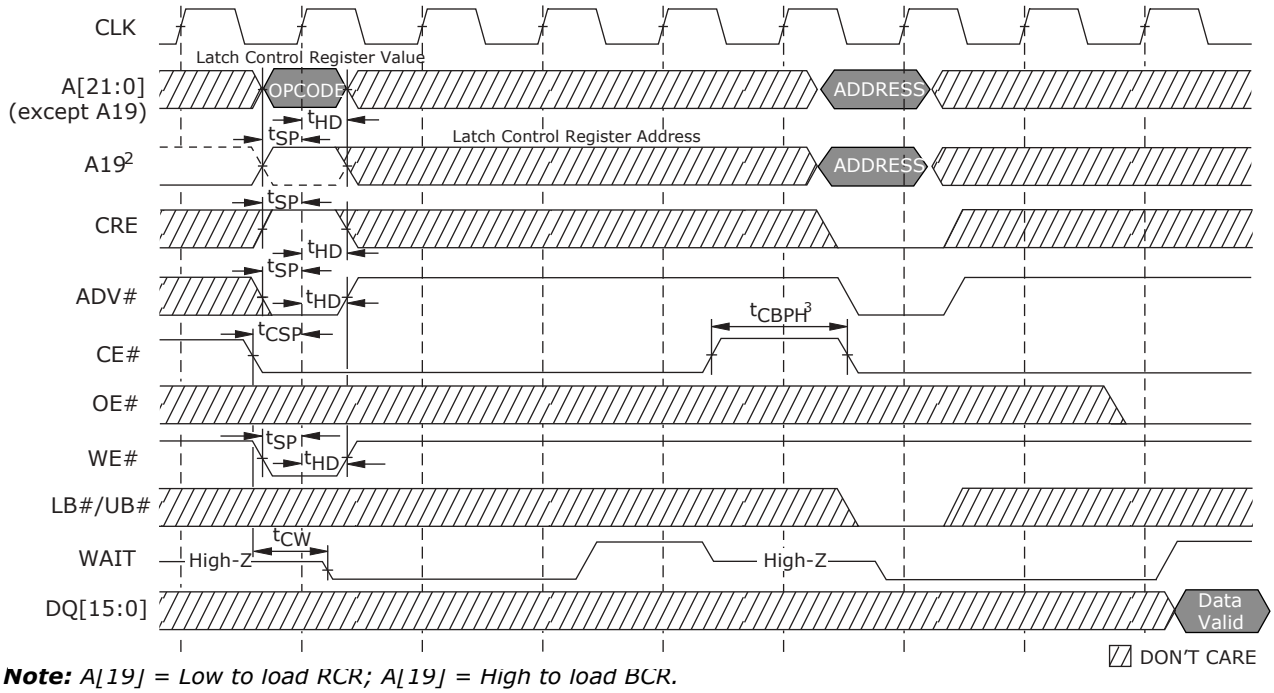
29.1 Access Using CRE

The configuration registers are loaded using either a synchronous or an asynchronous operation when the configuration register enable (CRE) input is High (see Figure 29.2). When CRE is Low, a Read or Write operation will access the memory array. The register values are written via address pins A[21:0]. In an asynchronous Write, the values are latched into the configuration register on the rising edge of ADV#, CE#, or WE#, whichever occurs first; LB# and UB# are *Don't Care*. The BCR is accessed when A[19] is High; the RCR is accessed when A[19] is Low.



Note: *A[19] = LOW to load RCR; A[19] = HIGH to load BCR.*

Figure 29.1 Configuration Register WRITE in Asynchronous Mode Followed by READ ARRAY Operation



Note: *A[19] = Low to load RCR; A[19] = High to load BCR.*

Figure 29.2 Configuration Register WRITE in Synchronous Mode Followed by READ ARRAY Operation

29.2 Software Access

Software access of the configuration registers uses a sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be read or modified using the software sequence.

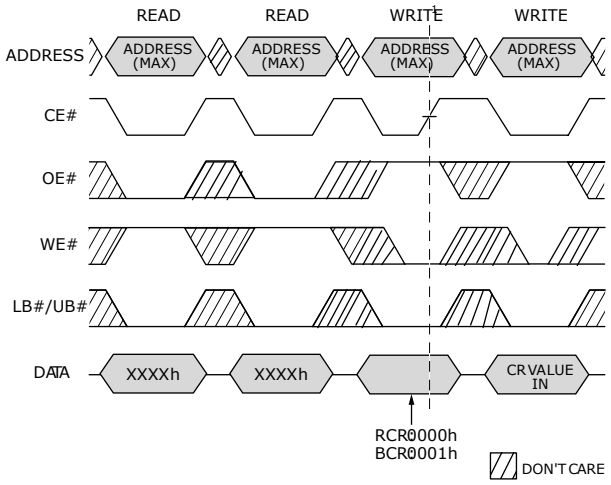
The configuration registers are loaded using a four step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations (see Figure 29.3). The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 29.4). Note that a third READ cycle cancels the access sequence.

The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (3FFFFFh for 64Mb); the content at this address is changed by using this sequence (note that this is a deviation from the CellularRAM specification).

The data value presented during the third operation (WRITE) in the sequence defines whether the BCR or the RCR is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR. During the fourth operation, the data bus is used to transfer data in to or out of the configuration registers.

The use of the software sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for the control register enable (CRE) pin. If the software mechanism is used, the CRE pin can simply be tied to V_{SS}. The port line often used for CRE control purposes is no longer required.

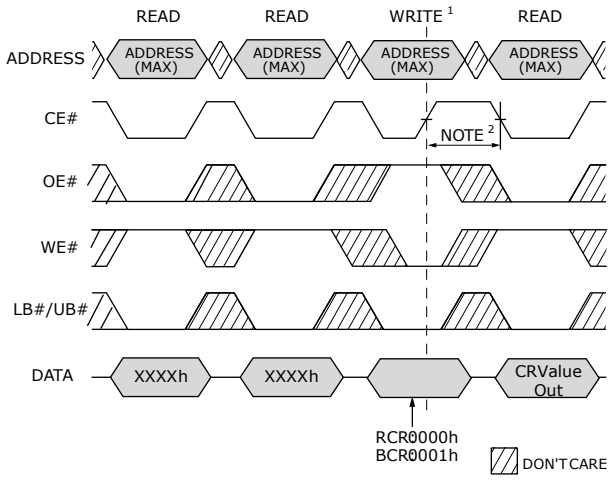
Software access of the RCR should not be used to enter or exit DPD.



Notes:

1. The WRITE on the third cycle must be CE# controlled.

Figure 29.3 Load Configuration Register



Notes:

1. *The WRITE on the third cycle must be CE# controlled.*
2. *CE# must be HIGH for 150ns before performing the cycle that reads a configuration register.*

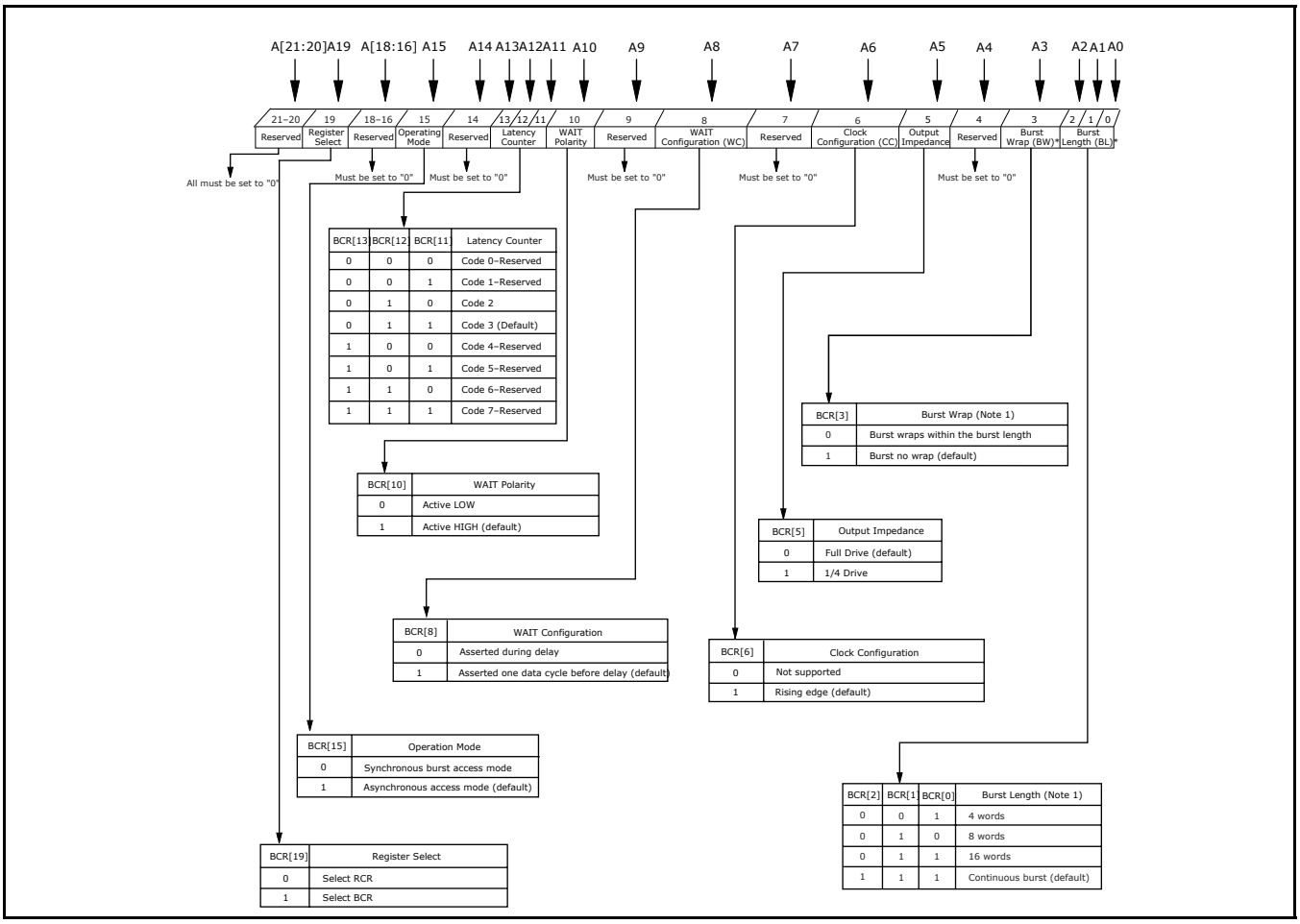
Figure 29.4 Read Configuration Register

29.3 Bus Configuration Register

The BCR defines how the CellularRAM device interacts with the system memory bus. Page mode operation is enabled by a bit contained in the RCR. Table 29.1 below describes the control bits in the BCR. At power-up, the BCR is set to 9D4Fh.

The BCR is accessed using CRE and A[19] High, or through the configuration register software sequence with DQ = 0001h on the third cycle.

Table 29.1 Bus Configuration Register Definition



Note: *All burs WRITEs are continuous.*

Table 29.2 Sequence and Burst Length

Burst Wrap		Starting Address	4-word Burst Length	8-word Burst Length	16-word Burst Length	Continuous Burst
BCR[3]	Wrap	(Decimal)	Linear	Linear	Linear	Linear
0	Yes	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-…
		1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-2-3-4-5-6-7-…
		2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-4-5-6-7-8-…
		3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-4-5-6-7-8-9-…
		4		4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-7-8-9-10-…
		5		5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-6-7-8-9-10-11-…
		6		6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-8-9-10-11-12-…
		7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-8-9-10-11-12-13-…
		…			…	…
		14			14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-16-17-18-19-20-…
		15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-18-19-20-21…
1	No	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-…
		1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16	1-2-3-4-5-6-7-…
		2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17	2-3-4-5-6-7-8-…
		3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18	3-4-5-6-7-8-9-…
		4		4-5-6-7-8-9-10-11	4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19	4-5-6-7-8-9-10-…
		5		5-6-7-8-9-10-11-12	5-6-7-8-9-10-11-12-13-…-15-16-17-18-19-20	5-6-7-8-9-10-11…
		6		6-7-8-9-10-11-12-13	6-7-8-9-10-11-12-13-14-…-16-17-18-19-20-21	6-7-8-9-10-11-12…
		7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-…-17-18-19-20-21-22	7-8-9-10-11-12-13…
		…			…	…
		14			14-15-16-17-18-19-…-23-24-25-26-27-28-29	14-15-16-17-18-19-20-…
		15			15-16-17-18-19-20-…-24-25-26-27-28-29-30	15-16-17-18-19-20-21-…

29.3.1 Burst Length (BCR[2:0]): Default = Continuous Burst

Burst lengths define the number of words the device outputs during burst Read operations. The device supports a burst length of 4, 8, or 16 words. The device can also be set in continuous burst mode where data is output sequentially without regard to address boundaries; the internal address wraps to 000000h if the device is read past the last address. Write bursts are always performed using continuous burst mode.

29.3.2 Burst Wrap (BCR[3]): Default = No Wrap

The burst-wrap option determines if a 4-, 8-, or 16-word Read burst wraps within the burst length or steps through sequential addresses. If the wrap option is not enabled, the device accesses data from sequential addresses without regard to burst boundaries; the internal address wraps to 000000h if the device is read past the last address.

29.3.3 Output Impedance (BCR[5]): Default = Outputs Use Full Drive Strength

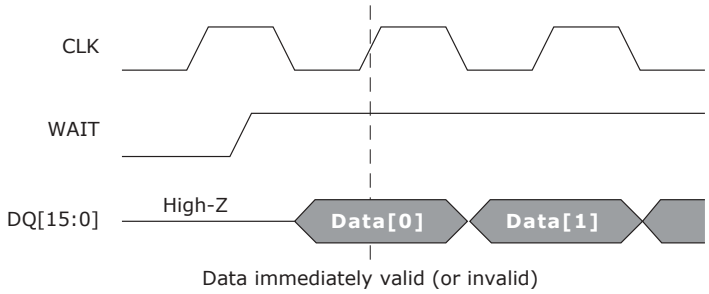
The output driver strength can be altered to full, one-half, or one-quarter strength to adjust for different data bus loading scenarios. The reduced-strength options are intended for stacked chip (Flash + CellularRAM) environments when there is a dedicated memory bus. The reduced-drive-strength option minimizes the noise generated on the data bus during Read operations. Normal output drive strength should be selected when using a discrete CellularRAM device in a more heavily loaded data bus environment. Outputs are configured at full drive strength during testing.

29.3.4 Wait Configuration (BCR[8]): Default = Wait Transitions One Clock Before Data Valid/Invalid

The Wait configuration bit is used to determine when Wait transitions between the asserted and the de-asserted state with respect to valid data presented on the data bus. The memory controller will use the Wait signal to coordinate data transfer during synchronous Read and Write operations. When BCR[8] = 0, data will be valid or invalid on the clock edge immediately after Wait transitions to the de-asserted or asserted state, respectively (Figure 29.5 and Figure 29.7). When A8 = 1, the Wait signal transitions one clock period prior to the data bus going valid or invalid (Figure 29.6).

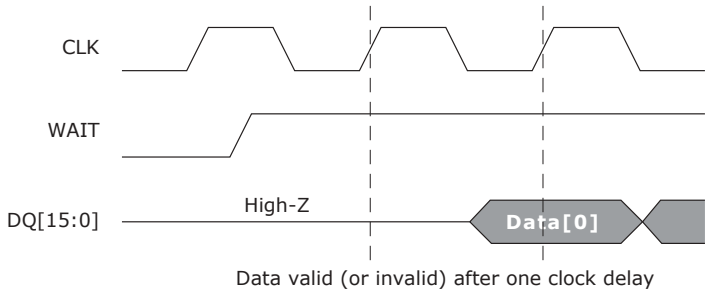
29.3.5 Wait Polarity (BCR[10]): Default = Wait Active High

The Wait polarity bit indicates whether an asserted Wait output should be High or Low. This bit will determine whether the Wait signal requires a pull-up or pull-down resistor to maintain the de-asserted state.



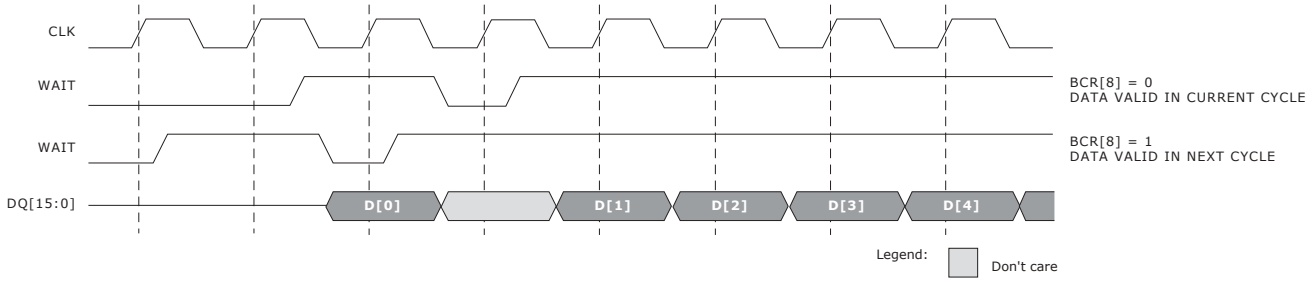
Note: *Data valid/invalid immediately after Wait transitions (BCR[8] = 0). See Figure 29.7.*

Figure 29.5 Wait Configuration (BCR[8] = 0)



Note: *Valid/invalid data delayed for one clock after Wait transitions (BCR[8] = 1). See Figure 29.7.*

Figure 29.6 Wait Configuration (BCR[8] = I)



Note: *Non-default BCR setting: Wait active Low.*

Figure 29.7 Wait Configuration During Burst Operation

29.3.6 Latency Counter (BCR[13:11]): Default = Three-Clock Latency

The latency counter bits determine how many clocks occur between the beginning of a Read or Write operation and the first data value transferred. Latency codes from two (three clocks) to six (seven clocks) are allowed (see Table 29.3 and Figure 29.8 below).

Table 29.3 Variable Latency Configuration Codes

Latency Configuration Code	Max Input Clk Frequency (MHz)	
	70 ns/80 MHz	70 ns/66 MHz
2 (3 clocks)	53 (18.75 ns)	44 (22.7 ns)
3 (4 clocks)—default	80 (12.5 ns)	66 (15.2 ns)

Note: *Clock rates below 50MHz are allowed as long as t_{CSP} specifications are met.*

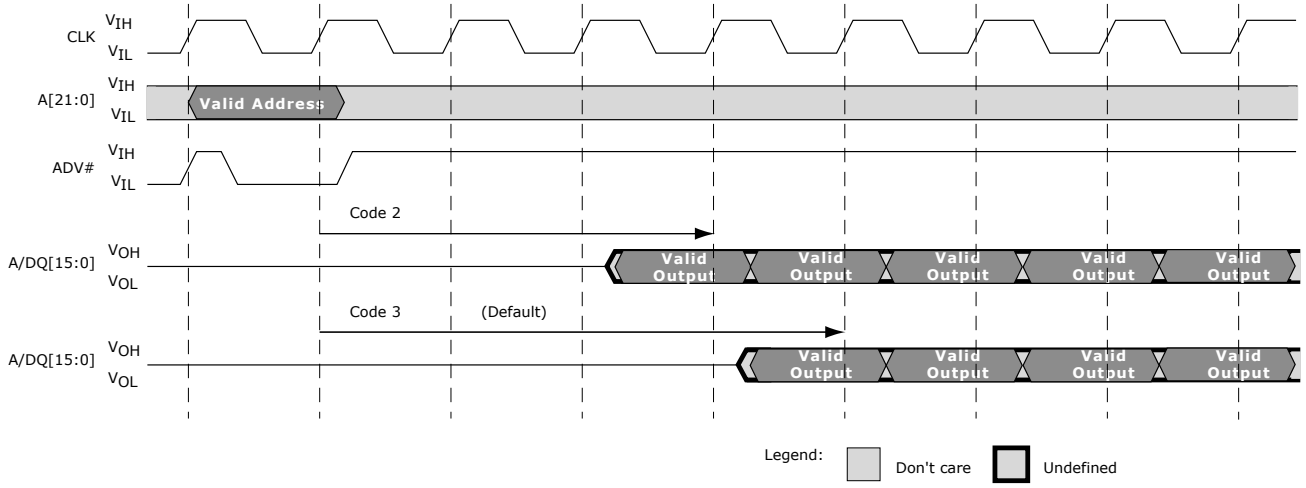


Figure 29.8 Latency Counter (Variable Initial Latency, No Refresh Collision)

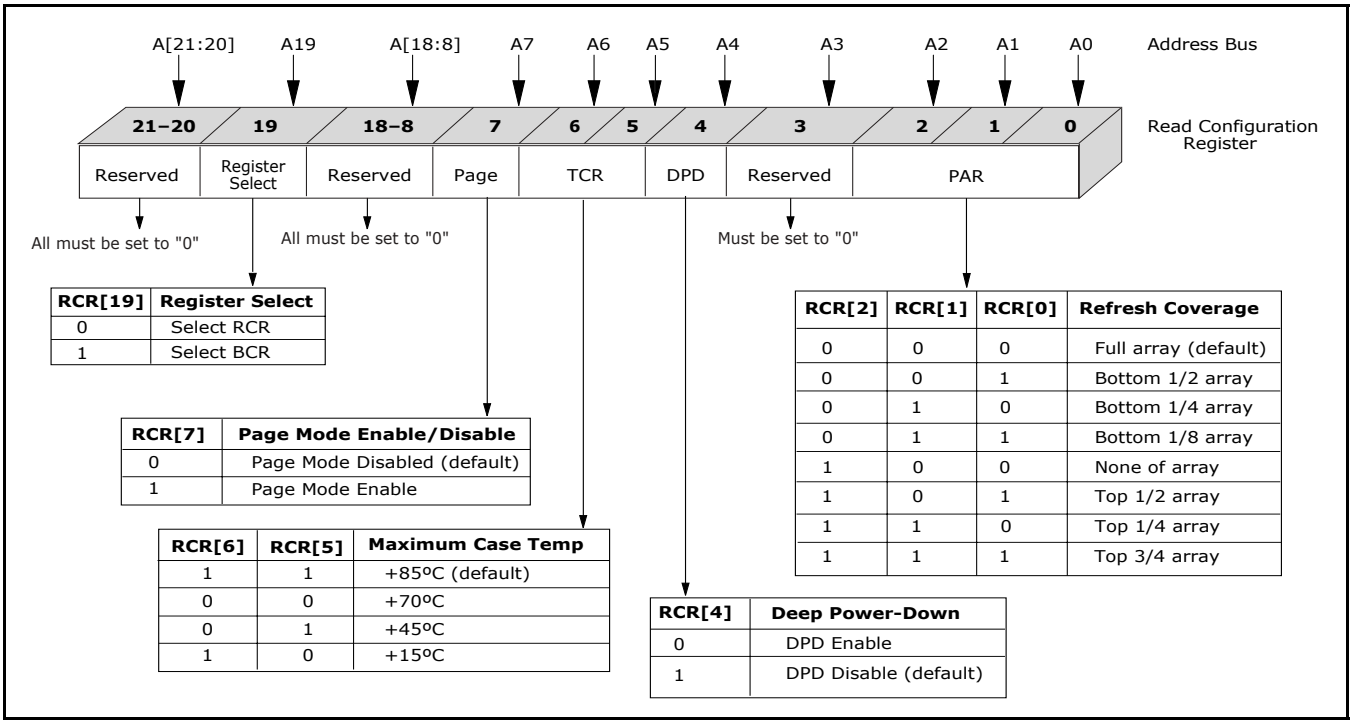
29.3.7 Operating Mode (BCR[15]): Default = Asynchronous Operation

The operating mode bit selects either synchronous burst operation or the default asynchronous mode of operation.

29.4 Refresh Configuration Register

The refresh configuration register (RCR) defines how the CellularRAM device performs its transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the RCR. Table 29.4 below describes the control bits used in the RCR. At power-up, the RCR is set to 0070h. The RCR is accessed using CRE and A[19] Low, or through the configuration register software access sequence with DQ = 0000h on the third cycle.

Table 29.4 Refresh Configuration Register Mapping



RCR[19]	Register Select
0	Select RCR
1	Select BCR

RCR[7]	Page Mode Enable/Disable
0	Page Mode Disabled (default)
1	Page Mode Enable

RCR[6]	RCR[5]	Maximum Case Temp
1	1	+85ºC (default)
0	0	+70ºC
0	1	+45ºC
1	0	+15ºC

RCR[4]	Deep Power-Down
0	DPD Enable
1	DPD Disable (default)

RCR[2]	RCR[1]	RCR[0]	Refresh Coverage
0	0	0	Full array (default)
0	0	1	Bottom 1/2 array
0	1	0	Bottom 1/4 array
0	1	1	Bottom 1/8 array
1	0	0	None of array
1	0	1	Top 1/2 array
1	1	0	Top 1/4 array
1	1	1	Top 3/4 array

29.4.1 Partial Array Refresh (RCR[2:0]): Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, three-quarters array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 29.5).

Table 29.5 64Mb Address Patterns for PAR (RCR[4] = l)

RCR[2]	RCR[l]	RCR[0]	Active Section	Address Space	Size	Density
0	0	0	Full die	000000h–3FFFFFh	4 Meg x 16	64Mb
0	0	1	One-half of die	000000h–2FFFFFh	2 Meg x 16	32Mb
0	1	0	One-quarter of die	000000h–1FFFFFh	1 Meg x 16	16Mb
0	1	1	One-eighth of die	000000h–0FFFFFh	512 K x 16	8Mb

Table 29.5 64Mb Address Patterns for PAR (RCR[4] = l) (Continued)

RCR[2]	RCR[l]	RCR[0]	Active Section	Address Space	Size	Density
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	100000h–3FFFFFh	2 Meg x 16	32Mb
1	1	0	One-quarter of die	200000h–3FFFFFh	1 Meg x 16	16Mb
1	1	1	One-eighth of die	300000h–3FFFFFh	512 K x 16	8Mb

29.4.2 Deep Power-Down (RCR[4]): Default = DPD Disabled

The deep power-down bit enables and disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume.

Deep power-down is enabled when RCR[4] = 0, and remains enabled until RCR[4] is set to *1*.

29.4.3 Temperature Compensated Refresh (RCR[6:5]): Default = +85ºC Operation

The TCR bits allow for adequate refresh at four different temperature thresholds (+15ºC, +45ºC, +70ºC, and +85ºC). The setting selected must be for a temperature higher than the case temperature of the CellurlarRAM device. If the case temperature is +50ºC, the system can minimize self refresh current consumption by selecting the +70ºC setting. The +15ºC and +45ºC settings would result in inadequate refreshing and cause data corruption.

29.4.4 Page Mode Operation (RCR[7]): Default = Disabled

The page mode operation bit determines whether page mode is enabled for asynchronous Read operations. In the power-up default state, page mode is disabled.

30 Absolute Maximum Ratings

Voltage to Any Ball Except V_{CC}, $V_{CC}Q$ Relative to V_{SS} -0.50V to (4.0V or V_{CCQ} + 0.3V, whichever is less)

Voltage on V_{CC} Supply Relative to V_{SS} . . . . . -0.2V to +2.45V

Voltage on V_{CCQ} Supply Relative to V_{SS} . . . . . -0.2V to +4.0V

Storage Temperature (plastic) . . . . . -55ºC to +150ºC

Operating Temperature (case)

Wireless (See Note)-30ºC to +85ºC

Industrial-40°C to +85°C

Soldering Temperature and Time

10s (lead only)+260°C

Note: *-30°C exceeds the CellularRAM Workgroup 1.0 specification of -25°C.*

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

31 DC Characteristics

Table 31.1 Electrical Characteristics and Operating Conditions

Description	Conditions	Symbol		Min	Max	Units	Notes
Supply Voltage		V_{CC}		1.70	1.95	V	
I/O Supply Voltage		$V_{CC}Q$	W: 1.8V	1.70	3.30	V	
Input High Voltage		V_{IH}		1.4	$V_{CC}Q$ + 0.2	V	2
Input Low Voltage		V_{IL}		-0.20	0.4	V	3
Output High Voltage	I_{OH} = -0.2mA	V_{OH}		0.80 $V_{CC}Q$		V	4
Output Low Voltage	I_{OL} = +0.2mA	V_{OL}			0.20 $V_{CC}Q$	V	4
Input Leakage Current	V_{IN} = 0 to $V_{CC}Q$	I_{LI}			1	µA	
Output Leakage Current	OE# = V_{IH} or Chip Disabled	I_{LO}			1	µA	
Operating Current							
Asynchronous Random Read	V_{IN} = $V_{CC}Q$ or 0V Chip Enabled, IOUT = 0	$I_{CC}1$	-70		25	mA	5
Asynchronous Page Read			-70		15		
Initial Access, Burst Read	V_{IN} = $V_{CC}Q$ or 0V Chip Enabled, IOUT = 0	$I_{CC}1$	80 MHz		35	mA	5
			66 MHz		30		
Continuous Burst Read			80 MHz		18		
			66 MHz		15		
Continuous Burst Write	V_{IN} = $V_{CC}Q$ or 0V Chip Enabled, I_{OUT} = 0	$I_{CC}2$	80 MHz		35	mA	5
			66 MHz		30		
Standby Current	V_{IN} = $V_{CC}Q$ or 0V CE# = $V_{CC}Q$	I_{SB}	64 M		120	µA	6

Notes:

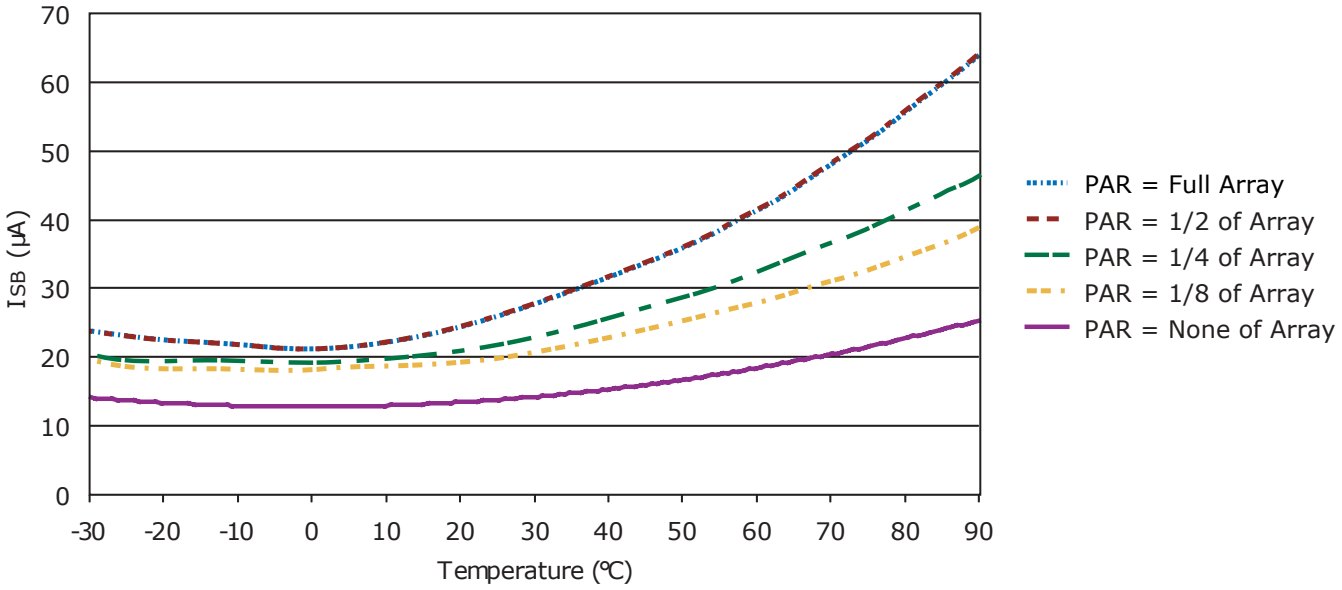
1. *Wireless Temperature (-25ºC < TC < +85ºC); Industrial Temperature (-40ºC < TC < +85ºC).*
2. *Input signals may overshoot to $V_{CC}Q$ + 1.0V for periods less than 2ns during transitions.*
3. *Input signals may undershoot to V_{SS} - 1.0V for periods less than 2ns during transitions.*
4. *BCR[5:4] = 00b.*
5. *This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.*
6. *ISB (MAX) values measured with PAR set to FULL ARRAY and TCR set to +85°C. To achieve Low standby current, all inputs must be driven to either $V_{CC}Q$ or V_{SS}.*

Table 31.2 Maximum Standby Currents for Applying PAR and TCR Settings

PAR	TCR		
	+15°C (RCR[6:5] = 10b)	+45°C (RCR[6:5] = 01b)	+85°C (RCR[6:5] = 11b)
Full Array	70	85	120
1/2 Array	65	80	115
1/4 Array	60	75	110
1/8 Array	57	70	105
0 Array	50	55	70

Notes:

1. *For RCR[6:5] = 00b (default), refer to Figure 31.1 for typical values.*
2. *In order to achieve low standby current, all inputs must be driven to either V_{CCQ} or V_{SS}. ISB might be slightly higher for up to 500ms after power-up, or after changes to the PAR array partition.*
3. *Values of TCR for 85 are 100% tested. Values of TCR for 15 and 45 are sampled only.*



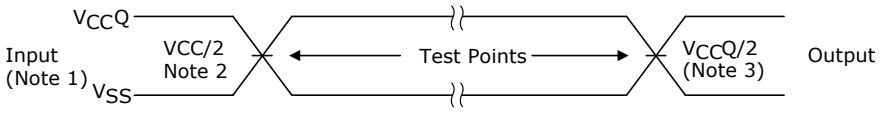
Note: *Typical ISB currents for each PAR setting with the appropriate TCR selected, or temperature sensor enabled.*

Figure 31.1 Typical Refresh Current vs. Temperature (I_{TCR})

Table 31.3 Deep Power-Down Specifications

Description	Conditions	Symbol	Typ	Units
Deep Power-down	V_{IN} = V_{CC}Q or 0V; +25°C	I_{ZZ}	10	µA

32 AC Characteristics



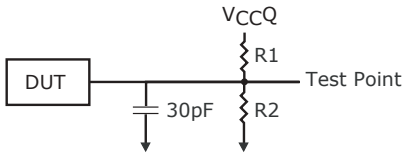
Notes:
1. *AC test inputs are driven at $V_{CC}Q$ for a logic 1 and V_{SS} for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.*
2. *Input timing begins at $V_{CC}/2$. Due to the possibility of a difference between V_{CC} and V_{CCQ}, the input test point may not be shown to scale.*
3. *Output timing ends at $V_{CC}Q/2$.*

Figure 32.1 AC Input/Output Reference Waveform

Table 32.1 Capacitance

Description	Conditions	Symbol	Min	Max	Units	Notes
Input Capacitance	T_C = +25ºC; f = 1 MHz; V_{IN} = 0V	C_{IN}	2.0	6	pF	1
Input/Output Capacitance (DQ)		C_{IO}	3.5	6	pF	1

Notes:
1. *These parameters are verified in device characterization and are not 100% tested.*



Note: *All tests are performed with the outputs configured for full drive strength (BCR[5] = 0).*

Figure 32.2 Output Load Circuit

Table 32.2 Output Load Circuit

$V_{CC}Q$	RI/R2
1.8 V	2.7 KΩ
2.5 V	3.7 KΩ
3.0 V	4.5 KΩ

Table 32.3 Asynchronous Read Cycle Timing Requirements

Parameter	Symbol	70ns		Units	Notes
		Min	Max		
Address Access Time	t_{AA}		70	ns	
ADV# Access Time	t_{AADV}		70	ns	
Page Access Time	t_{APA}		20	ns	
Address Hold from ADV# High	t_{AVH}	5		ns	
Address Setup to ADV# High	t_{AVS}	10		ns	
LB#/UB# Access Time	t_{BA}		70	ns	
LB#/UB# Disable to DQ High-Z Output	t_{BHZ}		8	ns	4
LB#/UB# Enable to Low-Z Output	t_{BLZ}	10		ns	3
Maximum CE# Pulse Width	t_{CEM}		8	µs	
CE# Low to Wait Valid	t_{CEW}	1	7.5	ns	
Chip Select Access Time	t_{CO}		70	ns	
CE# Low to ADV# High	t_{CVS}	10		ns	
Chip Disable to DQ and Wait High-Z Output	t_{HZ}		8	ns	4
Chip Enable to Low-Z Output	t_{LZ}	10		ns	3
Output Enable to Valid Output	t_{OE}		20	ns	
Output Hold from Address Change	t_{OH}	5		ns	
Output Disable to DQ High-Z Output	t_{OHZ}		8	ns	4
Output Enable to Low-Z Output	t_{OLZ}	5		ns	3
Page Cycle Time	t_{PC}	20		ns	
Read Cycle Time	t_{RC}	70		ns	
ADV# Pulse Width Low	t_{VP}	10		ns	
ADV# Pulse Width High	t_{VPH}	10		ns	

Notes:

1. *All tests are performed with the outputs configured for full drive strength (BCR[5] = 0).*
2. *High-Z to Low-Z timings are tested with the circuit shown in Figure 32.2. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.*
3. *Low-Z to High-Z timings are tested with the circuit shown in Figure 32.2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.*

Table 32.4 Burst Read Cycle Timing Requirements

Parameter	Symbol	70ns/80 MHz		70ns/66 MHz		Units	Notes
		Min	Max	Min	Max		
Burst to Read Access Time (Variable Latency)	t_{ABA}		46.5		56	ns	
CLK to Output Delay	t_{ACLK}		9		11	ns	
Burst OE# Low to Output Delay	t_{BOE}		20		20	ns	
CE# High between Subsequent Mixed-Mode Operations	t_{CBPH}	5		5		ns	
CE# Low to Wait Valid	t_{CEW}	1	7.5	1	7.5	ns	
CLK Period	t_{CLK}	12.5	20	15	20	ns	
CE# Setup Time to Active CLK Edge	t_{CSP}	4.5	20	5	20	ns	
Hold Time from Active CLK Edge	t_{HD}	2		2		ns	
Chip Disable to DQ and Wait High-Z Output	t_{HZ}		8		8	ns	2
CLK Rise or Fall Time	t_{KHKL}		1.8		2.0	ns	
CLK to Wait Valid	t_{KHTL}		9		11	ns	
CLK to DQ High-Z Output	t_{KHZ}	3	8	3	8	ns	
CLK to Low-Z Output	t_{KLZ}	2	5	2	5	ns	
Output Hold from CLK	t_{KOH}	2		2		ns	
CLK High or Low Time	t_{KP}	4		5		ns	
Output Disable to DQ High-Z Output	t_{OHZ}		8		8	ns	2
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns	3
Setup Time to Active CLK Edge	t_{SP}	3		3		ns	
Maximum CE# Pulse Width	t_{CBPH}		8		8	µs	2

Notes:

1. *All tests are performed with the outputs configured for full drive strength (BCR[5] = 0).*
2. *Low-Z to High-Z timings are tested with the circuit shown in Figure 32.2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.*
3. *High-Z to Low-Z timings are tested with the circuit shown in Figure 32.2. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.*

Table 32.5 Asynchronous Write Cycle Timing Requirements

Parameter	Symbol	70 ns		Units	Notes
		Min	Max		
Address and ADV# Low Setup Time	t_{AS}	0		ns	
Address Hold from ADV# Going High	t_{AVH}	5		ns	
Address Setup to ADV# Going High	t_{AVS}	10			
Address Valid to End of Write	t_{AW}	70		ns	
LB#/UB# Select to End of Write	t_{BW}	70		ns	
CE# Low to Wait Valid	t_{CEW}	1	7.5	ns	
Async Address-to-Burst Transition Time	t_{CKA}	70		ns	
CE# Low to ADV# High	t_{CVS}	10		ns	
Chip Enable to End of Write	t_{CW}	70		ns	
Data Hold from Write Time	t_{DH}	0		ns	
Data Write Setup Time	t_{DW}	23		ns	
Chip Disable to Wait High-Z Output	t_{HZ}		8	ns	
Chip Enable to Low-Z Output	t_{LZ}	10		ns	3
End Write to Low-Z Output	t_{OW}	5		ns	3
ADV# Pulse Width	t_{VP}	10		ns	
ADV# Pulse Width High	t_{VPH}	10		ns	
ADV# Setup to End of Write	t_{VS}	70		ns	
Write Cycle Time	t_{WC}	70		ns	
Write to DQ High-Z Output	t_{WHZ}		8	ns	2
Write Pulse Width	t_{WP}	46		ns	
Write Pulse Width High	t_{WPH}	10		ns	
Write Recovery Time	t_{WR}	0		ns	
CE# High between subsequent asynchronous operations	t_{CPH}	5		ns	

Notes:

1. *Low-Z to High-Z timings are tested with the circuit shown in Figure 32.2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.*
2. *High-Z to Low-Z timings are tested with the circuit shown in Figure 32.2. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.*

Table 32.6 Burst Write Cycle Timing Requirements

Parameter	Symbol	70ns/80 MHz		70ns/66 MHz		Units	Notes
		Min	Max	Min	Max		
CE# High between Subsequent Mixed-Mode Operations	t_{CBPH}	5		5		ns	
CE# Low to Wait Valid	t_{CEW}	1	7.5	1	7.5	ns	
Clock Period	t_{CLK}	12.5	20	15	20	ns	
CE# Setup to CLK Active Edge	t_{CSP}	4.5	20	5	20	ns	
Hold Time from Active CLK Edge	t_{HD}	2		2		ns	
Chip Disable to Wait High-Z Output	t_{HZ}		8		8	ns	
CLK Rise or Fall Time	t_{KHKL}		1.8		2.0	ns	
Clock to Wait Valid	t_{KHTL}		9		11	ns	
CLK High or Low Time	t_{KP}	4		5		ns	
Setup Time to Activate CLK Edge	t_{SP}	3		3		ns	
Minimum CE# Pulse Width	t_{CEM}		8		8	µs	

Notes:

1. *When configured for synchronous mode (BCR[15] = 0), a refresh opportunity must be provided every t_{CEM}. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for greater than 15ns.*
2. *Clock rates below 50 MHz (t_{CLK} > 20ns) are allowed as long as t_{CSP} specifications are met.*

33 Timing Diagrams

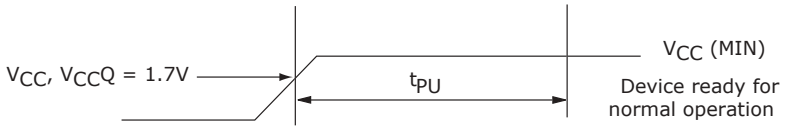


Figure 33.1 Initialization Period

Table 33.1 Initialization Timing Parameters

Parameter	Symbol	70ns/80 MHz		85ns/66 MHz		Units	Notes
		Min	Max	Min	Max		
Initialization Period (required before normal operations)	t_{PU}		150		150	µs	

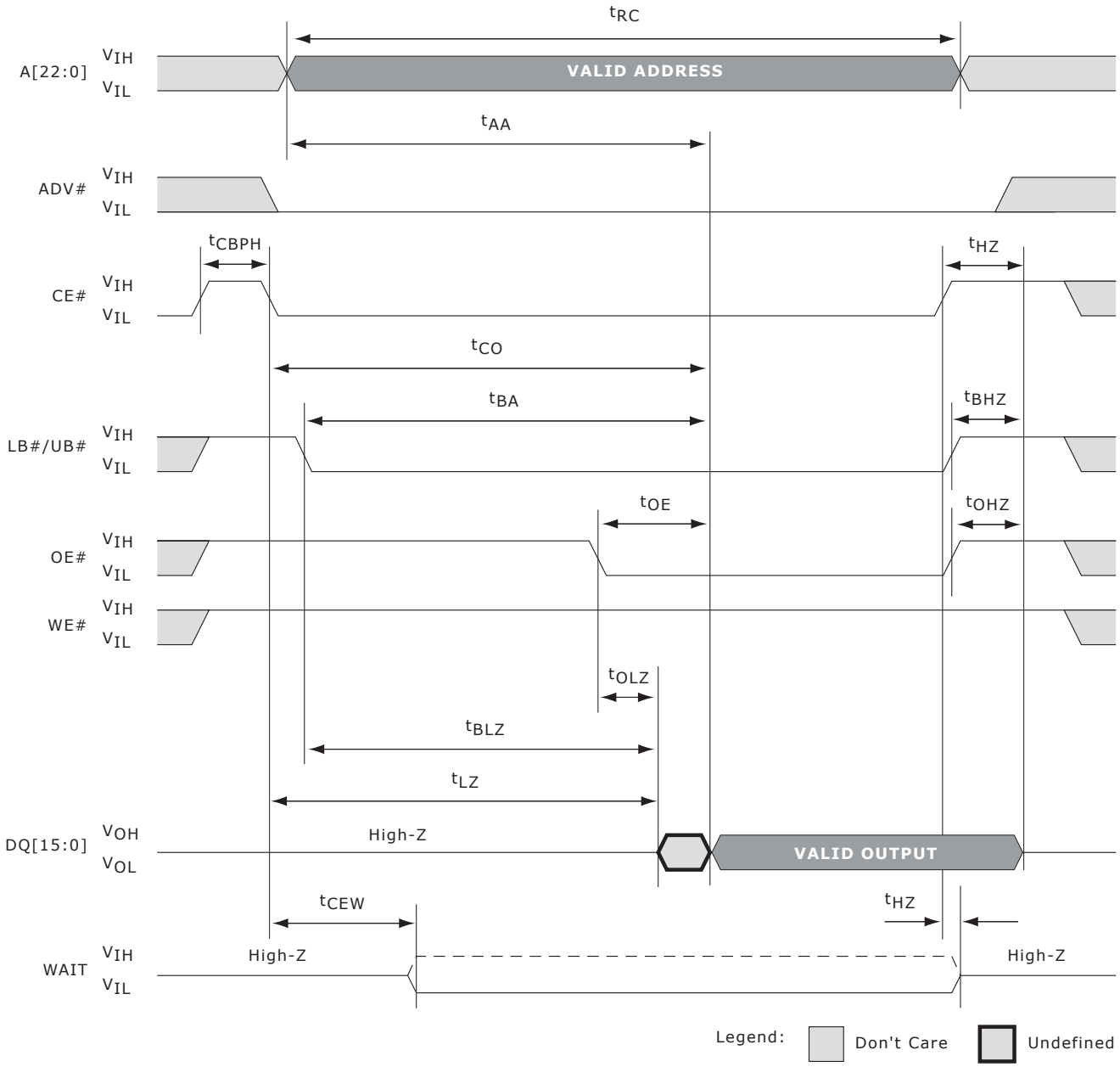


Figure 33.2 Asynchronous Read

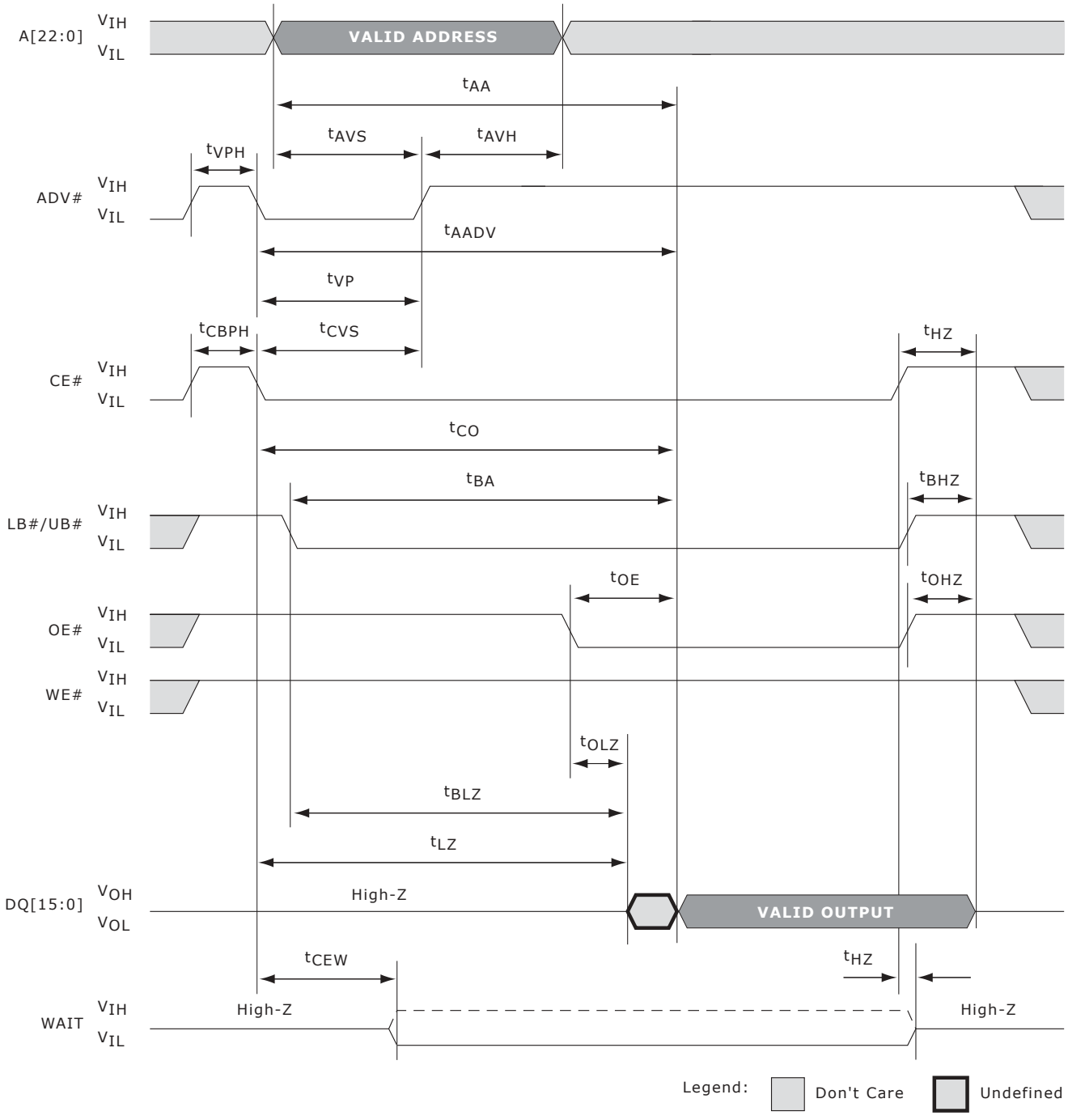


Figure 33.3 Asynchronous Read Using ADV#

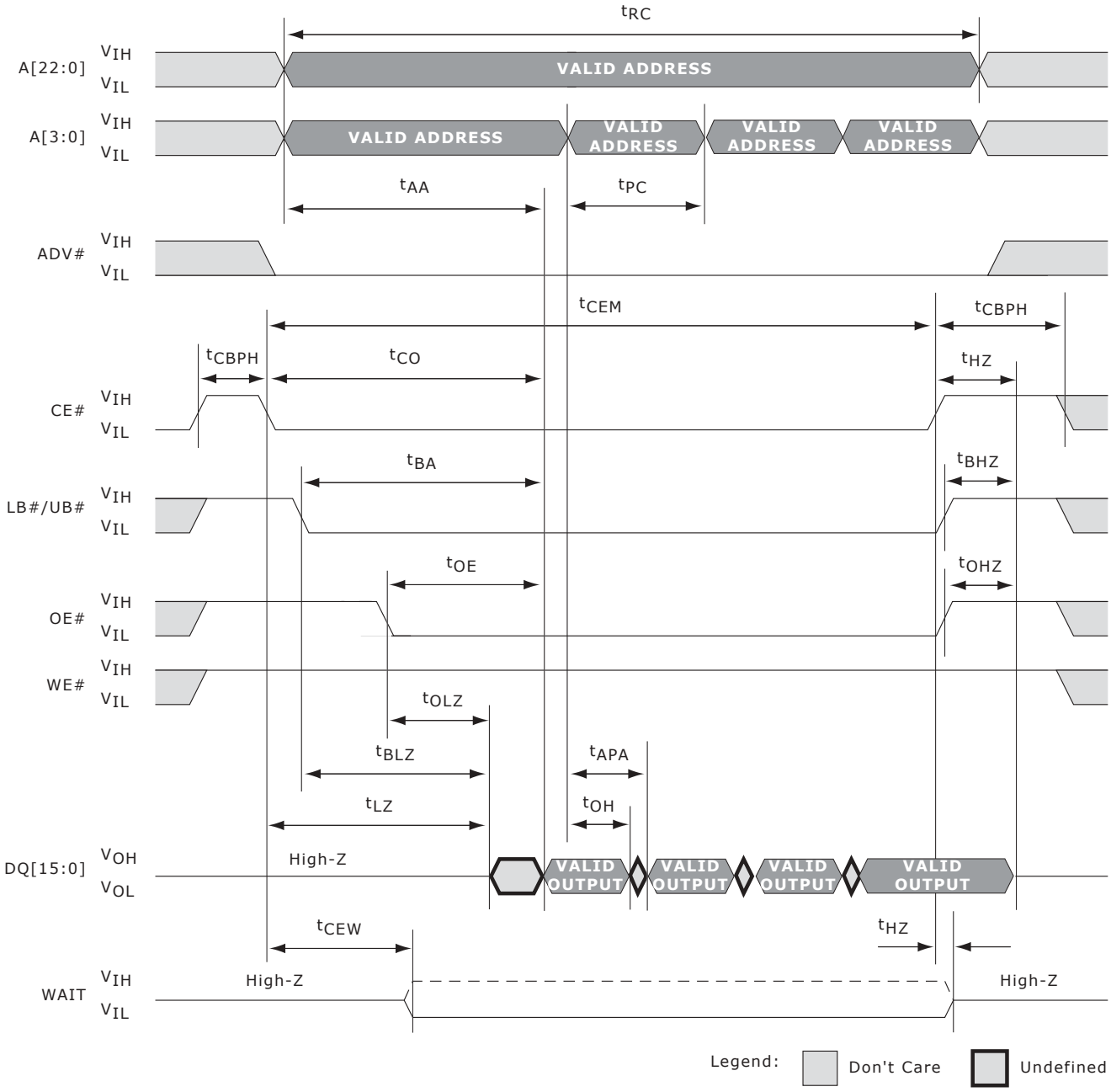
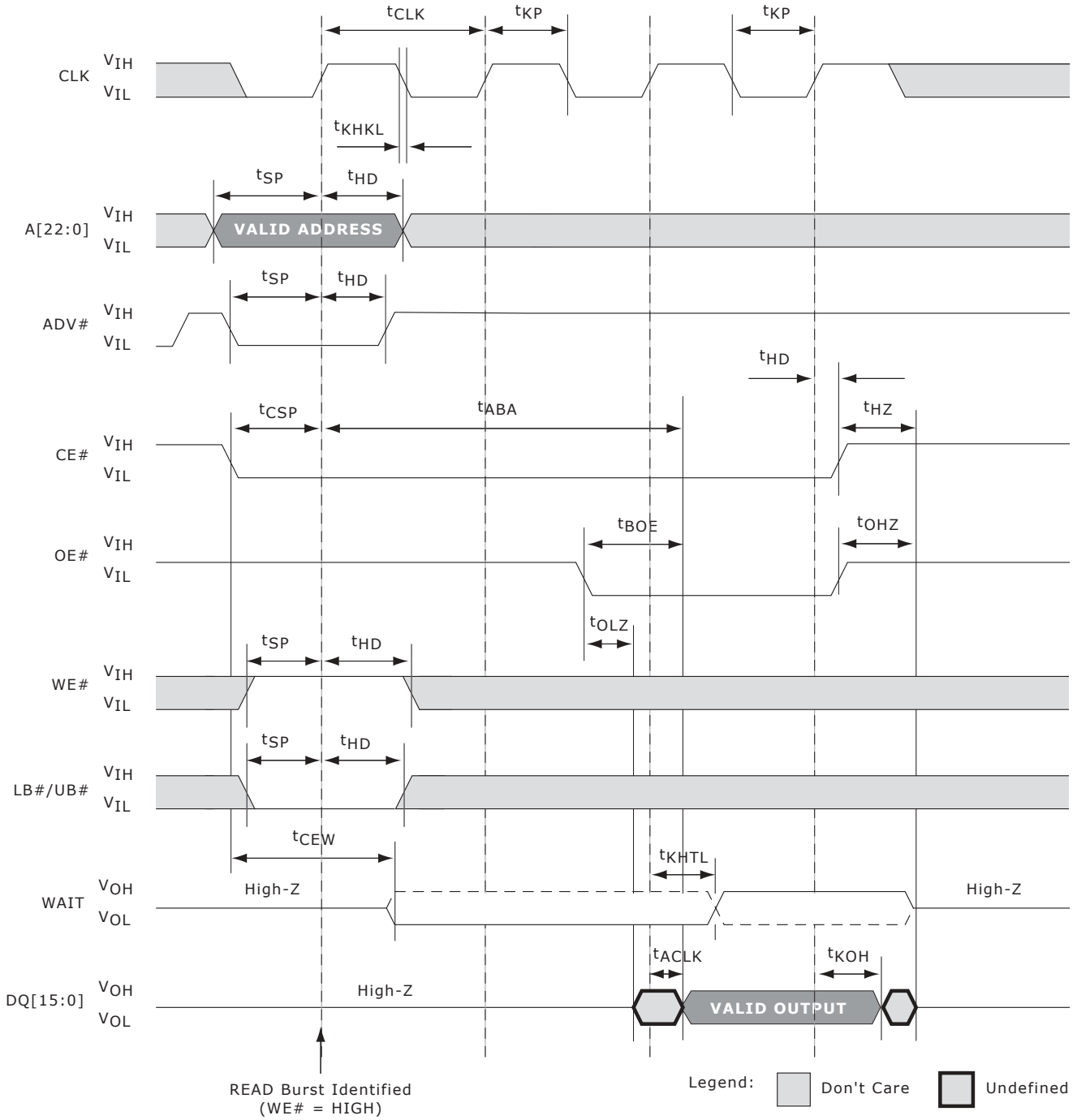
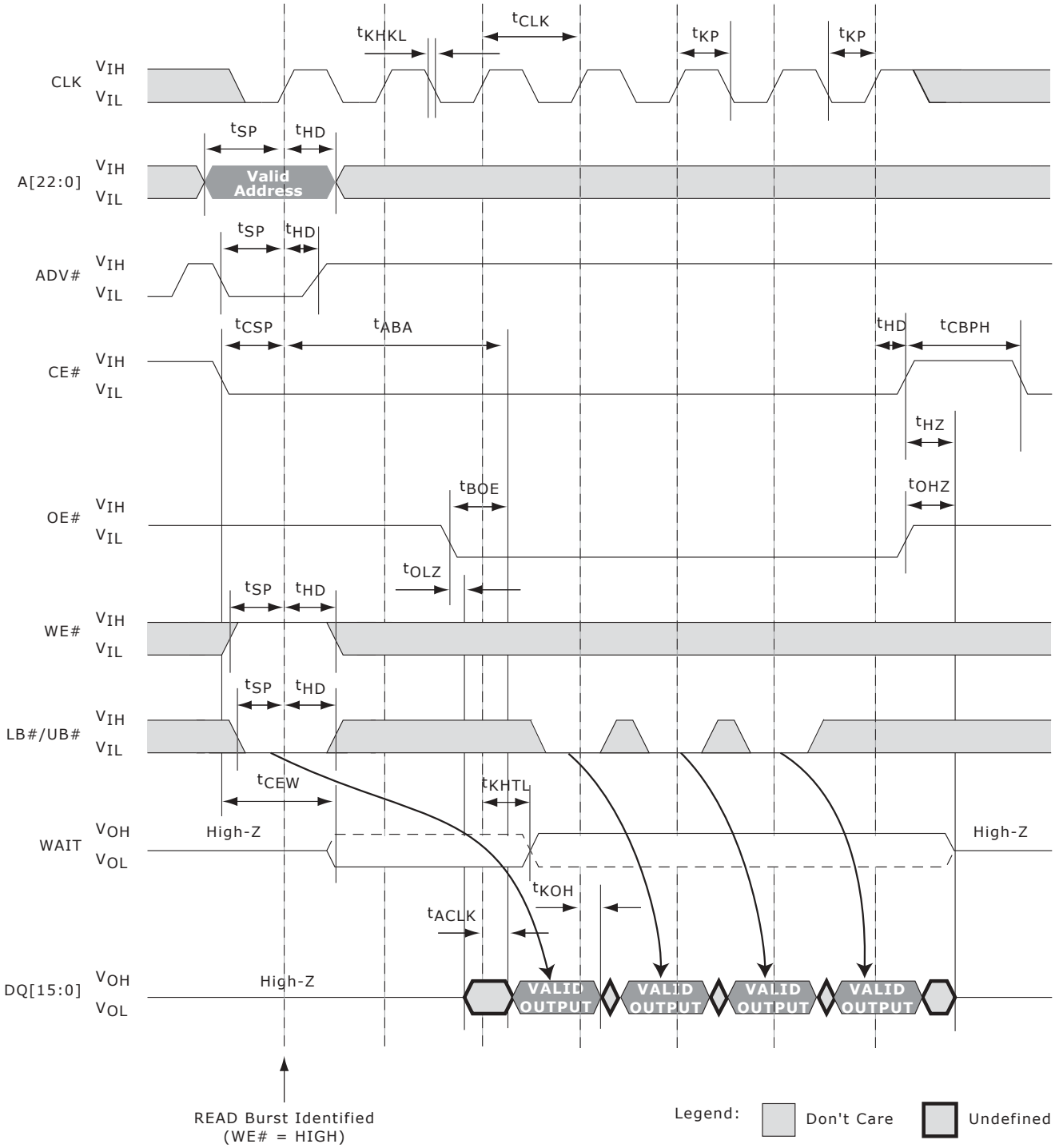


Figure 33.4 Page Mode Read



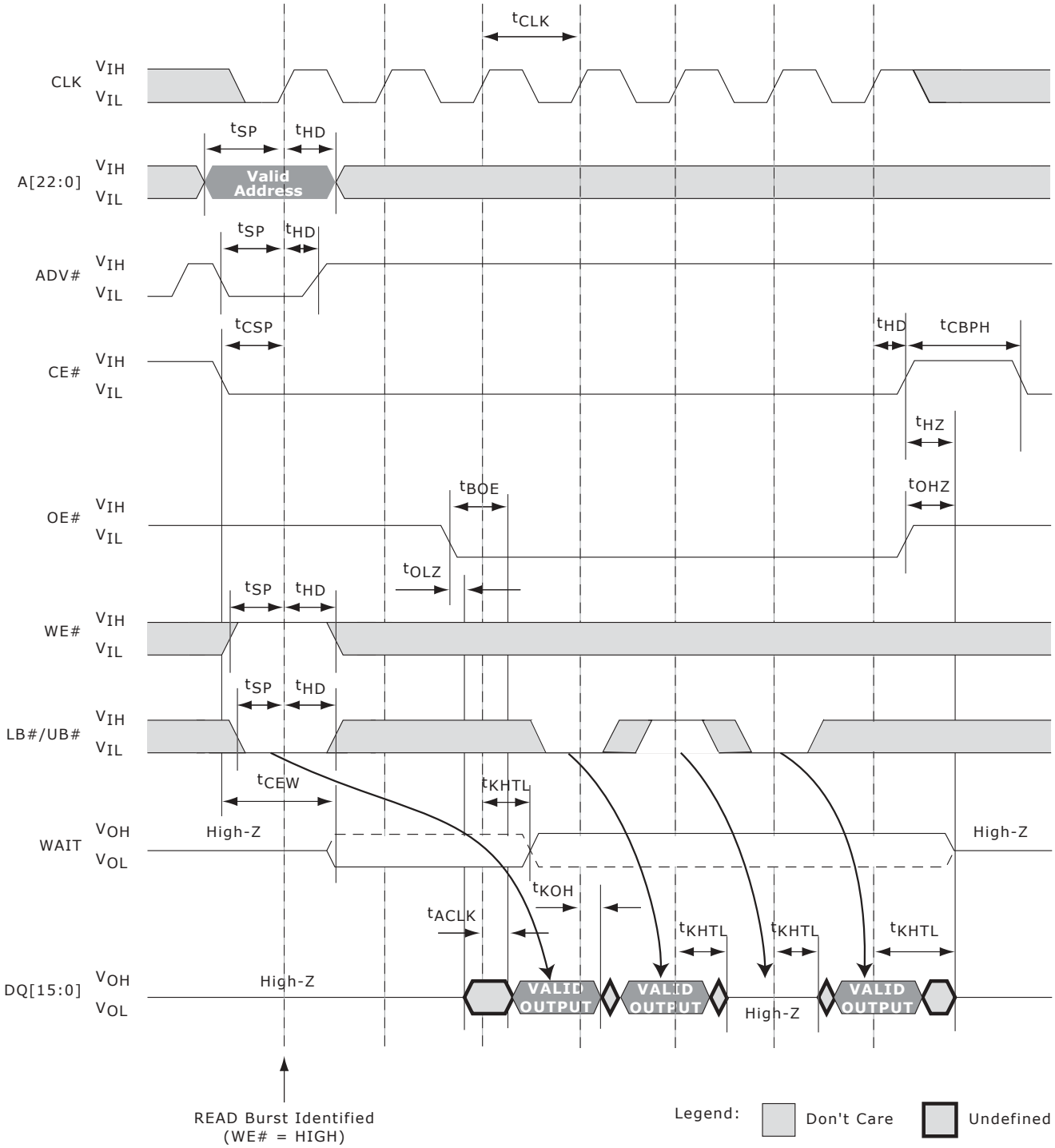
Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay. Clock rates below 50MHz (t_{CLK} > 20ns) are allowed as long as t_{CSP} specifications are met.*

Figure 33.5 Single-Access Burst Read Operation—Variable Latency



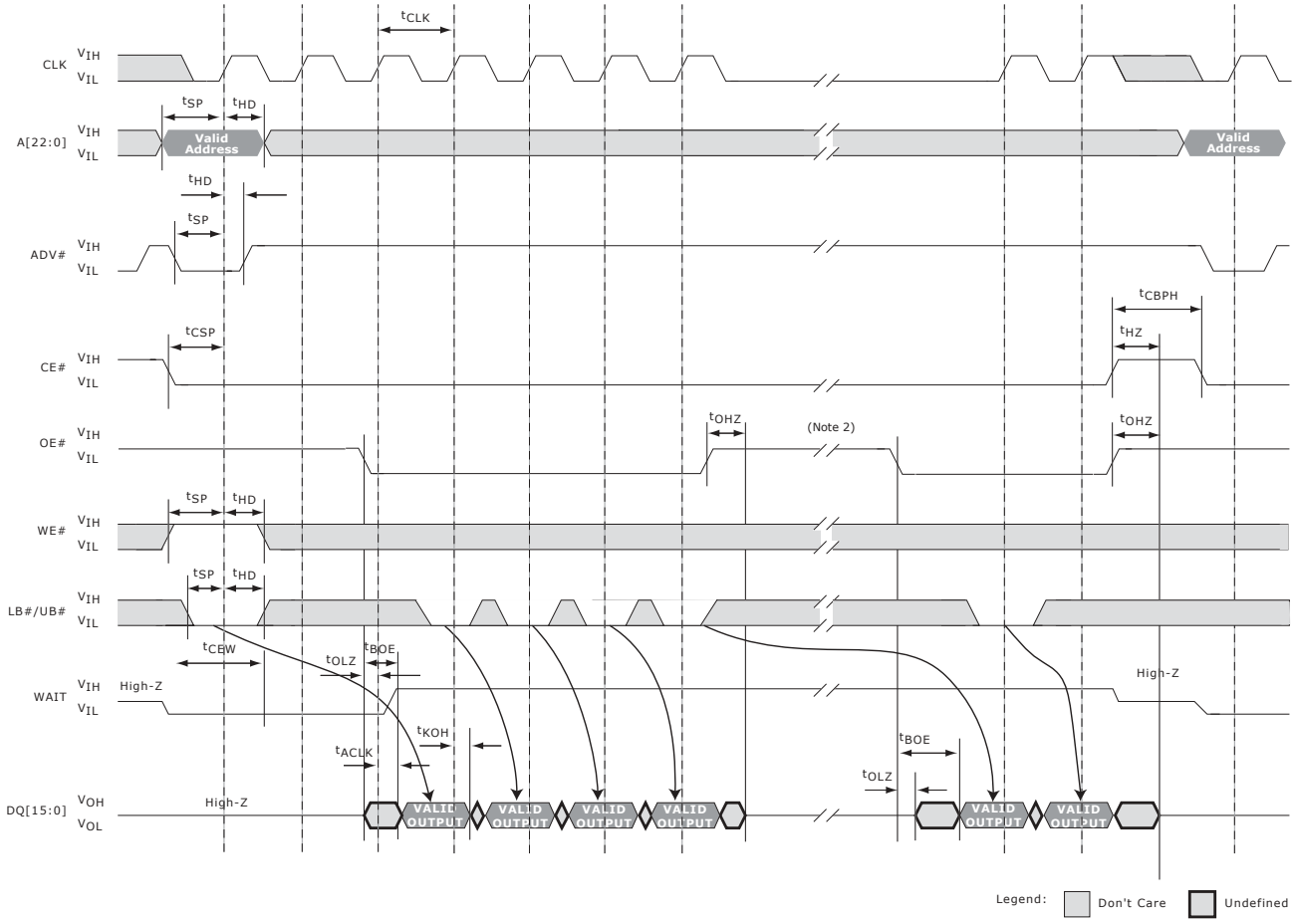
Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay. Clock rates below 50MHz (t_{CLK} > 20ns) are allowed as long as t_{CSP} specifications are met.*

Figure 33.6 Four-word Burst Read Operation—Variable Latency



Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*

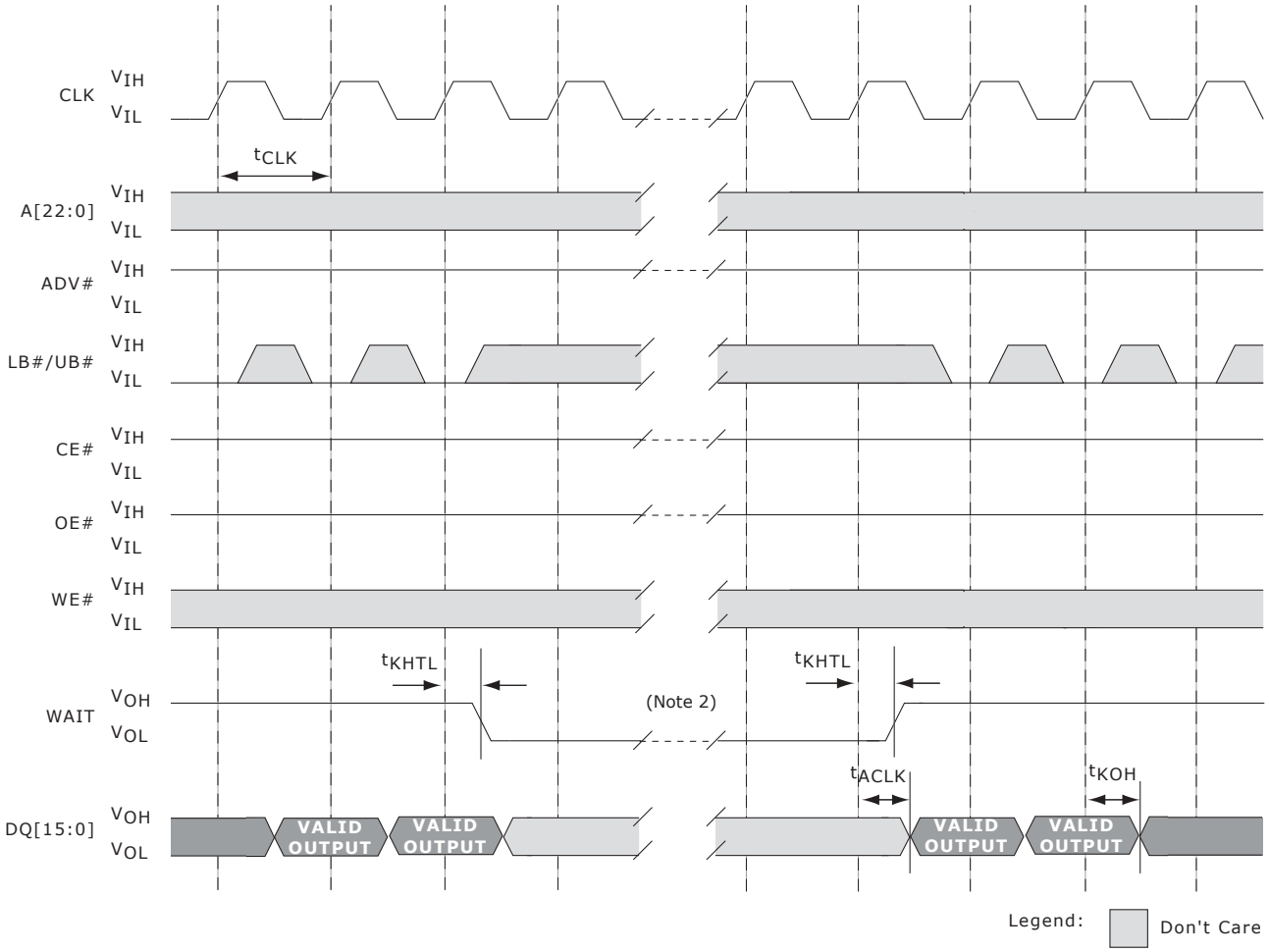
Figure 33.7 Four-word Burst Read Operation (with LB#/UB#)



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *OE# can stay Low during burst suspend. If OE# is Low, DQ[15:0] will continue to output valid data.*

Figure 33.8 Refresh Collision During Write Operation



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *Wait will assert LC + 1 or 2LC + 1 cycles for variable latency (depending upon refresh status).*

Figure 33.9 Continuous Burst Read Showing an Output Delay with BCR[8] = 0 for End-of-Row Condition

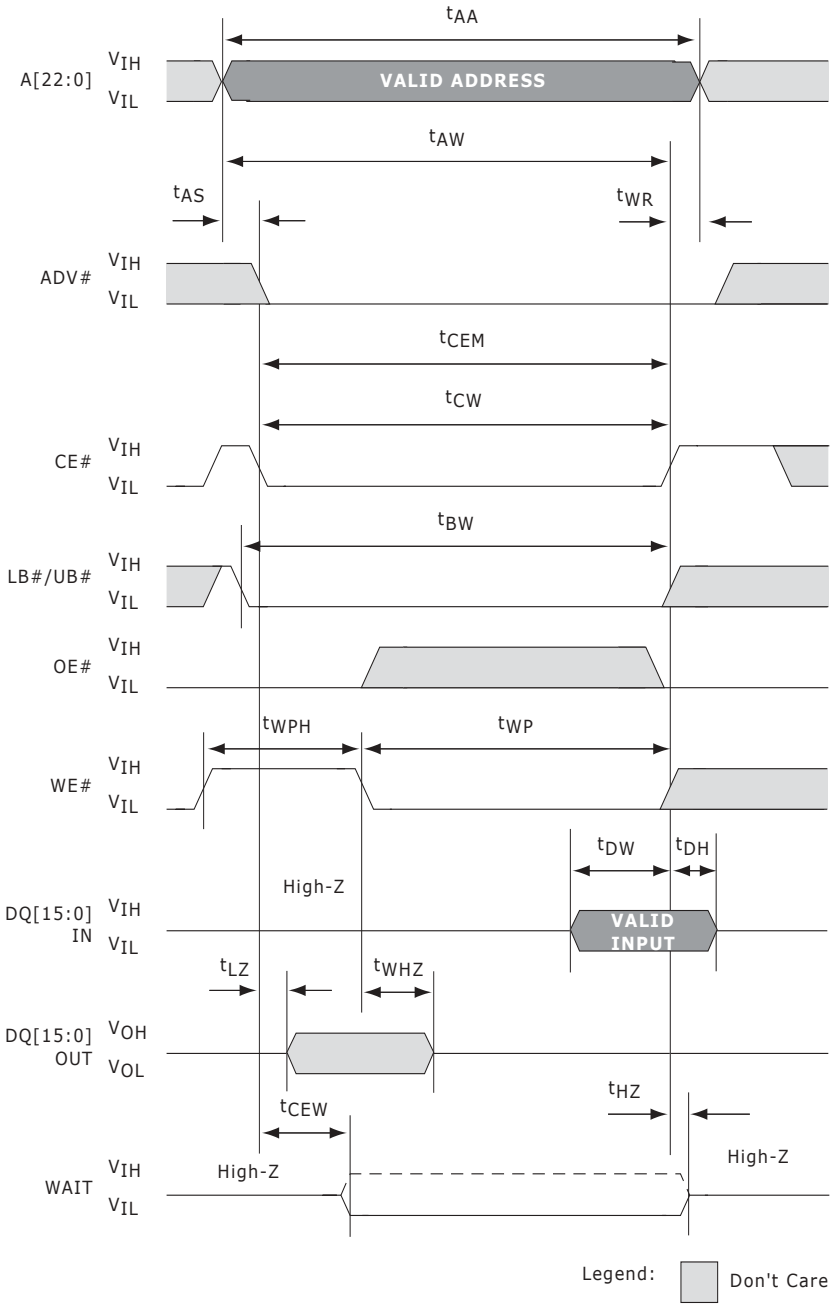


Figure 33.10 CE#-Controlled Asynchronous Write

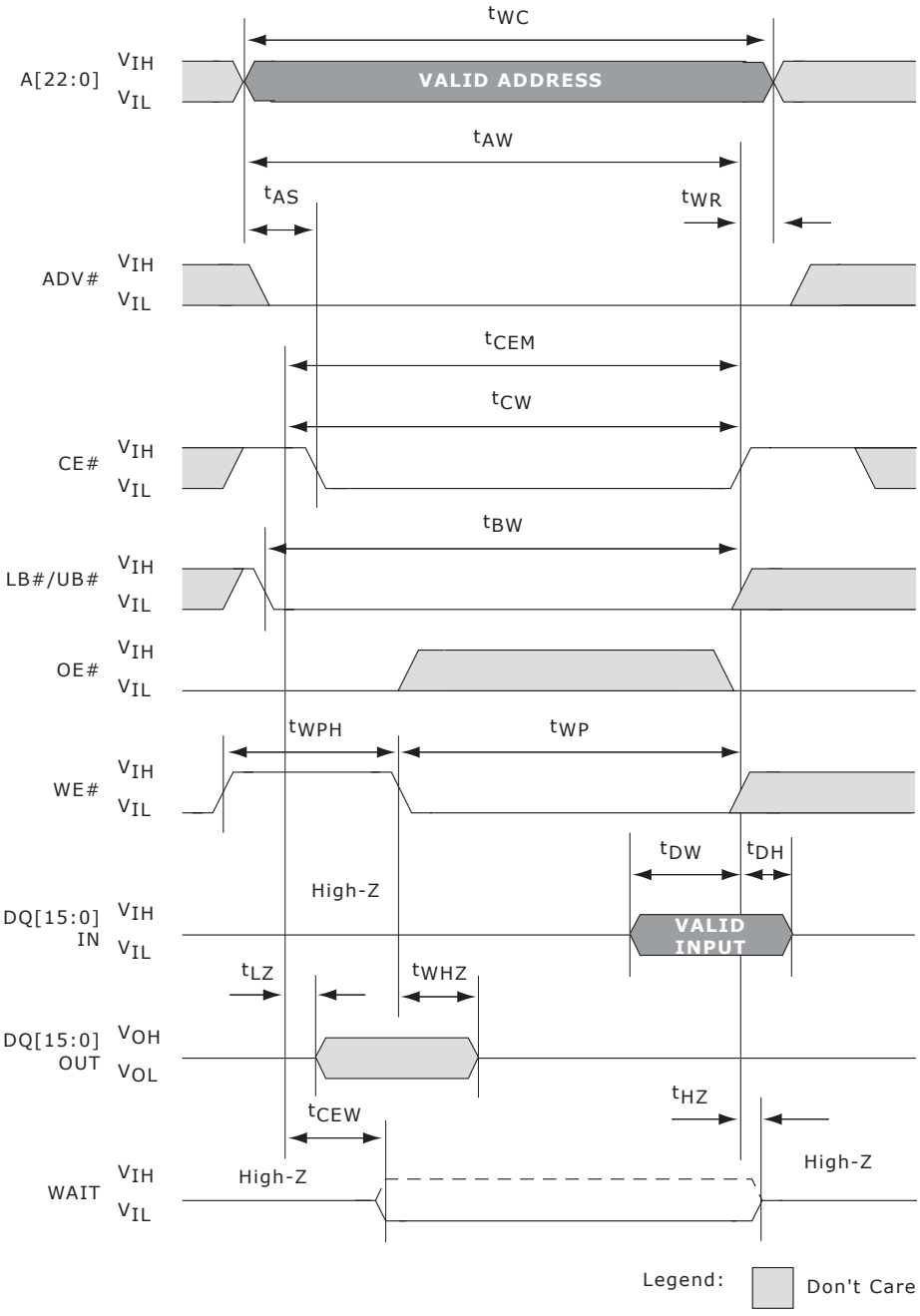


Figure 33.11 LB#/UB#-Controlled Asynchronous Write

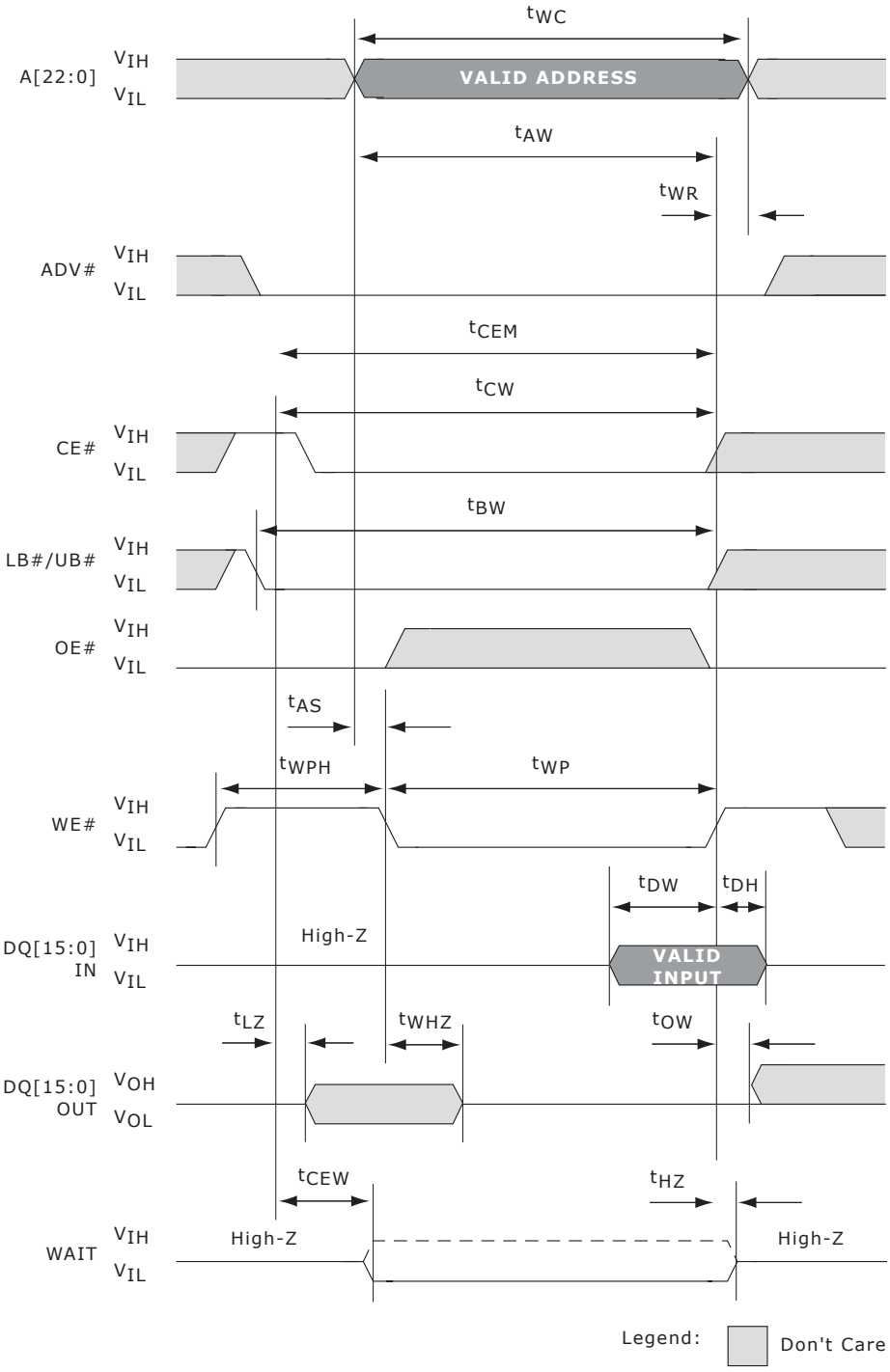


Figure 33.12 WE#-Controlled Asynchronous Write

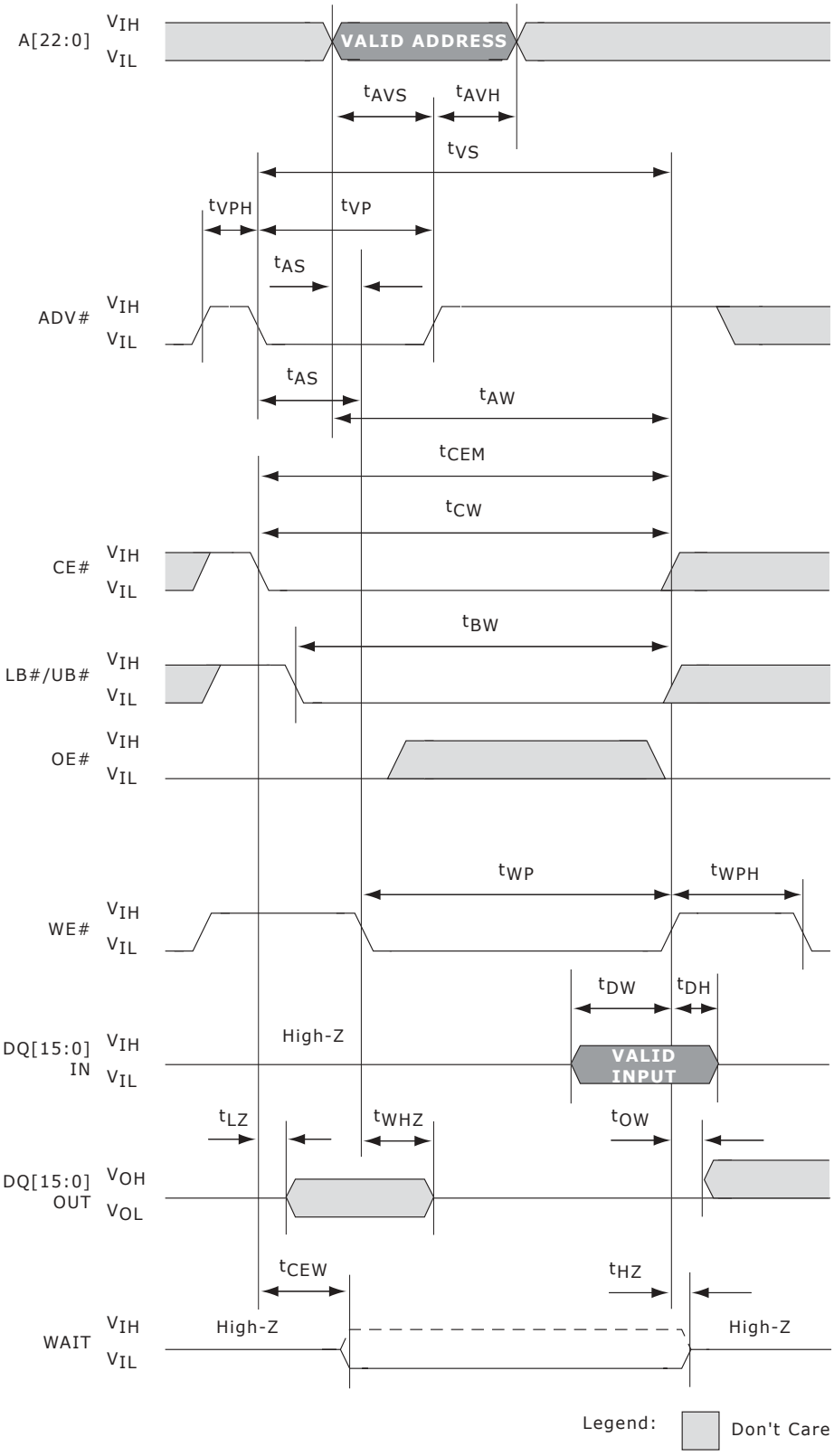
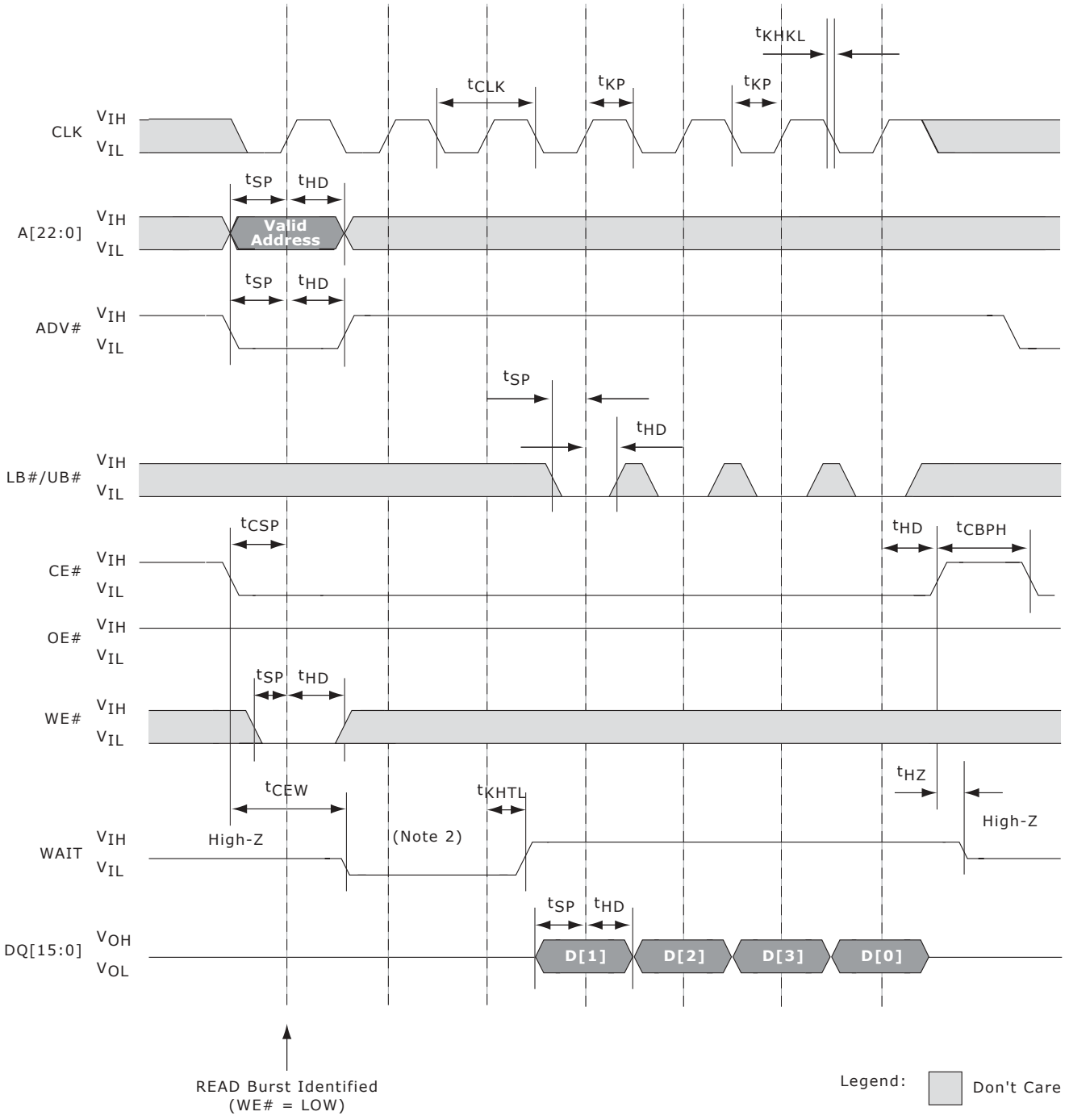


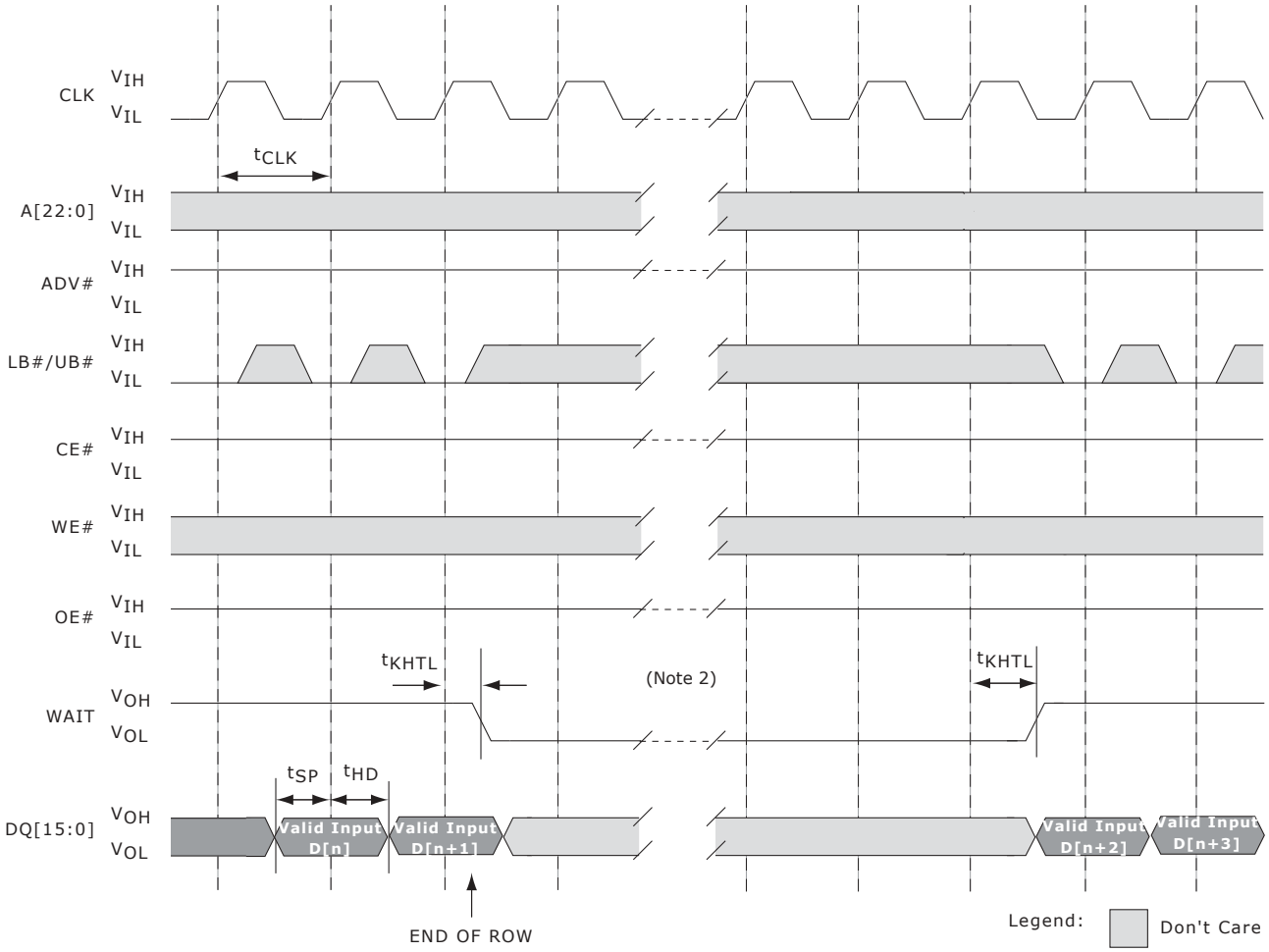
Figure 33.13 Asynchronous Write Using ADV#



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay; burst length four; burst wrap enabled.*

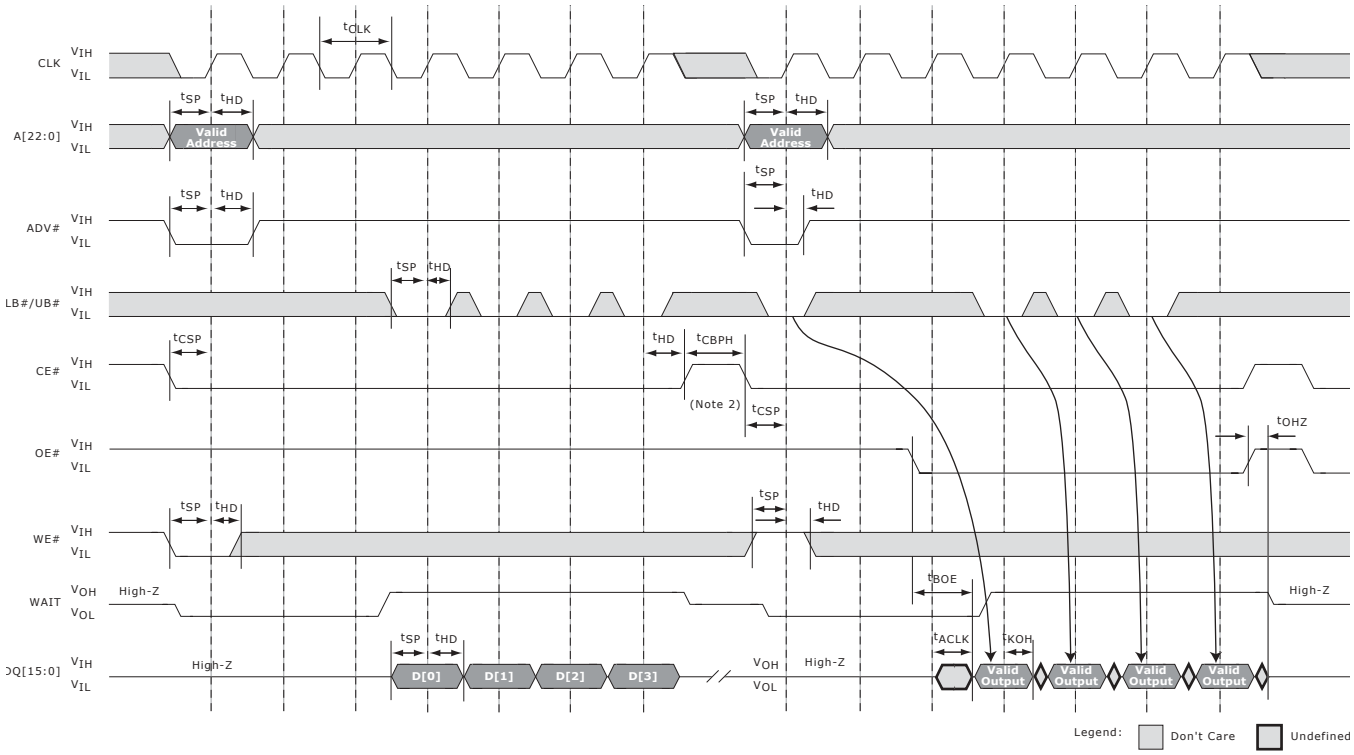
Figure 33.14 Burst Write Operation



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *Wait will assert LC + 1 or 2LC + 1 cycles for variable latency (depending upon refresh status).*

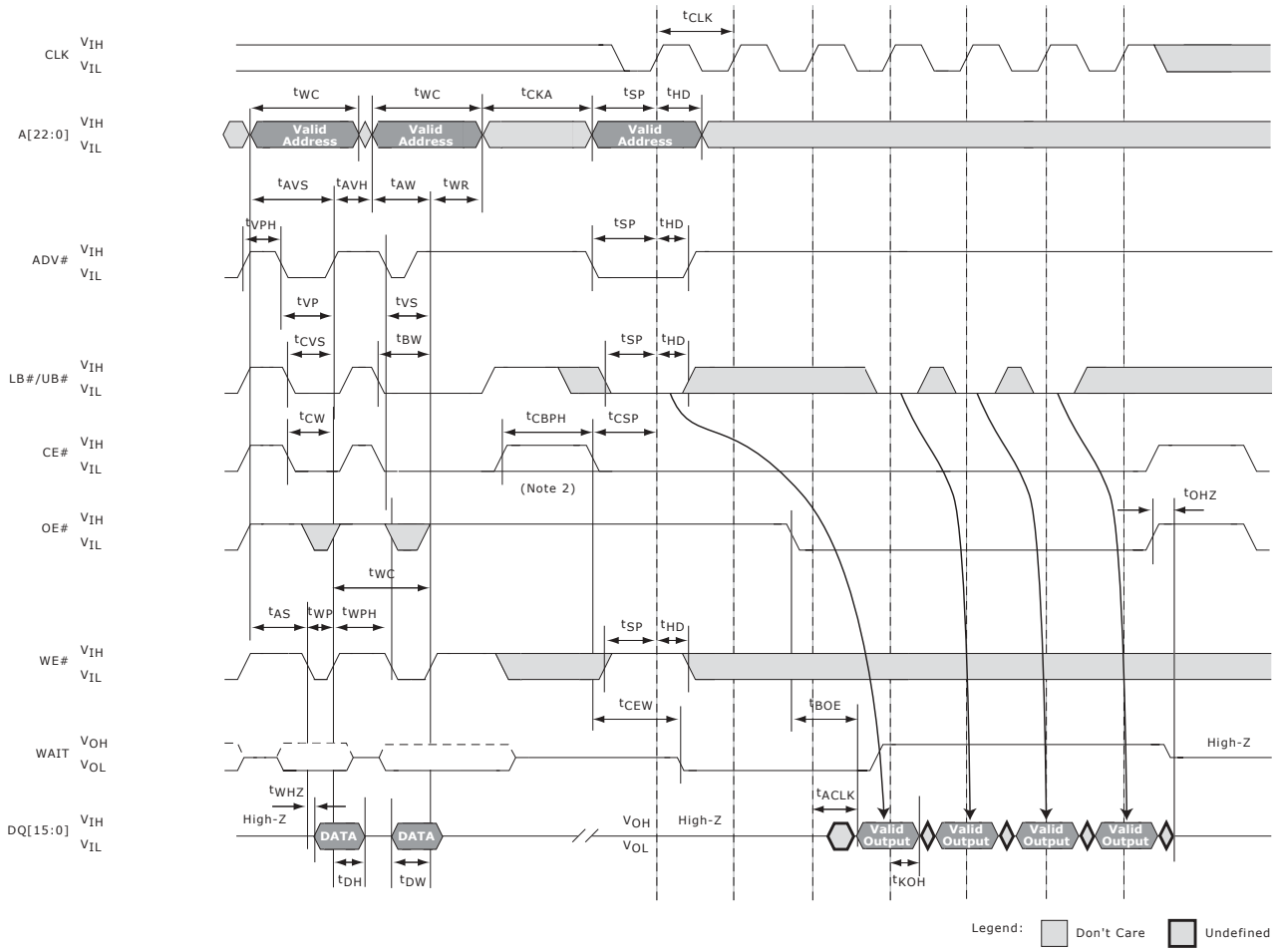
Figure 33.15 Continuous Burst Write Showing an Output Delay with BCR[8] = 0 for End-of-Row Condition



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *To allow self-refresh operations to occur between transactions, CE# must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation. CE# can stay Low between burst Read and burst Write operations.*

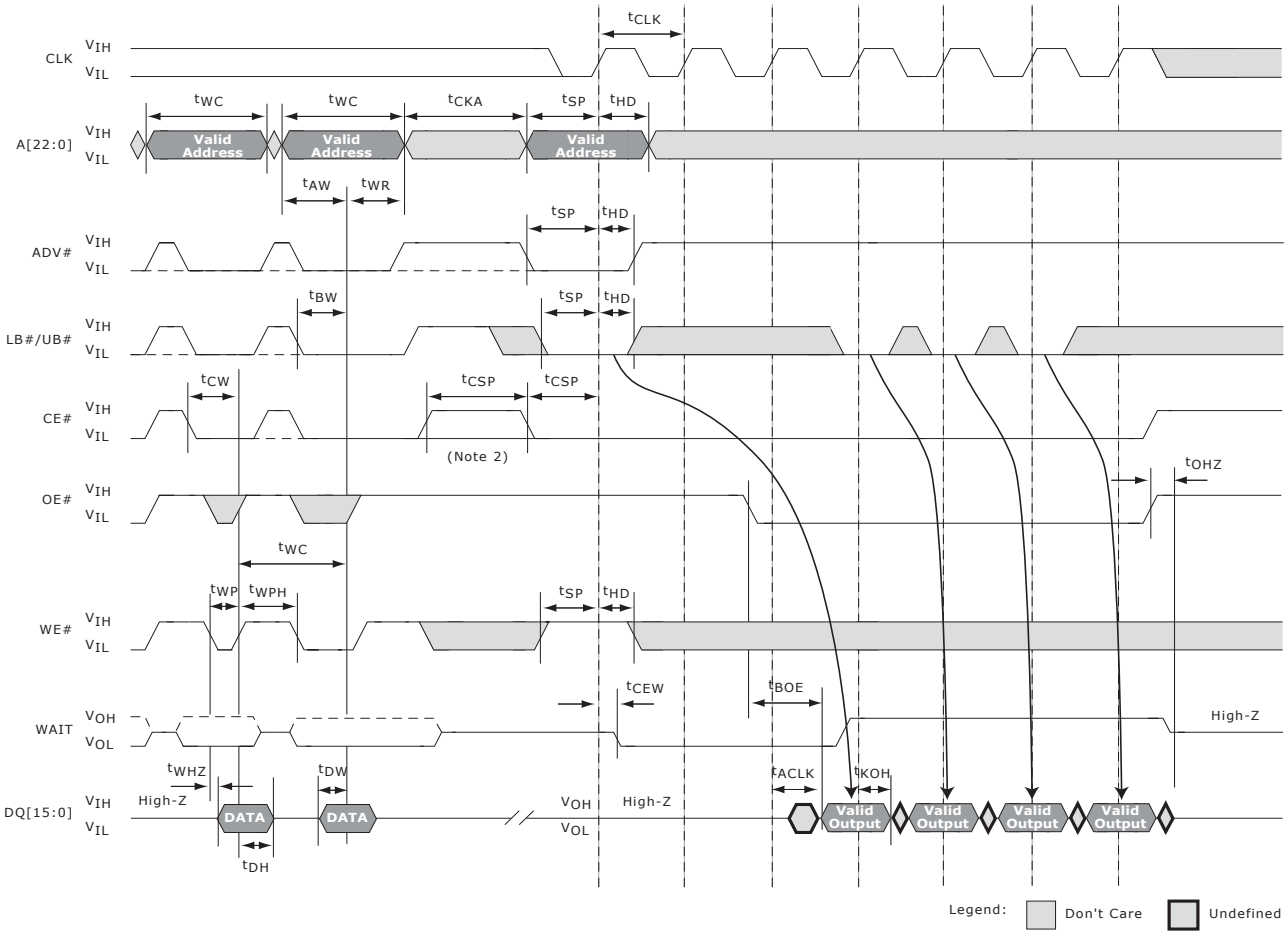
Figure 33.16 Burst Write Followed by Burst Read



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *When transitioning between asynchronous and variable-latency burst operations, CE# must go High. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation.*

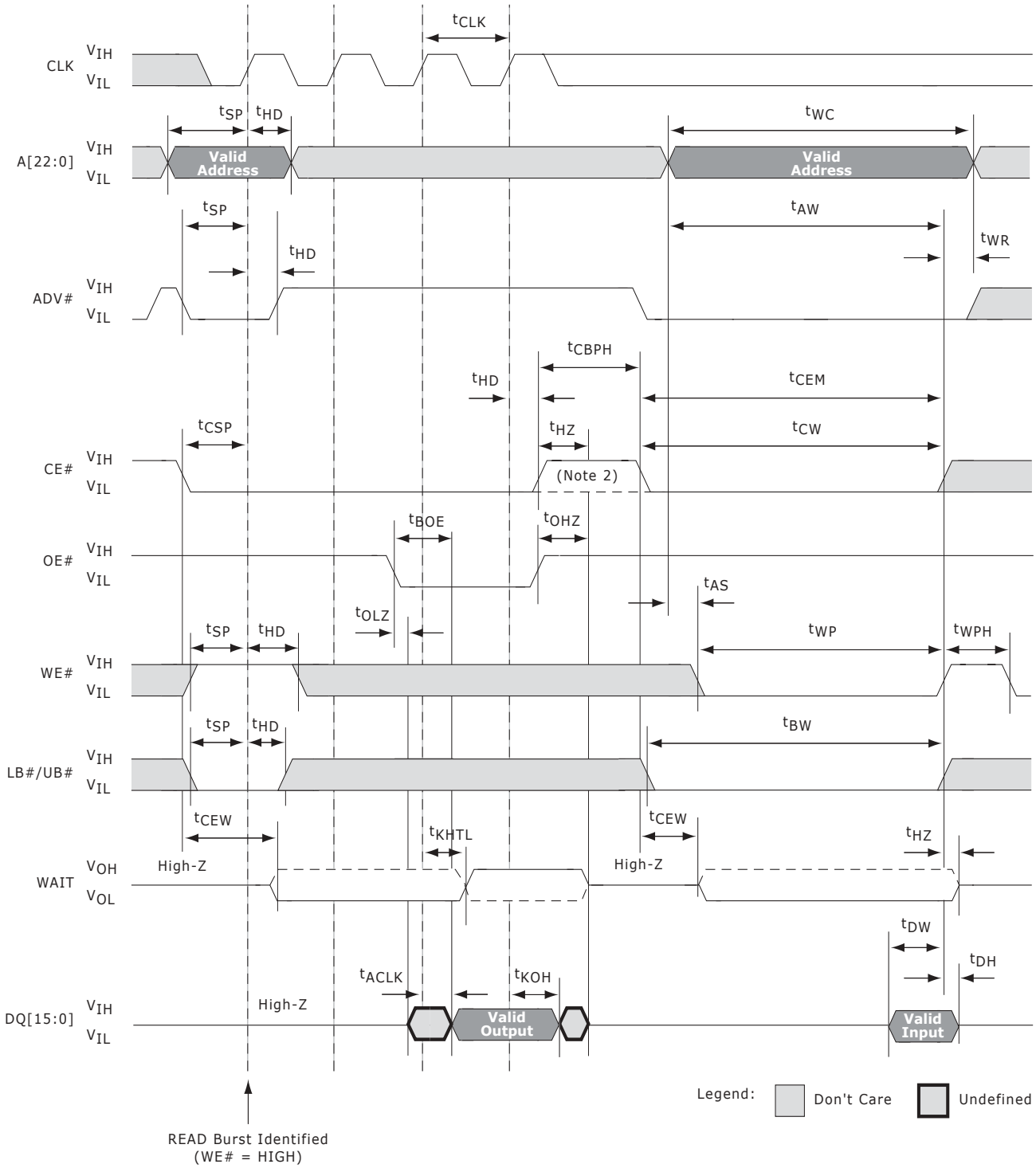
Figure 33.17 Asynchronous Write Followed by Burst Read



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *When transitioning between asynchronous and variable-latency burst operations, CE# must go High. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation.*

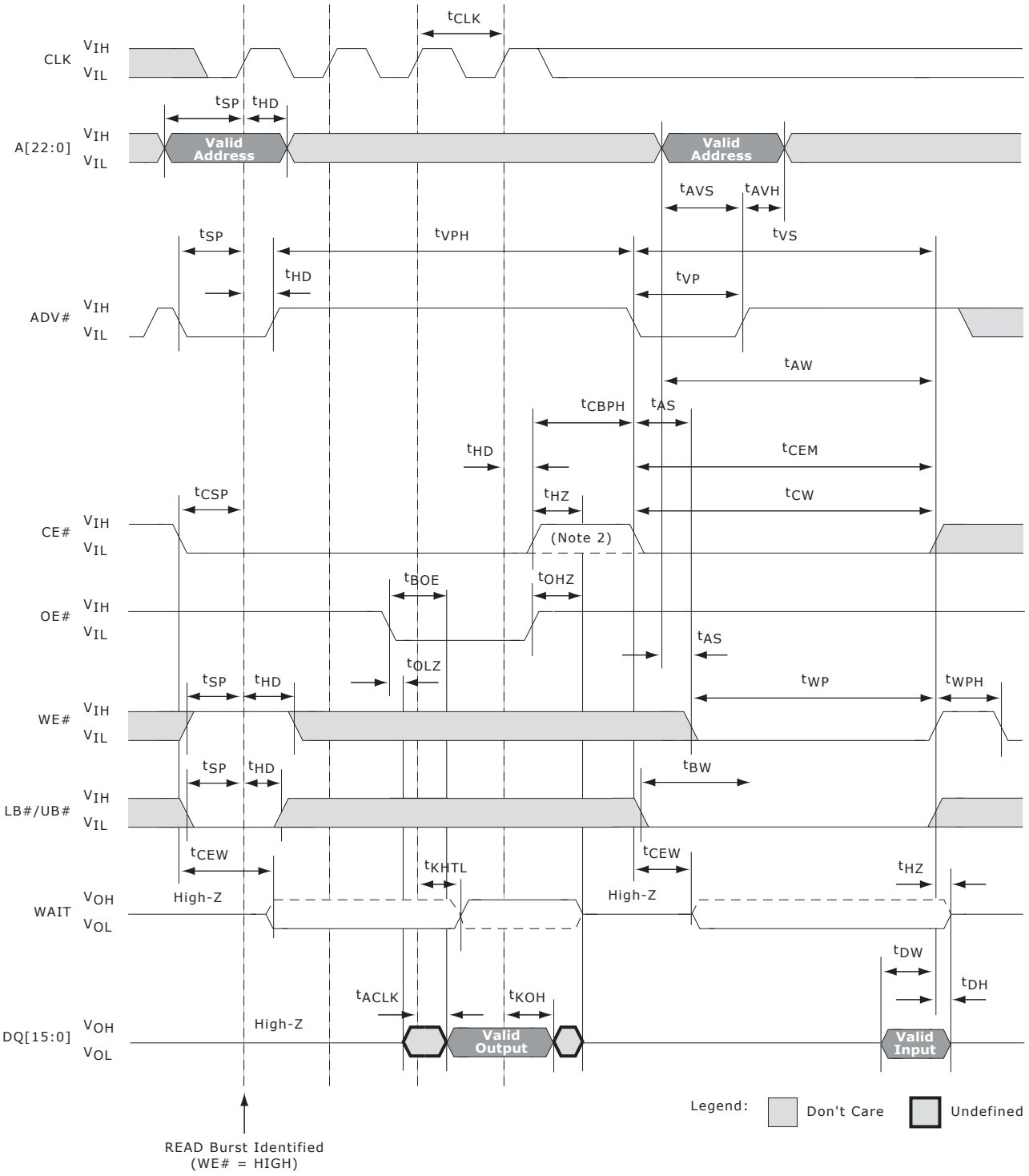
Figure 33.18 Asynchronous Write (ADV# Low) Followed By Burst Read



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *When transitioning between asynchronous and variable-latency burst operations, CE# must go High. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation.*

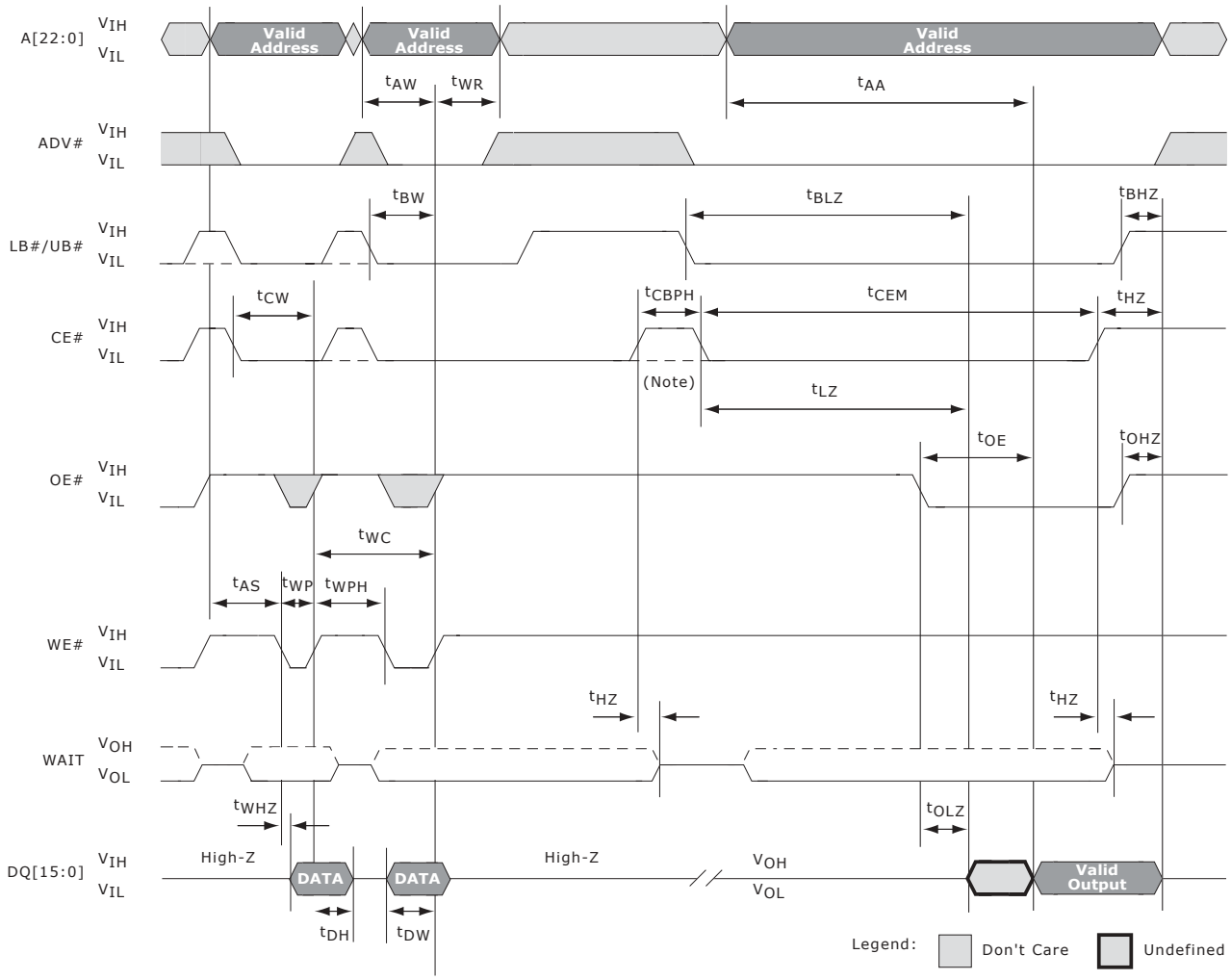
Figure 33.19 Burst Read Followed by Asynchronous Write (WE#-Controlled)



Notes:

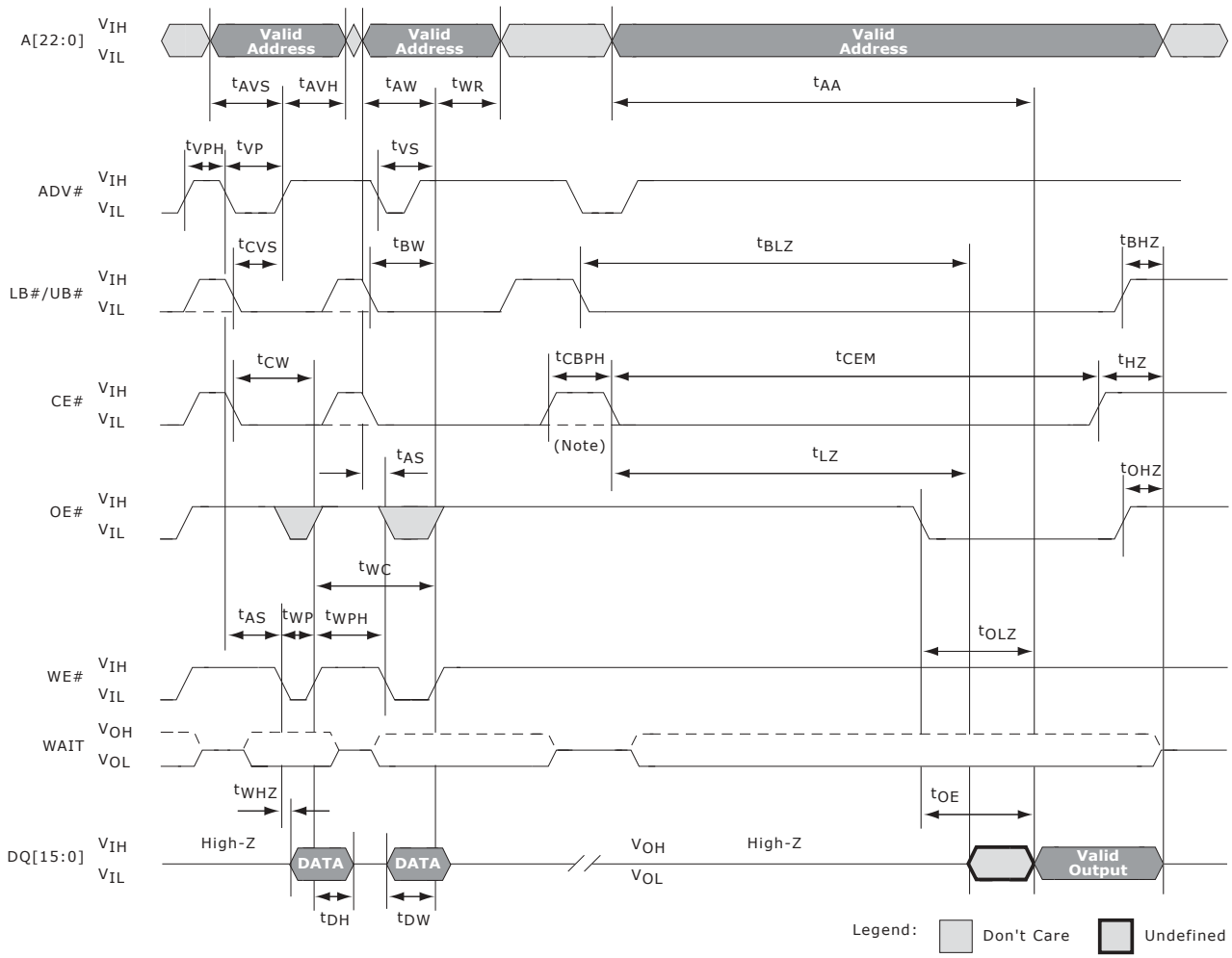
1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *When transitioning between asynchronous and variable-latency burst operations, CE# must go High. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation.*

Figure 33.20 Burst Read Followed by Asynchronous Write Using ADV#



Note: *CE# can stay Low when transitioning between asynchronous operations. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation.*

Figure 33.21 Asynchronous Write Followed by Asynchronous Read—ADV# Low



Note: *CE# can stay Low when transitioning between asynchronous operations. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation.*

Figure 33.22 Asynchronous Write Followed by Asynchronous Read

34 64M CellRAM Revision Summary

Revision A0 (March 9, 2005)

Initial release

Aysnc/Page CellularRAM Type 2

1.8V 32/16 Megabit (2Mx16, 1 Mx16) Asynchronous/Page CellularRAM

ADVANCE INFORMATION

Features

- **Asynchronous and page mode interface**
- **Random access time: 70 ns**
- **V_{CC}, V_{CCQ} voltages**
  1.70V–1.95V V_{CC}
  1.70V–3.30V V_{CCQ}
- **Page mode read access**
  Sixteen-word page size
  Interpage read access: 70 ns
  Intrapage read access: 20 ns
- **Low power consumption**
  Asynchronous READ < 20 mA
  Intrapage READ < 15 mA
  Standby: 110 µA (32 Mb), 80 µA (16 Mb)
  Deep power-down < 10 µA (TYP @ 25° C)
- **Low-power features**
  Temperature compensated refresh (TCR)
  On-chip temperature sensor
  Partial array refresh (PAR)
  Deep power-down (DPD) mode

General Description

CellularRAM™ products are high-speed, CMOS PSRAM memories developed for low-power, portable applications. The 32-Mb part is a DRAM core device organized as 2 Meg x 16 bits, and the 16-Mb part is a DRAM core device organized as 1 Meg x 16 bits. These devices include the industry-standard, asynchronous memory interface found on other low-power SRAM or Pseudo SRAM offerings.

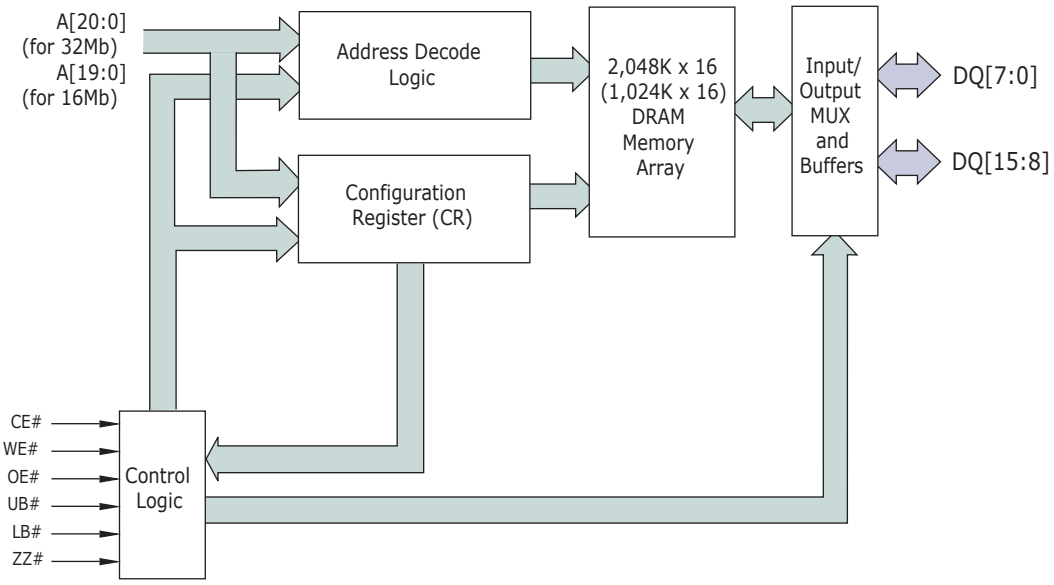
A user-accessible Configuration Register (CR) defines how the CellularRAM device performs on-chip refresh and whether page mode read accesses are permitted. This register is automatically loaded with a default setting during power-up and can be updated at any time during normal operation.

To operate seamlessly on an asynchronous memory bus, CellularRAM products incorporate a transparent self refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

Special attention has been focused on current consumption during self refresh. CellularRAM products include three system-accessible mechanisms to minimize refresh current. Temperature-Compensated Refresh (TCR) uses an on-chip sensor to adjust the refresh rate to match the device temperature. The refresh rate decreases at lower temperatures to minimize current consumption during standby. TCR can also be set by the system for maximum device temperatures of +85° C, +45° C, and +15° C. Setting sleep enable (ZZ#) to LOW enables one of two low-power modes: Partial Array Refresh (PAR); or Deep Power-Down (DPD). PAR limits refresh to only that part of the DRAM array that contains essential data. DPD halts refresh operation altogether and is used when no vital information is stored in the device. These three refresh mechanisms are accessed through the CR.

Publication Number CellRAM_05 **Revision** A **Amendment** 0 **Issue Date** August 25, 2005

35 Functional Block Diagram



Notes:*Funtional block diagrams illustrate simplified device operation. See truth table, signal descriptions, and timing diagrams for detailed information.*

Figure 35.1 Functional Block Diagram 2 Meg x 16 and 1 Meg x 16

Table 35.1 Signal Descriptions

Symbol	Type	Description
A[20:0]	Input	Address Inputs: Inputs for the address accessed during READ or WRITE operations. The address lines are also used to define the value to be loaded into the CR. On the 16-Mb device, A20 is not internally connected.
ZZ#	Input	Sleep Enable: When ZZ# is LOW, the CR can be loaded or the device can enter one of two low-power modes (DPD or PAR).
CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
OE#	Input	Output Enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
WE#	Input	Write Enable: Enables WRITE operations when LOW.
LB#	Input	Lower Byte Enable. DQ[7:0]
DQ[15:0]	Input/ Output	Data Inputs/Outputs.
NC		Not internally connected.
V_{CC}	Supply	Device Power Supply: (1.70V–1.95V) Power supply for device core operation.
V_{CCQ}	Supply	I/O Power Supply: (1.70V–3.30V) Power supply for input/output buffers.
V_{SS}	Supply	V_{SS} must be connected to ground.
$V_{SS}Q$	Supply	$V_{SS}Q$ must be connected to ground.

Table 35.2 Bus Operations

Mode	Power	CE#	WE#	OE#	LB#/ UB#	ZZ#	DQ[15:0]1	Notes
Standby	Standby	H	X	X	X	H	High-Z	(note 2),(note 5)
Read	Active	L	H	L	L	H	Data-Out	(note 1),(note 4)
Write	Active	L	L	X	L	H	Data-In	(note 1),(note 3),(note 4)
No Operation	Idle	L	X	X	X	H	X	(note 4),(note 5)
PAR	Partial Array Refresh	H	X	X	X	L	High-Z	(note 6)
DPD	Deep Power-Down	H	X	X	X	L	High-Z	(note 6)
Load Configuration Register	Active	L	L	X	X	L	High-Z	

Notes:

1. *When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When LB# only is in select mode, only DQ[7:0] are affected. When UB# only is in the select mode, DQ[15:8] are affected.*
2. *When the device is in standby mode, control inputs (WE#, OE#), address inputs, and data inputs/outputs are internally isolated from any external influence.*
3. *When WE# is invoked, the OE# input is internally disabled and has no effect on the I/Os.*
4. *The device consumes active power in this mode whenever addresses are changed.*
5. *$V_{IN} = V_{CCQ}$ or 0V; all device balls must be static (unswitched) in order to achieve minimum standby current.*
6. *DPD is enabled when configuration register bit CR[4] is "0"; otherwise, PAR is enabled.*

36 Functional Description

In general, the 32-Mb and 16-Mb CellularRAM Type 2 devices are high-density alternatives to SRAM and Pseudo-SRAM products, popular in low-power, portable applications. The 32-Mb device contains 33,554,432 bit DRAM core organized as 2,097,152 addresses by 16 bits. The 16-Mb device contains 16,777,216 bit DRAM core organized as 1,048,576 addresses by 16 bits. These devices include the industry standard, asynchronous memory interface found on other low-power SRAM or Pseudo-SRAM offerings. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

36.1 Power-Up Initialization

CellularRAM products include an on-chip voltage sensor that is used to launch the power-up initialization process. Initialization loads the CR with its default setting. V_{CC} and V_{CCQ} must be applied simultaneously. When they reach a stable level above 1.70V, the device requires 150 µs to complete its self-initialization process (see Figure 36.1). During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

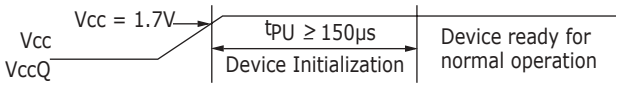


Figure 36.1 Power-Up Initialization Timing

37 Bus Operating Modes

These CellularRAM products incorporate the industry-standard, asynchronous interface found on other low-power SRAM or Pseudo SRAM offerings. This bus interface supports asynchronous READ and WRITE operations as well as the bandwidth-enhancing page mode READ operation. The specific interface that is supported is defined by the value loaded into the CR.

37.1 Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control interface (CE#, OE#, WE#, LB#/UB#). READ operations (Figure 37.1) are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH. Valid data is driven out of the I/Os after the specified access time has elapsed. WRITE operations (Figure 37.2) occur when CE#, WE#, and LB#/UB# are driven LOW. During WRITE operations, the level of OE# is a "Don't Care"; WE# overrides OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). WE# LOW time must be limited to t_{CEM}.

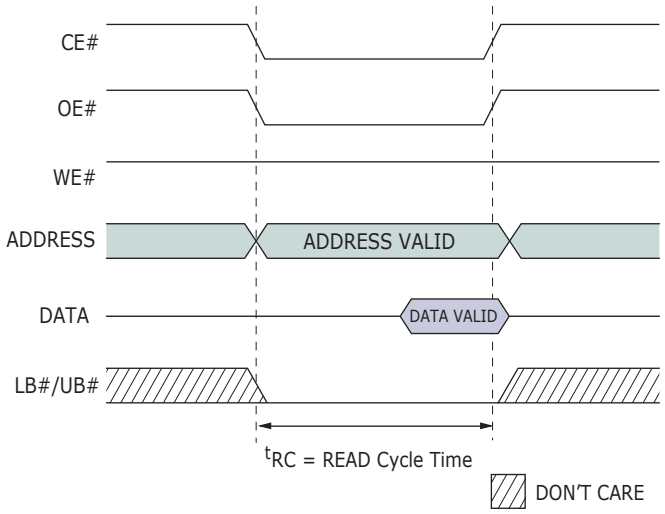


Figure 37.1 Asynchronous Mode READ Operation

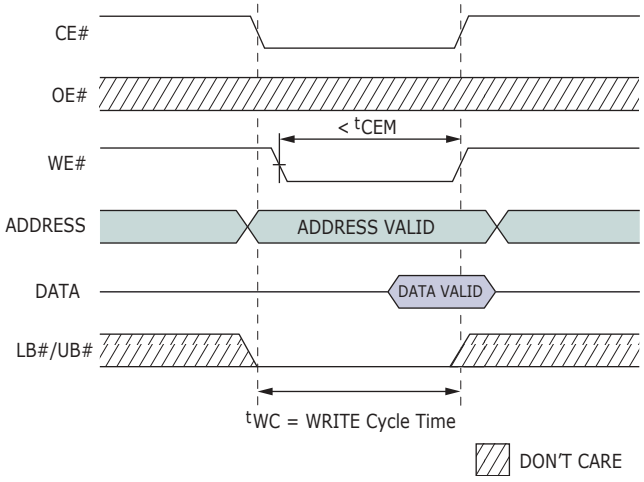


Figure 37.2 Asynchronous Mode WRITE Operation

37.2 Page Mode Read Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous read access is performed, then adjacent addresses can be quickly read by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Any change in addresses A[4] or higher initiates a new t_{AA} access. Figure 37.3 shows the timing diagram for a page mode access. Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality. The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than t_{CEM}.

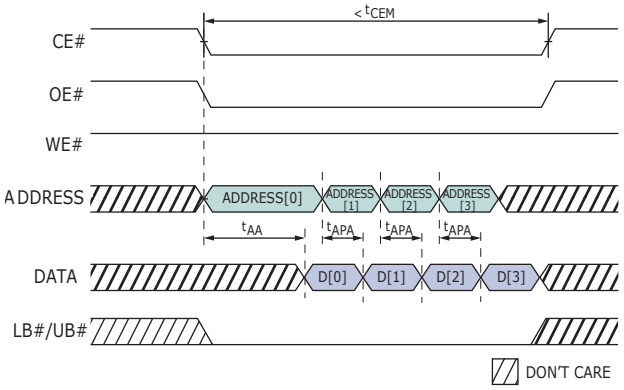


Figure 37.3 Page Mode READ Operation

37.3 LB#/UB# Operation

The Lower Byte (LB#) enable and Upper Byte (UB#) enable signals allow for byte-wide data transfers. During READ operations, enabled bytes are driven onto the DQs. The DQs associated with a disabled byte are put into a High-Z state during a READ operation. During WRITE operations, any disabled bytes are not transferred to the memory array; the internal value remains unchanged. During a WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first. When both the LB# and UB# are disabled (HIGH) during an operation, the device disables the data bus from receiving or transmitting data. Although the device seems to be deselected, the device remains in an active mode as long as CE# remains LOW.

38 Low-Power Operation

38.1 Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation on the full array. Standby operation occurs when CE# and ZZ# are HIGH.

The device enters a reduced power state during READ and WRITE operations where the address and control inputs remain static for an extended period of time. This mode continues until a change occurs to the address or control inputs.

38.2 Temperature Compensated Refresh

Temperature-Compensated Refresh (TCR) allows for adequate refresh at different temperatures. This CellularRAM device includes an on-chip temperature sensor. When the sensor is enabled, it continually adjusts the refresh rate according to the operating temperature. The on-chip sensor is enabled by default.

Three fixed refresh rates are also available, corresponding to temperature thresholds of +15° C, +45° C, and +85° C. The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. If the case temperature is +35° C, the system can minimize self-refresh current consumption by selecting the +45° C setting. The +15° C setting may result in inadequate refreshing and cause data corruption.

38.3 Partial Array Refresh

Partial Array Refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the system to reduce refresh current by only refreshing that part of the memory array that is absolutely necessary. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. Data stored in addresses not receiving refresh become corrupted. The mapping of these partitions can start at either the beginning or the end of the address map (Table 39.1 and Table 39.2 on page 179). READ and WRITE operations are ignored during PAR operation.

The device only enters PAR mode if the SLEEP bit in the CR has been set HIGH (CR[4] = 1). PAR can be initiated by bring the ZZ# ball to the LOW state for longer than 10 µs. Returning ZZ# to HIGH causes an exit from PAR and the entire array is immediately available for READ and WRITE operations.

Alternatively, PAR can be initiated using the CR software access sequence (see Software Access to the Configuration Register on page 176). PAR is enabled immediately upon setting CR[4] to "1" using this method. However, using software access to write to the CR alters the function of ZZ# so that ZZ# LOW no longer initiates PAR, although ZZ# continues to enable WRITEs to the CR. This functional change persists until the next time the device is powered up (see Figure 38.1).

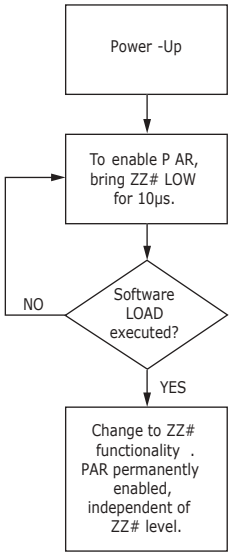


Figure 38.1 Software Access PAR Functionality

38.4 Deep Power-Down Operation

Deep Power-Down (DPD) operation disables all refresh-related activity. This mode is used when the system does not require the storage provided by the CellularRAM device. Any stored data becomes corrupted when DPD is entered. When refresh activity is re-enabled, the CellularRAM device requires 150 µs to perform an initialization procedure before normal operations can resume. READ and WRITE operations are ignored during DPD operation.

The device can only enter DPD if the SLEEP bit in the CR has been set LOW (CR[4] = 0). DPD is initiated by bringing ZZ# to the LOW state for longer than 10 µs. Returning ZZ# to HIGH causes the device to exit DPD and begin a 150-µs initialization process. During this 150–µs period, the current consumption is higher than the specified standby levels, but considerably lower than the active current specification.

Driving ZZ# LOW puts the device in the PAR mode if the SLEEP bit in the CR is set HIGH (CR[4] = 1).

The device should not be put into DPD using CR software access.

39 Configuration Register Operation

The Configuration Register (CR) defines how the CellularRAM device performs its transparent self-refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the CR. This register can be updated any time while the device is operating in a standby state. Figure 39.4 on page 178 describes the control bits used in the CR. At power up, the CR is set to 0010h.

39.1 Access Using ZZ#

The CR can be loaded using a WRITE operation immediately after ZZ# makes a HIGH-to-LOW transition (Figure 39.1). The values placed on addresses A[20:0] are latched into the CR on the rising edge of CE# or WE#, whichever occurs first. LB#/UB# are "Don't Care." Access using ZZ# is WRITE only.

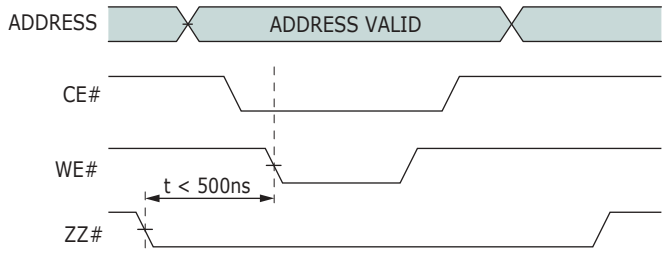


Figure 39.1 Load Configuration Register Operation

39.2 Software Access to the Configuration Register

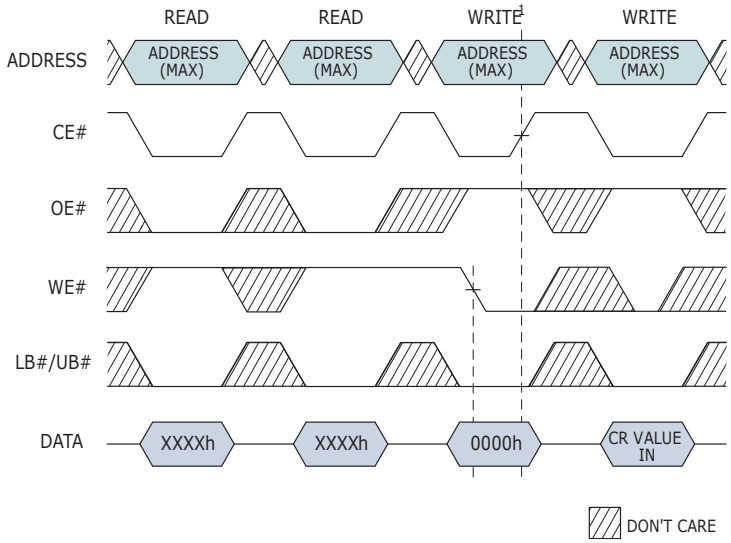
The contents of the CR can either be read or modified using a software sequence. The nature of this access mechanism may eliminate the need for the ZZ# ball.

If the software mechanism is used, ZZ# can simply be tied to V_{CCQ}. The port line typically used for ZZ# control purposes is no longer required. However, ZZ# should not be tied to V_{CCQ} if the system uses DPD; DPD cannot be enabled or disabled using the software access sequence.

The CR is loaded using a four-step sequence consisting of two READ operations followed by two WRITE operations (see Figure 39.2). The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 39.3). Note that a third READ cycle of the highest address cancels the access sequence until a different address is read.

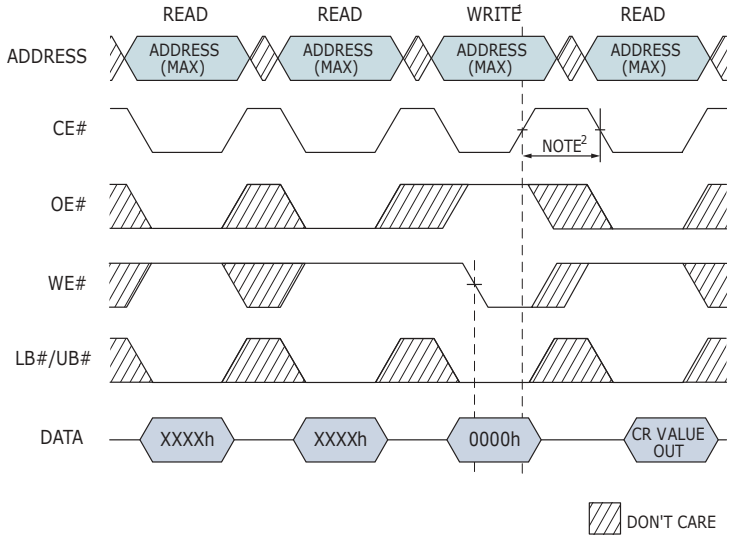
The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (1FFFFFh for 32 Mb and FFFFFh for 16 Mb); the content of this address is changed by using this sequence (note that this is a deviation from the CellularRAM specification). The data bus is used to transfer data into or out of bits 15–0 of the CR.

Writing to the CR using the software sequence modifies the function of the ZZ# ball. Once the software sequence loads the CR, the level of the ZZ# ball no longer enables PAR operation. PAR operation is updated whenever the software sequence loads a new value into the CR. This ZZ# functionality continues until the next time the device is powered-up. The operation of the ZZ# ball is not affected if the software sequence is only used to read the contents of the CR. The use of the software sequence does not affect the ability to perform the standard (ZZ#-controlled) method of loading the CR.



Note:
1.The WRITE on the third cycle must be CE#-controlled.

Figure 39.2 Software Access Load Configuration Register



Notes:
1.The WRITE on the third cycle must be CE#-controlled.
2.CE# must be HIGH for 150 ns before performing the cycle that reads the configuration register.

Figure 39.3 Software Access Read Configuration Register

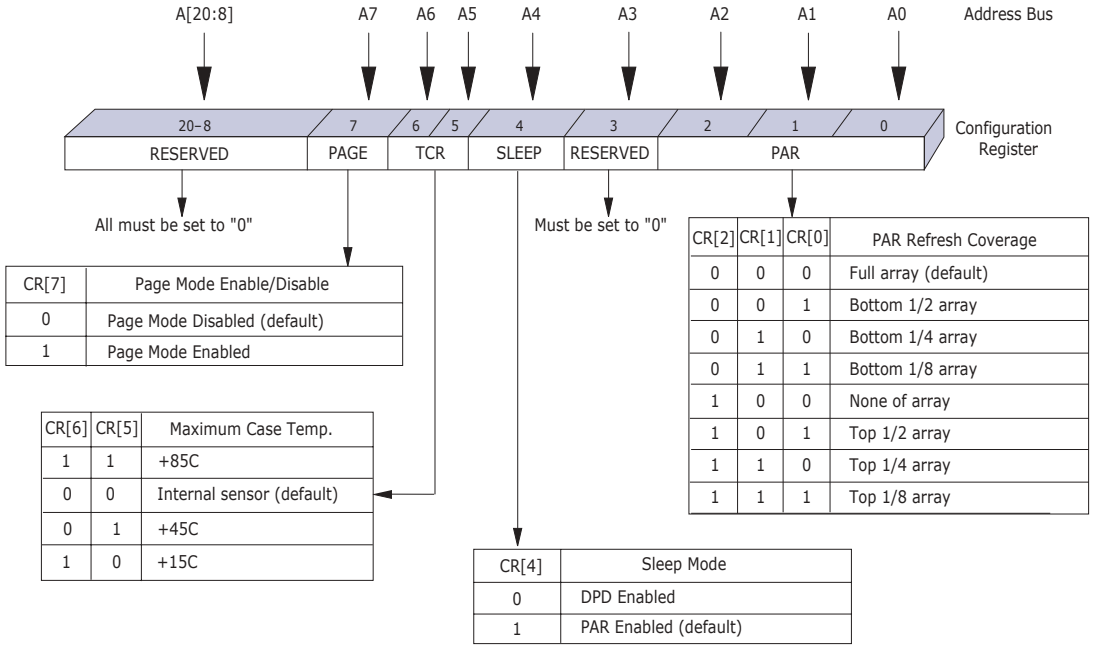


Figure 39.4 Configuration Register Bit Mapping

39.3 Partial Array Refresh (CR[2:0]) Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the system to reduce current by only refreshing that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 39.1 and Table 39.2 on page 179).

39.4 Sleep Mode (CR[4]) Default = PAR Enabled, DPD Disabled

The sleep mode bit determines which low-power mode is to be entered when ZZ# is driven LOW. If CR[4] = 1, PAR operation is enabled. If CR[4] = 0, DPD operation is enabled. PAR can also be enabled directly by writing to the CR using the software access sequence. Note that this then disables ZZ# initiation of PAR. DPD cannot be enabled or disabled using the software access sequence; this should only be done using ZZ# to access the CR.

DPD operation disables all refresh-related activity. This mode is used when the system does not require the storage provided by the CellularRAM device. Any stored data becomes corrupted when DPD is enabled. When refresh activity is re-enabled, the CellularRAM device requires 150 µs to perform an initialization procedure before normal operation can resume. DPD should not be enabled using CR software access.

39.5 Temperature Compensated Refresh (CR[6:5]) Default = On-Chip Temperature Sensor

This CellularRAM device includes an on-chip temperature sensor that automatically adjusts the refresh rate according to the operating temperature. The on-chip TCR is enabled by clearing both of the TCR bits in the refresh configuration register (CR[6:5] = 00b). Any other TCR setting enables a fixed refresh rate. When the on-chip temperature sensor is enabled, the device continually adjusts the refresh rate according to the operating temperature.

The TCR bits also allow for adequate fixed-rate refresh at three different temperature thresholds (+15° C, +45° C, and +85° C). The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. If the case temperature is +35° C, the system can minimize self-refresh current consumption by selecting the +45° C setting. The +15° C setting may result in inadequate refreshing and cause data corruption.

39.6 Page Mode READ Operation (CR[7]) Default = Disabled

The page mode operation bit determines whether page mode READ operations are enabled. In the power-up default state, page mode is disabled.

Table 39.1 32-Mb Address Patterns for PAR (CR[4] = 1)

CR[2]	CR[1]	CR[0]	Active Section	Address Space	Size	Density
0	0	0	Full die	000000h–1FFFFFh	2 Meg x 16	32Mb
0	0	1	One-half of die	000000h–0FFFFFh	1 Meg x 16	16Mb
0	1	0	One-quarter of die	000000h–07FFFFh	512K x 16	8Mb
0	1	1	One-eighth of die	000000h–03FFFFh	256K x 16	4Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	100000h–1FFFFFh	1 Meg x 16	16Mb
1	1	0	One-quarter of die	180000h–1FFFFFh	512K x 16	8Mb
1	1	1	One-eighth of die	1C0000h–1FFFFFh	256K x 16	4Mb

Table 39.2 16-Mb Address Patterns for PAR (CR[4] = 1)

CR[2]	CR[1]	CR[0]	Active Section	Address Space	Size	Density
0	0	0	Full die	00000h–FFFFFh	1 Meg x 16	16Mb
0	0	1	One-half of die	00000h–7FFFFh	512K x 16	8Mb
0	1	0	One-quarter of die	00000h–3FFFFh	256K x 16	4Mb
0	1	1	One-eighth of die	00000h–1FFFFh	128K x 16	2Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	80000h–FFFFFh	512K x 16	8Mb
1	1	0	One-quarter of die	C0000h–FFFFFh	256K x 16	4Mb
1	1	1	One-eighth of die	E0000h–FFFFFh	128K x 16	2Mb

40 Electrical Characteristics

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 40.1 Absolute Maximum Ratings

Parameter	Rating
Voltage to Any Ball Except V_{CC}, V_{CCQ} relative to V_{SS}	-0.50V to (4.0V or V_{CCQ} + 0.3V, whichever is less)
Voltage on V_{CC} Supply Relative to V_{SS}	-0.20V to 2.45V
Voltage on V_{CCQ} Supply Relative to V_{SS}	-0.20V to 4.0V
Storage Temperature	-55°C to 150°C
Wireless Operating Temperature	-30°C to 85°C

Note:
-30° C exceeds the CellularRAM Workgroup 1.0 specification of -25° C.

Table 40.2 Electrical Characteristics and Operating Conditions

Description	Conditions	Symbol		Min	Max	Units	Notes
Supply Voltage		V_{CC}		1.70	1.95	V	
I/O Supply Voltage		V_{CCQ}		1.70	3.30	V	
Input High Voltage		V_{IH}		1.4	V_{CCQ} + 0.2	V	(note 2),(note 3)
Input Low Voltage		V_{IL}		-0.2	+0.4	V	(note 4)
Output High Voltage	I_{OH} = -0.2mA	V_{OH}		0.80 V_{CCQ}		V	
Output Low Voltage	I_{OL} = 0.2mA	V_{OL}			0.20 V_{CCQ}	V	
Input Leakage Current	V_{IN} = 0 to V_{CCQ}	I_{LI}			1	µA	
Output Leakage Current	OE# = V_{IH} or Chip Disabled	I_{LO}			1	µA	
Operating Current							
Asynchronous Random READ/WRITE	V_{IN} = V_{CCQ} or 0V Chip Enabled, IOUT = 0	$I_{CC}1$			20	mA	(note 5)
Asynchronous Page READ		$I_{CC}1P$			15	mA	(note 5)
Standby Current	V_{IN} = V_{CCQ} or 0V CE# = V_{CCQ}	I_{SB}	32Mb		110	µA	(note 6)
			16Mb		80		

Notes:
1. *-30° C exceeds the CellularRAM Workgroup 1.0 specification of -25° C.*
2. *Input signals may overshoot to V_{CCQ} + 1.0 V for periods less than 2ns during transitions.*
3. *V_{IH} (MIN) value is not aligned with Cellular RAM Workgroup 1.0 specification of V_{CCQ} - 0.4 V.*
4. *Input signals may undershoot to V_{SS} - 1.0V for periods less than 2ns during transitions*
5. *This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.*
6. *I_{SB} (MAX) values measured with PAR set to FULL ARRAY and TCR set to +85° C. In order to achieve low standby current, all inputs must be driven to V_{CCQ} or V_{SS}. I_{SB} may be slightly higher for up to 500 ms after power-up or when entering standby mode.*

40.1 Maximum and Typical Standby Currents

The following tables and figures refer to the maximum and typical standby currents for the devices. The typical values shown in Figure 40.1 and Figure 40.2 are measured with the default on-chip temperature sensor control enabled. The maximum values shown in Table 40.7, Table 40.8, and Table 40.9 are measured with the relevant TCR bits set in the configuration register.

Table 40.3 Maximum Standby Currents for Applying PAR and TCR Settings – 32Mb

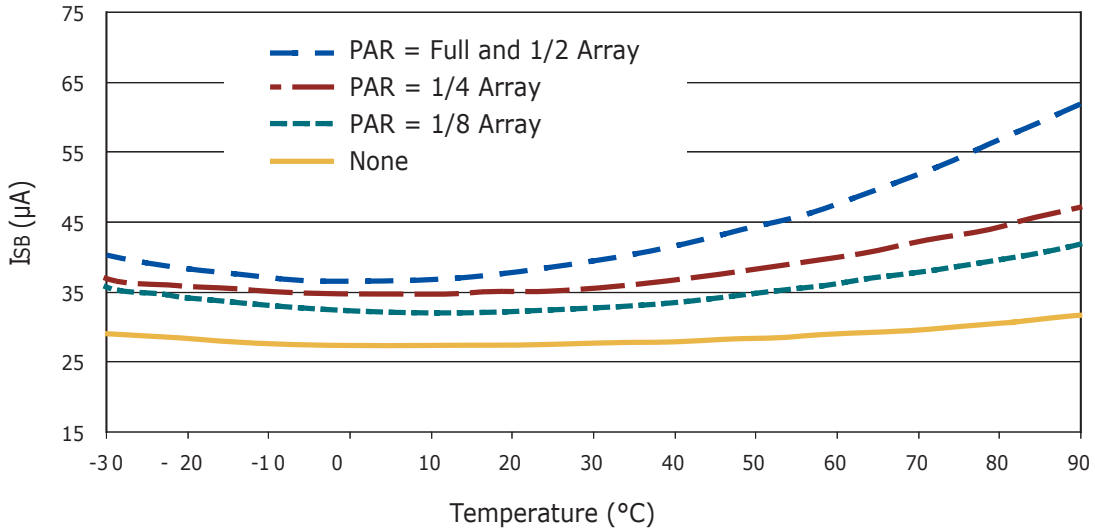
PAR	TCR		
	+15° C (CR[6:5] = 10b)	+45° C (CR[6:5] = 01b)	+85° C (CR[6:5] = 11b)
Full Array	70	80	110
1/2 Array	60	65	105
1/4 Array	57	60	95
1/8 Array	55	57	95
0 Array	50	55	70

Notes:
1. *For CR[6:5] = 00b (default), refer to Figure 40.1 for typical values.*
2. *In order to achieve low standby current, all inputs must be driven to V_{CCQ} or V_{SS}. ISB may be slightly higher for up to 500ms after power-up or when entering standby mode.*
3. *TCR values for 85° C are 100 percent tested. TCR values for 15° C and 45° C are sampled only.*

Table 40.4 Maximum Standby Currents for Applying PAR and TCR Settings – 16Mb

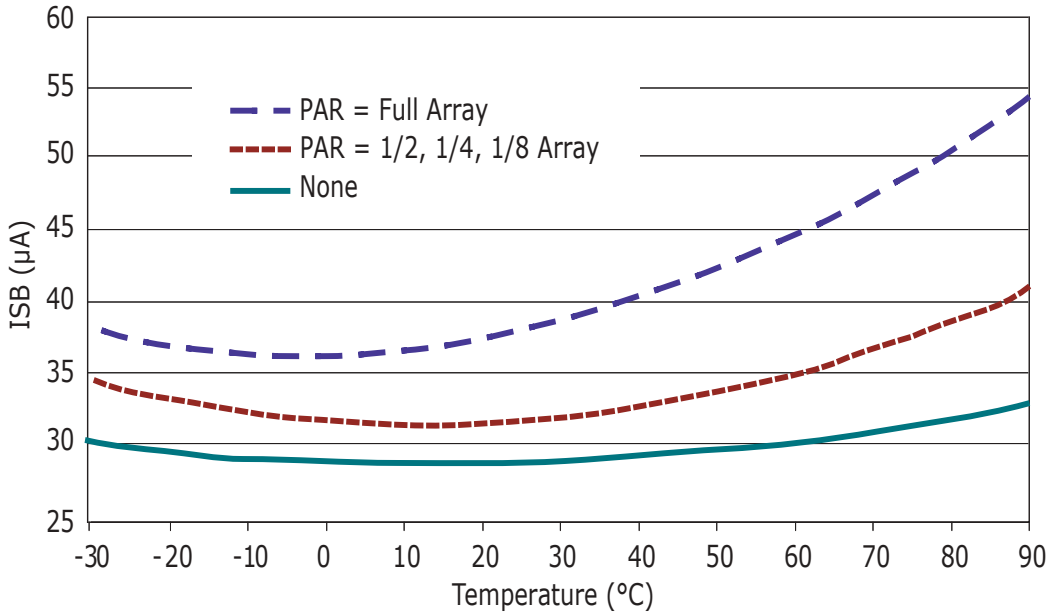
PAR	TCR		
	+15°C (CR[6:5] = 10b)	+45°C (CR[6:5] = 01b)	+85°C (CR[6:5] = 11b)
Full Array	40	50	80
1/2 Array	38	55	70
1/4 Array	38	55	70
1/8 Array	38	55	70
0 Array	35	40	65

Notes:
1. *For CR[6:5] = 00b (default), refer to Figure 40.2, "Typical Refresh Current vs. Temperature (ITCR) – 16Mb" on page 182 for typical values.*
2. *In order to achieve low standby current, all inputs must be driven to V_{CCQ} or V_{SS}. I_{SB} may be slightly higher for up to 500 ms after power-up or when entering standby mode.*
3. *TCR values for 85° C are 100 percent tested. TCR values for 15° C and 45° C are sampled only.*



Note: *Typical ISB currents for each PAR setting with the appropriate TCR selected, or temperature sensor enabled.*

Figure 40.1 Typical Refresh Current vs. Temperature (ITCR) – 32Mb



Note: *Typical I_{SB} currents for each PAR setting with the appropriate TCR selected, or temperaturesensor enabled.*

Figure 40.2 Typical Refresh Current vs. Temperature (ITCR) – 16Mb

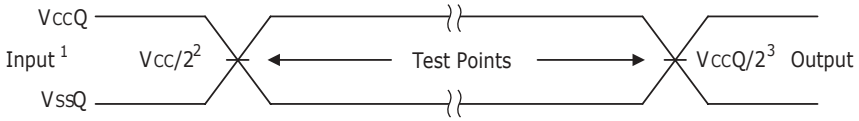
Table 40.5 Deep Power-Down Specifications and Conditions

Description	Conditions	Symbol	Typ	Units
Deep Power-Down	V_{IN} = V_{CCQ} or 0V; +25°C; ZZ# = 0V; CR[4] = 0	I_{ZZ}	10	µA

Table 40.6 Capacitance Specifications and Conditions

Description	Conditions	Symbol	Min	Max	Units	Notes
Input Capacitance	TC = +25ºC; f = 1 MHz; V_{IN} = 0V	CIN	2.0	6.5	pF	(note 1)
Input/Output Capacitance (DQ)		CIO	3.0	6.5	pF	(note 1)

Notes:
1. *These parameters are verified in device characterization and are not 100-percent tested.*



Notes:
1. *AC test inputs are driven at V_{CCQ} for a logic 1 and VSSQ for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.*
2. *Input timing begins at V_{CC}/2. Due to the possibility of a difference between V_{CC} and V_{CCQ}, the input test point may not be shown to scale.*
3. *Output timing ends at V_{CCQ}/2.*

Figure 40.3 AC Input/Output Reference Waveform

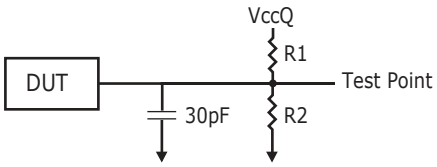


Figure 40.4 Output Load Circuit

Table 40.7 Output Load Circuit

V_{CCQ}	R1/R2
1.8V	2.7KΩ
2.5V	3.7KΩ
3.0V	4.5KΩ

Table 40.8 READ Cycle Timing Requirements

Parameter	Symbol	Min	Max	Units	Notes
Address Access Time	t_{AA}		70	ns	
Page Access Time	t_{APA}		20	ns	
LB#/UB# Access Time	t_{BA}		70	ns	
LB#/UB# Disable to High-Z Output	t_{BHZ}		8	ns	(note 2)
LB#/UB# Enable to Low-Z Output	t_{BLZ}	10		ns	(note 1)
Maximum CE# Pulse Width	t_{CEM}		8	µs	(note 3)
Chip Select Access Time	t_{CO}		70	ns	
Chip Disable to High-Z Output	t_{HZ}		8	ns	(note 2)
Chip Enable to Low-Z Output	t_{LZ}	10		ns	(note 1)
Output Enable to Valid Output	t_{OE}		20	ns	
Output Hold from Address Change	t_{OH}	5		ns	
Output Disable to High-Z Output	t_{OHZ}		8	ns	(note 2)
Output Enable to Low-Z Output	t_{OLZ}	5		ns	(note 1)
Page Cycle Time	t_{PC}	20		ns	
Read Cycle Time	t_{RC}	70		ns	

Notes:
1. *High-Z to Low-Z timings are tested with the circuit shown in Figure 40.4 on page 183. The Low-Z timings measure a 100-mV transition away from the High-Z ($V_{CCQ}/2$) level toward either V_{OH} or VOL.*
2. *Low-Z to High-Z timings are tested with the circuit shown in Figure 40.4 on page 183. The High-Z timings measure a 100-mV transition from either V_{OH} or V_{OL} toward $V_{CCQ}/2$.*
3. *Page mode enabled only.*

Table 40.9 WRITE Cycle Timing Requirements

Parameter	Symbol	Min	Max	Units	Notes
Address Setup Time	t_{AS}	0		ns	
Address Valid to End of Write	t_{AW}	70		ns	
Byte Select to End of Write	t_{BW}	70		ns	
CE# HIGH Time During Write	t_{CPH}	5		ns	
Chip Enable to End of Write	t_{CW}	70		ns	
Data Hold from Write Time	t_{DH}	0		ns	
Data Write Setup Time	t_{DW}	23		ns	
Chip Enable to Low-Z Output	t_{LZ}	10		ns	(note 1)
End Write to Low-Z Output	t_{OW}	5		ns	(note 1)
Write Cycle Time	t_{WC}	70		ns	
Write to High-Z Output	t_{WHZ}		8	ns	(note 2)
Write Pulse Width	t_{WP}	46		ns	(note 3)
Write Pulse Width HIGH	t_{WPH}	10		ns	
Write Recovery Time	t_{WR}	0		ns	

Notes:
1. *High-Z to Low-Z timings are tested with the circuit shown in Figure 40.4 on page 183. The Low-Z timings measure a 100-mV transition away from the High-Z ($V_{CCQ}/2$) level toward either V_{OH} or V_{OL}.*
2. *Low-Z to High-Z timings are tested with the circuit shown in Figure 40.4 on page 183. The High-Z timings measure a 100-mV transition from either V_{OH} or V_{OL} toward $V_{CCQ}/2$.*
3. *WE# LOW time must be limited to ^{t}CEM (8is).*

Table 40.10 Load Configuration Register Timing Requirements

Description	Symbol	Min	Max	Units
Address Setup Time	t_{AS}	0		ns
Address Valid to End of Write	t_{AW}	70		ns
Chip Deselect to ZZ# LOW	t_{CDZZ}	5		ns
Chip Enable to End of Write	t_{CW}	70		ns
Write Cycle Time	t_{WC}	70		ns
Write Pulse Width	t_{WP}	40		ns
Write Recovery Time	t_{WR}	0		ns
ZZ# LOW to WE# LOW	t_{ZZWE}	10	500	ns

Table 40.11 Deep Power-Down Timing Requirements

Description	Symbol	Min	Max	Units
Chip Deselect to ZZ# LOW	t_{CDZZ}	5		ns
Deep Power-Down Recovery	t_{R}	150		µs
Minimum ZZ# Pulse Width	t_{ZZMIN}	10		µs

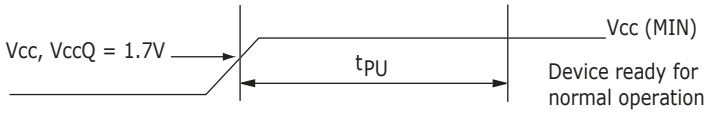


Figure 40.5 Power-Up Initialization Period

Table 40.12 Power-Up Initialization Timing Requirements

Description	Symbol	Min	Max	Units
Power-Up Initialization Period	t_{PU}	150		µs

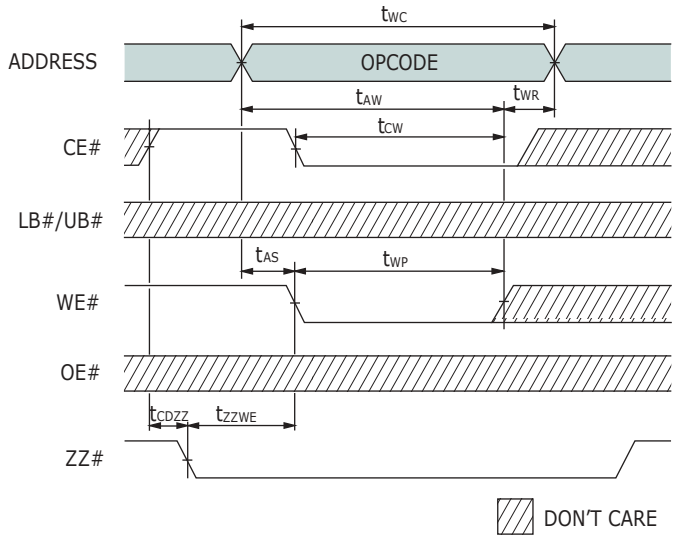


Figure 40.6 Load Configuration Register

Table 40.13 Load Configuration Register Timing Requirements

Symbol	Min	Max	Units
t_{AS}	0		ns
t_{AW}	70		ns
t_{CDZZ}	5		ns
t_{CW}	70		ns
t_{WC}	70		ns
t_{WP}	40		ns
t_{WR}	0		ns
t_{ZZWE}	10	500	ns

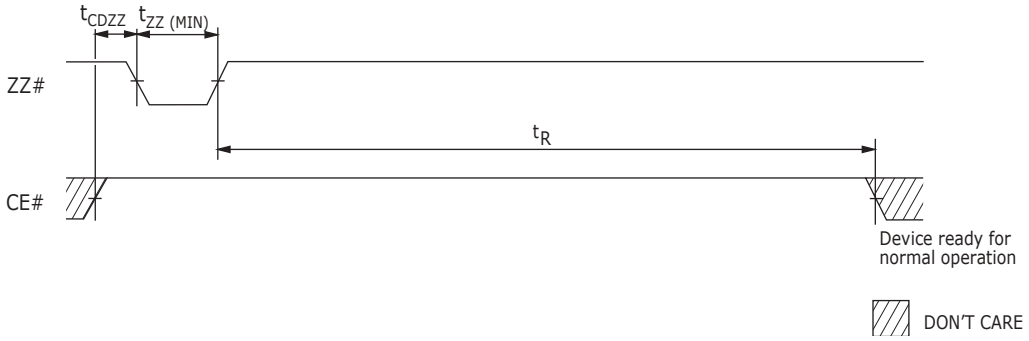


Figure 40.7 Deep Power-Down – Entry/Exit

Table 40.14 Deep Power-Down Timing Parameters

Symbol	Min	Max	Units
t_{CDZZ}	5		ns
t_R	150		µs
$t_{ZZ\ (MIN)}$	10		µs

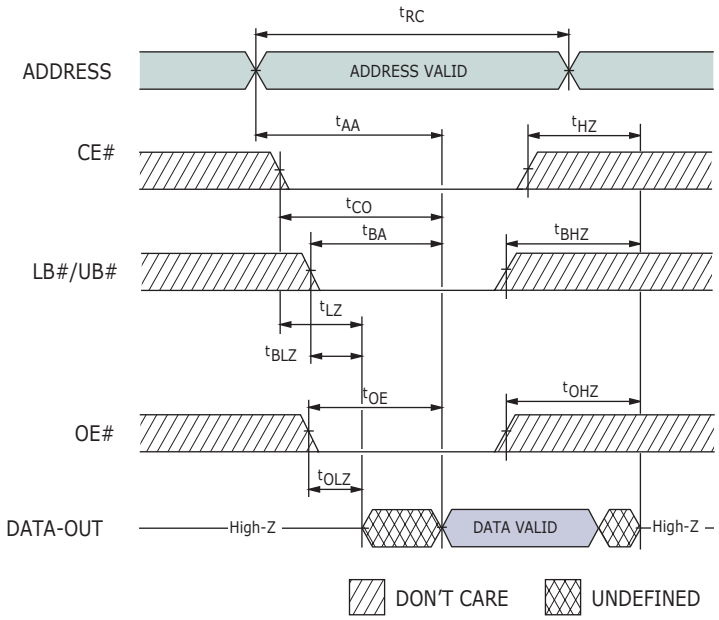


Figure 40.8 Single READ Operation (WE# = V_{IH})

Table 40.15 Single READ Timing Parameters

Symbol	Min	Max	Units
t_{AA}		70	ns
t_{BA}		70	ns
t_{BHZ}		8	ns
t_{BLZ}	10		ns
t_{CO}		70	ns
t_{HZ}		8	ns
t_{LZ}	10		ns
t_{OE}		20	ns
t_{OHZ}		8	ns
t_{OLZ}	5		ns
t_{RZ}	70		ns

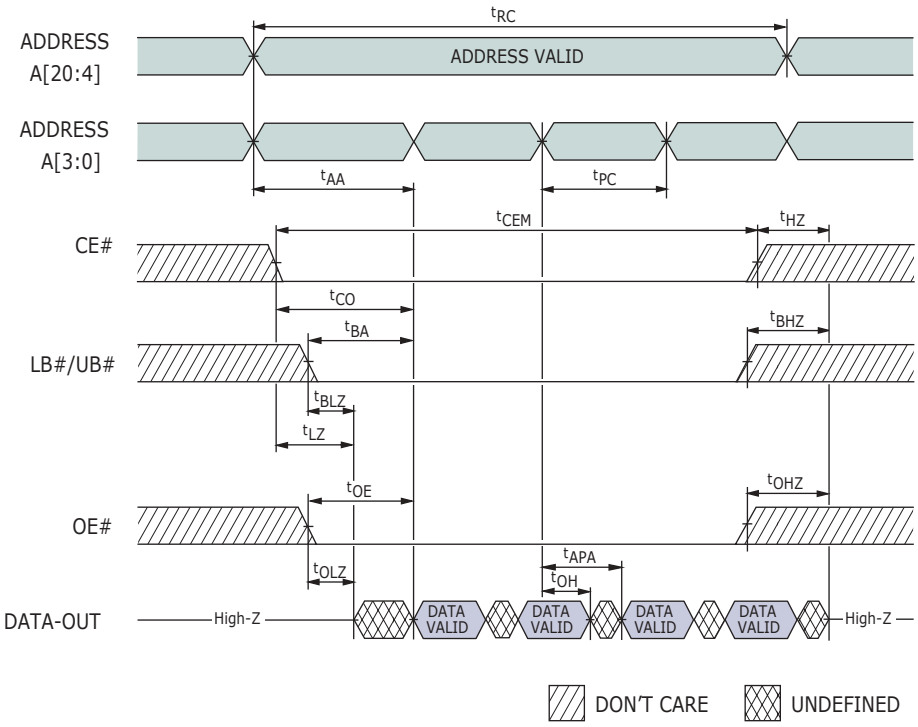


Figure 40.9 Page Mode READ Operation (WE# = V_{IH})

Table 40.16 Page Mode READ Timing Parameters (WE# = VIH)

Symbol	Min	Max	Units
t_{AA}		70	ns
t_{APA}		20	ns
t_{BA}		70	ns
t_{BHZ}		8	ns
t_{BLZ}	10		ns
t_{CEM}		8	µs
t_{CO}		70	ns
t_{HZ}		8	ns
t_{LZ}	10		ns
t_{OE}		20	ns
t_{OH}	5		ns
t_{OHZ}		8	ns
t_{OLZ}	5		ns
t_{PC}	20		ns
t_{RC}	70		ns

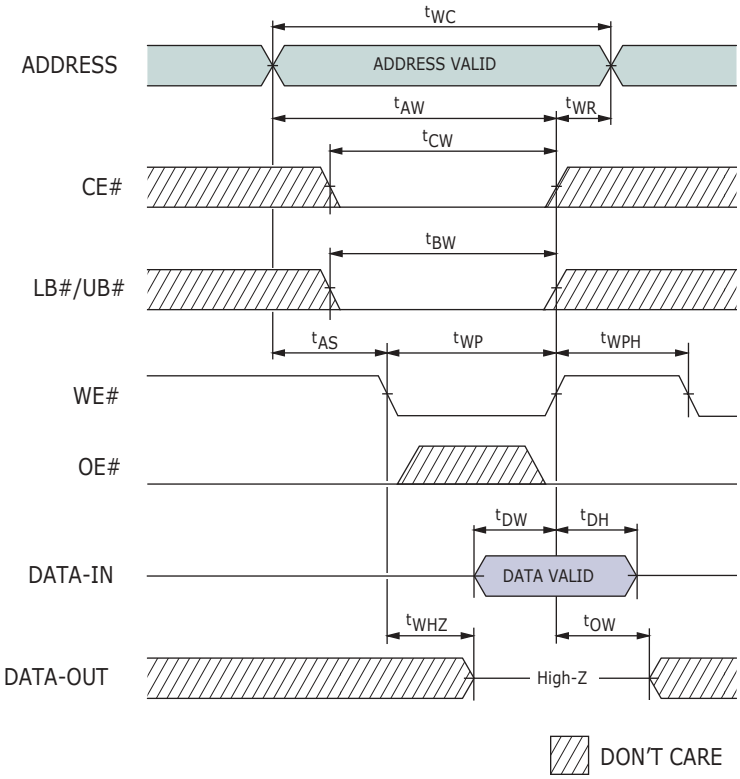


Figure 40.10 WRITE Cycle (WE# Control)

Table 40.17 WRITE Cycle Timing Parameters (WE# Control)

Symbol	Min	Max	Units
t_{AS}	0		ns
t_{AW}	70		ns
t_{BW}	70		ns
t_{CW}	70		ns
t_{DH}	0		ns
t_{DW}	23		ns
t_{OW}	5		ns
t_{WC}	70		ns
t_{WHZ}		8	ns
t_{WP}	46		ns
t_{WPH}	10		ns
t_{WR}	0		ns

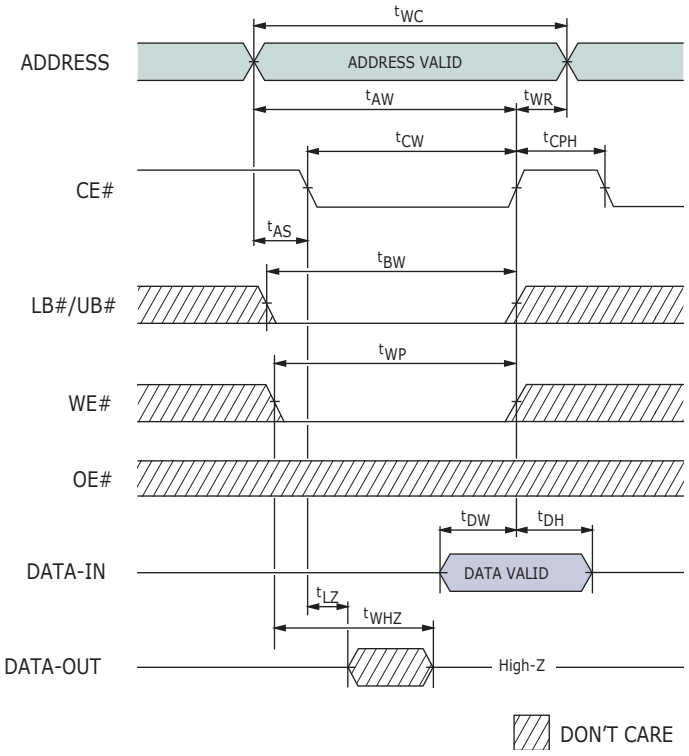


Figure 40.11 WRITE Cycle (CE# Control)

Table 40.18 WRITE Cycle Timing Parameters (CE# Control)

Symbol	Min	Max	Units
t_{AS}	0		ns
t_{AW}	70		ns
t_{BW}	70		ns
t_{CPH}	5		ns
t_{CW}	70		ns
t_{DH}	0		ns
t_{DW}	23		ns
t_{LZ}	10		ns
t_{WC}	70		ns
t_{WHZ}		8	ns
t_{WP}	46		ns
t_{WR}	0		ns

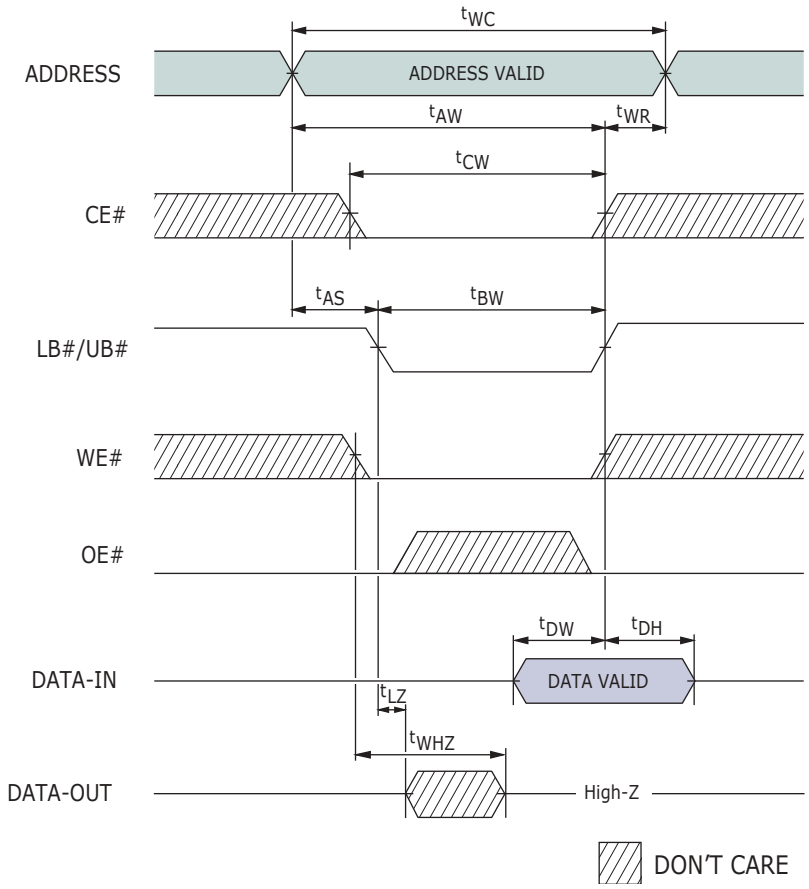


Figure 40.12 WRITE Cycle (LB#/UB# Control)

Table 40.19 WRITE Cycle Timing Parameters (LB#/UB# Control)

Symbol	Min	Max	Units
t_{AS}	0		ns
t_{AW}	70		ns
t_{BW}	70		ns
t_{CW}	70		ns
t_{DH}	0		ns
t_{DW}	23		ns
t_{LZ}	10		ns
t_{WC}	70	8	ns
t_{WHZ}		8	ns
t_{WR}	0		ns

41 32/16M CellRAM Revision Summary

Revision A (August 25, 2005)

Initial release.

42 MCP Revision Summary

42.1 Revision A0 (October 14, 2004)

Initial release.

42.2 Revision A1 (June 15, 2005)

Added two 80-ball pinouts
Added new TLC080 package drawing
Swapped 128/64/32 module with CellularRAM 16/32/64.

42.3 Revision A2 (October 28, 2005)

Global: added Package on Package (PoP) information

Updated the Ordering Information table

Added a valid combinations table for the 64/16 device

Added two 128-ball pinouts

Added new ALG128 package drawing

42.4 Revision A3 (November 28, 2005)

Replaced CellRAM modules with the *64M CellularRAM Type 2* and *32/16M Aysnc/Page CellularRAM Type 2*

Updated the Flash Module with latest version data sheet